

# FDBL86066-F085

## N-Channel POWERTRENCH<sup>®</sup> MOSFET

100 V, 240 A, 4.1 mΩ

### Features

- Typical  $R_{DS(on)}$  = 3.3 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 80\text{ A}$
- Typical  $Q_{g(tot)}$  = 47 nC at  $V_{GS} = 10\text{ V}$ ,  $I_D = 80\text{ A}$
- UIS Capability
- Qualified to AEC Q101
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Applications

- Automotive Engine Control
- PowerTrain Management
- Solenoid and Motor Drivers
- Electrical Power Steering
- Integrated Starter/Alternator
- Distributed Power Architectures and VRM
- Primary Switch for 12 V Systems

### MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Value	Unit
$V_{DSS}$	Drain-to-Source Voltage	100	V
$V_{GS}$	Gate-to-Source Voltage	±20	V
$I_D$	Drain Current – Continuous, ( $V_{GS} = 10\text{ V}$ ) $T_C = 25^\circ\text{C}$ (Note 1)	185	A
	Pulsed Drain Current, $T_C = 25^\circ\text{C}$	(See Figure 4)	A
$E_{AS}$	Single Pulse Avalanche Energy (Note 2)	93.6	mJ
$P_D$	Power Dissipation	300	W
	Derate Above $25^\circ\text{C}$	2	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature	-55 to +175	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

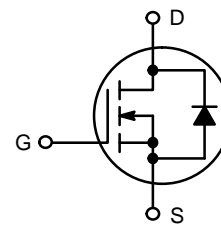
1. Current is limited by silicon.
2. Starting  $T_J = 25^\circ\text{C}$ ,  $L = 30\ \mu\text{H}$ ,  $I_{AS} = -79\text{ A}$ ,  $V_{DD} = 100\text{ V}$  during inductor charging and  $V_{DD} = 0\text{ V}$  during time in avalanche.



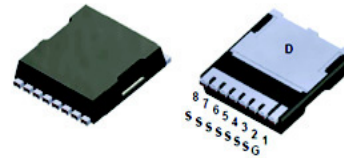
ON Semiconductor<sup>®</sup>

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$V_{DSS}$	$R_{DS(ON)}$ MAX	$I_D$ MAX
100 V	4.1 mΩ @ 10 V	240 A

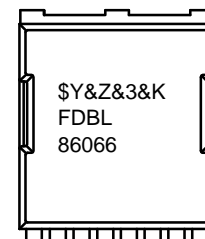


N-CHANNEL MOSFET



H-PSOF8L  
CASE 100CU

### MARKING DIAGRAM



\$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FDBL86066	= Specific Device Code

### ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

**THERMAL CHARACTERISTICS**

Symbol	Parameter	Value	Unit
R <sub>θJC</sub>	Thermal Resistance, Junction to Case	0.5	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction to Ambient (Note 3)	43	

3. R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJC</sub> is guaranteed by design, while R<sub>θJA</sub> is determined by the board design. The maximum rating presented here is based on mounting on a 1 in<sup>2</sup> pad of 2oz copper.

**ELECTRICAL CHARACTERISTICS** (T<sub>J</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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**OFF CHARACTERISTICS**

BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0 V	100	–	–	V
I <sub>DSS</sub>	Drain-to-Source Leakage Current	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V T <sub>J</sub> = 25°C T <sub>J</sub> = 175°C (Note 4)	–	–	1	μA
I <sub>GSS</sub>	Gate-to-Source Leakage Current	V <sub>GS</sub> = ±20 V	–	–	±100	nA

**ON CHARACTERISTICS**

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	2	2.9	4.0	V
R <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 80 A T <sub>J</sub> = 25°C T <sub>J</sub> = 175°C (Note 4)	–	3.3	4.1	mΩ
			–	7.3	8.8	

**DYNAMIC CHARACTERISTICS**

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 0 V, f = 1 MHz	–	3240	–	pF
C <sub>oss</sub>	Output Capacitance		–	1950	–	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		–	26	–	pF
R <sub>g</sub>	Gate Resistance	V <sub>GS</sub> = 0.5 V, f = 1 MHz	–	0.5	–	Ω
Q <sub>g(tot)</sub>	Total Gate Charge	V <sub>GS</sub> = 0 V to 10 V, V <sub>DD</sub> = 50 V, I <sub>D</sub> = 80 A	–	47	69	nC
Q <sub>g(th)</sub>	Threshold Gate Charge	V <sub>GS</sub> = 0 V to 2 V, V <sub>DD</sub> = 50 V, I <sub>D</sub> = 80 A	–	6	–	nC
Q <sub>gs</sub>	Gate to Source Charge	V <sub>DD</sub> = 50 V, I <sub>D</sub> = 80 A	–	15	–	nC
Q <sub>gd</sub>	Gate to Drain “Miller” Charge	V <sub>DD</sub> = 50 V, I <sub>D</sub> = 80 A	–	10	–	nC

**SWITCHING CHARACTERISTICS**

t <sub>on</sub>	Turn-On Time	V <sub>DD</sub> = 50 V, I <sub>D</sub> = 80 A, V <sub>GS</sub> = 10 V, R <sub>GEN</sub> = 6 Ω	–	–	35	ns
t <sub>d(on)</sub>	Turn-On Delay		–	18	–	ns
t <sub>r</sub>	Rise Time		–	9	–	ns
t <sub>d(off)</sub>	Turn-Off Delay		–	36	–	ns
t <sub>f</sub>	Fall Time		–	13	–	ns
t <sub>off</sub>	Turn-Off Time		–	–	68	ns

**DRAIN-SOURCE DIODE CHARACTERISTICS**

V <sub>SD</sub>	Source to Drain Diode Forward Voltage	I <sub>SD</sub> = 80 A, V <sub>GS</sub> = 0 V	–	0.9	1.25	V
		I <sub>SD</sub> = 40 A, V <sub>GS</sub> = 0 V	–	0.85	1.2	
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = 80 A, di <sub>SD</sub> /dt = 300 A/μs	–	36	54	ns
Q <sub>rr</sub>	Reverse Recovery Charge		–	84	126	nC
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = 80 A, di <sub>SD</sub> /dt = 1000 A/μs	–	32	48	ns
Q <sub>rr</sub>	Reverse Recovery Charge		–	243	365	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at T<sub>J</sub> = 175°C. Product is not tested to this condition in production.

TYPICAL CHARACTERISTICS

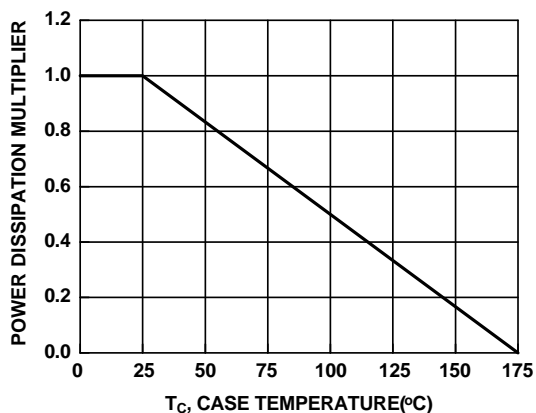


Figure 1. Normalized Power Dissipation vs. Case Temperature

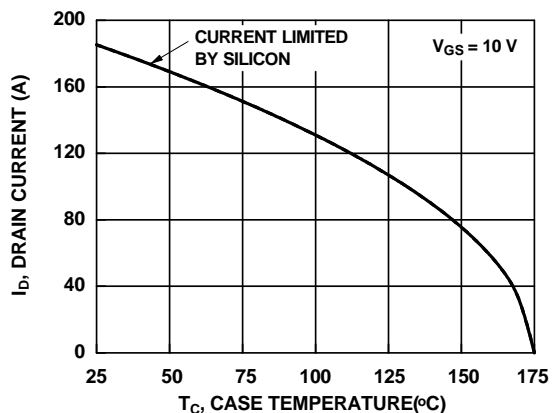


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

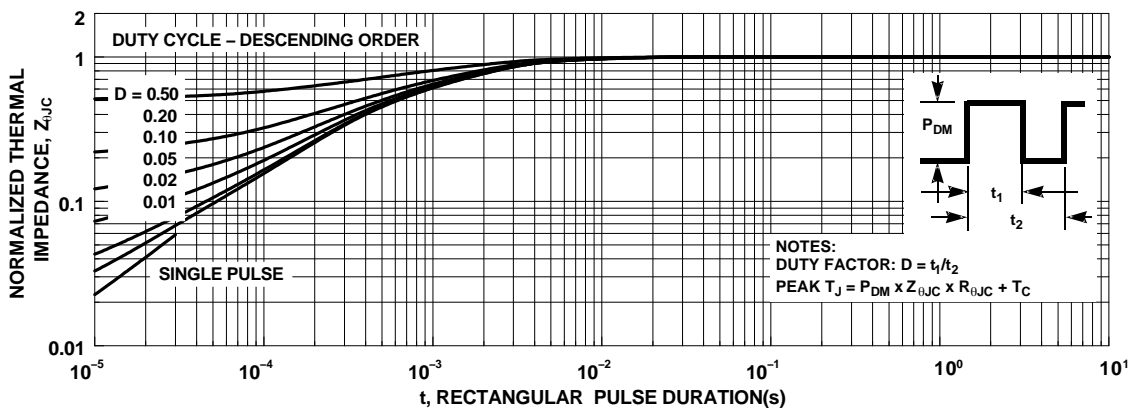


Figure 3. Normalized Maximum Transient Thermal Impedance

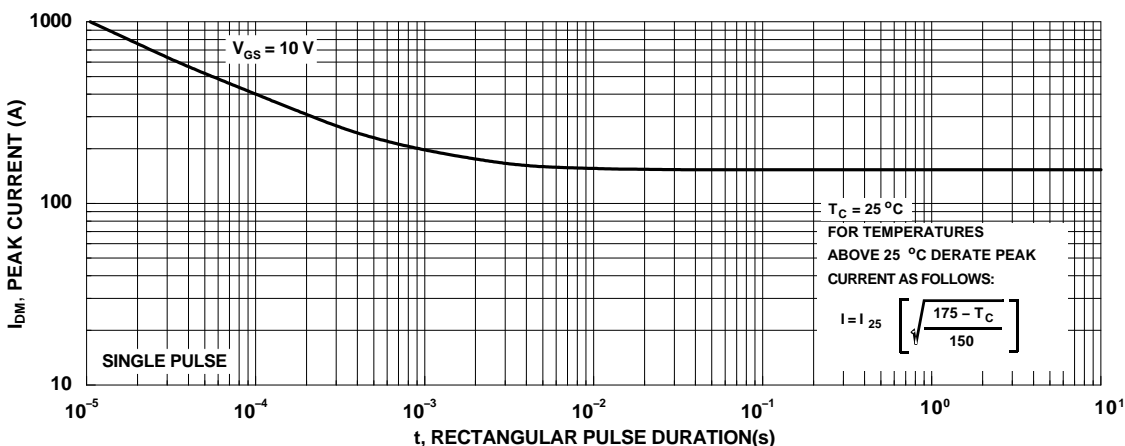


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS

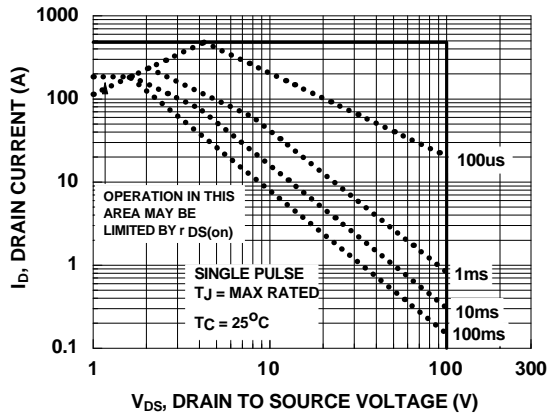


Figure 5. Forward Bias Safe Operating Area

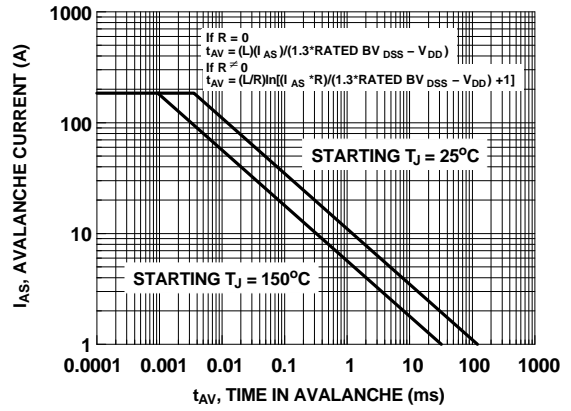


Figure 6. Unclamped Inductive Switching Capability

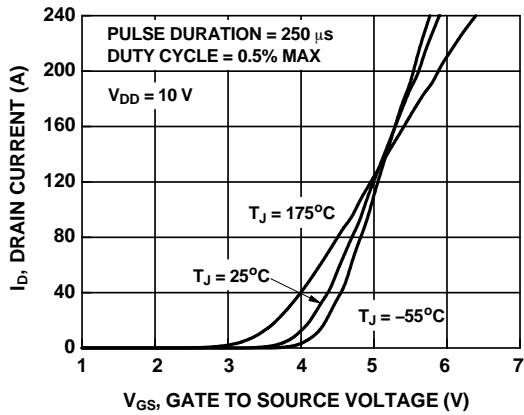


Figure 7. Transfer Characteristics

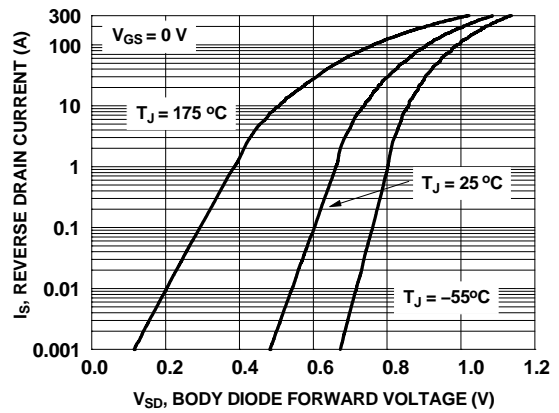


Figure 8. Forward Diode Characteristics

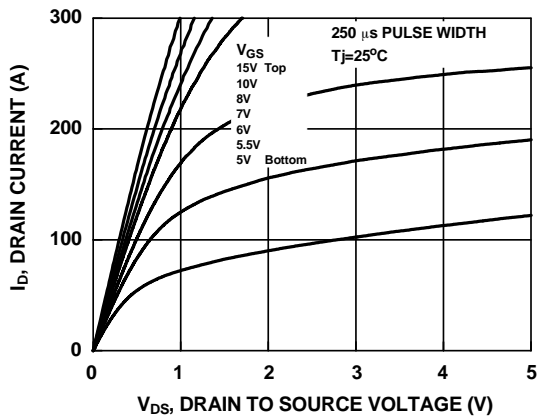


Figure 9. Saturation Characteristics

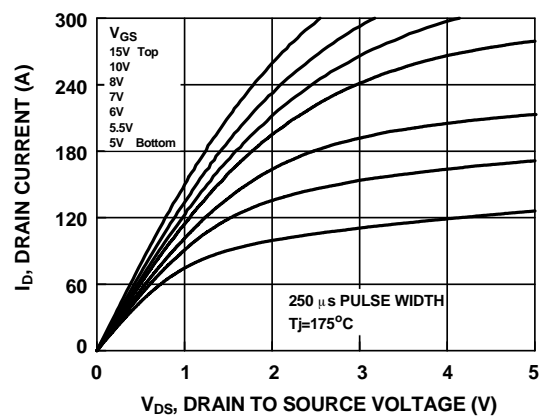


Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS

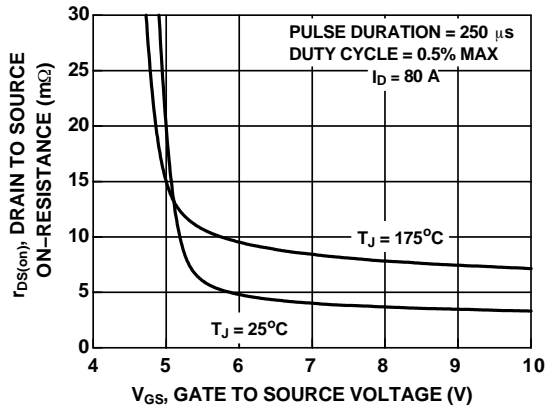


Figure 11.  $R_{DS(on)}$  vs. Gate Voltage

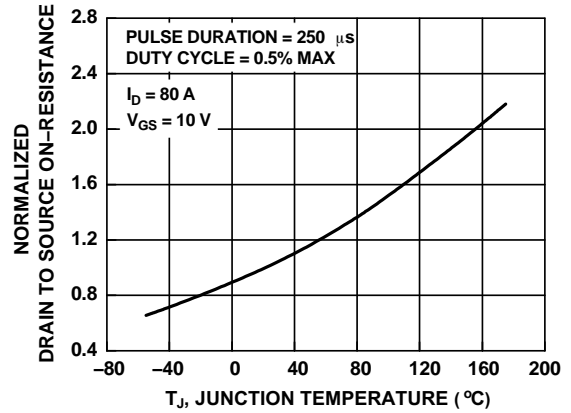


Figure 12. Normalized  $R_{DS(on)}$  vs. Junction Temperature

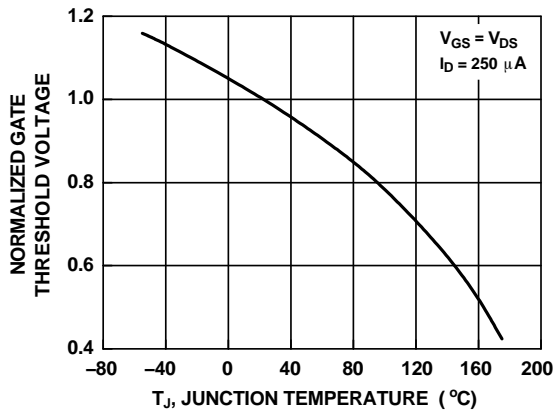


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

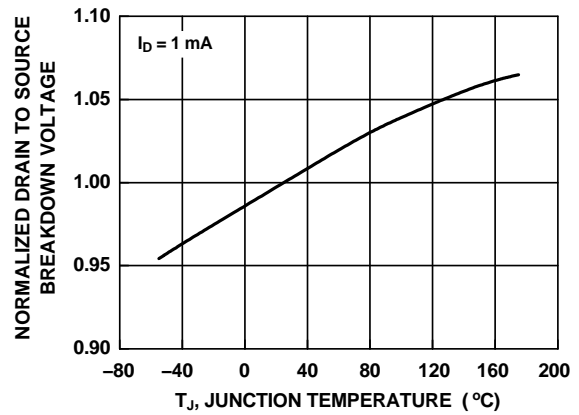


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

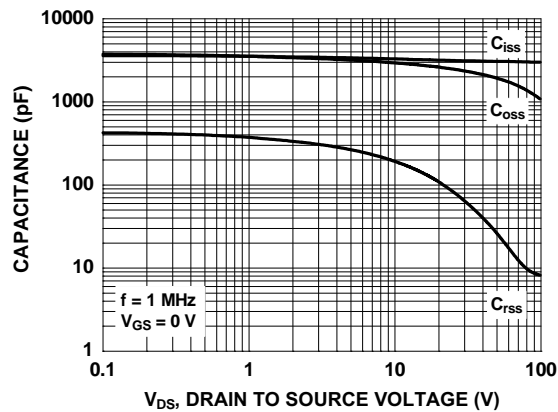


Figure 15. Capacitance vs. Drain to Source Voltage

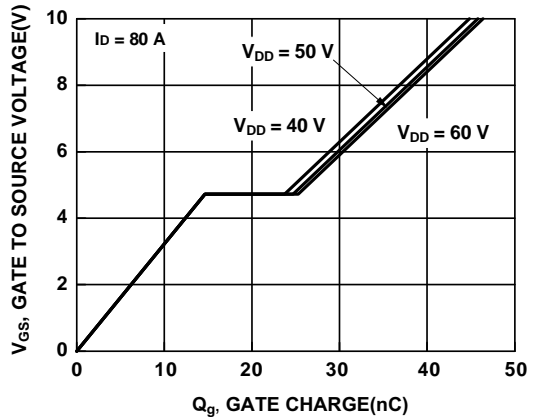


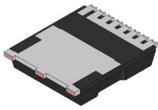
Figure 16. Gate Charge vs. Gate to Source Voltage

# FDBL86066–F085

## PACKAGE MARKING AND ORDERING INFORMATION

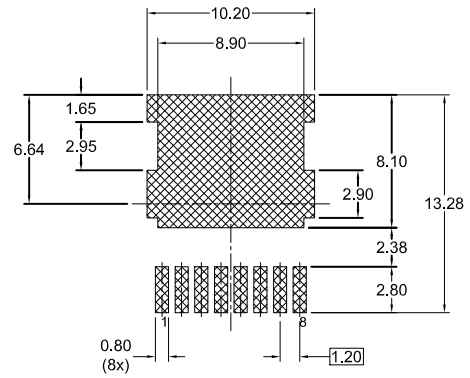
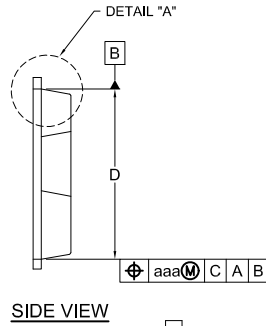
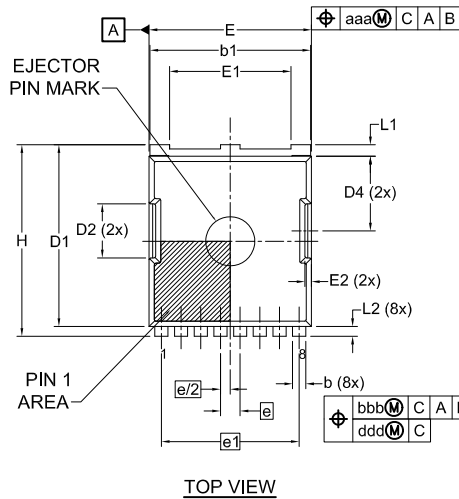
Device	Marking	Package	Reel Size	Tape Width	Quantity
FDBL86066–F085	FDBL86066	H-PSOF8L (Pb-Free / Halogen Free)	13"	24 mm	2000 Units

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



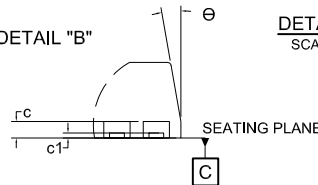
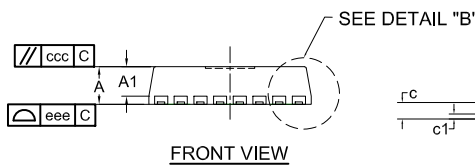
**H-PSOF8L 11.68x9.80**  
CASE 100CU  
ISSUE C

DATE 22 MAY 2023



### LAND PATTERN RECOMMENDATION

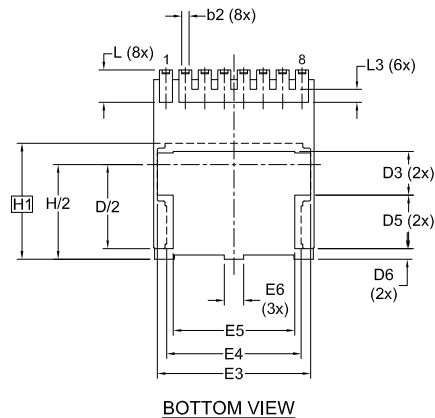
\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.



DETAIL "A"  
SCALE: 2X

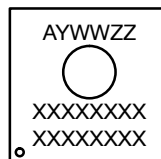
#### NOTES:

1. PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE A.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
3. CONTROLLING DIMENSION: MILLIMETERS.
4. COPLANARITY APPLIES TO THE EXPOSED WELL AS THE TERMINALS.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



DETAIL "B"  
SCALE: 2X

### GENERIC MARKING DIAGRAM\*



A = Assembly Location  
Y = Year  
WW = Work Week  
ZZ = Assembly Lot Code  
XXXX = Specific Device Code

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b2	0.35	0.45	0.55
c	0.40	0.50	0.60
c1	0.10	—	—
D	10.28	10.38	10.48
D/2	5.09	5.19	5.29
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D3	2.60	2.70	2.80
D4	4.45	4.55	4.65
D5	3.20	3.30	3.40
D6	0.55	0.65	0.75
E	9.80	9.90	10.00
E1	7.30	7.40	7.50
E2	0.30	0.40	0.50
E3	9.36	9.46	9.56

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
E4	8.20	8.30	8.40
E5	7.40	7.50	7.60
E6	1.10	1.20	1.30
e	1.20 BSC		
e/2	0.60 BSC		
e1	8.40 BSC		
H	11.58	11.68	11.78
H/2	5.74	5.84	5.94
H1	7.15 BSC		
L	1.90	2.00	2.10
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	0.70	0.80	0.90
theta	0°	—	12°
aaa	0.20		
bbb	0.25		
ccc	0.20		
ddd	0.20		
eee	0.10		

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "a", may or may not be present. Some products may not follow the Generic Marking.

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<b>DESCRIPTION:</b>	<b>H-PSOF8L 11.68x9.80</b>	<b>PAGE 1 OF 1</b>

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