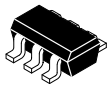
Offline Primary-Side-Regulation (PSR) Quasi-Resonant Valley Switch Controller

FAN105AM6X



SOT−23, 6 Lead
CASE 527AJ

FAN105A is offline Primary−Side−Regulation (PSR) PWM controller with Quasi−Resonant (QR) mode controller to achieved constant−voltage (CV) and constant−current (CC) control for Travel Adaptor (TA) requirement, and provide cost−effective, simplified circuit for energy−efficient power supplies.

FAN105A integrates proprietary operation of energy saving feature at no load, MWSAVER® Technology that combines our most energy efficient process and circuit technologies for power adapter design.

FAN105A can be used in Travel Adapter design by stand−alone or co−work with secondary−side SR controller FAN6240. When paired FAN105A with FAN6240, SR is compatible to achieve higher power applications.

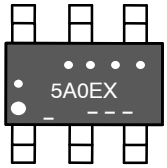
Features

- MWSAVER Technology Provides Ultra−Low Standby Power Consumption for Energy Star's 5−Star Level (<30 mW with HV FET)
- Constant−Current (CC) and Constant−Voltage (CV) with Primary−Side Regulation Eliminates Secondary−Side Feedback Component
- Valley Switch Operation for Highest Average Efficiency
- Programmable Cable Drop Compensation (CDC) with One External Resistor
- Low EMI Emissions and Common Mode Noise
- Cycle−by−Cycle Current Limiting
- Output Short−Circuit Protection
- Secondary Side Rectifier Short Detection via Current Sense Protection (CSP)
- Integrated Constant Current Compensation for Precise CC Regulation
- Output Over−Voltage Protection (VSOVP)
- Output Under−Voltage Protection (VSUVP)
- VDD Over−Voltage Protection (VDD OVP)
- Internal Thermal−Shutdown Protection (OTP)
- Programmable Brown−In and Brown−Out Protection
- This is a Pb−Free Device

Typical Applications

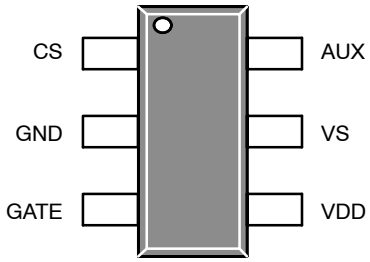
- Travel Adapter for Smart Phones, Feature Phones, and Tablet PCs
- AC−DC Adapters for Portable Devices that Require CV/CC Control

MARKING DIAGRAM



· · ·	= Date Code
5A0	= Device Code
EX	= Die Run Code
− − −	= Week Code

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 13 of this data sheet.

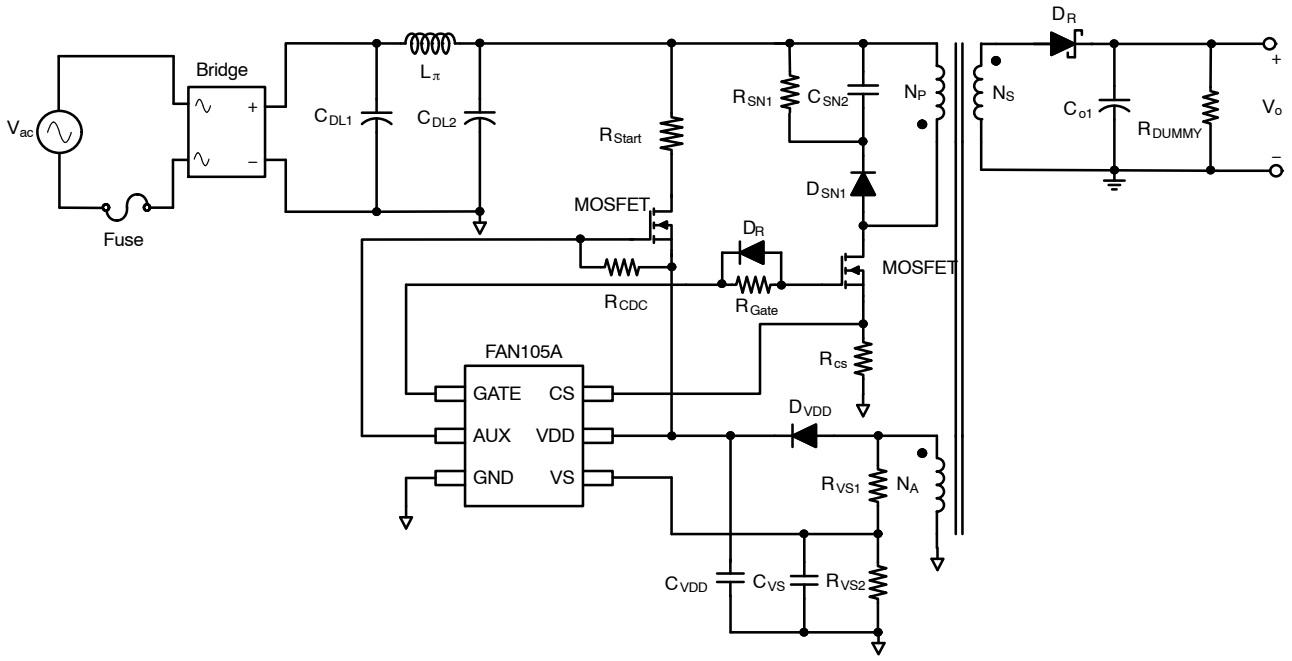


Figure 1. FAN105A Typical Application Schematic

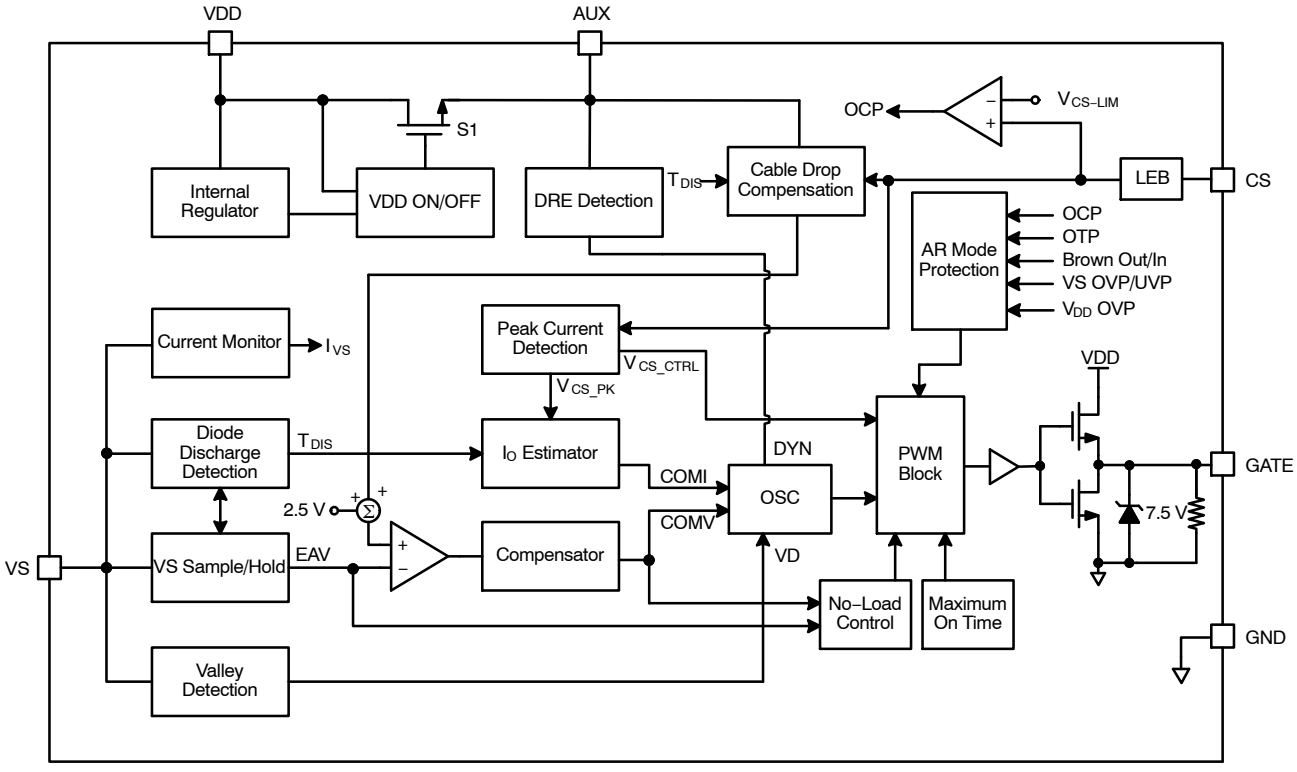


Figure 2. FAN105A Function Block Diagram

PIN DESCRIPTION

Pin #	Name	Description
1	CS	*Current Sense.* This pin connects to a current−sense resistor to detect the MOSFET current for Peak−Current−Mode control for output regulation. The current−sense information is also used to estimate the output current for CC regulation.
2	GND	*Ground*
3	GATE	*PWM Signal Output.* This pin has an internal totem−pole output driver to drive the power MOSFET. The gate driving voltage is internally clamped at 7.5 V.
4	VDD	*Power Supply.* IC operating current and MOSFET driving current are supplied through this pin. This pin is typically connected to an external V_{DD} capacitor.
5	VS	*Voltage Sense.* This pin detects the output voltage information and diode current discharge time based on the voltage of auxiliary winding. It also senses sink current through the auxiliary winding to detect input voltage information.
6	AUX	*Auxiliary Function.* This pin generates one voltage level proportional to output current to compensate output voltage drop due to cable resistance. The pin is also used for startup with external HV FET. Integrated Dynamic Response Enhancement (DRE) function through secondary feedback signal.

MAXIMUM RATINGS (Note 1, 2, 3)

Parameter		Symbol	Min	Max	Unit
DC Supply Voltage		V_{VDD}	−0.3	30	V
AUX Pin Input Voltage		V_{AUX}	−0.3	30	V
VS Pin Input Voltage		V_{VS}	−0.3	6.0	V
CS Pin Input Voltage		V_{CS}	−0.3	6.0	V
Power Dissipation (T_A = 25°C)		P_D	−	0.391	mW
Operating Junction Temperature		T_J	−40	+150	°C
Storage Temperature Range		T_{STG}	−60	+150	°C
Lead Temperature (Soldering, 10 Seconds)		T_L	−	+260	°C
Electrostatic Discharge Capability	Human Body Model, ANSI/ESDA/JEDEC, JESD22_A114	ESD	>1.5		kV
	Charged Device Model, JEDEC:JESD22_C101		>0.5		

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. All voltage values, except differential voltages, are given with respect to the GND pin.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
3. Meets JEDEC standards JS−001−2012 and JESD 22−C101.

THERMAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Value	Value	Unit
Junction−to−Ambient Thermal Impedance	θ_{JA}	−	242	°C/W
Junction−to−Top Thermal Impedance	θ_{JT}	−	56	°C/W

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
CS Pin Input Voltage	V_{CS}	0	0.8	V
Gate Pin Input Voltage	V_{GATE}	0	8.0	V
VDD Pin Input Voltage	V_{DD}	7.0	25	V
VS Pin Input Voltage	V_{VS}	1.6	3.2	V
AUX Pin Input Voltage	V_{AUX}	5.0	25	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (V_{DD} = 12 V and T_A = −40~85°C unless noted)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
VDD SECTION						
Turn−On Threshold Voltage		V_{DD-ON}	16.5	17.5	18.5	V
Turn−Off Threshold Voltage		V_{DD-OFF}	6.1	6.5	6.9	V
V_{DD} Over−Voltage−Protection Level		V_{DD-OVP}	26.5	28.0	29.5	V
V_{DD} Over−Voltage−Protection De−bounce Time		$t_{D-VDD-OVP}$	−	120	200	μs
Startup Current (Note 5)		I_{DD-ST}	−	−	20	μA
Operating Current		I_{DD-OP}	1	1.4	1.7	mA
Deep Green−Mode Operating Current		$I_{DD-DPGN}$	375	450	525	μA
OSCILLATOR SECTION						
Maximum Voltage−Mode Quasi−Resonant Blanking Frequency		$f_{OSC-BNK-MAX}$	70	76	82	kHz
Minimum Current−Mode Time−Out Blanking Frequency		$f_{OSC-BNK-MIN}$	4.5	5.0	5.5	kHz
Deep Green Mode Operating Frequency (Note 5)		$f_{OSC-DPGN}$	1.125	1.25	1.375	kHz
Minimum CCM Prevention Frequency (Note 4)		$f_{OSC-CCM-PRVENT}$	18	21	24	kHz
OVER−TEMPERATURE PROTECTION SECTION						
Over−Temperature Protection Threshold (Note 4)		T_{OTP-H}	−	120	−	°C
Over−Temperature Protection Recovery Threshold (Note 4)		T_{OTP-L}	−	100	−	°C
VOLTAGE SAMPLING SECTION						
Reference Voltage of Constant Voltage Feedback		V_{VR}	2.475	2.500	2.525	V
VS Sampling Phase−Shift Resistance (Note 4)		$R_{VS-S/H}$	−	300	−	kΩ
VS Sampling Phase−Shift Capacitance (Note 4)		$C_{VS-S/H}$	−	5	−	pF
VS Sampling Blanking Time		t_{VS_BNK-L}	1.15	1.30	1.50	μs
VS Sampling Blanking Time to High	Io over 100 mA	t_{VS_BNK-H}	1.65	1.80	2.00	μs
VS Sampling Blanking Time at CC Controlling		t_{VS_BNK-CC}	2.05	2.20	2.35	μs
VS Discharging Time Judgment Threshold Voltage (Note 4)		$V_{VS-Offset}$	150	200	250	mV
VOLTAGE SENSE SECTION						
Temperature−Independent Bias Current		I_{TC}	9.0	10.0	11.0	μA
VS Pin Source Current Threshold to Enable Brown−Out		$I_{VS-BROWN-OUT}$	260	310	360	μA
Brown−Out De−bounce Time		$t_{D-BROWN-OUT}$	12	17	22	ms
VS Pin Source Current Threshold to Enable Brown−In		$I_{VS-BROWN-IN}$	405	475	545	μA
Brown−In De−bounce Time		$N_{BROWN-IN}$	3	4	5	Cycle
Output Over−Voltage−Protection of V_S Sampling Threshold		V_{VS-OVP}	2.70	2.80	2.90	V
Output Over−Voltage−Protection Debounce Cycle Counts		N_{VS-OVP}	3	4	5	Cycle
Output Low Level Under−Voltage−Protection of V_S Sampling Threshold		V_{VS-UVP}	1.50	1.60	1.70	V
Output Under−Voltage Protection Debounce Time		t_{VS-UVP}	30	40	50	ms

ELECTRICAL CHARACTERISTICS (V_{DD} = 12 V and T_A = −40~85°C unless noted) (continued)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
NO−LOAD CONTROL SECTION						
Deep Green Mode Entry Threshold Voltage of COMV (Note 4)		$V_{COMV-CV-DPGN-ENTRY}$	0.4	0.5	0.6	V
Criteria to Enter Deep Green Mode		$V_{VS\_EAV\_Hi}$	2.550	2.600	2.650	V
Deep Green Mode Band−Band Control High Threshold Voltage		$V_{VS-EAV-H}$	−	2.550	−	V
Deep Green Mode Band−Band Control Low Threshold Voltage		$V_{VS-EAV-L}$	−	2.525	−	V
Criteria to Exit Deep Green Mode		$V_{VS\_EAV\_Lo}$	2.425	2.450	2.475	V
Dynamic Event Trigger Threshold Voltage in Deep Green Mode		$V_{VS-EAV-DYN}$	2.375	2.400	2.425	V
Minimum On−time at 264 VAC	C_{GATE} = 1 nF	$t_{ON-MIN-264VAC}$	165	200	235	ns
Minimum On−time at 230 VAC	C_{GATE} = 1 nF	$t_{ON-MIN-230VAC}$	180	215	250	ns
Minimum On−time at 115 VAC	C_{GATE} = 1 nF	$t_{ON-MIN-115VAC}$	570	660	750	ns
Minimum On−time at 90 VAC	C_{GATE} = 1 nF	$t_{ON-MIN-90VAC}$	630	815	1000	ns
CURRENT FEEDBACK SECTION						
Reference Voltage of Constant Current Feedback		V_{CCR}	1.19	1.2	1.21	V
VCS Peak Value Amplifying Gain (Note 4)		A_{PK}	−	3.6	−	V/V
Attenuator Ratio of Constant Current Feedback Loop (Note 4)		A_{V-CC}	−	1/3.5	−	V/V
CURRENT SENSE SECTION						
Current Limit Threshold Voltage		V_{CS-LIM}	0.70	0.75	0.80	V
GATE Output Turn−Off Delay (Note 4)		t_{PD}	−	100	−	ns
Leading−Edge Blanking Time (Note 4)		t_{LEB}	150	200	250	ns
GATE SECTION						
Maximum On−Time		t_{ON-MAX}	15	17	20	μs
Gate Output Voltage Low		V_{GATE-L}	0	−	1.5	V
Internal Gate PMOS Driver ON		$V_{DD-PMOS-ON}$	7.0	7.5	8.0	V
Internal Gate PMOS Driver OFF		$V_{DD-PMOS-OFF}$	9.0	9.5	10.0	V
Gate Output Clamping Voltage	VDD level higher than 9 V	$V_{GATE-CLAMP}$	7.0	7.5	8.0	V
AUX SECTION						
CDC Compensation Voltage at Internal Reference	R_{CDC} is 330 kΩ	$V_{VS-CDC4}$	0.298	0.320	0.343	V
	R_{CDC} is 560 kΩ	$V_{VS-CDC3}$	0.223	0.240	0.257	V
	R_{CDC} is 920 kΩ	$V_{VS-CDC2}$	0.149	0.160	0.171	V
	R_{CDC} is 1.3 MΩ	$V_{VS-CDC1}$	0.074	0.080	0.086	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Guaranteed by Design.
5. T_A guaranteed range at 25°C

TYPICAL PERFORMANCE CHARACTERISTICS

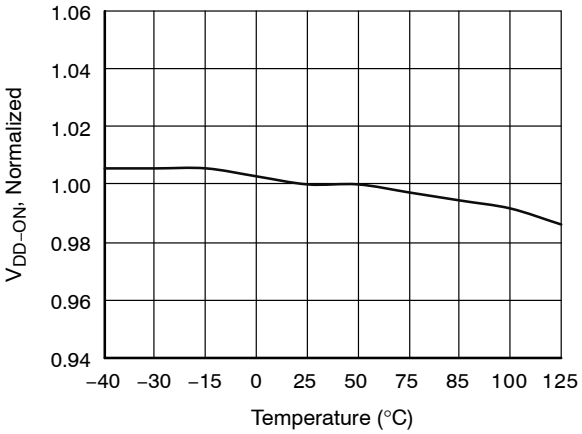


Figure 3. Turn−On Threshold Voltage (V_{DD-ON}) vs. Temperature

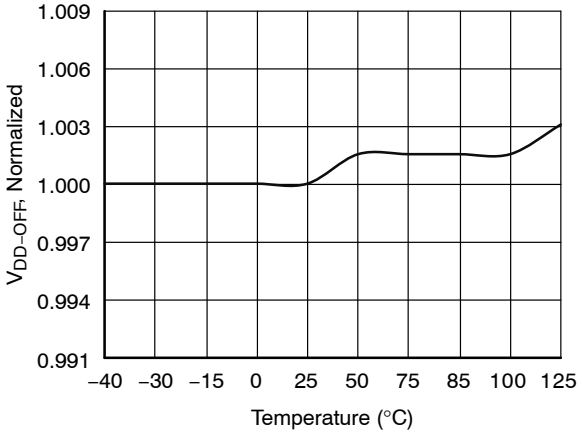


Figure 4. Turn−Off Threshold Voltage (V_{DD-OFF}) vs. Temperature

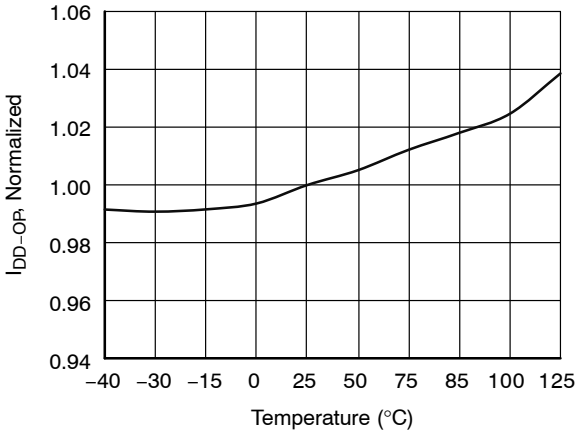


Figure 5. Operating Supply Current (I_{DD-OP}) vs. Temperature

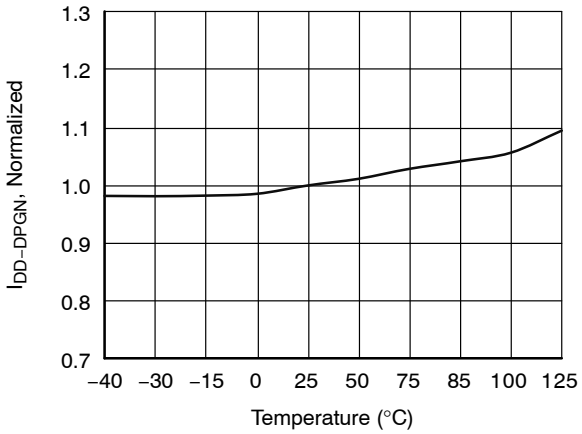


Figure 6. Deep Green Mode Operation Current ($I_{DD-DPGN}$) vs. Temperature

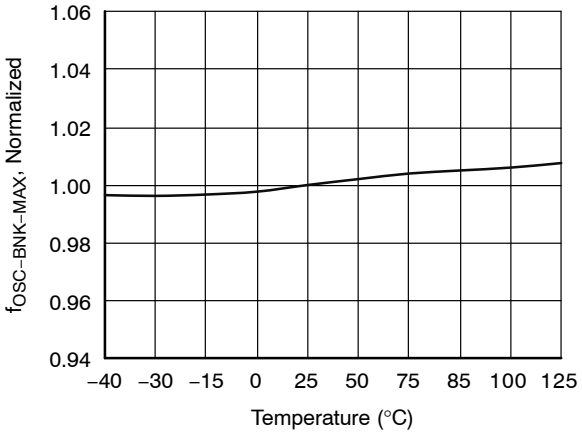


Figure 7. Maximum Operation Frequency of QR Blanking Time ($f_{OSC-BNK-MAX}$) vs. Temperature

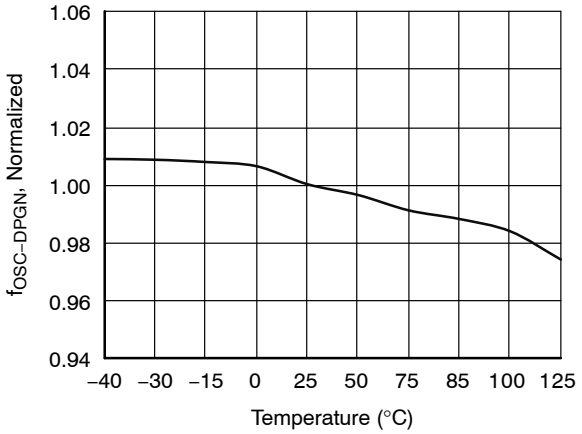


Figure 8. Deep Green Mode Operation Frequency ($f_{OSC-DPGN}$) vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

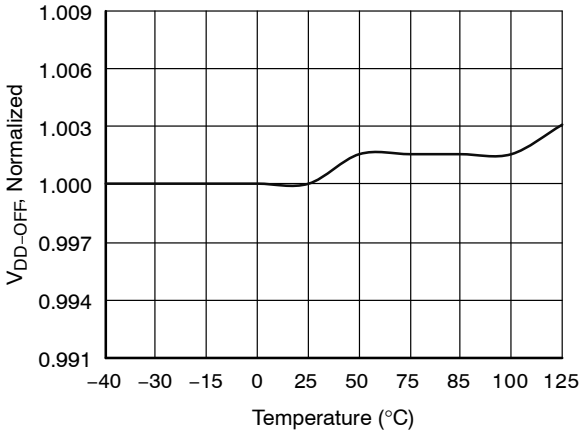


Figure 9. Reference Voltage of CV Feedback (V_{VR}) vs. Temperature

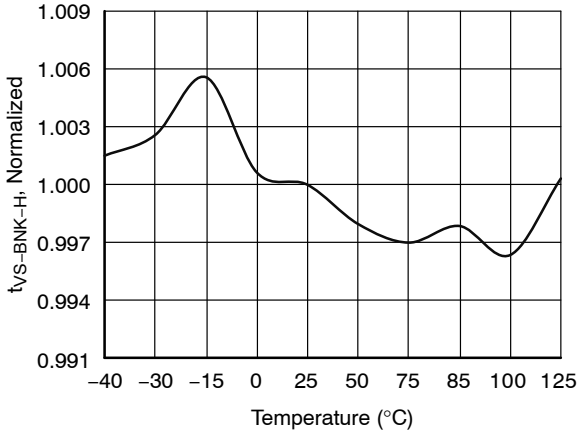


Figure 10. Vs Sampling Blanking Time ($t_{VS-BNK-H}$) vs. Temperature

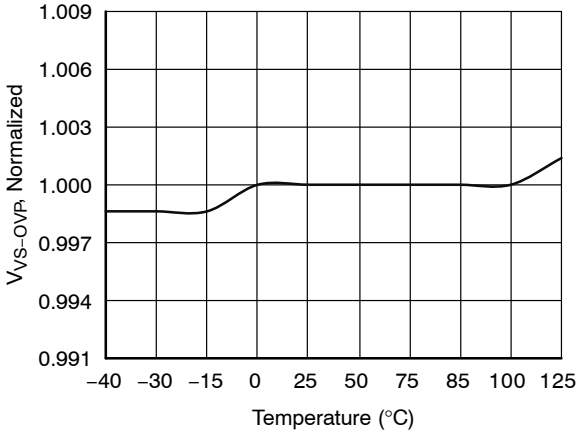


Figure 11. Output Over−Voltage Protection of Vs Sampling Threshold (V_{VS-OVP}) vs. Temperature

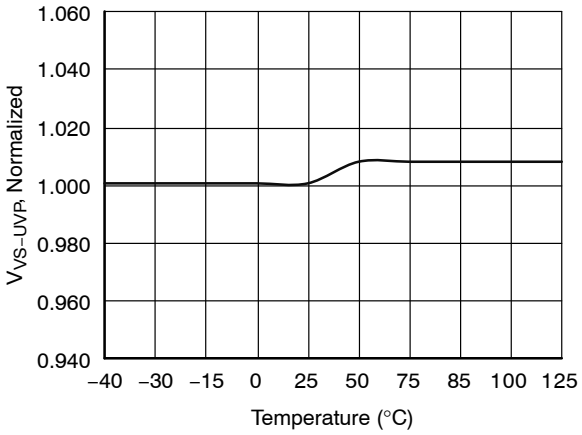


Figure 12. Output Under−Voltage of Vs Sampling Threshold (V_{VS-UVP}) vs. Temperature

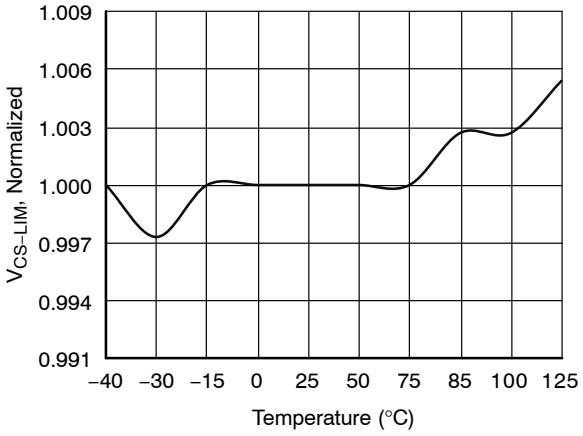


Figure 13. Current Limit Threshold Voltage (V_{CS-LIM}) vs. Temperature

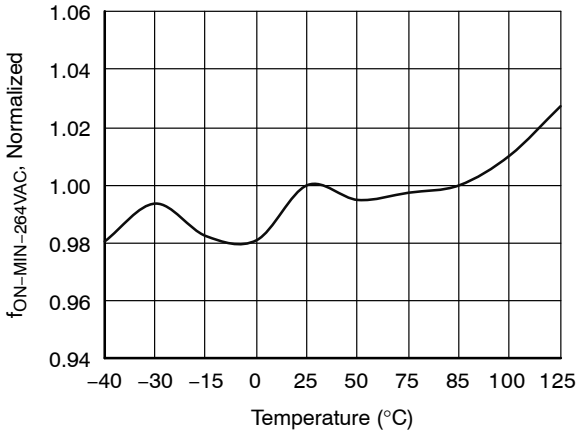


Figure 14. Minimum Gate Turn On Time ($t_{ON-MIN-264VAC}$) vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

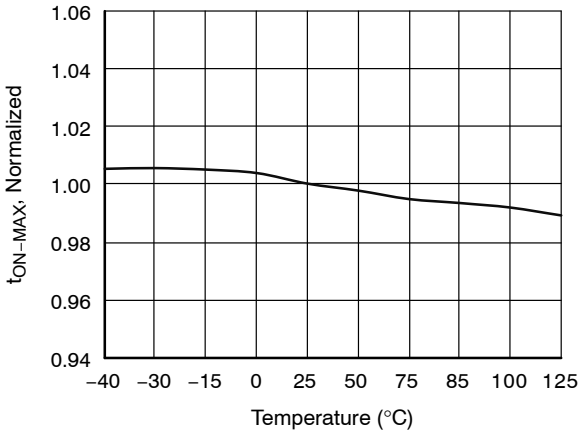


Figure 15. Maximum Gate Turn On Time (t_{ON-MAX}) vs. Temperature

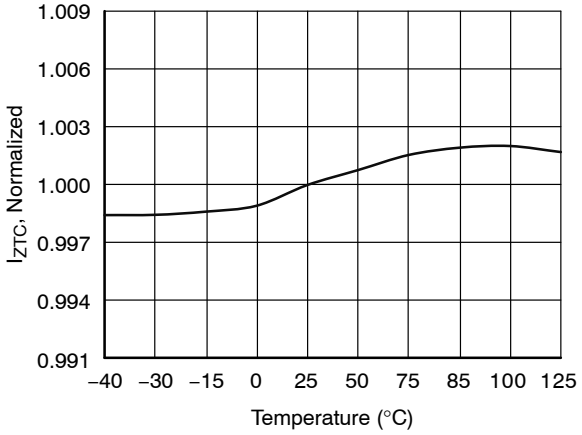


Figure 16. Dynamic Trigger Current Threshold (I_{ZTC}) vs. Temperature

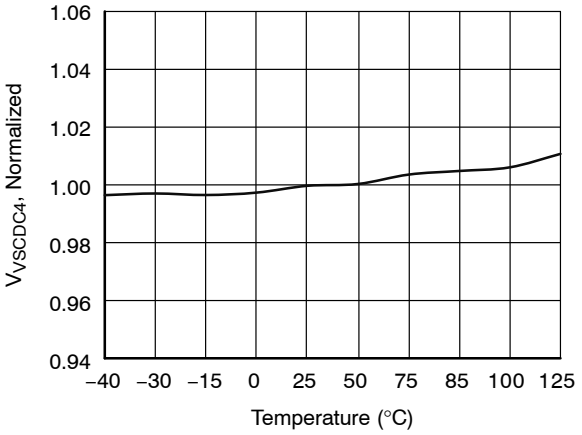


Figure 17. Cable Compensation Level 4 Reference Voltage ($V_{VS-CDC4}$) vs. Temperature

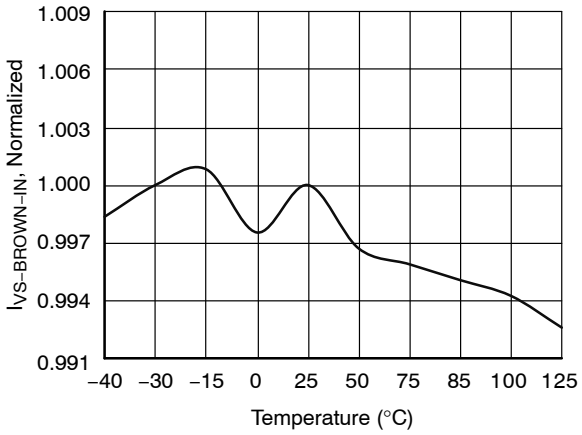


Figure 18. Brown In Threshold Current ($I_{VS-BROWN-IN}$) vs. Temperature

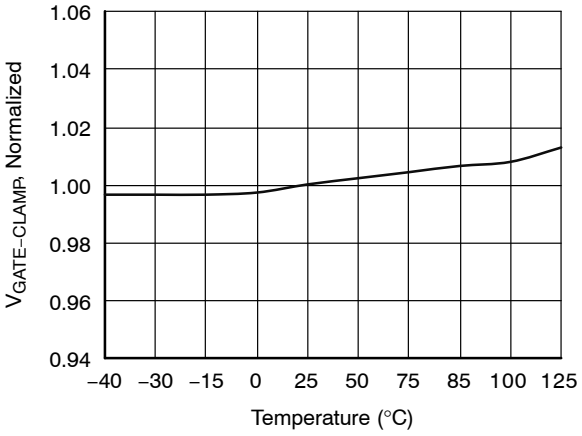


Figure 19. Clamp Voltage ($V_{GATE-CLAMP}$) vs. Temperature

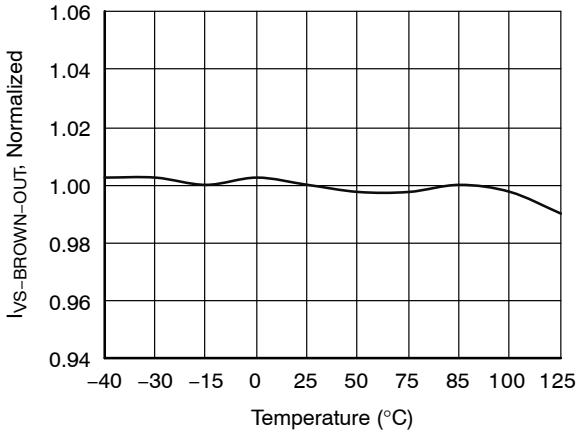


Figure 20. Brown Out Threshold Current ($I_{VS-BROWN-OUT}$) vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

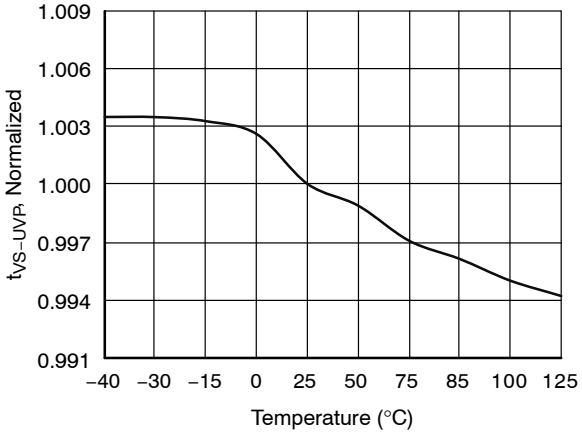


Figure 21. Blanking Time of VSUVP (t_{VS-UVP}) vs. Temperature

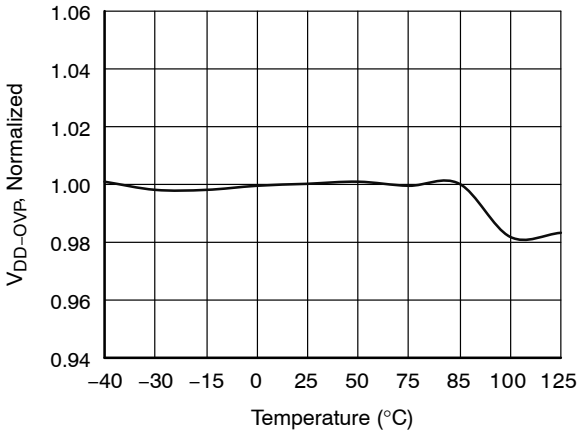


Figure 22. VDD Over Voltage Protection Threshold (V_{DD-OVP}) vs. Temperature

FUNCTIONAL DESCRIPTION

FAN105A is an offline PWM and Primary−Side Regulated (PSR) fly−back controller that can simplify feedback circuit and secondary side circuit compare to traditional fly−back converter. In addition, FAN105A detects Quasi−Resonant valley switching to minimize the switching loss and get better EMI performance.

FAN105A modulates pulse width and switching frequency based on feedback signal auxiliary winding signal (VS) and current sense signal (CS). Extremely accurately Constant Voltage (CV) with Cable Drop Compensation (CDC) and Constant Current (CC) could meet strict requirement from market. The CV and CC output characteristic is shown as Figure 23. There are 4 levels (80 mV − 320 mV) choices in CDC compensation weighting that is easily set via external SMD resistor.

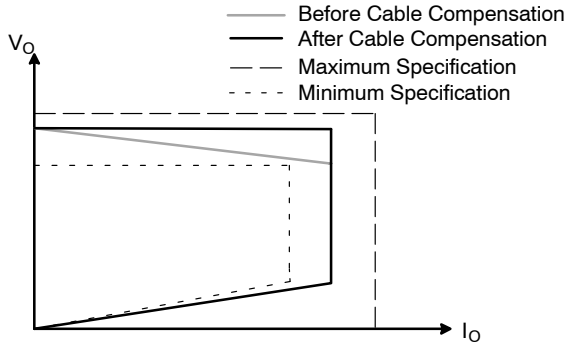


Figure 23. CV with CDC and CC V/I Curve at the Cable End

FAN105A implements DeeP GreeN mode (DPGN) with lowest switching frequency, limites IC current consumption (450 μA) for excellent system standby power performance. Furthermore, the system design allows two kinds of startup circuit with resistor or high voltage FET.

Protections are: over/under voltage protection (VSOVP, VSUVP), Brown In and Brown Out, cycle by cycle over current protection (OCP), current sense resistor short protection, secondary rectifier short protection.

Basic CV/CC Control Principle

Figure 24 shows the circuit diagram of a PSR fly−back converter, FAN105A estimates output current through primary side peak current from CS, output voltage via auxiliary winding signal that proportional to secondary side voltage, the current and voltage sampling are shown in Figure 25. Generally, Discontinuous Conduction Mode (DCM) with valley switching operation is preferred for PSR since it allows better output regulation. The operation principles of DCM/BCM flyback converter are as follows:

During the MOSFET turn on time (t_{ON}), input voltage (V_{DL}) is applied across the primary−side inductor (L_m). Then MOSFET current (I_{DS}) increases linearly from zero to the peak value (I_{pk}). Meanwhile, the energy is drawn from the input and stored in the inductor.

When the MOSFET is turned off, the energy stored in the inductor forces the secondary diode (D_{sec}) to turn on. While the diode is conducting, the output voltage (V_o), together with diode forward voltage drop (V_F), are applied across the secondary−side inductor ($L_m \times Ns^2 / N_p^2$) and the diode current (I_D) decreases linearly from the peak value ($Ipk \times N_p / N_s$) to zero. At the end of inductor current discharge time (t_{DIS}), all the energy stored in the inductor has been delivered to the output.

When the diode current reaches zero, the transformer auxiliary winding voltage (V_{Aux}) begins to oscillate by the resonance between the primary−side inductor (L_m) and the effective capacitor loaded across MOSFET.

During the inductor current discharge time, the sum of output voltage and diode forward−voltage drop is reflected to the auxiliary winding side as $(V_o + V_F) \times N_{aux} / N_s$. Since the diode forward−voltage drop decreases as current decreases, the auxiliary winding voltage reflects the output voltage best at the end of diode conduction time, where the diode current diminishes to zero. By sampling the winding voltage at the end of the diode conduction time, the output voltage information can be obtained. The internal error amplifier for output voltage regulation (EAV) compares the sampled voltage with internal precise reference to generate error voltage (COMV), which determines the duty cycle of the MOSFET in CV Mode.

The output current is obtained by averaging the triangular output diode current area over a switching cycle as:

$$I_O = < I_D >_{AVG} = \frac{1}{2} \cdot I_{PK} \cdot \frac{N_P}{N_S} \cdot \frac{T_{DIS}}{T_S} \quad \text{(eq. 1)}$$

The internal FAN105A circuits identify the peak value of the drain current with a peak detection circuit and calculate the output current using the inductor discharge time (t_{DIS}) and switching period (t_S). This output information (EAI) is compared with internal precise reference to generate error voltage (COMI), which determines the duty cycle of the MOSFET in CC Mode. With TRUECURRENT® technique, constant output current can be precisely controlled.

With a given current sensing resistor, the output current can be programmed as:

$$I_O = \frac{1}{6} \cdot \frac{N_P}{N_S} \cdot \frac{V_{CCR}}{R_{CS}} \quad \text{(eq. 2)}$$

Of the two error voltages, COMV and COMI, the smaller one determines the duty cycle. During Constant Voltage regulation, COMV determines the duty cycle while COMI is saturated to HIGH. During Constant Current regulation, COMI determines the duty cycle while COMV is saturated to HIGH.

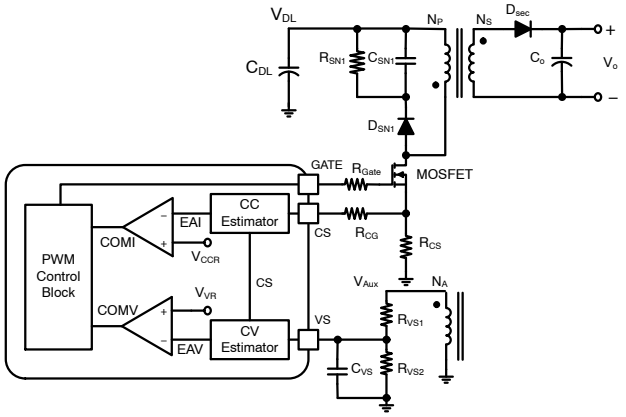


Figure 24. Simplified PSR Flyback Converter Circuit

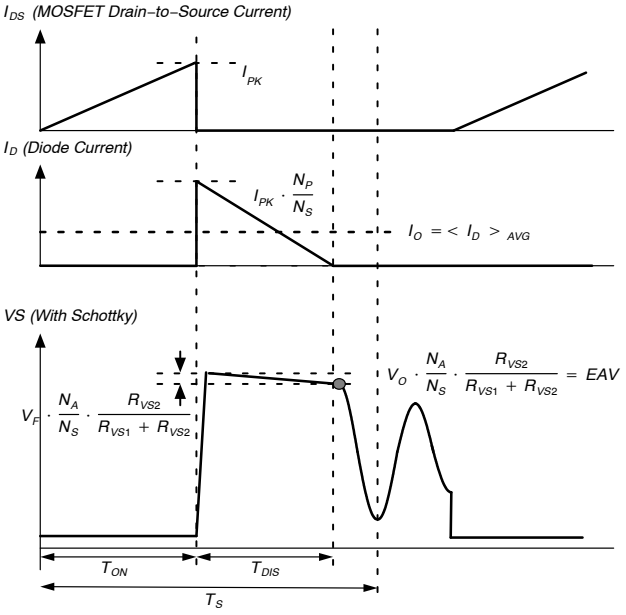


Figure 25. Cycling Current and VS Sampling in DCM

Quasi−Resonant Valley Switch

FAN105A Build−In Quasi−Resonant valley detecting function and inductor discharging time detecting function. During MOSFET turn off period, FAN105A checked falling of VVS, TDIS information will update as falling of VVS checked. FAN105A keep monitor both VVS and IVS after TDIS checked. FAN105A maximum period of MOSFET on time and off time could be reach 45 μs, it was depending on whether valley checked. Quasi−Resonant valley switching could minimize MOSFET switching loss during switch on, meanwhile, to eliminate EMI and Common mode switching component noise. Charger system would be getting better efficiency than non−valley switching methodology.

Output Voltage Sampling

VS voltage which is reflected auxiliary winding and proportional to output voltage. Therefore, It is possible to regulate output voltage by sensing VS voltage. Figure 26 shown VS sampling waveform with secondary rectifier that using Schottky diode or Synchronous Rectifier (SR).

In order to regulate output voltage in accurately range, FAN105A build−in VS sampling methodology for signal like Figure 26 showed, FAN105A samples and hold VS voltage as EAV at timing like gray point showed. Base on EAV level to regulate Pulse width to achieve estimation output voltage.

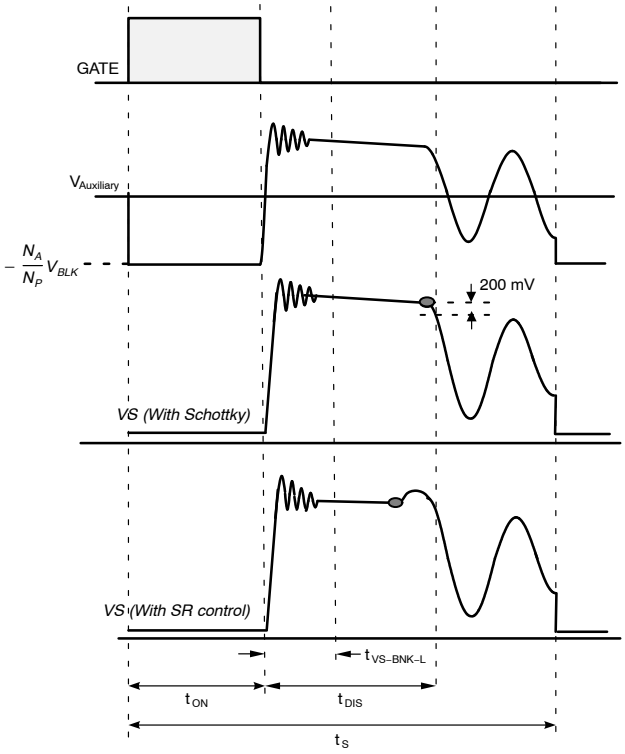


Figure 26. VS sampling with Diode or Synchronous Rectifier

A leading edge blanking time ($t_{VS-BNK-H/L}$) start from primary switch turned off, that is caused by the resonance of leakage inductance and parasistic capacitance at transformer. In order to avoid VS sampling procedure get impacted by that ringing, the oscillation should be settle before settle down before $t_{VS-BNK-L}$ ended as Figure 26 showed. t_{DIS} is secondary rectifier current discharging time which recommend better design is longer than $t_{VS-BNK-H}$ during minimum on time controlling. t_{DIS} is predictable by following formula:

$$t_{DIS} = \frac{V_{DL}\,(t_{ON-MIN} + t_{OFF-DELAY})}{(V_o + V_D)} \cdot \frac{N_S}{N_P} \qquad \text{(eq. 3)}$$

Where parameter: $t_{OFF-DELAY}$ is switch turn off delay time that level is chaging in differences system criteria, t_{ON-MIN} is minimum turn on time in design that should consider propagation delay from IC Gate to switch Gate.

The output voltage can be describe by below equation:

$$V_O = V_{VR} \cdot \left(1 + \frac{R_{VS1}}{R_{VS2}}\right) \cdot \frac{N_S}{N_A} \qquad \text{(eq. 4)}$$

Deep Green Mode (DPGN) Operation in CV Mode

FAN105A integrated MWSAVER technology that minimize current consumption and frequency at DPGN mode is fixed to minimum switching frequency ($f_{OSC-DPGN}$) and variable Pulse width based on VS sampling voltage (EAV). V_{VS} regulated boundary are between $V_{VS-EAV-H}$ and $V_{VS-EAV-L}$.

After exit DPGN, internal regulation reference voltage was changed to V_{VR}.

FAN105A DPGN entry and exit criteria showed as below:

- DPGN entry need to meet both criteria as below:
  - Minimum frequency ($f_{OSC-MIN}$) operation continues over than $N_{DPGN-Entry}$ switching cycles.
  - EAV > $V_{VS-EAV-H}$ (2.550 V).
- DPGN exit criteria, meet one of below criteria:
  - EAV < $V_{VS-EAV-L}$ (2.525 V) and maximum on time at DPGN.
  - EAV < $V_{VS-EAV-DYN}$ (2.4 V).

During the DPGN mode controlling, FAN105A decreases the operating current down to 450 μA. Therefore, the standby power could meet international standard requirement when work with flexible start up circuit, designer have flexible start up circuit that HV FET or start up resistor depending on cost and better standby power consideration.

Cable Drop Compensation (CDC)

FAN105A integrates cable drop compensation function and the compensation weighting is calculated based on t_{DIS}, current sense voltage (V_{CS}), and CDC setting resistor (R_{CDC}) needed to between VDD and AUX pin. During startup, as VDD reached V_{DD-ON}, CDC programming block detects AUX pin current and determine cable drop compensation weighting based on current weighting of AUX pin. Once finished CDC compensation weighting detecting, the information will stored until shunt−down by protections or VDD lower than V_{DD-OFF}. The CDC weighting automatic detected input current during start up. which provides a constant output voltage at the end of the cable over the entire load range in CV Mode. The table shows the compensation weighting with corresponding R_{CDC} setting as below:

Table 1. CDC WEIGHTING AND R_{CDC} SETTING

R_{CDC}	Label	V_{VS} Compensation Weighting
1.3 MΩ	$V_{VS-CDC1}$	0.08 V
920 kΩ	$V_{VS-CDC2}$	0.16 V
560 kΩ	$V_{VS-CDC3}$	0.24 V
330 kΩ	$V_{VS-CDC4}$	0.32 V

TA designer can easily to set up CDC weighting via choose R_{CDC} following above table. In the table, resistance of R_{CDC} is recommended for corresponding compensation level. Cable drop compensation voltage at output is proportional to V_{VS} compensation weighting that is internal reference voltage for CDC compensation.

Programmable Brown In/ Brown Out

FAN105A implement Brown out and Brown In through high side resistor setting at VS PIN. In actual system operation, VS PIN is drain a current (I_{VS}) that proportional to line voltage during MOSFET turns on. IVS could predict by below equation:

$$I_{VS} = V_{DL} \cdot \frac{N_A}{N_P} \cdot \frac{1}{R_{VS1}} \quad \text{(eq. 5)}$$

Operating Current

The operating current in FAN105A is as small as 1.4 mA. The small operating current results in higher efficiency and reduces the V_{DD} hold−up capacitance requirement. During DPGN mode, the FAN105A consumption current is reduced to 450 μA, assisting the power supply meet standby power standard requirements.

Protections

The FAN105A self−protection includes V_{DD} Over−Voltage−Protection (V_{DD} OVP), Internal Chip Over−Temperature−Protection (OTP), VS Over−Voltage Protection (VSOVP), VS Under−Voltage Protection (VSUVP), CS pin Protection (CSP), Brownout and Brown In protection, and all of protection are implemented as Auto Restart (AR) mode.

When an Auto−Restart Mode protection is triggered, switching is terminated and the MOSFET remains off, causing V_{DD} to drop till V_{DD-OFF} and shut−down the system then all protections are reset. After then V_{DD} will be charged again by the input AC voltage and once touch V_{DD-ON} then switching resumes. This is the reason why it is called Auto− Restart, resumes switching automatically.

V_{DD} Over−Voltage−Protection (V_{DD} OVP)

When V_{DD} is raised up to higher level by some reasons, transformer V_{DD} winding turns are too many, load regulation is not good between transformer winding, VS information is not available anyhow and so on, and touches V_{DD-OVP}, then FAN105A stops switching and protects IC from higher V_{DD} voltage. This is different then output voltage is over than pre determined level.

VS Under−Voltage Protection (VSUVP)

FAN105A build−in VSUVP function that prevent TA keep deliver power to phone side when output voltage is under the set voltage at VS pin. VSUVP has a 40 ms de−bounce time and once VDD touches V_{DD-ON}, during the later 40 ms VSUVP is disabled because VSUVP should not be triggered during the start up. VSUVP level can be calculated as below:

$$V_{O-UVP} = V_{VS-UVP} \cdot \left(1 + \frac{R_{VS1}}{R_{VS2}}\right) \cdot \frac{N_S}{N_A} \quad \text{(eq. 6)}$$

VS Over−Voltage Protection (VSOVP)

The VSOVP is designed to prevent TA output voltage is over then the rating of used components, like capacitor. VSOVP has 4 switching cycles of denounce time and that prevent mis−triggered of VSOVP by switching noise. The protection level is changed in proportional to the CDC weighting.

VSOVP trigger level can be illustrates as following formula:

$$V_{O-OVP} = \left(V_{VS-UVP} + V_{VS-CDC} \cdot \frac{I_O}{I_{O-CC}}\right) \cdot \left(1 + \frac{R_{VS1}}{R_{VS2}}\right) \cdot \frac{N_S}{N_A} \quad \text{(eq. 7)}$$

CS Pin Protection (CSP)

In order to prevent MOSFET current over than safe operating area, FAN105A build−in cycle by cycle over current protection. The protection could protect MOSFET damaged by saturation current and CS pin sensing error. As CS PIN signal meet below conditions FAN105A will turn off Gate immediately. Current Sensing Protection (CSP) criteria shows as below:

- V_{CS} < 0.2 V after switching turn on 4.5 μs at low line or 1.5us at high line.
- V_{CS} > 1.5 V

Over−Temperature Protection (OTP)

In order to guarantee FAN105A works within recommended temperature. FAN105A build−in chip Over−Temperature−Protection (OTP). As chip junction temperature over threshold T_{OTP-H} IC immediately terminated Gate switching signal until chip junction temperature recover to T_{OTP-L}.

Start Up Function with AUX

FAN105A supports high voltage start up with HV FET that can make better standby power and shorter start up time. Figure 27 shows start up controlling function block. Figure 28 shows start up relative signal sequence with AUX controlling.

At system power on moment, initial VDD voltage is zero, internal PMOS switch is turn on and external high voltage FET also turn on, C_{VDD} is charged through HV FET till VDD reach V_{DD-ON}. While Internal PMOS switch S1 turn off and VGS of HV FET will close to internal clamping voltage (V_{AUX-CL}) which less than HV FET VGS turn on threshold. Meanwhile VDD energy supplement is turn to auxiliary winding. The voltage gap between VDD and VAUX is keep at 5 V till controller shut−down by protection or VDD touching V_{DD-OFF}.

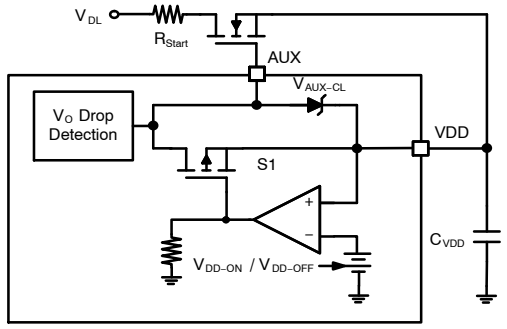


Figure 27. Internal Function for Start Up of AUX PIN

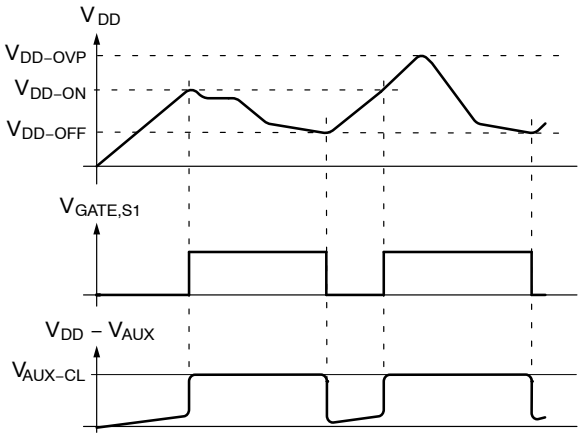


Figure 28. Start Up Sequence With AUX Controlling

Accurately Constant Current (CC) Compensation

FAN105A provides accurate constant current with universal line voltage range, In order to achieve this accurately output current regulated, FAN105A build in circuits that compensate a DC level at CS signal based on difference line voltage. It could avoid output current gap of difference line voltage during constand current controlling. For noise immunity, the recommendation of CS pin series resistor is 10 Ω.

ORDERING INFORMATION

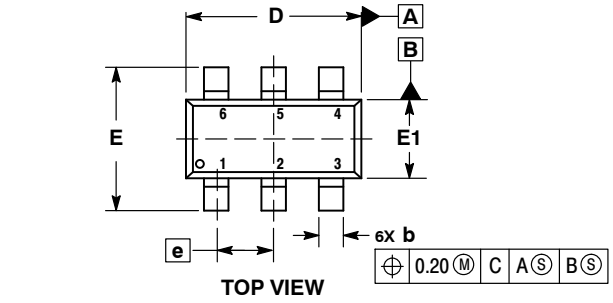
Part Number	Operating Temperature Range	Package	Shipping†
FAN105AM6X	−40°C ~125°C	SOT−23, 6 Lead (Pb−Free)	3000 / Tape & Reel

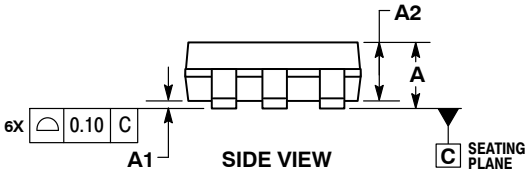
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

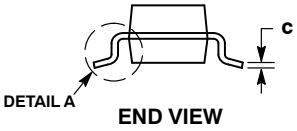
SOT−23, 6 Lead
CASE 527AJ
ISSUE B

DATE 29 FEB 2012

SCALE 2:1



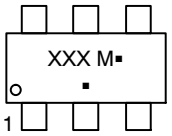




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DATUM C IS THE SEATING PLANE.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.20	0.50
c	0.08	0.26
D	2.70	3.00
E	2.50	3.10
E1	1.30	1.80
e	0.95 BSC	
L	0.20	0.60
L2	0.25 BSC	

GENERIC MARKING DIAGRAM*

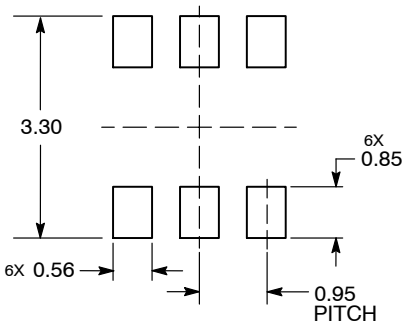


XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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