

ESD8018

ESD Protection Diode

Low Capacitance Array for High Speed Data Lines

The ESD8018 surge protection is specifically designed to protect four high speed data points from ESD. Ultra-low capacitance and low ESD clamping voltage make this device an ideal solution for protecting voltage sensitive high speed data lines. The flow-through style package allows for easy PCB layout and matched trace lengths necessary to maintain consistent impedance between high speed differential lines.

Features

- Low Capacitance (0.32 pF Max, I/O to GND)
- Protection for the Following IEC Standards:
 - IEC 61000-4-2 (Level 4)
 - IEC 61000-4-5 (Lightning) 5A (8/20 μ s)
- Low ESD Clamping Voltage
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- V-by-One HS
- LVDS
- USB 3.1 Type C
- 10 GbE

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|-----------|-------------|------------------|
| Operating Junction Temperature Range | T_J | -55 to +125 | $^\circ\text{C}$ |
| Storage Temperature Range | T_{stg} | -55 to +150 | $^\circ\text{C}$ |
| Lead Solder Temperature - Maximum (10 Seconds) | T_L | 260 | $^\circ\text{C}$ |
| IEC 61000-4-2 Contact (ESD) | ESD | ± 17 | kV |
| IEC 61000-4-2 Air (ESD) | ESD | ± 17 | kV |
| Maximum Peak Pulse Current 8/20 μ s @ $T_A = 25^\circ\text{C}$ (I/O-GND) | I_{pp} | 5.0 | A |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

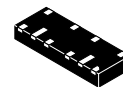
See Application Note AND8308/D for further description of survivability specs.



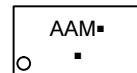
ON Semiconductor®

www.onsemi.com

MARKING DIAGRAM



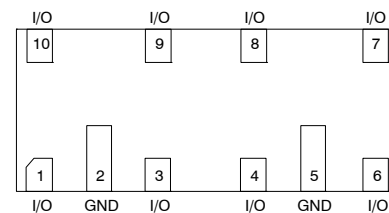
UDFN10
CASE 517CY



- AA = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

PIN CONFIGURATION

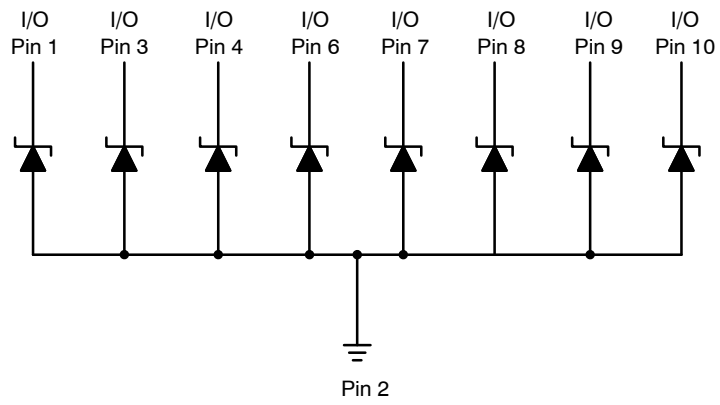


ORDERING INFORMATION

| Device | Package | Shipping |
|--------------|------------------|--------------------|
| ESD8018MUTAG | UDFN10 (Pb-Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ESD8018



Note: Common GND – Only Minimum of 1 GND connection required

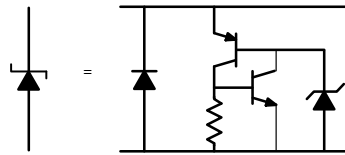


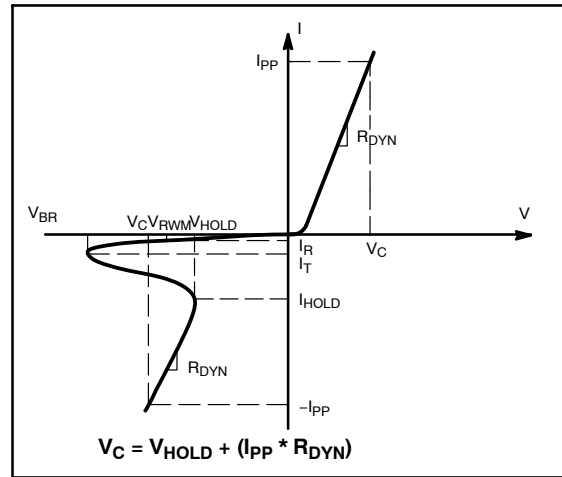
Figure 1. Pin Schematic

ESD8018

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

| Symbol | Parameter |
|-------------------|--|
| V _{RWM} | Working Peak Voltage |
| I _R | Maximum Reverse Leakage Current @ V _{RWM} |
| V _{BR} | Breakdown Voltage @ I _T |
| I _T | Test Current |
| V _{HOLD} | Holding Reverse Voltage |
| I _{HOLD} | Holding Reverse Current |
| R _{DYN} | Dynamic Resistance |
| I _{PP} | Maximum Peak Pulse Current |
| V _C | Clamping Voltage @ I _{PP} V _C = V _{HOLD} + (I _{PP} * R _{DYN}) |



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit | | | | | | | | |
|--|-------------------|--|--|--------------|--|--|--|---|---|-------------------------|------------------------------|-------------|--|---|
| Reverse Working Voltage | V _{RWM} | I/O Pin to GND | | | 3.3 | V | | | | | | | | |
| Breakdown Voltage | V _{BR} | I _T = 1 mA, I/O Pin to GND | 5.5 | 7.0 | | V | | | | | | | | |
| Reverse Leakage Current | I _R | V _{RWM} = 3.3 V, I/O Pin to GND | | | 1.0 | μA | | | | | | | | |
| Holding Reverse Voltage | V _{HOLD} | I/O Pin to GND | | 1.19 | | V | | | | | | | | |
| Holding Reverse Current | I _{HOLD} | I/O Pin to GND | | 25 | | mA | | | | | | | | |
| Clamping Voltage (Note 1) | V _C | IEC61000-4-2, ±8 kV Contact | See Figures 2 and 3 | | | V | | | | | | | | |
| Clamping Voltage | V _C | I _{PP} = 1 A, Any I/O to GND (8/20 μs pulse) | | 1.7 | | V | | | | | | | | |
| Clamping Voltage | V _C | I _{PP} = 5 A, Any I/O to GND (8/20 μs pulse) | | 4.8 | | V | | | | | | | | |
| Clamping Voltage TLP (Note 2) See Figures 6 through 9 | V _C | <table style="display: inline-table; border: none;"> <tr> <td style="padding-right: 5px;">I_{PP} = 8 A</td> <td rowspan="2" style="font-size: 2em; padding: 0 5px;">}</td> <td rowspan="2">IEC 61000-4-2 Level 2 equivalent (±4 kV Contact, ±4 kV Air)</td> </tr> <tr> <td>I_{PP} = -8 A</td> </tr> <tr> <td style="padding-right: 5px;">I_{PP} = 16 A</td> <td rowspan="2" style="font-size: 2em; padding: 0 5px;">}</td> <td rowspan="2">IEC 61000-4-2 Level 4 equivalent (±8 kV Contact, ±15 kV Air)</td> </tr> <tr> <td>I_{PP} = -16 A</td> </tr> </table> | I _{PP} = 8 A | } | IEC 61000-4-2 Level 2 equivalent (±4 kV Contact, ±4 kV Air) | I _{PP} = -8 A | I _{PP} = 16 A | } | IEC 61000-4-2 Level 4 equivalent (±8 kV Contact, ±15 kV Air) | I _{PP} = -16 A | | 4.9 -5.0 | | V |
| I _{PP} = 8 A | } | IEC 61000-4-2 Level 2 equivalent (±4 kV Contact, ±4 kV Air) | | | | | | | | | | | | |
| I _{PP} = -8 A | | | | | | | | | | | | | | |
| I _{PP} = 16 A | } | IEC 61000-4-2 Level 4 equivalent (±8 kV Contact, ±15 kV Air) | | | | | | | | | | | | |
| I _{PP} = -16 A | | | | | | | | | | | | | | |
| Dynamic Resistance | R _{DYN} | I/O Pin to GND GND to I/O Pin | | 0.44 0.49 | | Ω | | | | | | | | |
| Junction Capacitance | C _J | <table style="display: inline-table; border: none;"> <tr> <td style="padding-right: 5px;">V_R = 0 V, f = 1 MHz between I/O Pins and GND</td> <td rowspan="4" style="font-size: 2em; padding: 0 5px;">}</td> <td rowspan="4"></td> </tr> <tr> <td>V_R = 0 V, f = 2.5 GHz between I/O Pins and GND</td> </tr> <tr> <td>V_R = 0 V, f = 5.0 GHz between I/O Pins and GND</td> </tr> <tr> <td>V_R = 0 V, f = 1 MHz, between I/O Pins</td> </tr> </table> | V _R = 0 V, f = 1 MHz between I/O Pins and GND | } | | V _R = 0 V, f = 2.5 GHz between I/O Pins and GND | V _R = 0 V, f = 5.0 GHz between I/O Pins and GND | V _R = 0 V, f = 1 MHz, between I/O Pins | | | 0.32 0.25 0.25 0.16 | pF | | |
| V _R = 0 V, f = 1 MHz between I/O Pins and GND | } | | | | | | | | | | | | | |
| V _R = 0 V, f = 2.5 GHz between I/O Pins and GND | | | | | | | | | | | | | | |
| V _R = 0 V, f = 5.0 GHz between I/O Pins and GND | | | | | | | | | | | | | | |
| V _R = 0 V, f = 1 MHz, between I/O Pins | | | | | | | | | | | | | | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- For test procedure see Figures 4 and 5 and application note AND8307/D.
- ANSI/ESD STM5.5.1 – Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.
TLP conditions: Z₀ = 50 Ω, t_p = 100 ns, t_r = 4 ns, averaging window; t₁ = 30 ns to t₂ = 60 ns.

ESD8018

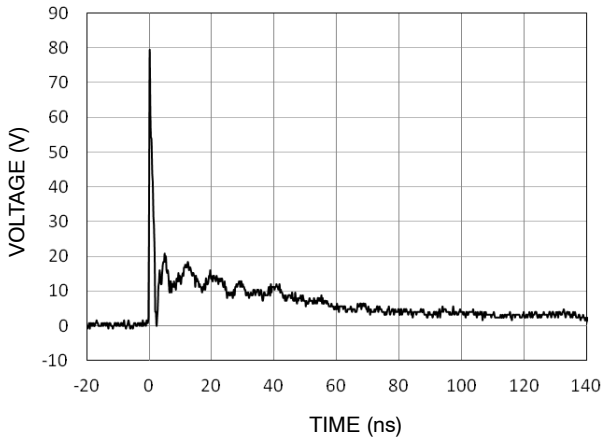


Figure 2. IEC61000-4-2 +8 kV Contact ESD Clamping Voltage

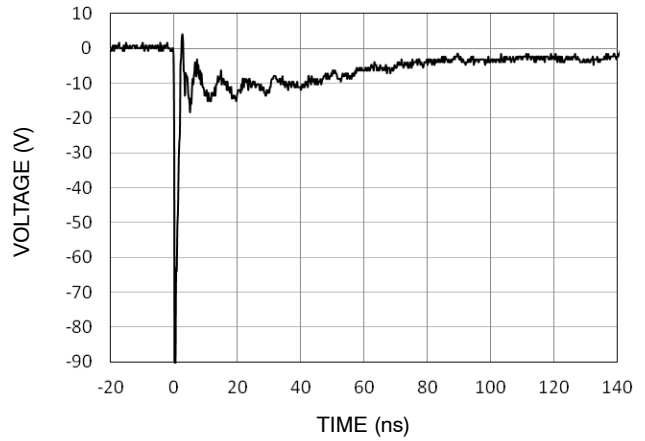


Figure 3. IEC61000-4-2 -8 kV Contact Clamping Voltage

IEC 61000-4-2 Spec.

| Level | Test Voltage (kV) | First Peak Current (A) | Current at 30 ns (A) | Current at 60 ns (A) |
|-------|-------------------|------------------------|----------------------|----------------------|
| 1 | 2 | 7.5 | 4 | 2 |
| 2 | 4 | 15 | 8 | 4 |
| 3 | 6 | 22.5 | 12 | 6 |
| 4 | 8 | 30 | 16 | 8 |

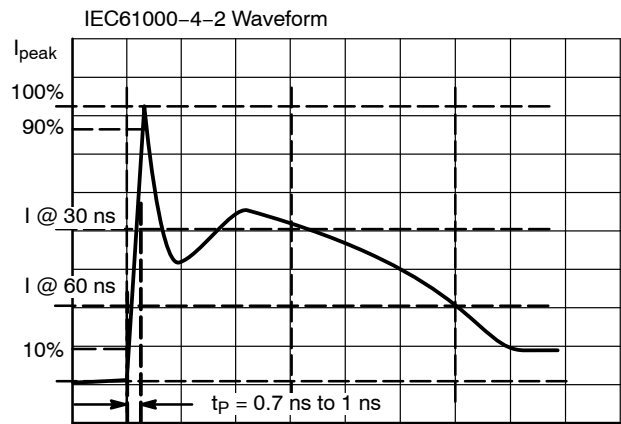


Figure 4. IEC61000-4-2 Spec

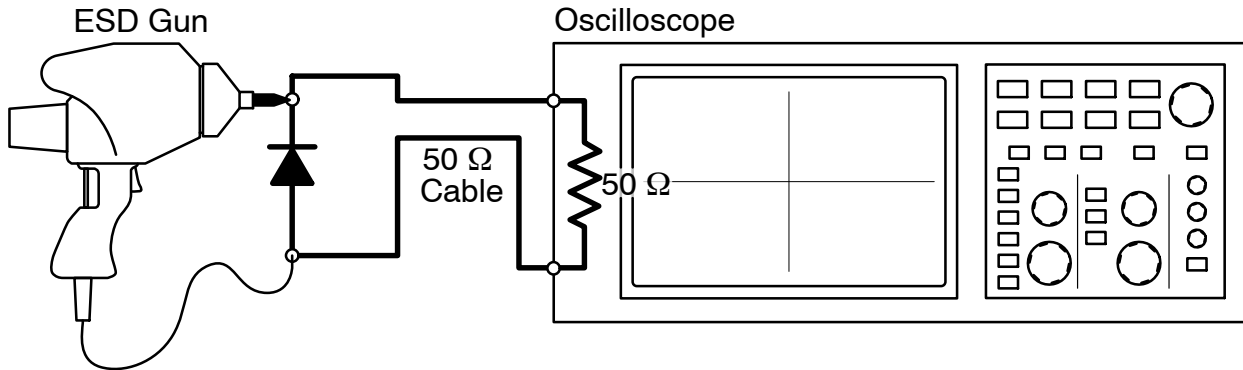


Figure 5. Diagram of ESD Clamping Voltage Test Setup

The following is taken from Application Note AND8307/D – Characterization of ESD Clamping Performance.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger

systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D and AND8308/D.

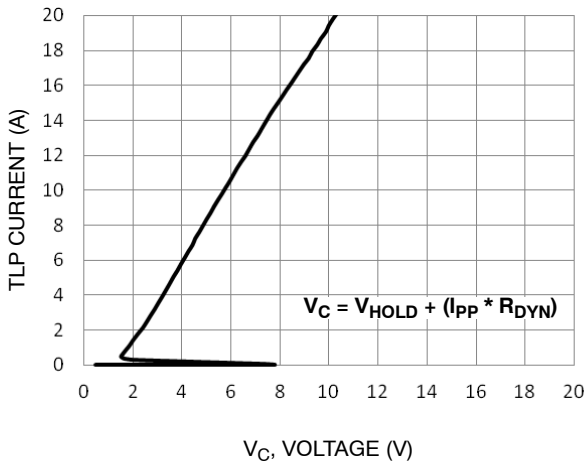


Figure 6. Positive TLP I-V Curve

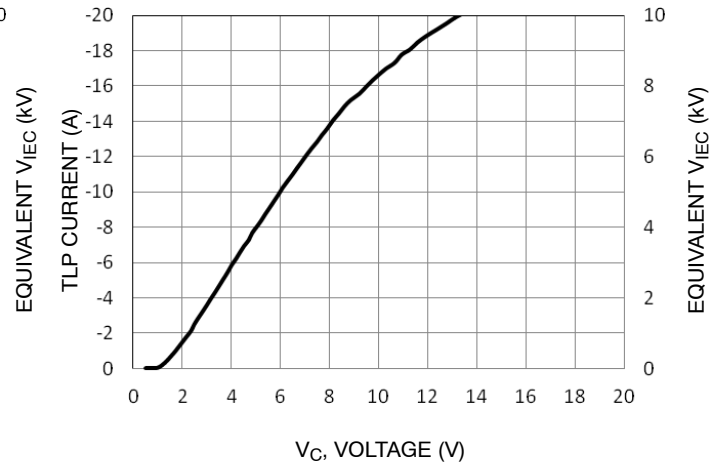


Figure 7. Negative TLP I-V Curve

NOTE: TLP parameter: $Z_0 = 50 \Omega$, $t_p = 100 \text{ ns}$, $t_r = 300 \text{ ps}$, averaging window: $t_1 = 30 \text{ ns}$ to $t_2 = 60 \text{ ns}$. V_{IEC} is the equivalent voltage stress level calculated at the secondary peak of the IEC 61000-4-2 waveform at $t = 30 \text{ ns}$ with 2 A/kV . See TLP description below for more information.

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I-V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 8. TLP I-V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 9 where an 8 kV IEC 61000-4-2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I-V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels. For more information on TLP measurements and how to interpret them please refer to AND9007/D.

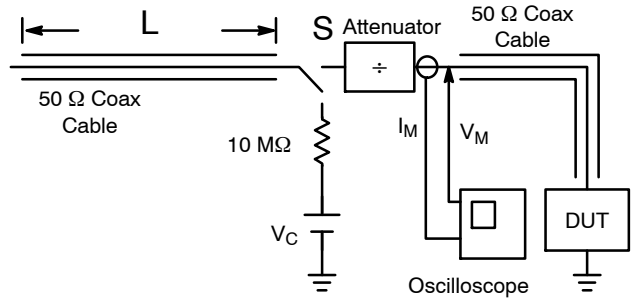


Figure 8. Simplified Schematic of a Typical TLP System

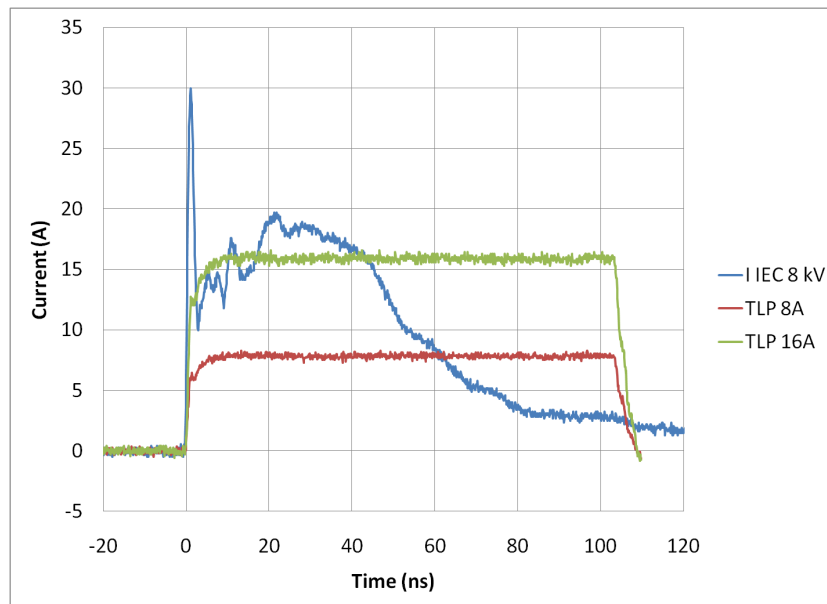


Figure 9. Comparison Between 8 kV IEC 61000-4-2 and 8 A and 16 A TLP Waveforms

ESD8018

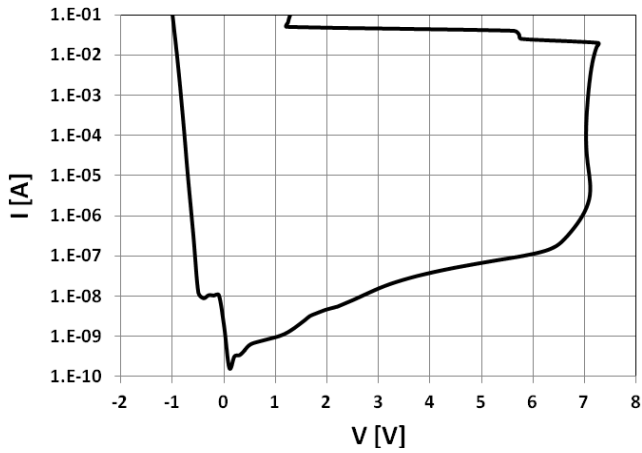


Figure 10. IV Characteristics

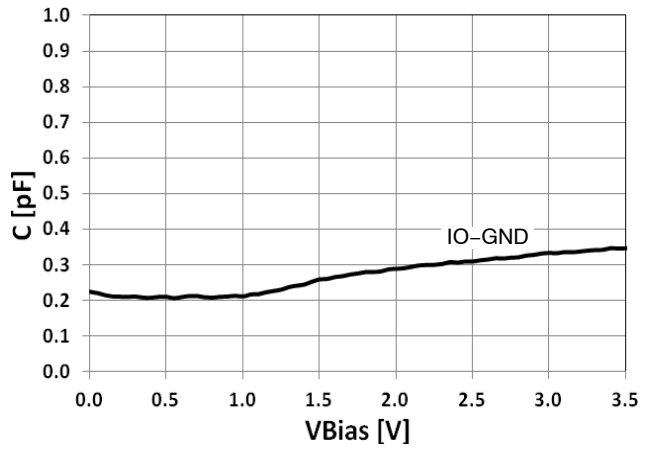


Figure 11. CV Characteristics

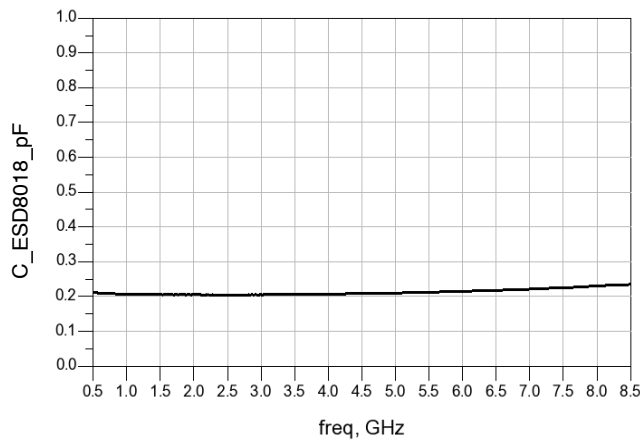


Figure 12. Capacitance over Frequency

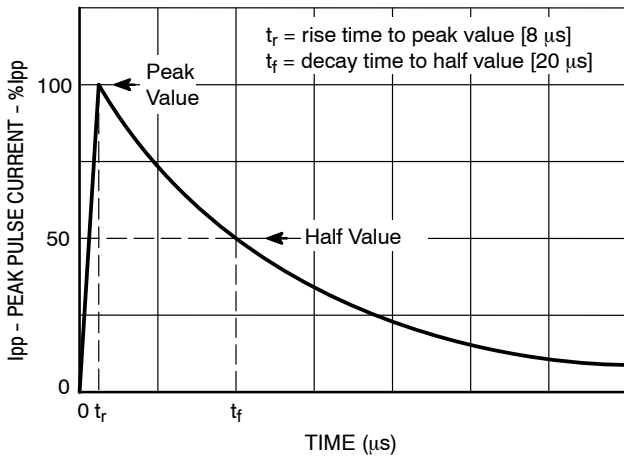


Figure 13. IEC61000-4-5 8/20 μ s Pulse Waveform

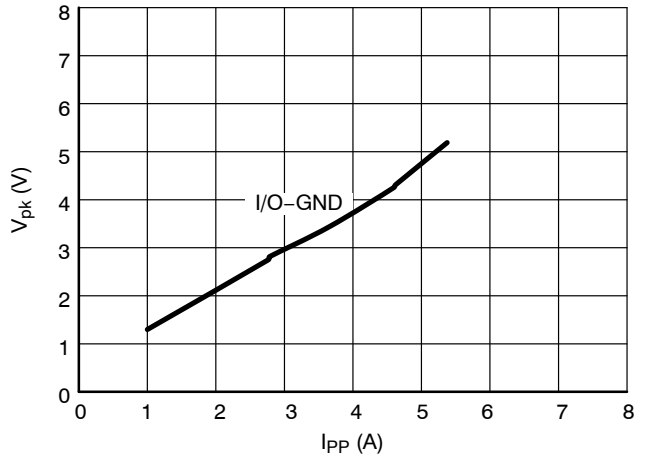


Figure 14. Clamping Voltage vs. Peak Pulse Current ($t_p = 8/20 \mu$ s per Figure 13)

ESD8018

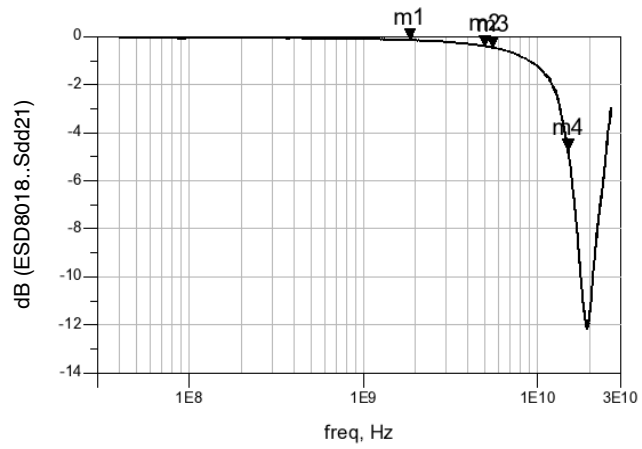


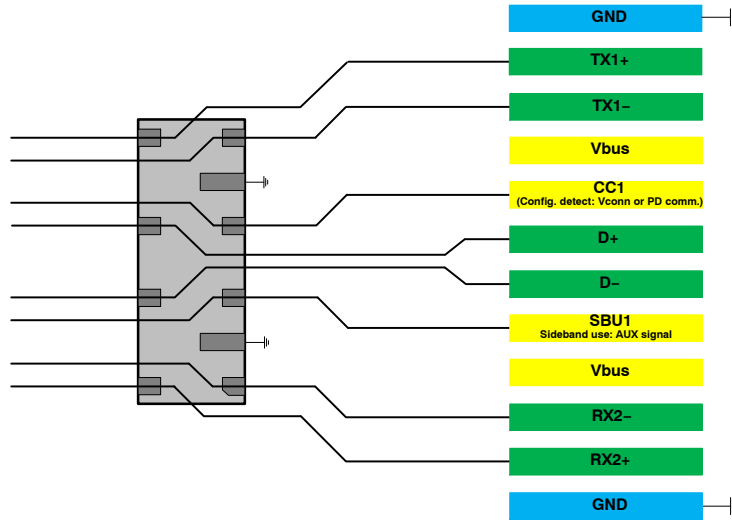
Figure 15. RF Insertion Loss

TABLE 1. RF Insertion Loss: Application Description

| Interface | Data Rate (Gb/s) | Fundamental Frequency (GHz) | 3 rd Harmonic Frequency (GHz) | ESD8018 Insertion Loss (dB) |
|--|------------------|-----------------------------|--|-----------------------------|
| V-by-One HS Full HD (1920 x 1080p) 240 Hz, 36bit color depth | 3.71 | 1.854 (m1) | 5.562 (m3) | m1 = 0.146 m3 = 0.451 |
| USB 3.1 | 10 | 5.0 (m2) | 15 (m4) | M2 = 0.240 m4 = 5.000 |

ESD8018

Type-C Hybrid Top Mount Connector Top Layer



Type-C Hybrid Top Mount Connector Bottom Layer

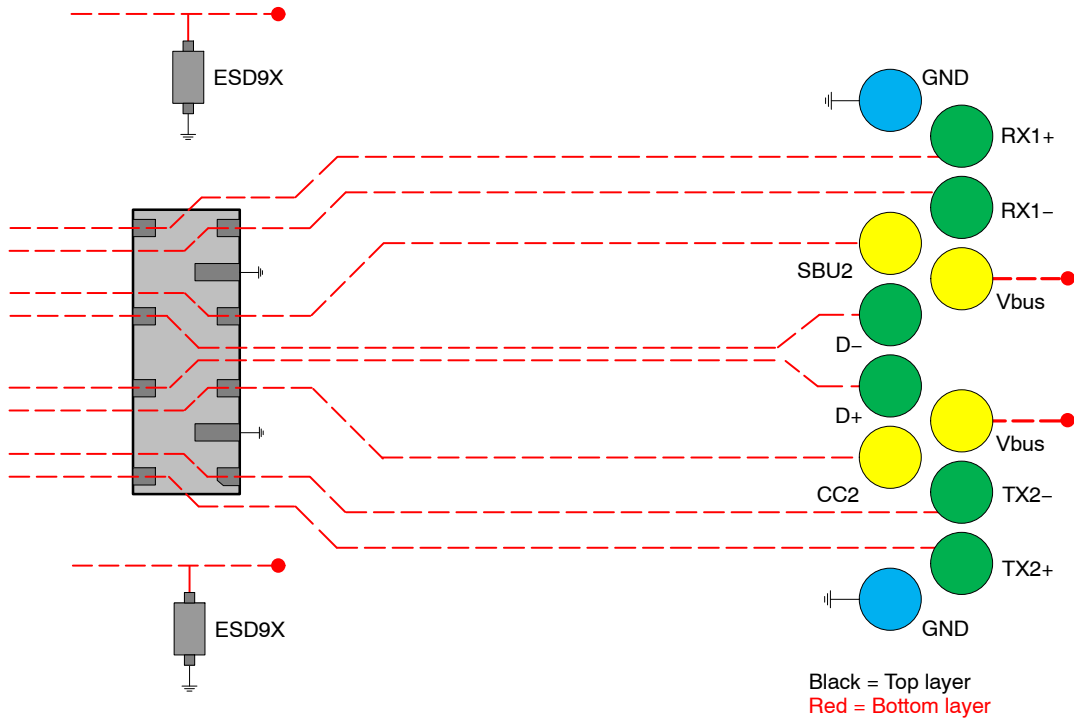


Figure 16. USB 3.1 Type-C Layout Diagram

ESD8018

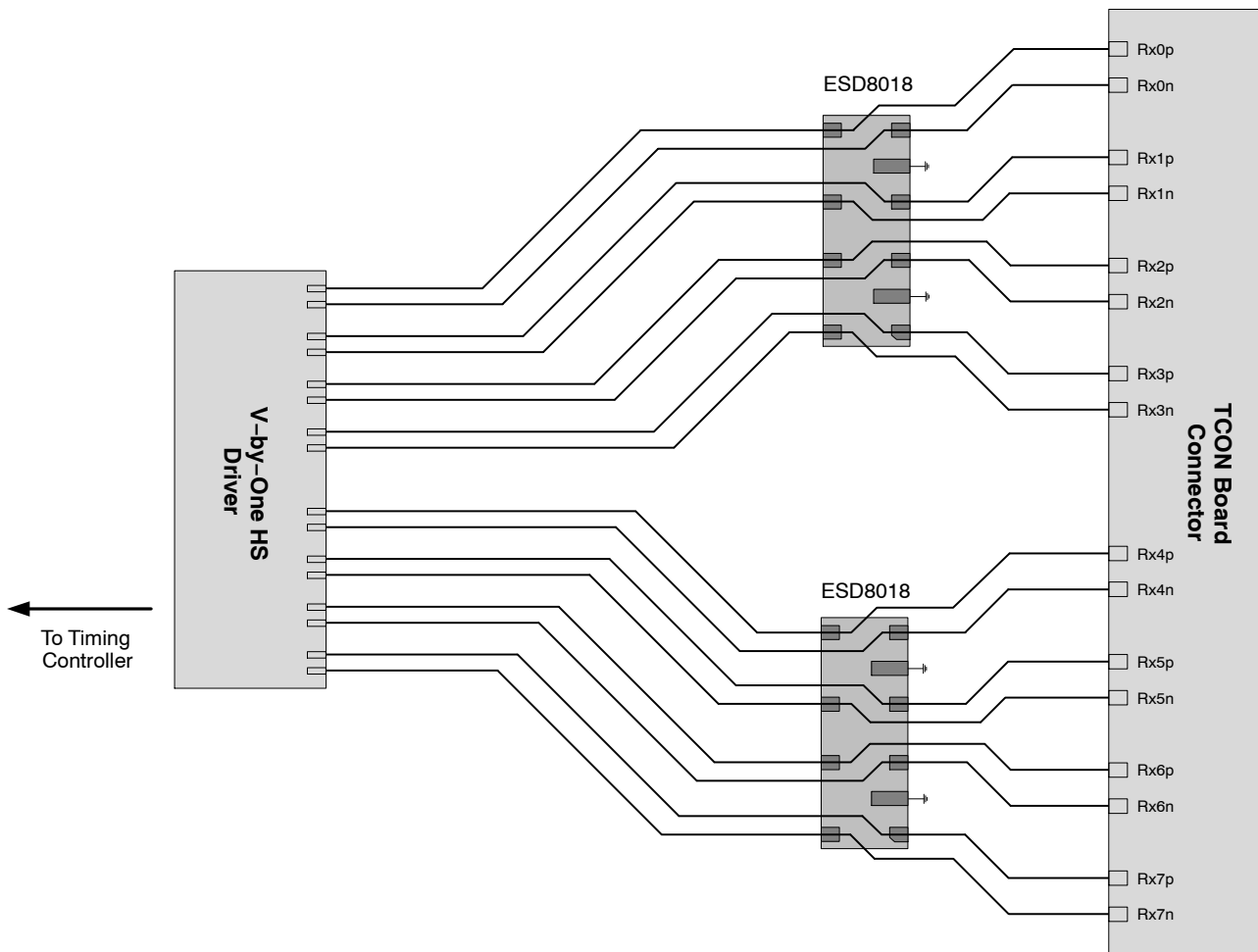


Figure 17. V-by-One HS Layout Diagram (for LCD Panel)

PCB Layout Guidelines

Steps must be taken for proper placement and signal trace routing of the ESD protection device in order to ensure the maximum ESD survivability and signal integrity for the application. Such steps are listed below.

- Place the ESD protection device as close as possible to the I/O connector to reduce the ESD path to ground and improve the protection performance.
 - ◆ In USB 3.1 applications, the ESD protection device should be placed between the AC coupling capacitors and the I/O connector on the TX differential lanes. In this configuration, no DC current can flow through the ESD protection device preventing any potential latch-up condition.
- Make sure to use differential design methodology and impedance matching of all high speed signal traces.
 - ◆ Use curved traces when possible to avoid unwanted reflections.
 - ◆ Keep the trace lengths equal between the positive and negative lines of the differential data lanes to avoid common mode noise generation and impedance mismatch.
 - ◆ Place grounds between high speed pairs and keep as much distance between pairs as possible to reduce crosstalk.

Latch-Up Considerations

ON Semiconductor’s 8000 series of ESD protection devices utilize a snap-back, SCR type structure. By using this technology, the potential for a latch-up condition was taken into account by performing load line analyses of common high speed serial interfaces. Example load lines for latch-up free applications and applications with the potential for latch-up are shown below with a generic IV characteristic of a snapback, SCR type structured device overlaid on each. In the latch-up free load line case, the IV characteristic of the snapback protection device intersects the load-line in one unique point (V_{OP} , I_{OP}). This is the only stable operating point of the circuit and the system is

therefore latch-up free. Please note that for USB 3.1 applications, ESD8018 latch-up free considerations are explained in more detail in the above PCB guidelines. In the non-latch up free load line case, the IV characteristic of the snapback protection device intersects the load-line in two points (V_{OPA} , I_{OPA}) and (V_{OPB} , I_{OPB}). Therefore in this case, the potential for latch-up exists if the system settles at (V_{OPB} , I_{OPB}) after a transient. Because of this, ESD8018 should not be used for HDMI applications – ESD8114 or ESD8040 have been designed to be acceptable for HDMI applications without latch-up. Please refer to Application Note AND9116/D for a more in-depth explanation of latch-up considerations using ESD8000 series devices.

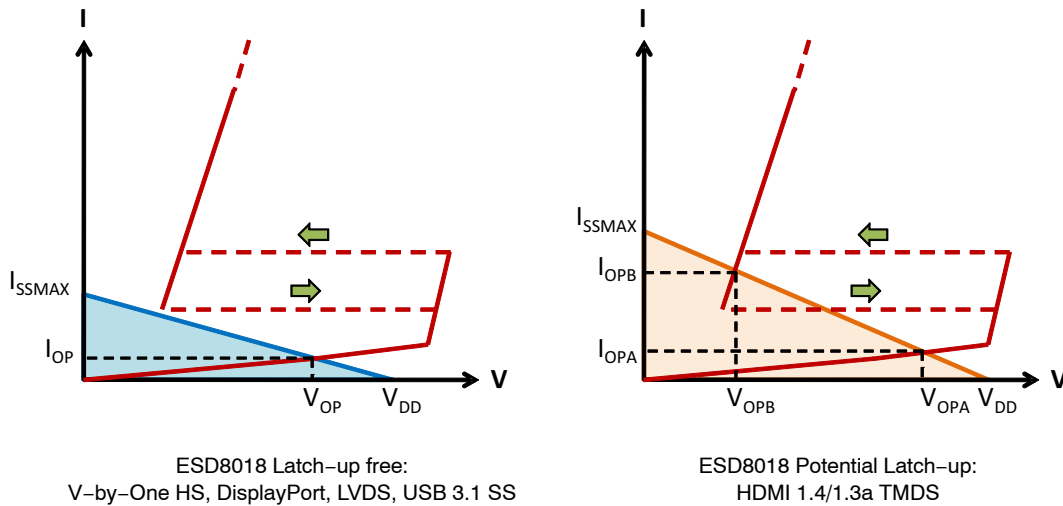


Figure 18. Example Load Lines for Latch-up Free Applications and Applications with the Potential for Latch-up

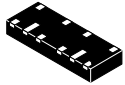
Table 1. SUMMARY OF SCR REQUIREMENTS FOR LATCH-UP FREE APPLICATIONS

| Application | VBR (min) (V) | IH (min) (mA) | VH (min) (V) | ON Semiconductor ESD8000 Series Recommended PN |
|--------------------|---------------|---------------|--------------|--|
| HDMI 1.4/1.3a TMDS | 3.465 | 54.78 | 1.0 | ESD8040 |
| DisplayPort | 3.600 | 25.00 | 1.0 | ESD8016, ESD8018 |
| V-by-One HS | 1.980 | 21.70 | 1.0 | ESD8018 |
| LVDS | 1.829 | 9.20 | 1.0 | ESD8018 |
| USB 3.1 SS | 2.800 | N/A | 1.0 | ESD8016, ESD8018 |

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

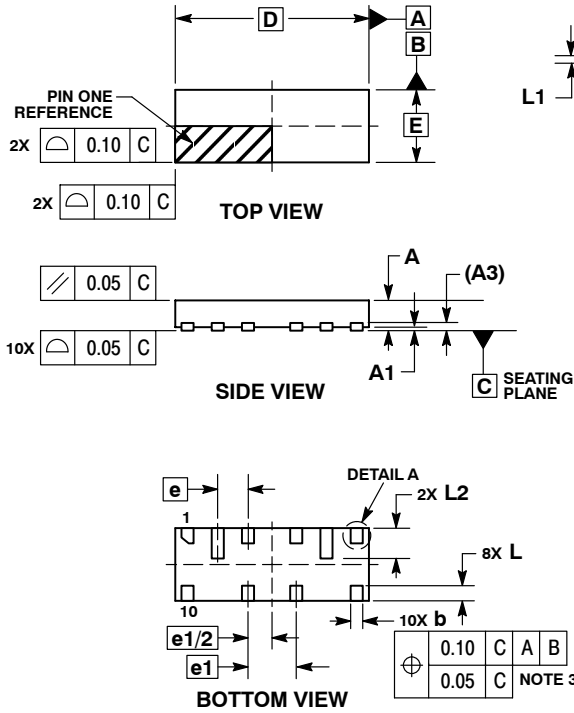
ON Semiconductor®



SCALE 4:1

UDFN10 3.2x1.2, 0.5P
CASE 517CY
ISSUE O

DATE 31 JUL 2014

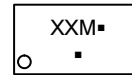


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 mm FROM TERMINAL.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 0.45 | 0.55 |
| A1 | 0.00 | 0.05 |
| A3 | 0.13 | REF |
| b | 0.15 | 0.25 |
| D | 3.20 | BSC |
| E | 1.20 | BSC |
| e | 0.50 | BSC |
| e1 | 0.80 | BSC |
| L | 0.15 | 0.35 |
| L1 | --- | 0.10 |
| L2 | 0.40 | 0.60 |

GENERIC MARKING DIAGRAM*

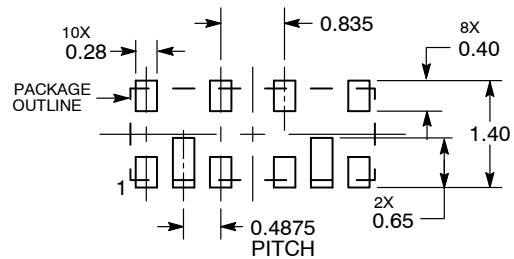


- XX = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G", may or not be present.

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | |
|-------------------------|-----------------------------|--|
| DOCUMENT NUMBER: | 98AON88711F | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | UDFN10 3.2X1.2, 0.5P | PAGE 1 OF 1 |

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales