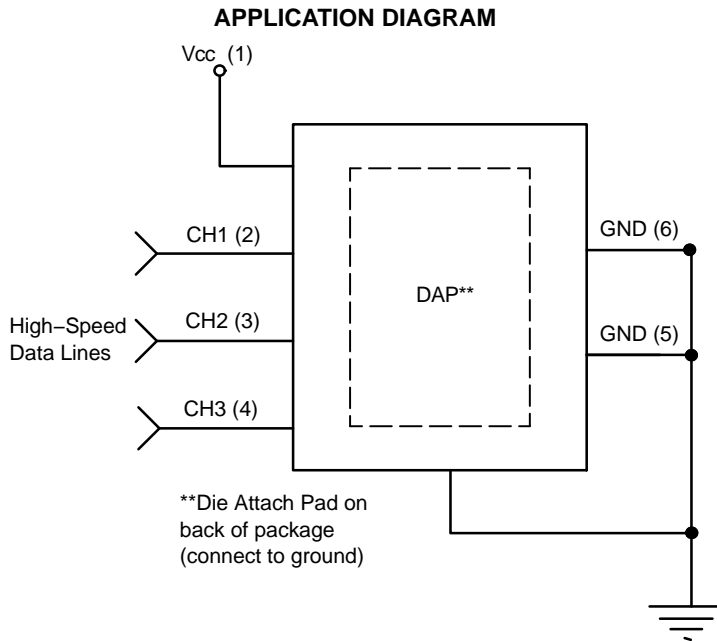


# ESD7124

## 4-Channel Low Capacitance Dual-Voltage ESD and Surge Protection Array

### Features

- 3 Channels of Low Voltage ESD Protection
- 1 Channel of High Voltage ESD Protection
- Provides ESD Protection to IEC61000-4-2 Level 4:  $\pm 25$  kV Contact Discharge
- IEC 61000-4-5 (lighting)
- Low Channel Input Capacitance
- High Voltage Zener Diode Protects Supply Rail up to 100 A (8/20  $\mu$ s)
- These Devices are Pb-Free and are RoHS Compliant



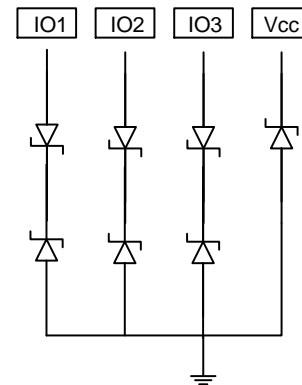
**ON Semiconductor®**

<http://onsemi.com>



**UDFN-6  
D4 SUFFIX  
CASE 517CS**

### BLOCK DIAGRAM



### MARKING DIAGRAM



AD = Specific Device Code  
M = Date Code  
■ = Pb-Free Package

### ORDERING INFORMATION

Device	Package	Shipping†
ESD7124MUTBG	UDFN-6 (Pb-Free)	3000/Tape & Reel

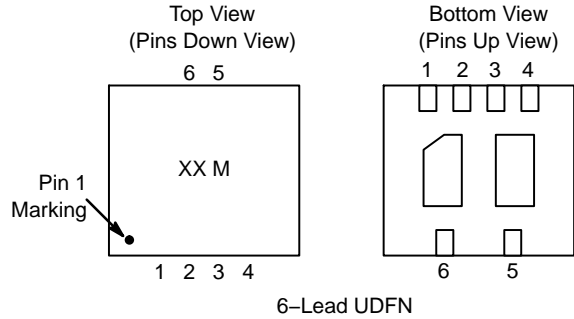
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# ESD7124

**Table 1. PIN DESCRIPTIONS**

4-Channel, 6-Lead, UDFN-8 Package			
Pin	Name	Type	Description
1	V <sub>CC</sub>	HV V <sub>DD</sub>	HV ESD Channel
2	CH1	I/O	LV Low-capacitance ESD Channel
3	CH2	I/O	LV Low-capacitance ESD Channel
4	CH3	I/O	LV Low-capacitance ESD Channel
5	GND		Ground
6	GND		Ground

**PACKAGE / PINOUT DIAGRAMS**



**SPECIFICATIONS**

**Table 2. ABSOLUTE MAXIMUM RATINGS**

Parameter	Rating	Units
Operating Temperature Range	-55 to +125	°C
Storage Temperature Range	-65 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**Table 3. ELECTRICAL CHARACTERISTICS**

Device Name	Reverse Working Voltage	Breakdown Voltage V <sub>br</sub> (V)		Reverse Current Leakage I <sub>r</sub> (μA)	R <sub>dyn</sub>	Junction Capacitance C <sub>j</sub> (pF)	
	V <sub>rwm</sub> (V)	at 1 mA		at V <sub>rwm</sub>	Ω	V <sub>r</sub> = 0 V, f = 1 MHz	
	Max	Min	Typ	Max	Typ	Typ	Max
Pin2-4 (LV)	3.3	5.5	6.5	1	1	0.35	0.5
Pin1 (HV)	12	13.3	14	1			

Device Name	Clamping Voltage V <sub>c</sub> (V) t <sub>p</sub> = 8 x 20 μs		Max Ratings t <sub>p</sub> = 8 x 20 μs	
	I <sub>pp</sub> = 1 A	I <sub>pp</sub> = 16 A	I <sub>pp</sub> (A)	V <sub>c</sub> @ Max I <sub>pp</sub> (V)
	Typ	Typ	Max	Max
Pin1 (HV)	15	16	100	27
Pin2-4 (LV)	9.5			

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Clamping Voltage TLP (Note 1) All Devices Pin2-4(LV) See Figures 3 – 6	V <sub>C</sub>	I <sub>PP</sub> = ±8 A } IEC 61000-4-2 Level 2 equivalent (±4 kV Contact, ±4 kV Air)		16.8		V
		I <sub>PP</sub> = ±16 A } IEC 61000-4-2 Level 4 equivalent (±8 kV Contact, ±15 kV Air)		24.9		

1. ANSI/ESD STM5.5.1 – Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.  
TLP conditions: Z<sub>0</sub> = 50 Ω, t<sub>p</sub> = 100 ns, t<sub>r</sub> = 4 ns, averaging window; t<sub>1</sub> = 30 ns to t<sub>2</sub> = 60 ns.

# ESD7124

## TYPICAL CHARACTERISTICS

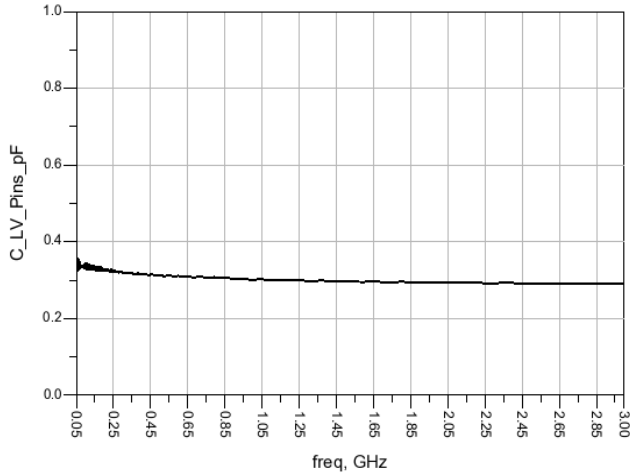


Figure 1. Capacitance Over Frequency

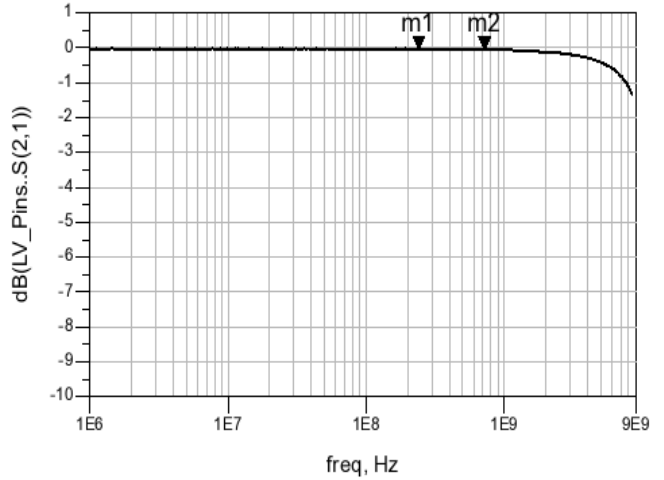


Figure 2. Insertion Loss

Interface	Data Rate (Mb/s)	Fundamental Frequency (MHz)	3 <sup>rd</sup> Harmonic Frequency (MHz)	ESD7124 Insertion Loss (dB)
USB 2.0	480	240 (m1)	720 (m2)	m1 = 0.031 m2 = 0.047

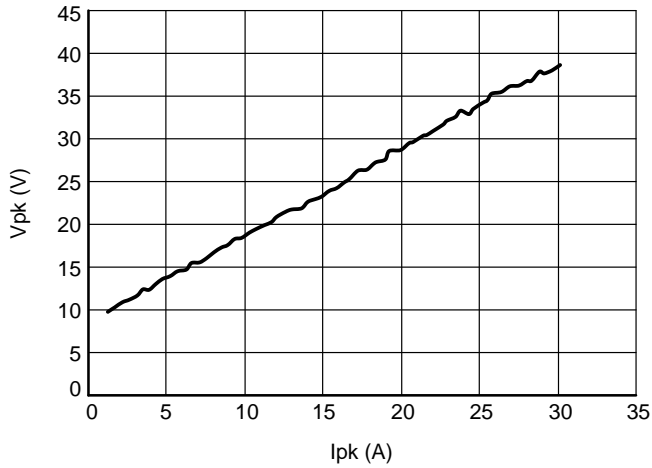


Figure 3. Positive TLP I-V Curve

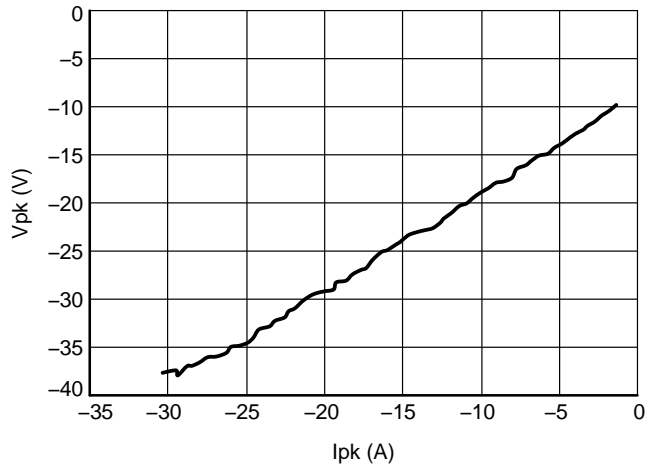
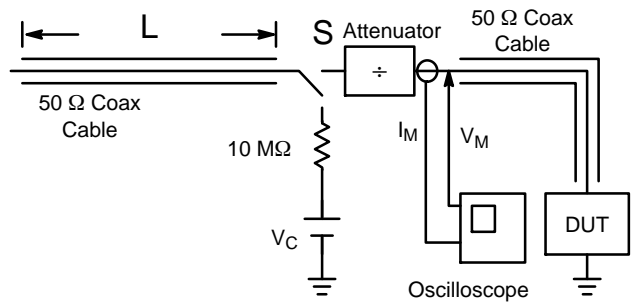


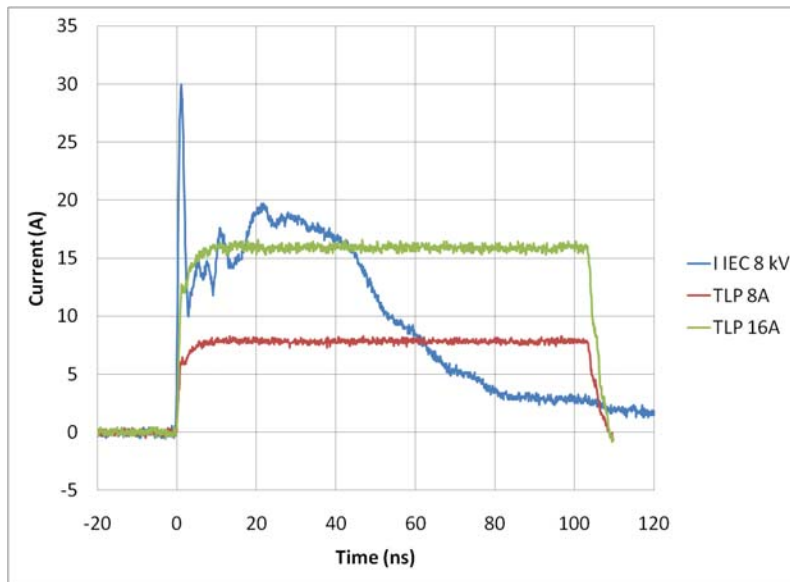
Figure 4. Negative TLP I-V Curve

**Transmission Line Pulse (TLP) Measurement**

Transmission Line Pulse (TLP) provides current versus voltage (I-V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 5. TLP I-V curves of ESD protection devices accurately demonstrate the product’s ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 6 where an 8 kV IEC 61000-4-2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I-V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels. For more information on TLP measurements and how to interpret them please refer to AND9007/D.



**Figure 5. Simplified Schematic of a Typical TLP System**



**Figure 6. Comparison Between 8 kV IEC 61000-4-2 and 8 A and 16 A TLP Waveforms**

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

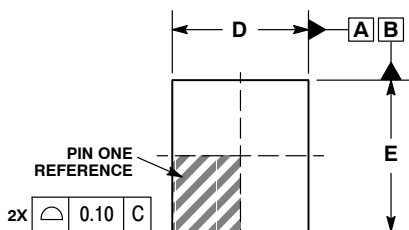
ON Semiconductor®



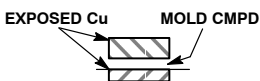
SCALE 4:1

## UDFN6, 1.8x2, 0.4P CASE 517CS ISSUE 0

DATE 30 APR 2013



TOP VIEW

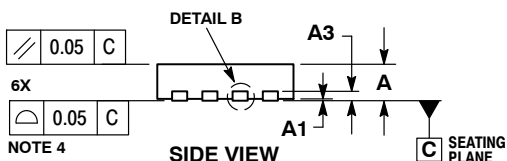


DETAIL B  
ALTERNATE  
CONSTRUCTION

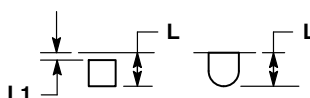
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.125 REF	
b	0.15	0.25
D	1.80 BSC	
D2	0.35	0.55
E	2.00 BSC	
E2	0.74	0.94
e	0.40 BSC	
e1	0.80 BSC	
e2	0.95 BSC	
L	0.20	0.40
L1	---	0.15



SIDE VIEW



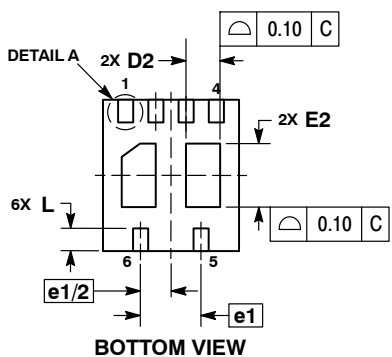
DETAIL A  
ALTERNATE  
CONSTRUCTIONS

### GENERIC MARKING DIAGRAM\*

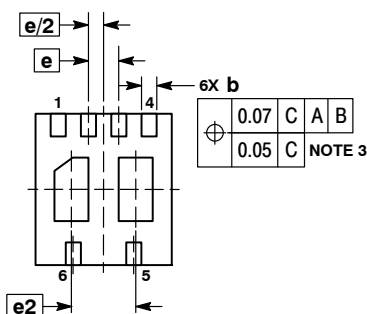


XX = Specific Device Code  
M = Date Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

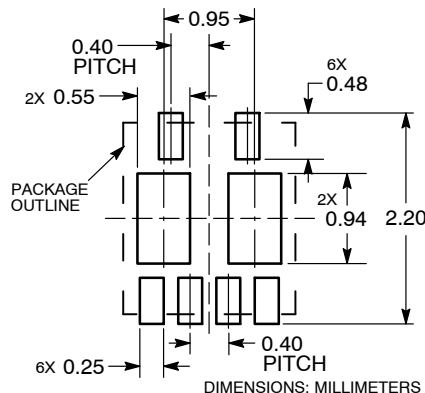


BOTTOM VIEW



SUPPLEMENTAL  
BOTTOM VIEW

### RECOMMENDED MOUNTING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON89602E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	UDFN6 1.8X2, 0.4P	PAGE 1 OF 1

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at [www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)