TSU111IY, TSU112IY

Datasheet

Automotive grade, nanopower (920 nA), high accuracy (150 µV) 5 V CMOS operational amplifier

TSU111IYLT
TSU111RILT
SOT23-5

TSU111IYCT
SC70-5

TSU112IYQ3T
DFN8 (2x2 mm WF)

TSU112IYST
MiniSO8

Product status link
TSU111IY, TSU112IY

Related products	
See TSU101, TSU102 and TSU104	For further power savings
See TSZ121, TSZ122 and TSZ124	For increased accuracy

Features

- AEC-Q100 qualified for Y version
- Sub-micro ampere current consumption: I_{CC} = 920 nA typ. at 25 °C
- Low offset voltage: 150 µV max. at 25 °C, 400 µV max. over full temperature range (-40 to 125 °C)
- Low noise over 0.1 to 10 Hz bandwidth: 4.6 µVpp
- Low supply voltage: 1.5 V to 5.5 V
- Rail-to-rail input and output
- Gain bandwidth product: 9 kHz typ.
- Low input bias current: 10 pA max. at 25 °C
- High tolerance to ESD: 4 kV HBM
- More than 25 years of typical equivalent lifetime supplied by a 220 mA.h CR2032 coin type Lithium battery
- High accuracy without calibration
- Tolerance to power supply transient drops

Applications

- Battery management system: ultra-low power op-amp detects when battery is charging/discharging and wakes up CPU
- On-board chargers
- Signal conditioning for energy harvesting
- Wireless chargers

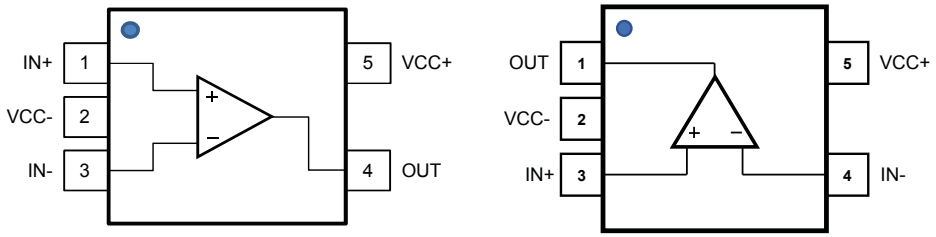
Description

The TSU111IY and TSU112IY operational amplifiers (op-amp) offer an ultra low-power consumption per channel of 920 nA typical and 1.3 µA maximum when supplied by 3.3 V. Combined with a supply voltage range of 1.5 V to 5.5 V, these features allow the TSU111IY and TSU112IY to be efficiently supplied by a coin type Lithium battery or a regulated voltage in low-power applications.

The high accuracy of 150 µV max. and 9 kHz gain bandwidth make the TSU111IY and TSU112IY ideal for sensor signal conditioning, battery management system, on-board (OBC) and wireless chargers.

1 Package pin connections

Figure 1. Pin connections for SC70-5 and SOT23-5 package (top view)



SOT23-5 for TSU111IYLT
SC70-5 for TSU111IYCT

SOT23-5 for TSU111RILT

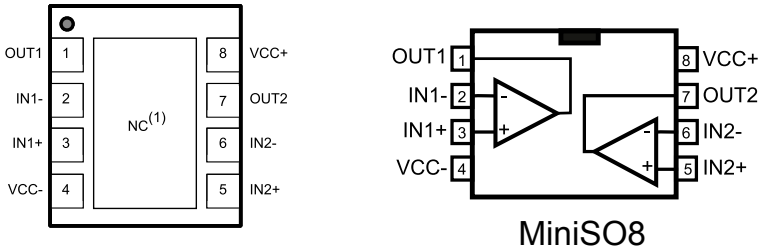
Table 1. Pin description for TSU111IYLT and TSU111IYCT

Pin n°	Pin name	Description
1	IN+	Non-inverting input channel
2	VCC-	Negative supply voltage
3	IN-	Inverting input channel
4	OUT	Output channel
5	VCC+	Positive supply voltage

Table 2. Pin description for TSU111RILT

Pin n°	Pin name	Description
1	OUT	Output channel
2	VCC-	Negative supply voltage
3	IN+	Non-inverting input channel
4	IN-	Inverting input channel
5	VCC+	Positive supply voltage

Figure 2. Pin connections for each package (top view)



DFN8 2x2

MiniSO8

1. The exposed pad of the DFN8 2x2 can be connected to V_{CC-} or left floating.

Table 3. Pin description

Pin n°	Pin name	Description
1	OUT1	Output channel
2	IN1-	Inverting input channel
3	IN1+	Non-inverting input channel
4	VCC-	Negative supply voltage
5	IN2+	Non-inverting input channel
6	IN2-	Inverting input channel
7	OUT2	Output channel
8	VCC+	Positive supply voltage

2 Absolute maximum ratings and operating conditions

Table 4. Absolute maximum ratings (AMR)

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage (1)		6	V
V_{id}	Differential input voltage (2)		$\pm V_{CC}$	
V_{in}	Input voltage (3)		$(V_{CC-}) - 0.2$ to $(V_{CC+}) + 0.2$	
I_{in}	Input current (4)		10	mA
T_{stg}	Storage temperature		-65 to 150	°C
T_j	Maximum junction temperature		150	
R_{thja}	Thermal resistance junction-to-ambient (5) (6)	SC70-5	205	°C/W
		SOT23-5	250	
		DFN8 2x2	57	
		MiniSO8	190	
ESD	HBM: human body model (7)		4000	V
	CDM: charged device model (8)		1500	
	Latch-up immunity (9)		200	mA

1. *All voltage values, except the differential voltage, are with respect to the network ground terminal.*
2. *The differential voltage is the non-inverting input terminal with respect to the inverting input terminal.*
3. *$(V_{CC+}) - V_{in}$ must not exceed 6 V, $V_{in} - (V_{CC-})$ must not exceed 6 V.*
4. *The input current must be limited by a resistor in-series with the inputs.*
5. *R_{th} are typical values.*
6. *Short-circuits can cause excessive heating and destructive dissipation.*
7. *HBM test according to the standard AEC-Q100-002 and related to ESDA/JEDEC JS-001-2017.*
8. *The test CDM is performed in accordance with the standard AEC-Q100-011 and related to ESDA/JEDEC JS-002-2018.*
9. *Related to JEDEC JESD78E Apr. 2016.*

Table 5. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	1.5 to 5.5	V
V_{icm}	Common-mode input voltage range	$(V_{CC-}) - 0.1$ to $(V_{CC+}) + 0.1$	
T_{oper}	Operating free-air temperature range	-40 to 125	°C

3 Electrical characteristics

Table 6. Electrical characteristics at (V_{CC+}) = 1.8 V with (V_{CC-}) = 0 V, V_{icm} = V_{CC}/2, T_{amb} = 25 °C, and R_L = 1 MΩ connected to V_{CC}/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	T = 25 °C			150	µV
		-40 °C < T< 125 °C			400	
$\Delta V_{io}/\Delta T$	Input offset voltage drift	-40 °C < T< 125 °C			2.5	µV/°C
I_{io}	Input offset current (1)	T = 25 °C		1	2	pA
		-40 °C < T< 125 °C		20	100	
I_{ib}	Input bias current (1)	T = 25 °C		1	2	
		-40 °C < T< 125 °C		75	200	
CMR	Common mode rejection ratio, 20 log ($\Delta V_{icm}/\Delta V_{io}$), V_{icm} = 0 to 1.8 V	T = 25 °C	76	99		dB
		-40 °C < T< 125 °C	71			
A_{vd}	Large signal voltage gain, V_{out} = 0.2 V to (V_{CC+}) - 0.2 V	R_L = 100 kΩ, T = 25 °C	95	120		
		R_L = 100 kΩ, -40 °C < T< 125 °C	82			
V_{OH}	High-level output voltage, (drop from V_{CC+})	R_L = 10 kΩ, T = 25 °C		11	25	mV
		R_L = 10 kΩ, -40 °C < T< 125 °C			40	
V_{OL}	Low-level output voltage	R_L = 10 kΩ, T = 25 °C		9	25	
		R_L = 10 kΩ, -40 °C < T< 125 °C			40	
I_{out}	Output sink current, V_{out} = V_{CC} , V_{ID} = -200 mV	T = 25 °C	2.8	5		mA
		-40 °C < T< 125 °C	1.5			
	Output source current, V_{out} = 0 V, V_{ID} = 200 mV	T = 25 °C	2	4		
		-40 °C < T< 125 °C	1.5			
I_{CC}	Supply current (per channel), no load, V_{out} = V_{CC}/2	T = 25 °C		840	1300	nA
		-40 °C < T< 125 °C			1580	
AC performance						
GBP	Gain bandwidth product	R_L = 1 MΩ, C_L = 60 pF		9		kHz
F_u	Unity gain frequency			5.5		
Φ_m	Phase margin			70		degrees
G_m	Gain margin			30		dB
SRp	Slew rate (10 % to 90 %)	R_L = 1 MΩ, C_L = 60 pF, V_{out} = 0.3 V to (V_{CC+}) - 0.3 V	0.8	1.8		V/ms
SRn	Slew rate (10 % to 90 %)	R_L = 1 MΩ, C_L = 60 pF, V_{out} = 0.3 V to (V_{CC+}) - 0.3 V	1.2	3.0		V/ms
e_n	Equivalent input noise voltage	f = 100 Hz		220		nV/√Hz
$\int e_n$	Low-frequency, peak-to-peak input noise	Bandwidth: f = 0.1 to 10 Hz		4.6		μV_{pp}
t_{rec} P	Overload recovery time (from positive rail)	100 mV from rail in comparator, R_L = 100 kΩ, V_{ID} = ±1 V, -40 °C < T< 125 °C		220		µs
t_{rec} N	Overload recovery time (from negative rail)	100 mV from rail in comparator, R_L = 100 kΩ, V_{ID} = ±1 V, -40 °C < T< 125 °C		430		µs

1. *Guaranteed by design*

Table 7. Electrical characteristics at (V_{CC+}) = 3.3 V with (V_{CC-}) = 0 V, V_{icm} = V_{CC}/2, T_{amb} = 25 °C, and R_L = 1 MΩ connected to V_{CC}/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	T = 25 °C			150	µV
		-40 °C < T< 125 °C			400	
$\Delta V_{io}/\Delta T$	Input offset voltage drift	-40 °C < T< 125 °C			2.5	µV/°C
I_{io}	Input offset current (1)	T = 25 °C		1	2	pA
		-40 °C < T< 125 °C		20	100	
I_{ib}	Input bias current (1)	T = 25 °C		1	2	
		-40 °C < T< 125 °C		75	200	
CMR	Common mode rejection ratio, 20 log ($\Delta V_{icm}/\Delta V_{io}$), V_{icm} = 0 to 3.3 V	T = 25 °C	81	102		dB
		-40 °C < T< 125 °C	76			
A_{vd}	Large signal voltage gain, V_{out} = 0.2 V to (V_{CC+}) - 0.2 V	R_L = 100 kΩ, T = 25 °C	100	128		
		R_L = 100 kΩ, -40 °C < T< 125 °C	88			
V_{OH}	High-level output voltage, (drop from V_{CC}+)	R_L = 10 kΩ, T = 25 °C		11	25	mV
		R_L = 10 kΩ, -40 °C < T< 125 °C			40	
V_{OL}	Low-level output voltage	R_L = 10 kΩ, T = 25 °C		9	25	
		R_L = 10 kΩ, -40 °C < T< 125 °C			40	
I_{out}	Output sink current, V_{out} = V_{CC} , V_{ID} = -200 mV	T = 25 °C	12	22		mA
		-40 °C < T< 125 °C	6			
	Output source current, V_{out} = 0 V, V_{ID} = 200 mV	T = 25 °C	9	17		
		-40 °C < T< 125 °C	5			
I_{CC}	Supply current (per channel), no load, V_{out} = V_{CC}/2	T = 25 °C		920	1300	nA
		-40 °C < T< 125 °C			1650	
AC performance						
GBP	Gain bandwidth product	R_L = 1 MΩ, C_L = 60 pF		9		kHz
F_u	Unity gain frequency			5.5		
Φ_m	Phase margin			70		degrees
G_m	Gain margin			30		dB
SRp	Slew rate (10 % to 90 %)	R_L = 1 MΩ, C_L = 60 pF, V_{out} = 0.3 V to (V_{CC+}) - 0.3 V	0.9	1.8		V/ms
SRn	Slew rate (10 % to 90 %)	R_L = 1 MΩ, C_L = 60 pF, V_{out} = 0.3 V to (V_{CC+}) - 0.3 V	1.5	3.0		V/ms
e_n	Equivalent input noise voltage	f = 100 Hz		200		nV/√Hz
$\int e_n$	Low-frequency, peak-to-peak input noise	Bandwidth: f = 0.1 to 10 Hz		4.6		μV_{pp}
t_{rec} P	Overload recovery time (from positive rail)	100 mV from rail in comparator, R_L = 100 kΩ, V_{ID} = ±1 V, -40 °C < T< 125 °C		420		µs
t_{rec} N	Overload recovery time (from negative rail)	100 mV from rail in comparator, R_L = 100 kΩ, V_{ID} = ±1 V, -40 °C < T< 125 °C		880		µs

1. *Guaranteed by design*

Table 8. Electrical characteristics at (V_{CC+}) = 5 V with (V_{CC-}) = 0 V, V_{icm} = V_{CC}/2, T_{amb} = 25 °C, and R_L = 1 MΩ connected to V_{CC}/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	T = 25 °C			150	µV
		-40 °C < T< 125 °C			400	
$\Delta V_{io}/\Delta T$	Input offset voltage drift	-40 °C < T< 125 °C			2.5	µV/°C
I_{io}	Input offset current (1)	T = 25 °C		1	2	pA
		-40 °C < T< 125 °C		20	100	
I_{ib}	Input bias current (1)	T = 25 °C		1	2	
		-40 °C < T< 125 °C		75	200	
CMR	Common mode rejection ratio, 20 log ($\Delta V_{icm}/\Delta V_{io}$), V_{icm} = 0 to 5 V	T = 25 °C	85	106		dB
		-40 °C < T< 125 °C	80			
SVR	Supply voltage rejection ratio, V_{CC} = 1.5 to 5.5 V, V_{icm} = 0 V	T = 25 °C	89	107		
		-40 °C < T< 125 °C	84			
A_{vd}	Large signal voltage gain, V_{out} = 0.2 V to (V_{CC+}) - 0.2 V	R_L = 100 kΩ, T = 25 °C	105	132		
		R_L = 100 kΩ, -40 °C < T< 125 °C	92			
V_{OH}	High-level output voltage, (drop from V_{CC+})	R_L = 10 kΩ, T = 25 °C		12	25	mV
		R_L = 10 kΩ, -40 °C < T< 125 °C			40	
V_{OL}	Low-level output voltage	R_L = 10 kΩ, T = 25°C		10	25	
		R_L = 10 kΩ, -40 °C < T< 125 °C			40	
I_{out}	Output sink current, V_{out} = V_{CC} , V_{ID} = - 200 mV	T = 25 °C	30	45		mA
		-40 °C < T< 125 °C	15			
	Output source current, V_{out} = 0 V, V_{ID} = 200 mV	T = 25 °C	25	39		
		-40 °C < T< 125 °C	18			
I_{CC}	Supply current (per channel), no load, V_{out} = V_{CC}/2	T = 25 °C		1000	1400	nA
		-40 °C < T< 125 °C			2000	
AC performance						
GBP	Gain bandwidth product	R_L = 1 MΩ, C_L = 60 pF		9		kHz
F_u	Unity gain frequency			6		
Φ_m	Phase margin			70		degrees
G_m	Gain margin			30		dB
SRp	Slew rate (10 % to 90 %)	R_L = 1 MΩ, C_L = 60 pF, V_{out} = 0.3 V to (V_{CC+}) - 0.3 V	0.9	1.9		V/ms
SRn	Slew rate (10 % to 90 %)	R_L = 1 MΩ, C_L = 60 pF, V_{out} = 0.3 V to (V_{CC+}) - 0.3 V	1.5	3.1		V/ms
e_n	Equivalent input noise voltage	f = 100 Hz		220		nV/√Hz
$\int e_n$	Low-frequency, peak-to-peak input noise	Bandwidth: f = 0.1 to 10 Hz		4.6		μV_{pp}
t_{rec} P	Overload recovery time (from positive rail)	100 mV from rail in comparator, R_L = 100 kΩ, V_{ID} = ±1 V -40 °C < T< 125 °C		650		µs
t_{rec} N	Overload recovery time (from negative rail)	100 mV from rail in comparator, R_L = 100 kΩ, V_{ID} = ±1 V, -40 °C < T< 125 °C		1300		µs

1. *Guaranteed by design*

4 Electrical characteristic curves

Figure 3. Supply current vs. supply voltage at low V_{ICM}

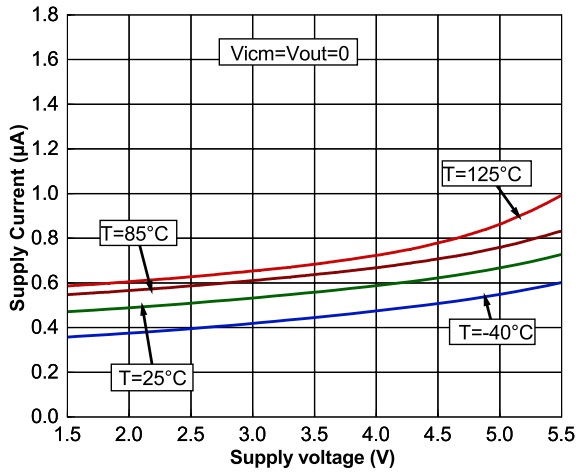


Figure 4. Supply current vs. supply voltage at high V_{ICM}

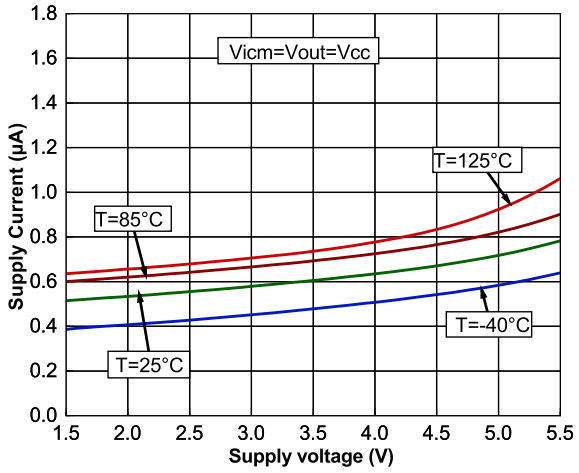


Figure 5. Supply current vs. supply voltage at mid V_{ICM}

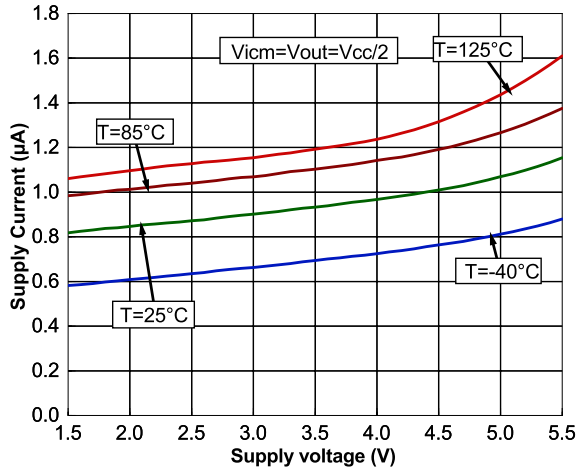


Figure 6. Supply current vs. input common-mode voltage

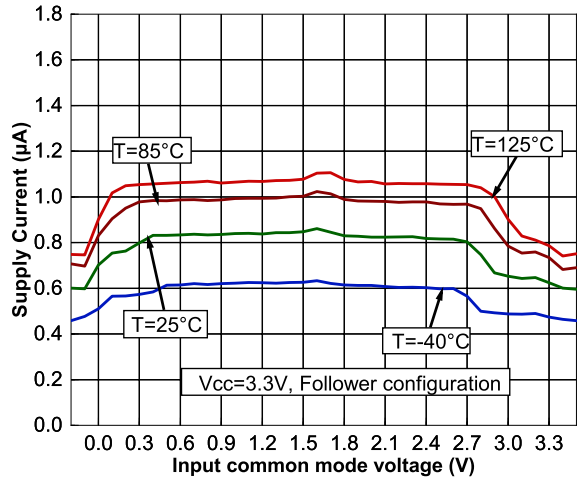


Figure 7. Input offset voltage vs. input common-mode voltage

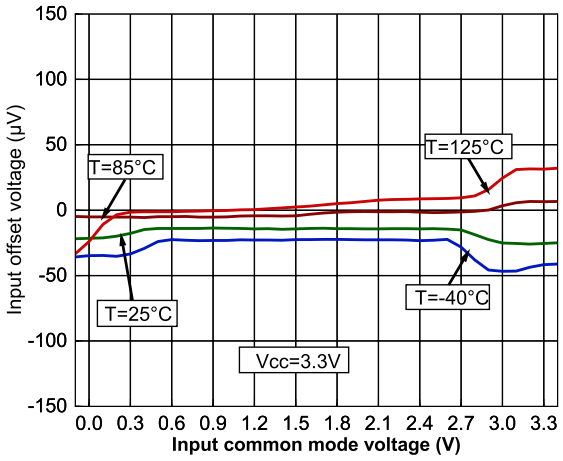


Figure 8. Input offset voltage distribution

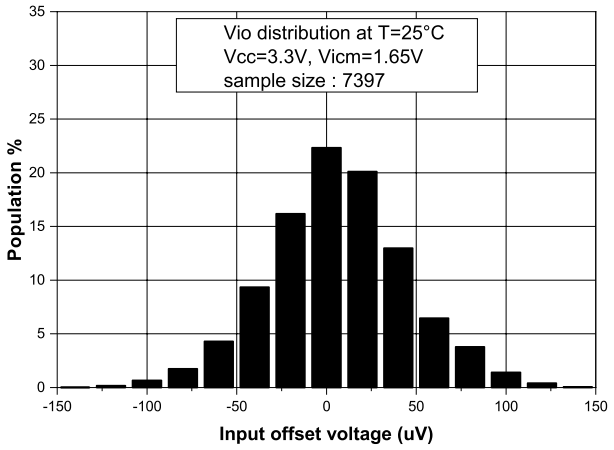


Figure 9. Input offset voltage temperature coefficient distribution from -40 °C to 25 °C

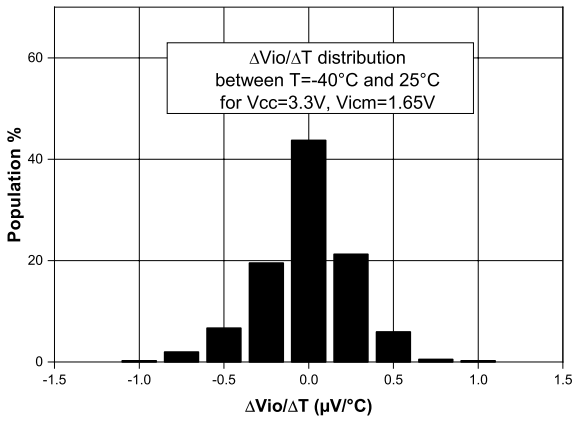


Figure 10. Input offset voltage temperature coefficient distribution from 25 °C to 125 °C

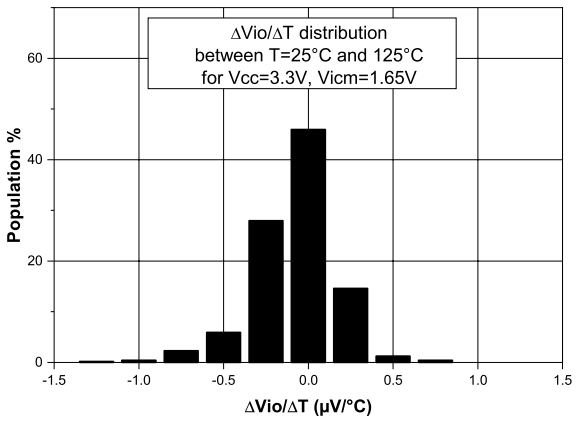


Figure 11. Input offset voltage vs. temperature at 3.3 V

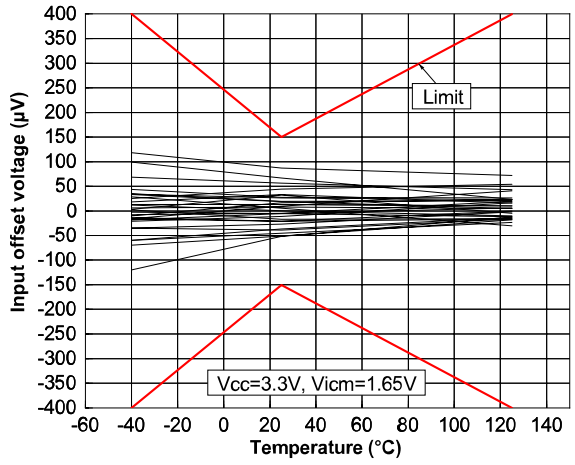


Figure 12. Input bias current vs. temperature at mid V_{ICM}

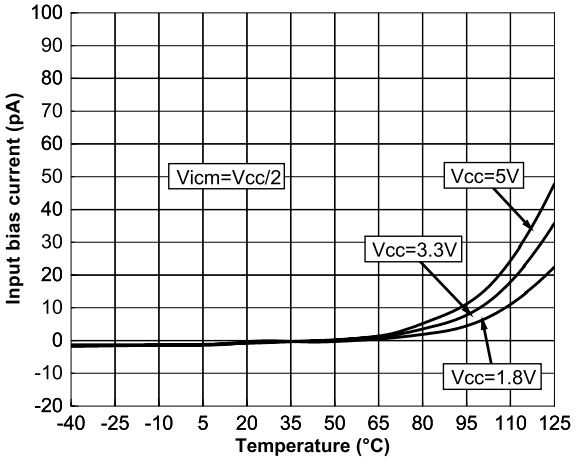


Figure 13. High level output voltage (drop from V_{CC}+)

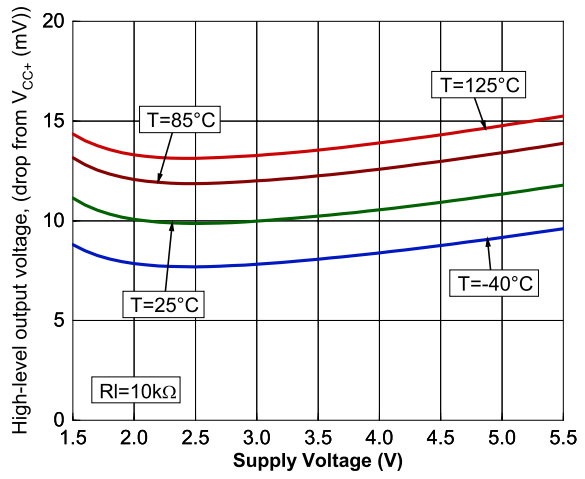


Figure 14. Low level output voltage

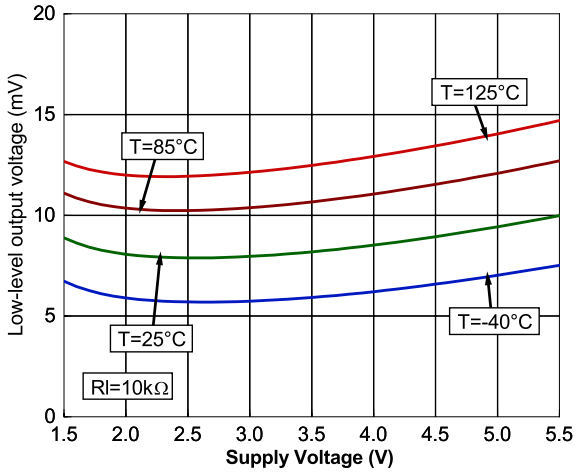


Figure 15. Output characteristics at 1.5 V supply voltage

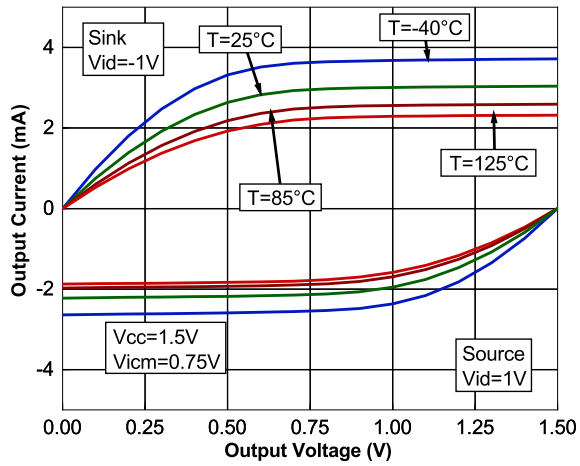


Figure 16. Output characteristics at 1.8 V supply voltage

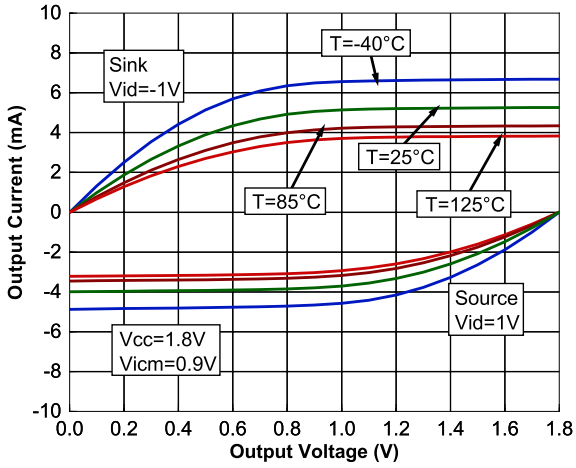


Figure 17. Output characteristics at 3.3 V supply voltage

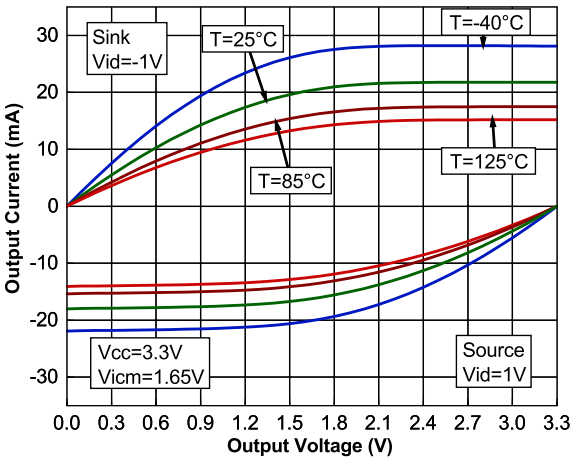


Figure 18. Output characteristics at 5 V supply voltage

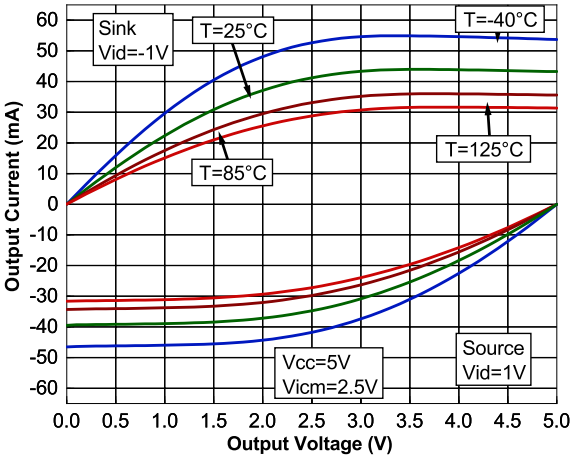


Figure 19. Output characteristics at 5.5 V supply voltage

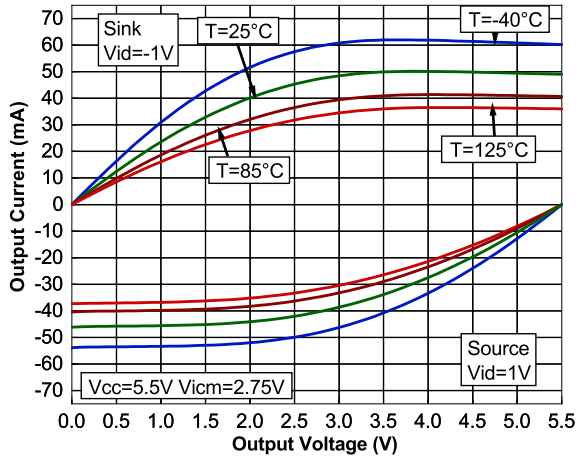


Figure 20. Output saturation with a sinewave on the input

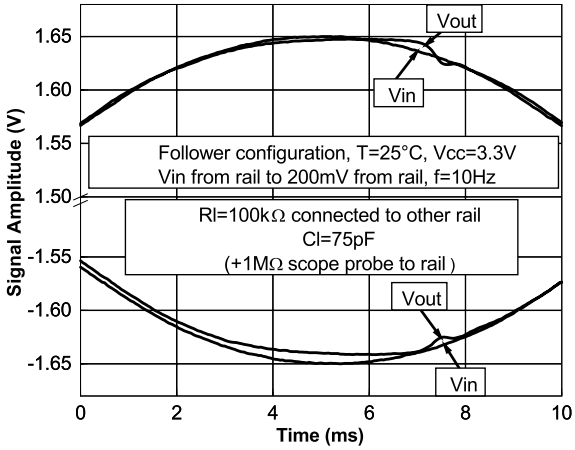


Figure 21. Output saturation with a square wave on the input

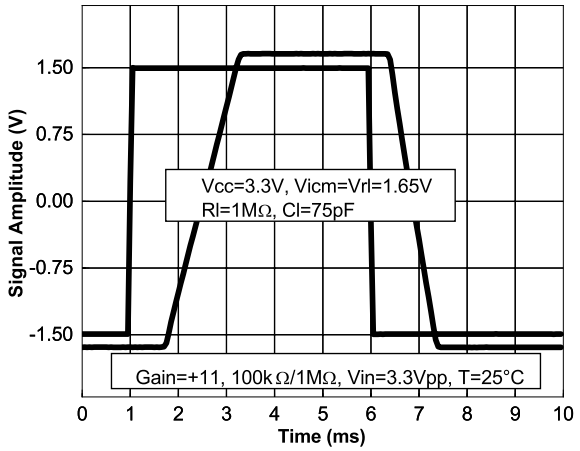


Figure 22. Phase reversal free

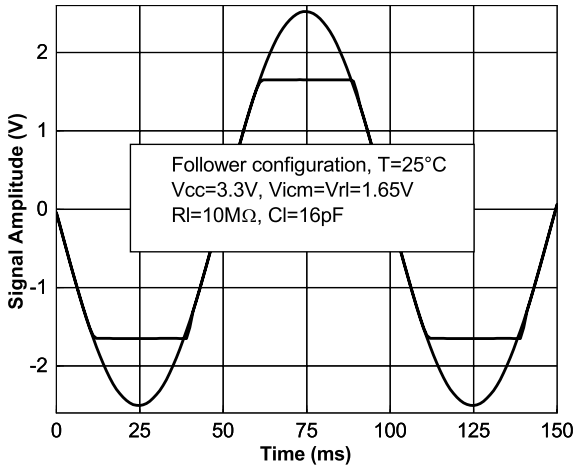


Figure 23. Recovery time from negative saturation vs. supply voltage

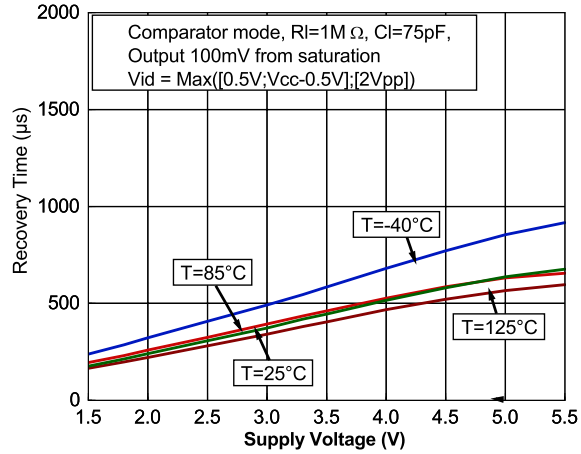


Figure 24. Recovery time from positive saturation vs. supply voltage

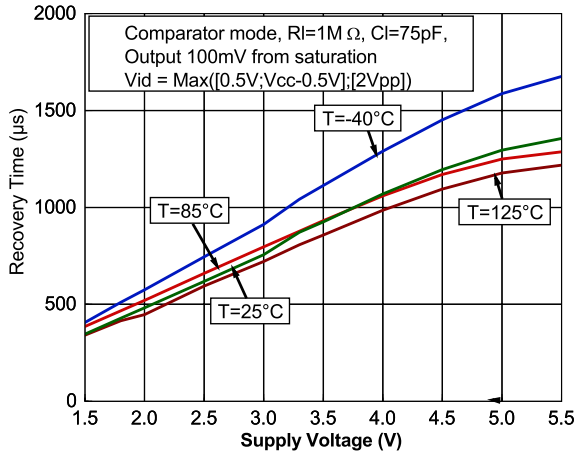


Figure 25. Slew rate vs. supply voltage

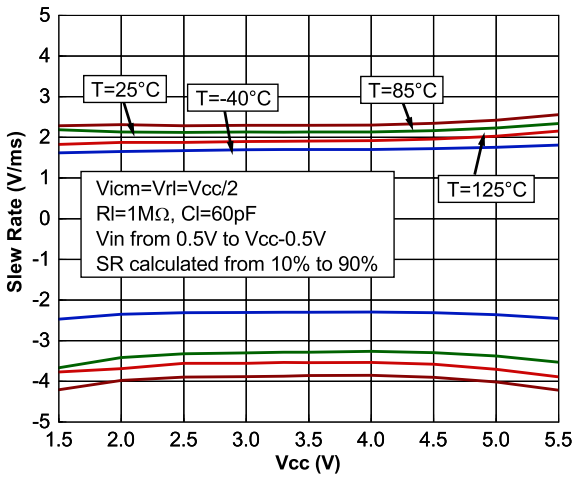


Figure 26. Output swing vs. input signal frequency

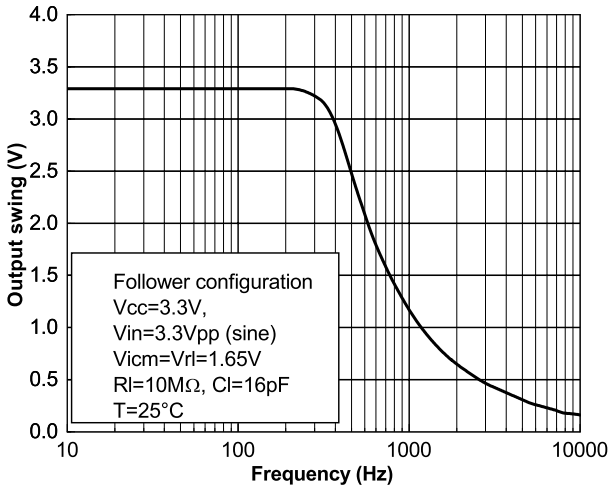


Figure 27. Triangulation of a sine wave

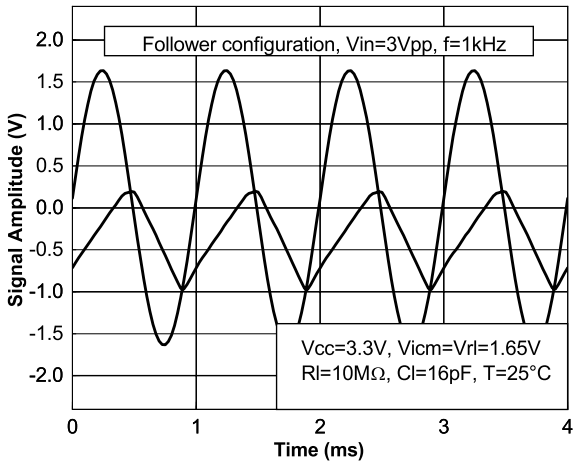


Figure 28. Large signal response at 3.3 V supply voltage

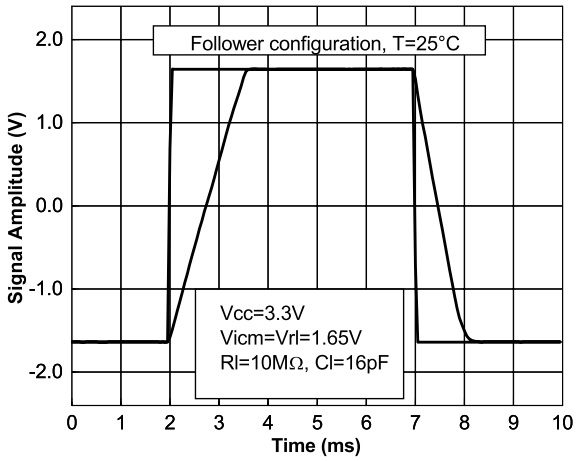


Figure 29. Small signal response at 3.3 V supply voltage

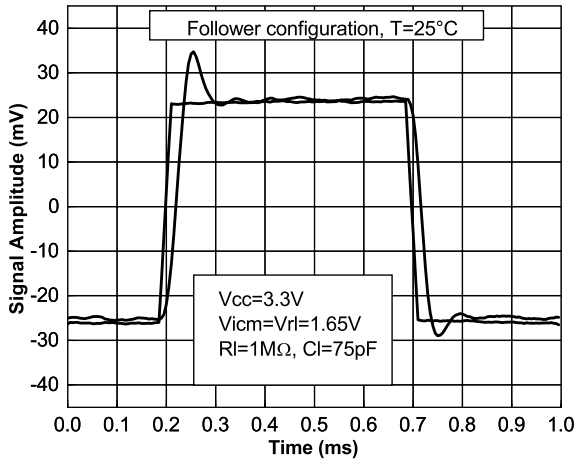


Figure 30. Overshoot vs. capacitive load at 3.3 V supply voltage

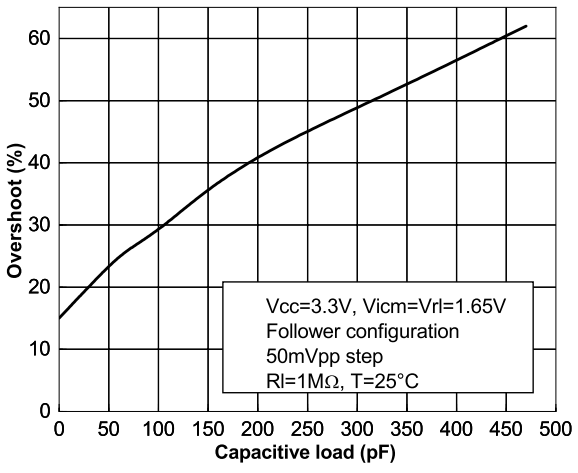


Figure 31. Over/under shoot vs supply voltage

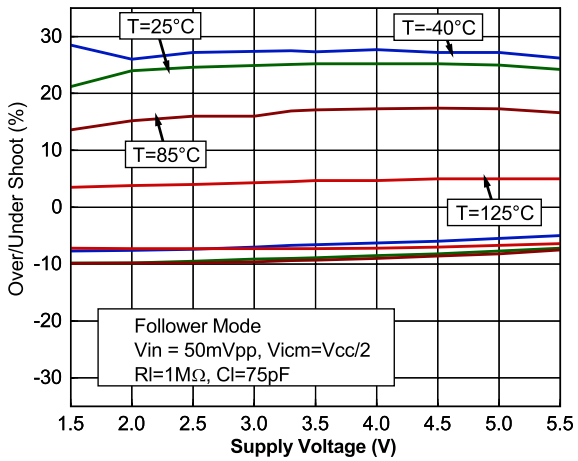


Figure 32. Bode diagram at 1.5 V supply voltage

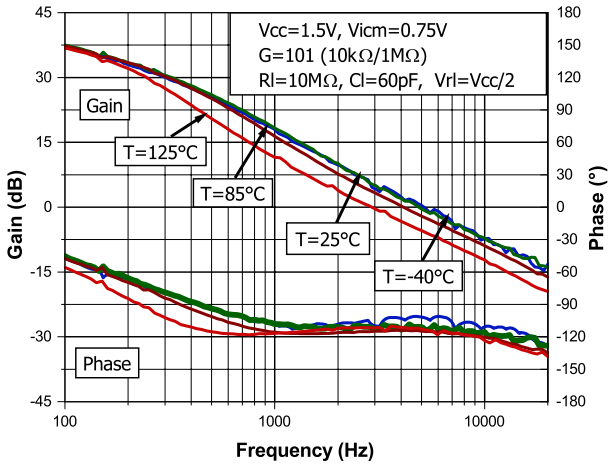


Figure 33. Bode diagram at 1.8 V supply voltage

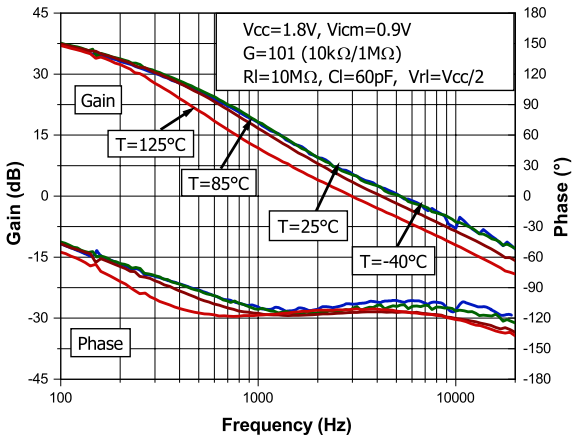


Figure 34. Bode diagram at 3.3 V supply voltage

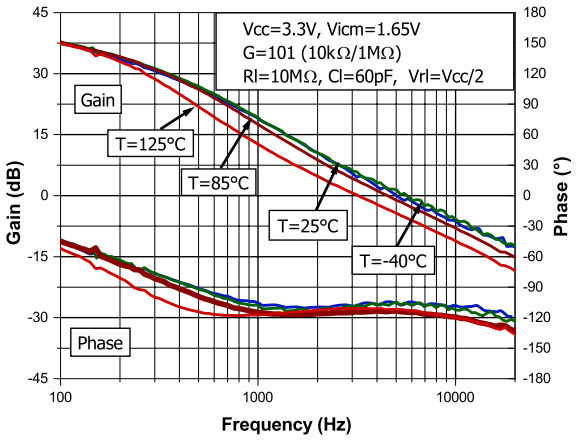


Figure 35. Bode diagram at 5 V supply voltage

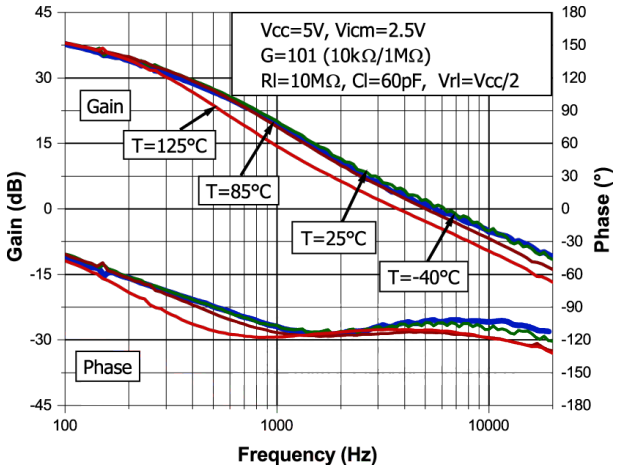


Figure 36. Bode diagram at 5.5 V supply voltage

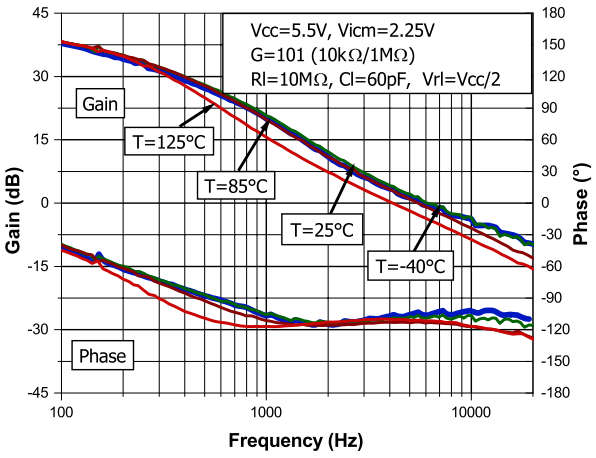


Figure 37. In series resistor Riso vs. capacitive load

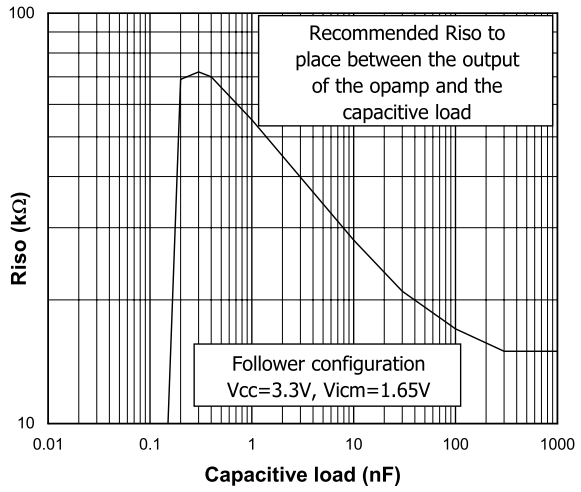


Figure 38. Noise amplitude on 0.1 to 10 Hz freq. range

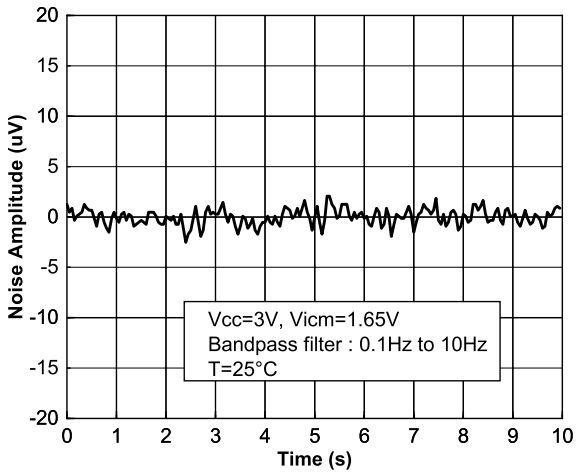


Figure 39. Noise vs. frequency for different common mode input voltages

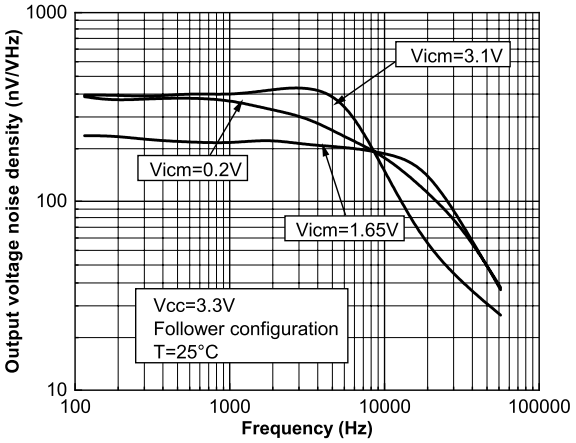
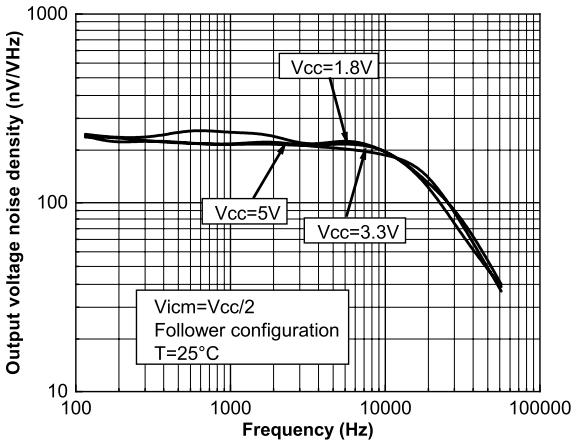


Figure 40. Noise vs. frequency for different power supply voltages



5 Application information

5.1 Nanopower applications

The TSU111IY and TSU112IY can operate from 1.5 V to 5.5 V. The parameters are fully specified at 1.8 V, 3.3 V, and 5 V supply voltages and are very stable in the full V_{CC} range. Additionally, the main specifications are guaranteed on the industrial temperature range from -40 to 125 °C.

5.1.1 Schematic optimization aiming for nanopower

To benefit from the full performance of the TSU111IY and TSU112IY, the impedances must be maximized so that current consumption is not lost where it is not required.

For example, an aluminum electrolytic capacitance can have significantly high leakage. This leakage may be greater than the current consumption of the op-amp. For this reason, ceramic type capacitors are preferred.

For the same reason, big resistor values should be used in the feedback loop. However, there are two main limitations to be considered when choosing a resistor.

1. Noise generated: a 100 kΩ resistor generates 40 nV/√Hz, a bigger resistor value generates even more noise.
2. Leakage on the PCB: leakage can be generated by moisture. This can be improved by using a specific coating process on the PCB.

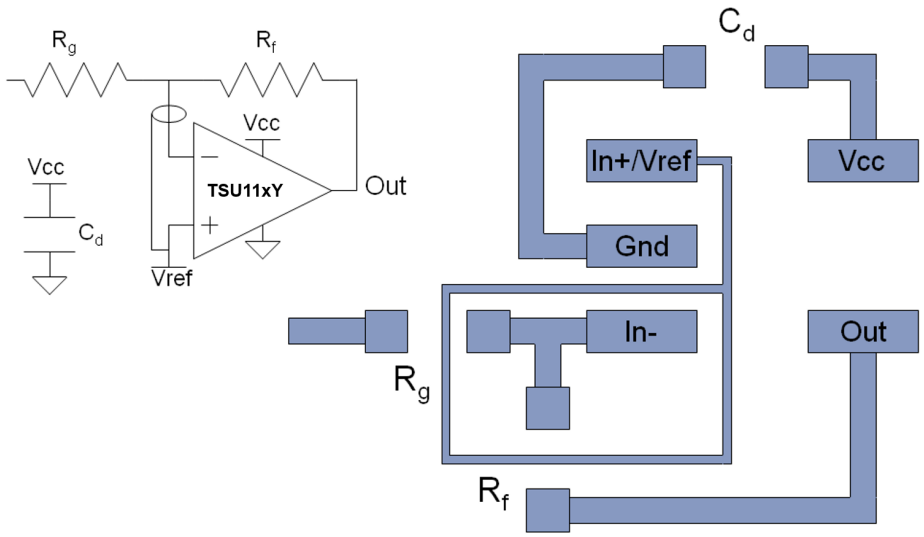
5.1.2 PCB layout considerations

For correct operation, it is advised to add 10 nF decoupling capacitors as close as possible to the power supply pins.

Minimizing the leakage from sensitive high impedance nodes on the inputs of the TSU111IY and TSU112IY can be performed with a guarding technique. The technique consists of surrounding high impedance tracks by a low impedance track (the ring). The ring is at the same electrical potential as the high impedance node.

Therefore, even if some parasitic impedance exists between the tracks, no leakage current can flow through them as they are at the same potential (see Figure 41).

Figure 41. Guarding on the PCB



5.2 Rail-to-rail input

The TSU111IY and TSU112IY are built with two complementary PMOS and NMOS input differential pairs. Thus, the device has a rail-to-rail input, and the input common mode range is extended from (V_{CC-}) - 0.1 V to (V_{CC+}) + 0.1 V.

The TSU111IY and TSU112IY have been designed to prevent phase reversal behavior.

5.3 Input offset voltage drift overtemperature

The maximum input voltage drift variation overtemperature is defined as the offset variation related to the offset value measured at 25 °C. The operational amplifier is one of the main circuits of the signal conditioning chain, and the amplifier input offset is a major contributor to the chain accuracy. The signal chain accuracy at 25 °C can be compensated during production at application level. The maximum input voltage drift over temperature enables the system designer to anticipate the effect of temperature variations.

The maximum input voltage drift over temperature is computed using Equation 1.

Equation 1

$$\frac{\Delta V_{io}}{\Delta T} = \max\left|\frac{V_{io}(T) - V_{io}(25\,°C)}{T - 25\,°C}\right|$$

Where T = -40 °C and 125 °C.

The TSU111IY and TSU112IY datasheet maximum values are guaranteed by measurements on a representative sample size ensuring a C_{pk} (process capability index) greater than 1.3.

5.4 Long term input offset voltage drift

To evaluate product reliability, two types of stress acceleration are used:

- Voltage acceleration, by changing the applied voltage
- Temperature acceleration, by changing the die temperature (below the maximum junction temperature allowed by the technology) with the ambient temperature.

The voltage acceleration has been defined based on JEDEC results, and is defined using Equation 2.

Equation 2

$$A_{FV} = e^{\beta \cdot (V_S - V_U)}$$

Where:

A_{FV} is the voltage acceleration factor

β is the voltage acceleration constant in 1/V, constant technology parameter (β = 1)

V_S is the stress voltage used for the accelerated test

V_U is the voltage used for the application

The temperature acceleration is driven by the Arrhenius model, and is defined in Equation 3.

Equation 3

$$A_{FT} = e^{\frac{E_a}{k} \cdot \left(\frac{1}{T_U} - \frac{1}{T_S}\right)}$$

Where:

A_{FT} is the temperature acceleration factor

E_a is the activation energy of the technology based on the failure rate

k is the Boltzmann constant (8.6173×10^{-5} eV.K^{-1})

T_U is the temperature of the die when V_U is used (°K)

T_S is the temperature of the die under temperature stress (°K)

The final acceleration factor, A_F, is the multiplication of the voltage acceleration factor and the temperature acceleration factor (Equation 4).

Equation 4

$$A_F = A_{FT} \times A_{FV}$$

A_F is calculated using the temperature and voltage defined in the mission profile of the product. The A_F value can then be used in Equation 5 to calculate the number of months of use equivalent to 1000 hours of reliable stress duration.

Equation 5

$$\text{Months} = A_F \times 1000\ \text{h} \times 12\ \text{months} / (24\ \text{h} \times 365.25\ \text{days})$$

To evaluate the op amp reliability, a follower stress condition is used where V_{CC} is defined as a function of the maximum operating voltage and the absolute maximum rating (as recommended by JEDEC rules).

The V_{io} drift (in µV) of the product after 1000 h of stress is tracked with parameters at different measurement conditions (see Equation 6).

Equation 6

$$V_{CC} = \max V_{op} \text{ with } V_{icm} = V_{CC} / 2$$

The long term drift parameter (ΔV_{io}), estimating the reliability performance of the product, is obtained using the ratio of the V_{io} (input offset voltage value) drift over the square root of the calculated number of months (Equation 7).

Equation 7

$$\Delta V_{io} = \frac{V_{io}\text{drift}}{\sqrt{(\text{months})}}$$

Where V_{io} drift is the measured drift value in the specified test conditions after 1000 h stress duration.

5.5 Using the TSU111IY and TSU112IY with sensors

The TSU111IY and TSU112IY have MOS inputs, thus input bias currents can be guaranteed down to 10 pA maximum at ambient temperature. This is an important parameter when the operational amplifier is used in combination with high impedance sensors.

The TSU111IY and TSU112IY are perfectly suited for trans-impedance configuration. This configuration allows a current to be converted into a voltage value with a gain set by the user. It is an ideal choice for portable electrochemical gas sensing or photo/UV sensing applications. The TSU111IY and TSU112IY, using trans-impedance configuration, are able to provide a voltage value based on the physical parameter sensed by the sensor.

5.6 Fast desaturation

When the TSU111IY and TSU112IY go into saturation mode, it takes a short period of time to recover, typically 420/880 µs. When recovering after go saturation, the TSU111IY and TSU112IY do not exhibit any voltage peaks that could generate issues (such as false alarms) in the application (see Figure 15).

We can observe that this circuit still exhibits good gain even close to the rails i.e. A_{vd} greater than 88 dB for V_{cc} = 3.3 V with V_{out} varying from 200 mV up to a supply voltage minus 200 mV. With a trans-impedance schematic, a voltage reference can be used to keep the signal away from the supply rails.

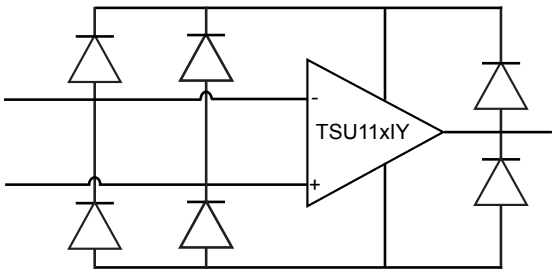
5.7 Using the TSU111IY and TSU112IY in comparator mode

The TSU111IY and TSU112IY can be used as a comparator. In this case, the output stage of the device always operates in saturation mode. In addition, Figure 4 shows that the current consumption is not higher and even decreases smoothly close to the rails. The TSU111IY and TSU112IY are obviously some operational amplifier and are therefore optimized for use in linear mode. We recommend using the TS88 series of nanopower comparators if the primary function is to perform a signal comparison only.

5.8 ESD structure of the TSU111IY and TSU112IY

The TSU111IY and TSU112IY are protected against electrostatic discharge (ESD) with dedicated diodes (see Figure 2). These diodes must be considered at application level especially when signals applied on the input pins go beyond the power supply rails (V_{CC+}) or (V_{CC-}).

Figure 42. ESD structure



Current through the diodes must be limited to a maximum of 10 mA as stated in Table 1. A serial resistor on the inputs can be used to limit this current.

5.9 EMI robustness of nanopower devices

Nanopower devices exhibit higher impedance nodes and consequently they are more sensitive to EMI. To improve the natural robustness of the TSU111IY and TSU112IY devices, we recommend to add three capacitors of around 22 pF each between the two inputs, and between each input and ground. These capacitors lower the impedance of the input at high frequencies and therefore reduce the impact of the radiation

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 SC70-5 (or SOT323-5) package information

Figure 43. **SC70-5 (or SOT323-5) package outline**

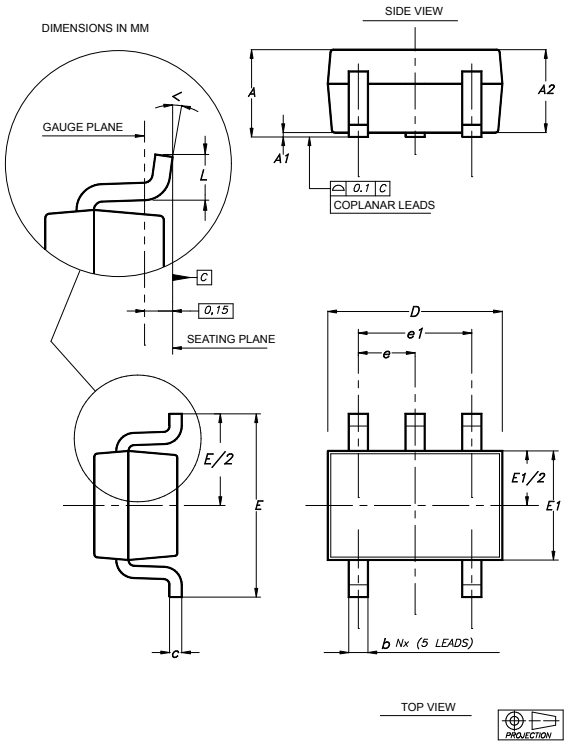


Table 9. **SC70-5 (or SOT323-5) mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80		1.10	0.032		0.043
A1			0.10			0.004
A2	0.80	0.90	1.00	0.032	0.035	0.039
b	0.15		0.30	0.006		0.012
c	0.10		0.22	0.004		0.009
D	1.80	2.00	2.20	0.071	0.079	0.087
E	1.80	2.10	2.40	0.071	0.083	0.094
E1	1.15	1.25	1.35	0.045	0.049	0.053
e		0.65			0.025	
e1		1.30			0.051	
L	0.26	0.36	0.46	0.010	0.014	0.018
<	0°		8°	0°		8°

6.2 SOT23-5L package information

Figure 44. **SOT23-5L package outline**

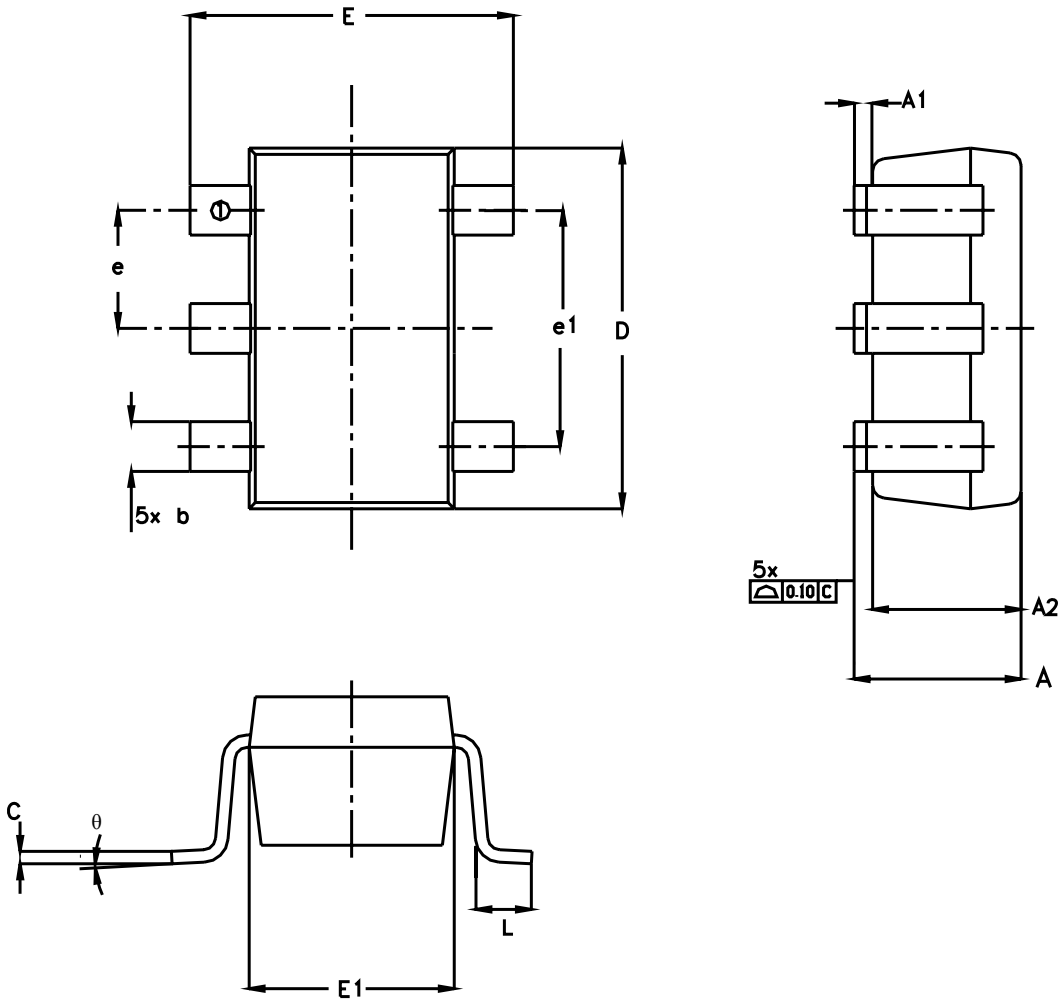
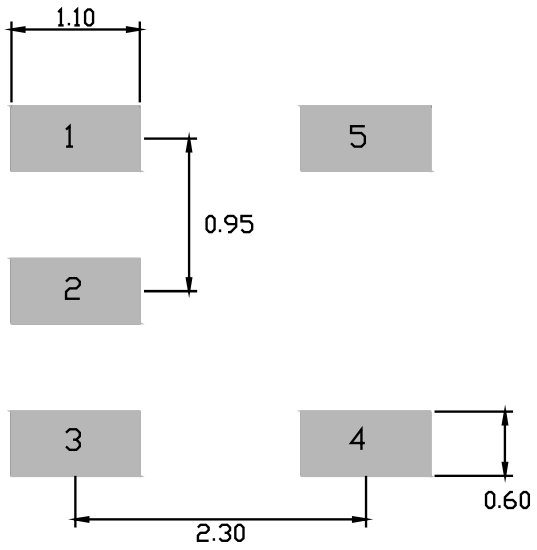


Table 10. SOT23-5L mechanical data

Symbol	mm			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.45			0.057
A1	0.00		0.15	0.000		0.006
A2	0.90	1.15	1.30	0.035	0.045	0.051
b	0.30		0.50	0.012		0.020
c	0.08		0.22	0.003		0.009
D		2.90			0.114	
E		2.80			0.110	
E1		1.60			0.063	
e		0.95			0.037	
e1		1.90			0.075	
L	0.30	0.45	0.60	0.012	0.018	0.024
θ	0	4	8	0	4	8
N	5			5		

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*

Figure 45. SOT23-5L recommended footprint



6.3 DFN8 2x2 package information

Figure 46. **DFN8 2x2 package outline**

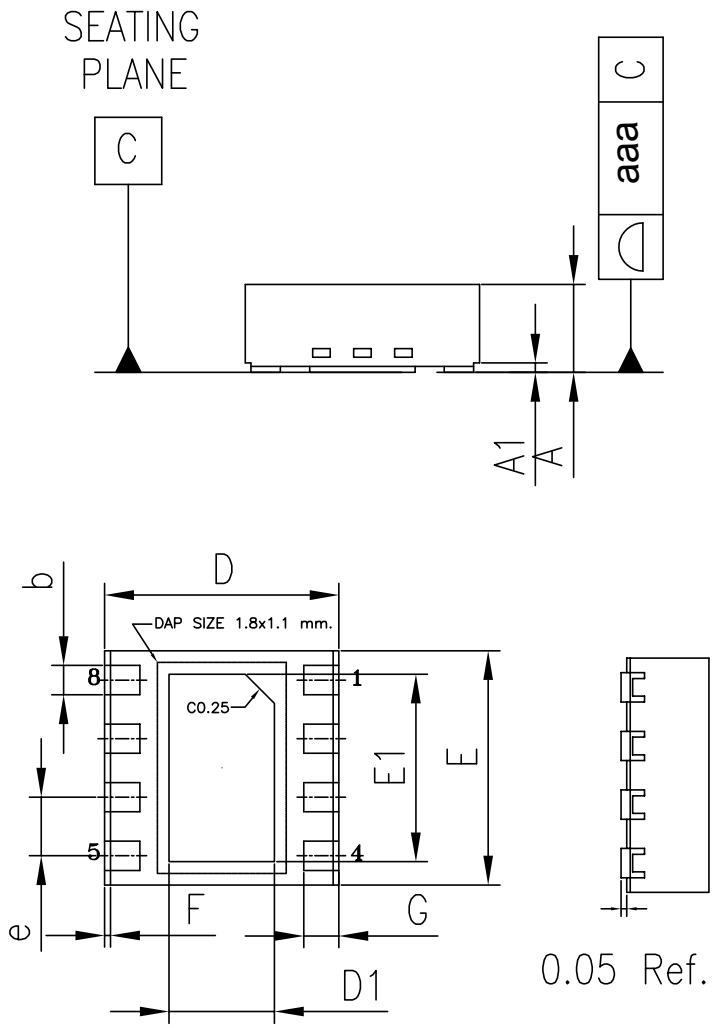
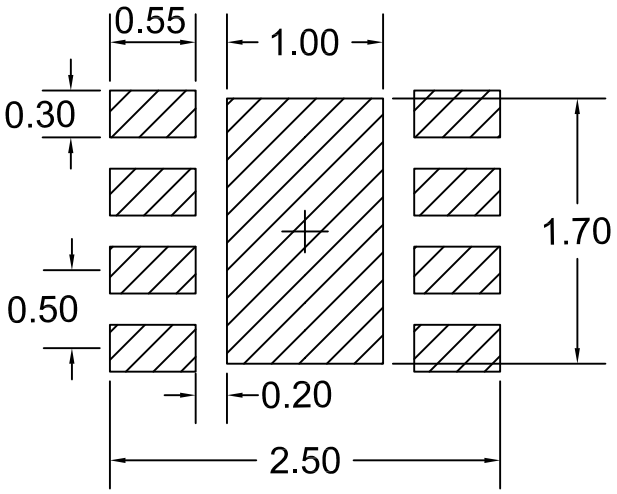


Table 11. DFN8 2x2 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.70	0.75	0.80	0.70	0.75	0.80
A1		0.10			0.10	
b	0.20	0.25	0.30	0.20	0.25	0.30
D	1.95	2.00	2.05	1.95	2.00	2.05
D1	0.80	0.90	1.00	0.80	0.90	1.00
E	1.95	2.00	2.05	1.95	2.00	2.05
E1	1.50	1.60	1.70	1.50	1.60	1.70
e		0.50			0.50	
F		0.05			0.05	
G	0.25	0.30	0.35	0.25	0.30	0.35
aaa		0.10			010	

Note: The terminal 1 corner must be identified on the top surface by using a laser marking dot.

Figure 47. DFN8 2x2 recommended footprint



6.4 MiniSO8 package information

Figure 48. **MiniSO8 package outline**

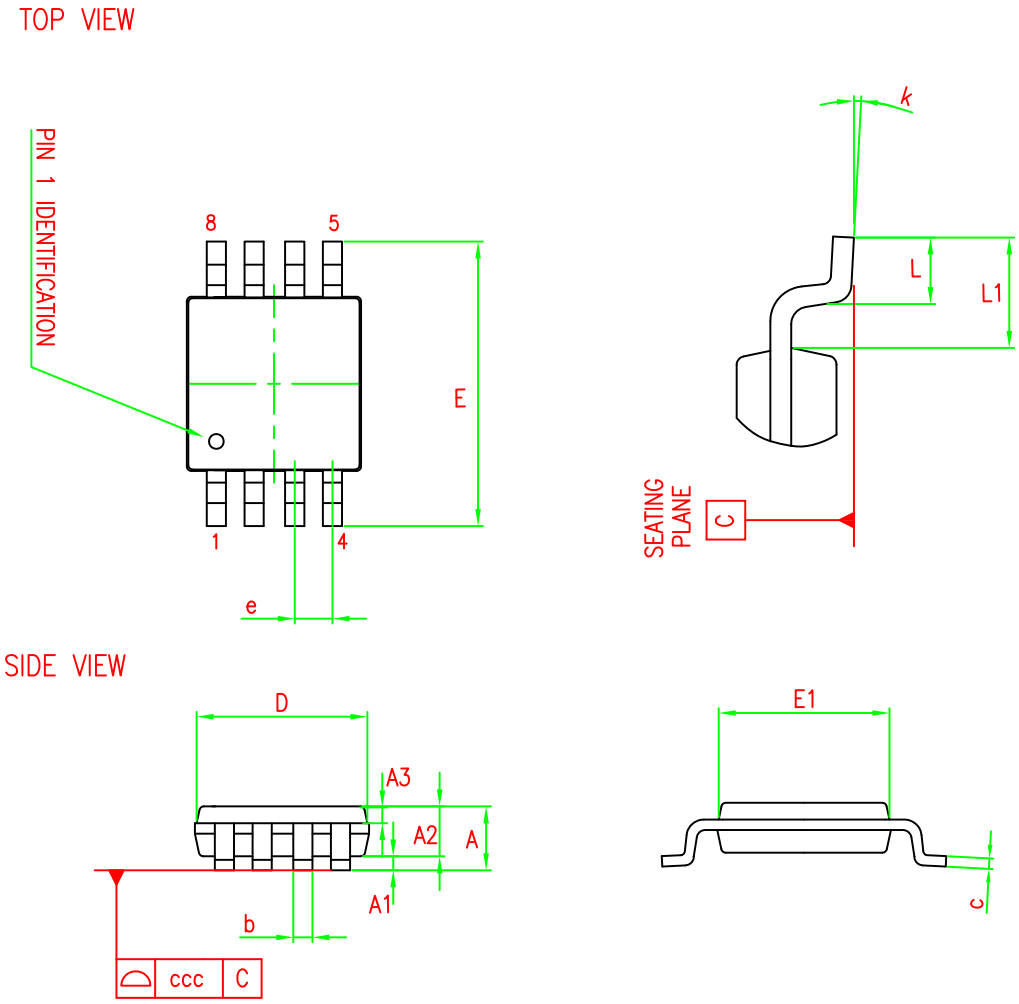
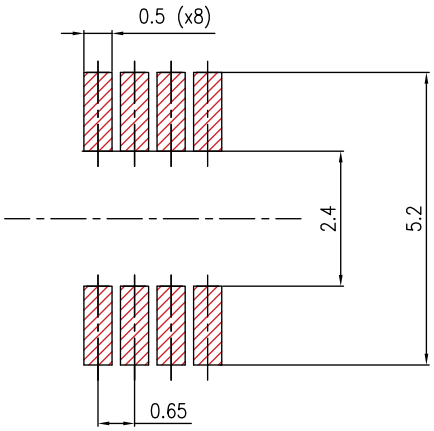


Table 12. MiniSO8 package mechanical data

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.10			1.10
A1	0		0.15	0.05		0.15
A2	0.75	0.85	0.95	0.75	0.85	0.95
A3	0.30	0.35	0.40	0.30	0.35	0.40
b	0.22		0.40	0.28		0.36
c	0.08		0.23	0.15		0.19
D	2.80	3.00	3.20	2.90	3.00	3.10
E	4.65	4.90	5.15	4.70	4.90	5.10
E1	2.80	3.00	3.10	2.90	3.00	3.10
e		0.65			0.65	
L	0.40	0.60	0.80	0.40		0.70
L1		0.95			0.95	
k	0		8	0		8
ccc			0.10			0.10

Note: TSSOP stands for thin shrink small outline package. Dimensions "D" and "E1" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.

Figure 49. MiniSO8 recommended footprint



7 Ordering information

Table 13. Order code

Order code	Temperature range	Package [1]	Marking
TSU111RILT	-40 °C to +125 °C [2]	SOT23-5	KIJ
TSU111IYLT	-40 °C to +125 °C [3]		K1M
TSU111IYCT		SC70-5	
TSU112IYQ3T		DFN8 2x2	K30
TSU112IYST		MiniSO8 [4]	

1. *All devices are delivered in tape and reel packing.*
2. *Industrial grade*
3. *Automotive grade, qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q002 or equivalent.*
4. *This package is under qualification.*

Revision history

Table 14. **Document revision history**

Date	Revision	Changes
01-Mar-2021	1	Initial release
09-Jul-2021	2	Updated the first row features on the cover page.
14-Feb-2022	3	Added new part number TSU111IY and new Section 6.1 SOT23-5L package information. Updated Table 11 Order code
10-Nov-2022	4	Updated figure on the cover page, Figure 1 and Table 11. Order code
01-Jun-2023	5	Added new package SC70-5 (or SOT323-5) package information, new Table 2 and new TSU111IYCT order code in Table 13. Updated figure on the cover page and Figure 1.

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