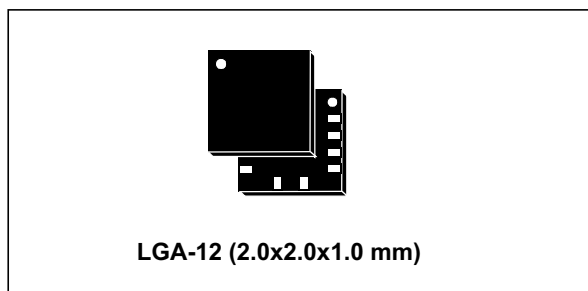


## Ultracompact high-performance eCompass module: ultralow-power 3-axis accelerometer and 3-axis magnetometer

Datasheet - production data



- Click/double-click recognition
- Pedometers
- Intelligent power saving for handheld devices
- Display orientation
- Gaming and virtual reality input devices
- Impact recognition and logging
- Vibration monitoring and compensation

### Features

- 3 magnetic field channels and 3 acceleration channels
- $\pm 50$  gauss magnetic dynamic range
- $\pm 2/\pm 4/\pm 8/\pm 16$  g selectable acceleration full scales
- 16-bit data output
- SPI / I<sup>2</sup>C serial interfaces
- Analog supply voltage 1.71 V to 3.6 V
- Selectable power mode/resolution for accelerometer and magnetometer
- Single measurement mode for magnetometer
- Programmable interrupt generators for free-fall, motion detection, and magnetic field detection
- Embedded self-test
- Embedded temperature sensor
- Embedded FIFO
- ECOPACK and RoHS compliant

### Applications

- Tilt-compensated compasses
- Map rotation
- Position detection
- Motion-activated functions
- Free-fall detection

### Description

The LSM303AGR is an ultralow-power high-performance system-in-package featuring a 3-axis digital linear acceleration sensor and a 3-axis digital magnetic sensor.

The LSM303AGR has linear acceleration full scales of  $\pm 2g/\pm 4g/\pm 8g/\pm 16g$  and a magnetic field dynamic range of  $\pm 50$  gauss.

The LSM303AGR includes an I<sup>2</sup>C serial bus interface that supports standard, fast mode, fast mode plus, and high-speed (100 kHz, 400 kHz, 1 MHz, and 3.4 MHz) and an SPI serial standard interface.

The system can be configured to generate an interrupt signal for free-fall, motion detection, and magnetic field detection.

The magnetic and accelerometer blocks can be enabled or put into power-down mode separately.

The LSM303AGR is available in a plastic land grid array package (LGA) and is guaranteed to operate over an extended temperature range from  $-40$  °C to  $+85$  °C.

Table 1. Device summary

Part number	Temp. range [°C]	Package	Packaging
LSM303AGR	-40 to +85	LGA-12	Tray
LSM303AGRTR	-40 to +85	LGA-12	Tape and reel

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# 1 Block diagram and pin description

## 1.1 Block diagram

Figure 1. Block diagram

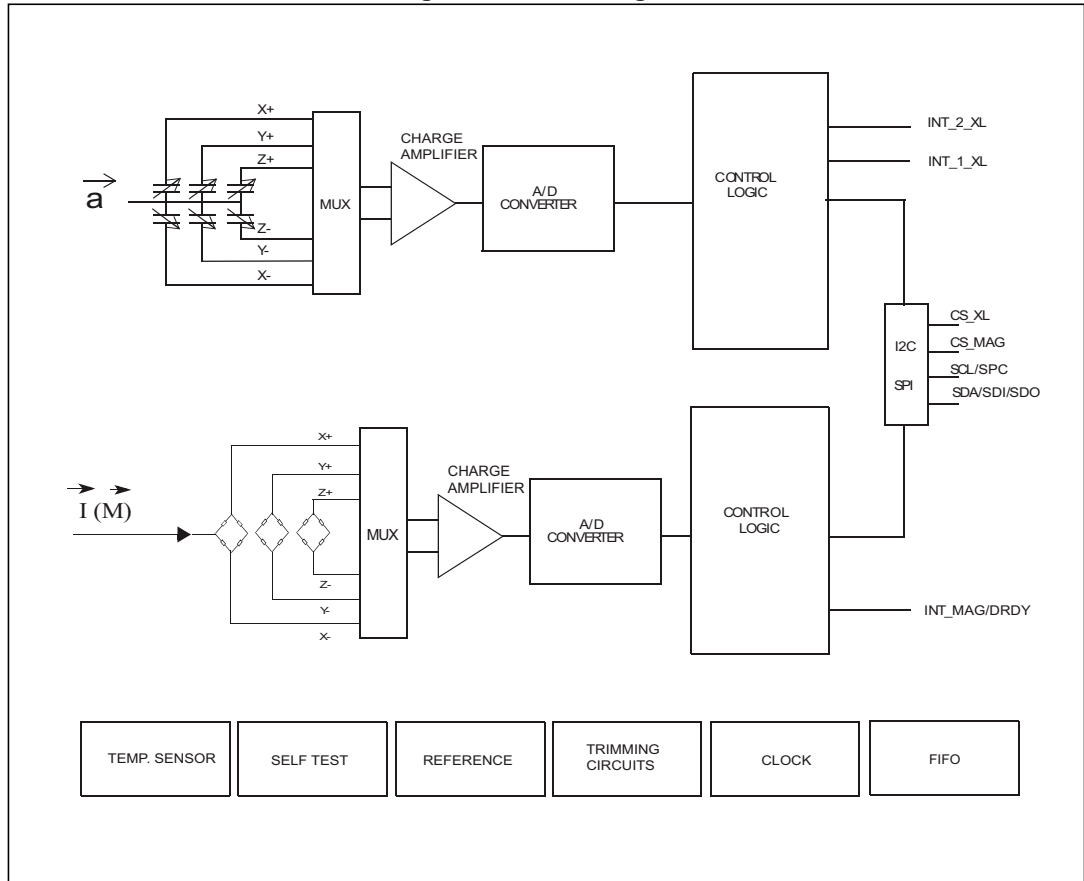




Table 2. Pin description

Pin#	Name	Function
1	SCL SPC	I <sup>2</sup> C serial clock (SCL) SPI serial port clock (SPC)
2	CS_XL	Accelerometer: SPI enable I <sup>2</sup> C/SPI mode selection 1: SPI idle mode / I <sup>2</sup> C communication enabled; 0: SPI communication mode / I <sup>2</sup> C disabled
3	CS_MAG	Magnetometer: SPI enable I <sup>2</sup> C/SPI mode selection 1: SPI idle mode / I <sup>2</sup> C communication enabled; 0: SPI communication mode / I <sup>2</sup> C disabled
4	SDA SDI SDO	I <sup>2</sup> C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
5	C1	Capacitor connection (C1 = 220 nF)
6	GND	Connected to GND
7	INT_MAG/DRDY	Magnetometer interrupt/data-ready signal
8	GND	0 V
9	Vdd	Power supply
10	Vdd_IO	Power supply for I/O pins
11	INT_2_XL	Accelerometer interrupt 2
12	INT_1_XL	Accelerometer interrupt 1

## 2 Module specifications

### 2.1 Sensor characteristics

@ V<sub>dd</sub> = 2.5 V, T = 25 °C unless otherwise noted<sup>(a)</sup>.

**Table 3. Sensor characteristics**

Symbol	Parameter	Test conditions	Min.	Typ. <sup>(1)</sup>	Max.	Unit
LA_FS	Linear acceleration measurement range			±2		g
				±4		
				±8		
				±16		
M_FS	Magnetic dynamic range		±49.152		gauss	
LA_So	Linear acceleration sensitivity <sup>(2)</sup>	FS = ±2 g and in high-resolution mode	-7%	0.98	+7%	mg/LSB
		FS = ±4 g and in high-resolution mode	-7%	1.95	+7%	
		FS = ±8 g and in high-resolution mode	-7%	3.9	+7%	
		FS = ±16 g and in high-resolution mode	-7%	11.72	+7%	
		FS = ±2 g and in normal mode	-7%	3.9	+7%	
		FS = ±4 g and in normal mode	-7%	7.82	+7%	
		FS = ±8 g and in normal mode	-7%	15.63	+7%	
		FS = ±16 g and in normal mode	-7%	46.9	+7%	
		FS = ±2 g and in low-power mode	-7%	15.63	+7%	
		FS = ±4 g and in low-power mode	-7%	31.26	+7%	
		FS = ±8 g and in low-power mode	-7%	62.52	+7%	
		FS = ±16 g and in low-power mode	-7%	187.58	+7%	
M_So	Magnetic sensitivity <sup>(2)</sup>		-7%	1.5	+7%	mgauss/LSB
LA_TCSO	Linear acceleration sensitivity change vs. temperature <sup>(3)</sup>			0.01		%/°C
M_TCSO	Magnetic sensitivity change vs. temperature <sup>(3)</sup>			±0.03		%/°C
LA_TyOff	Linear acceleration zero-g level offset accuracy <sup>(2)</sup>		-80	±40	+80	mg
M_TyOff	Magnetic sensor offset	With offset cancellation <sup>(4)(5)</sup>	-60		+60	mgauss
LA_TCOff	Linear acceleration zero-g level change vs. temp. <sup>(3)</sup>	Max. delta from 25 °C		±0.5		mg/°C
M_TCOff	Magnetic sensor offset change vs. temp. <sup>(4)</sup>	With offset cancellation	-0.3		+0.3	mgauss/°C

a. The product is factory calibrated at 2.5 V. The operational power supply range is from 1.71 V to 3.6 V.

Table 3. Sensor characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ. <sup>(1)</sup>	Max.	Unit
LA_An	Linear acceleration RMS noise	ODR = 100 Hz, high-resolution mode, FS = $\pm 2 g$		3		mg (RMS)
M_R	Magnetic RMS noise <sup>(6)</sup>	High-performance mode		3		mgauss (RMS)
LA_ST	Linear acceleration self-test positive output change <sup>(7)(8)(9)</sup>	FS = $\pm 2 g$ ; normal mode	17		360	LSB
M_ST	Magnetic self-test <sup>(10)</sup>		15		500	mgauss
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. Values after factory calibration test and trimming.
3. Measurements are performed in a uniform temperature setup and they are based on characterization data in a limited number of samples, not measured during final test for production.
4. Based on characterization data on a limited number of samples, not measured during final test for production.
5. Excluding drift due to magnetic shock.
6. With low-pass filter or offset cancellation enabled.
7. The sign of "Self-test output change" is defined by the ST bit in [CTRL\\_REG4\\_A \(23h\)](#), for all axes.
8. "Self-test output change" is defined as the absolute value of:  
 $OUTPUT[LSb]_{(Self-test\ enabled)} - OUTPUT[LSb]_{(Self-test\ disabled)}$ . 1LSb = 3.9 mg in normal mode (10-bit) at FS= $\pm 2 g$ .
9. After enabling the ST bit, correct data is obtained after two samples (low-power mode / normal mode) or after eight samples (high-resolution mode).
10. Magnetic "self-test" is defined as:  $OUTPUT[gau]_{(Self-test\ enabled)} - OUTPUT[gau]_{(Self-test\ disabled)}$ .

## 2.2 Temperature sensor characteristics

@ Vdd = 2.5 V, T = 25 °C unless otherwise noted <sup>(b)</sup>.

**Table 4. Temperature sensor characteristics**

Symbol	Parameter	Test conditions	Min.	Typ. <sup>(1)</sup>	Max.	Unit
TSDr	Temperature sensor output change vs. temp.			1		digit/°C <sup>(2)</sup>
TODR	Temperature refresh rate			ODR <sup>(3)</sup>		Hz
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. 8-bit resolution.
3. Refer to [Table 35](#).

## 2.3 Electrical characteristics

@ Vdd = 2.5 V, T = 25 °C unless otherwise noted <sup>(b)</sup>.

**Table 5. Electrical characteristics**

Symbol	Parameter	Test conditions	Min.	Typ. <sup>(1)</sup>	Max.	Unit
Vdd	Supply voltage		1.71		3.6	V
Vdd_IO	Module power supply for I/O <sup>(2)</sup>		1.71	1.8	Vdd+0.1	V
LA_Idd_NM	Accelerometer current consumption Magnetic sensor in power-down mode.	50 Hz ODR in normal mode		12.6		µA
		1 Hz ODR in normal mode		3.7		
		50 Hz ODR in low-power mode		7.7		
M_Idd_HR	Magnetic current consumption in high-resolution mode Accelerometer in power-down mode.	ODR = 20 Hz		200		µA
M_Idd_LP	Magnetic current consumption in low-power mode Accelerometer in power-down mode.	ODR = 20 Hz		50		µA
Idd_PD	Current consumption in power-down			2		µA
V <sub>IH</sub>	Digital high-level input voltage		0.7*Vdd_IO			V
V <sub>IL</sub>	Digital low-level input voltage				0.3*Vdd_IO	V
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = 4 mA <sup>(3)</sup>	Vdd_IO - 0.2			V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 4 mA <sup>(3)</sup>			0.2	V
T <sub>OP</sub>	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. It is possible to remove Vdd maintaining Vdd\_IO without blocking the communication bus, in this condition the measurement chain is powered off.
3. 4 mA is the maximum driving capability, that is, the maximum DC current that can be sourced/sunk by the digital pin in order to guarantee the correct digital output voltage levels V<sub>OH</sub> and V<sub>OL</sub>.

b. The product is factory calibrated at 2.5 V. The operational power supply range is from 1.71 V to 3.6 V.

## 2.4 Communication interface characteristics

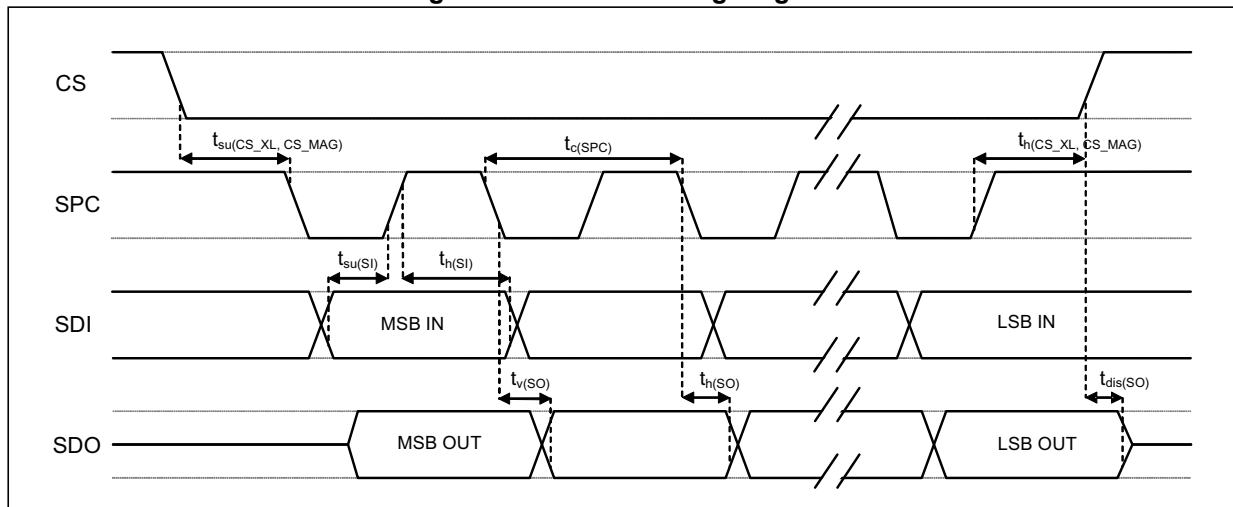
### 2.4.1 SPI - serial peripheral interface

Subject to general operating conditions for Vdd and Top.

Table 6. SPI slave timing values

Symbol	Parameter	Value <sup>(1)</sup>		Unit
		Min	Max	
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10	MHz
$t_{su(CS\_XL, CS\_MAG)}$	CS setup time	5		ns
$t_h(CS\_XL, CS\_MAG)$	CS hold time	20		
$t_{su(SI)}$	SDI input setup time	5		
$t_h(SI)$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_h(SO)$	SDO output hold time	5		
$t_{dis(SO)}$	SDO output disable time		50	

Figure 3. SPI slave timing diagram



Note: Values are guaranteed at 10 MHz clock frequency for SPI with 3 wires, based on characterization results, not tested in production.  
 Measurement points are done at  $0.3 \cdot V_{dd\_IO}$  and  $0.7 \cdot V_{dd\_IO}$  for both input and output ports.



## 2.4.2 I<sup>2</sup>C - inter-IC control interface

Subject to general operating conditions for V<sub>dd</sub> and Top.

**Table 7. I<sup>2</sup>C slave timing values (standard and fast mode)**

Symbol	Parameter	I <sup>2</sup> C standard mode <sup>(1)</sup>		I <sup>2</sup> C fast mode <sup>(1)</sup>		Unit
		Min	Max	Min	Max	
f <sub>(SCL)</sub>	SCL clock frequency	0	100	0	400	kHz
t <sub>w(SCLL)</sub>	Low period of the SCL clock	4.7		1.3		μs
t <sub>w(SCLH)</sub>	High period of the SCL clock	4.0		0.6		
t <sub>su(SDA)</sub>	Data setup time	250		100		ns
t <sub>h(SDA)</sub>	Data hold time	0	3.45	0	0.9	μs
t <sub>h(ST)</sub>	START condition hold time	4		0.6		
t <sub>su(SR)</sub>	Setup time for a repeated START condition	4.7		0.6		
t <sub>su(SP)</sub>	Setup time for STOP condition	4		0.6		
t <sub>w(SP:SR)</sub>	Bus free time between STOP and START condition	4.7		1.3		

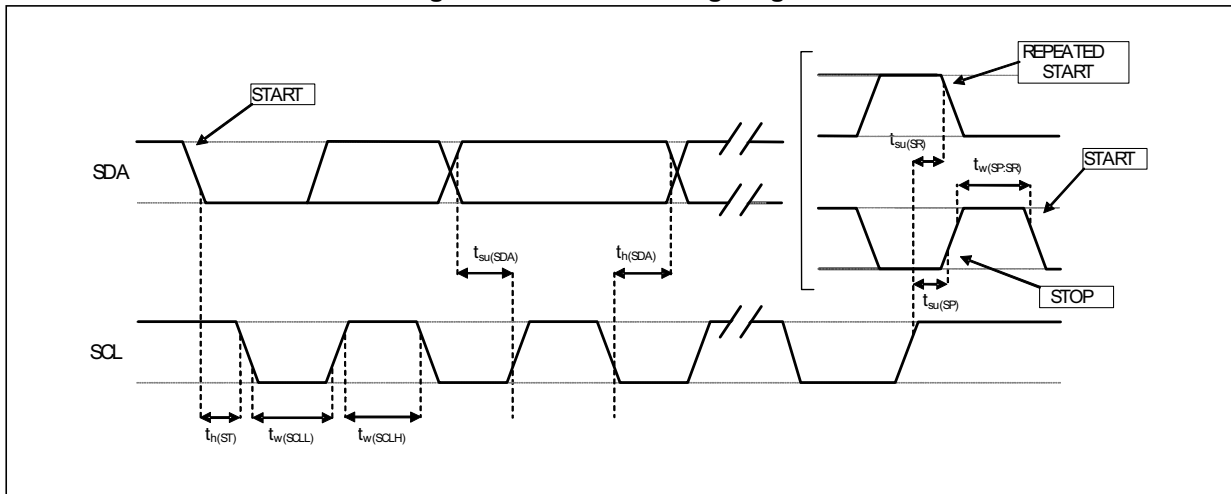
1. Data based on standard I<sup>2</sup>C protocol requirement, not tested in production.

**Table 8. I<sup>2</sup>C slave timing values (fast mode plus and high speed)**

Symbol	Parameter	I <sup>2</sup> C fast mode plus <sup>(1)</sup>		I <sup>2</sup> C high speed <sup>(1)</sup>		Unit
		Min	Max	Min	Max	
f <sub>(SCL)</sub>	SCL clock frequency	0	1	0	3.4	MHz
t <sub>w(SCLL)</sub>	Low period of the SCL clock	0.5		0.16		μs
t <sub>w(SCLH)</sub>	High period of the SCL clock	0.26		0.06		
t <sub>su(SDA)</sub>	Data setup time	50		10		ns
t <sub>h(SDA)</sub>	Data hold time	0		0	0.07	μs
t <sub>h(ST)</sub>	START condition hold time	0.26		0.16		
t <sub>su(SR)</sub>	Setup time for a repeated START condition	0.26		0.16		
t <sub>su(SP)</sub>	Setup time for STOP condition	0.26		0.16		
t <sub>w(SP:SR)</sub>	Bus free time between STOP and START condition	0.5				

1. Data based on standard I<sup>2</sup>C protocol requirement, not tested in production.

Figure 4. I<sup>2</sup>C slave timing diagram



Note: Measurement points are done at  $0.3 \cdot V_{dd\_IO}$  and  $0.7 \cdot V_{dd\_IO}$  for both ports.

## 2.5 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 9. Absolute maximum ratings**

Symbol	Ratings	Maximum value	Unit
V <sub>dd</sub>	Supply voltage	-0.3 to 4.8	V
V <sub>dd_IO</sub>	I/O pins supply voltage	-0.3 to 4.8	V
V <sub>in</sub>	Input voltage on any control pin (CS_XL, CS_MAG, SCL/SPC, SDA/SDI/SDO)	-0.3 to V <sub>dd_IO</sub> +0.3	V
A <sub>POW</sub>	Acceleration (any axis, powered, V <sub>dd</sub> = 2.5 V)	3000 for 0.5 ms	<i>g</i>
		10000 for 0.2 ms	<i>g</i>
A <sub>UNP</sub>	Acceleration (any axis, unpowered)	3000 for 0.5 ms	<i>g</i>
		10000 for 0.2 ms	<i>g</i>
M <sub>EF</sub>	Maximum exposed field	10000	gauss
T <sub>OP</sub>	Operating temperature range	-40 to +85	°C
T <sub>STG</sub>	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection (HBM)	2	kV

*Note:* Supply voltage on any pin should never exceed 4.8 V



This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.



This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

## 3 Terminology

### 3.1 Sensitivity

#### 3.1.1 Linear acceleration sensor sensitivity

Sensitivity describes the gain of the sensor and can be determined by applying 1 *g* acceleration to it. As the sensor can measure DC accelerations this can be done easily by pointing the axis of interest towards the center of the Earth, noting the output value, rotating the sensor by 180 degrees (pointing to the sky) and noting the output value again. By doing so,  $\pm 1$  *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and time. The sensitivity tolerance describes the range of sensitivities of a large population of sensors.

#### 3.1.2 Magnetic sensor sensitivity

Sensitivity describes the ratio of the output digital data expressed in LSB units and the applied magnetic field expressed in mG (milligauss). It can be measured, for example, by applying a known magnetic field along one axis and measuring the digital output of the device.

### 3.2 Zero-g level

The zero-*g* level offset (LA\_TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface measures 0 *g* on the X-axis and 0 *g* on the Y-axis whereas the Z-axis measures 1 *g*. The output is ideally in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as two's complement number). A deviation from the ideal value in this case is called zero-*g* offset. Offset is to some extent a result of stress to MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little with temperature, see [Table 3](#) "Zero-*g* level change vs. temperature" (LA\_TCOff). The zero-*g* level tolerance (TyOff) describes the standard deviation of the range of zero-*g* levels of a population of sensors.

### 3.3 Zero-gauss level

Zero-gauss level offset (M\_TyOff) describes the deviation of an actual output signal from the ideal output if no magnetic field is present.

### 3.4 Magnetic dynamic range

The magnetic dynamic range is defined as the magnetic field driven along one sensitive axis, giving the maximum digital output value.

## 4 Functionality

### 4.1 Magnetometer

#### 4.1.1 Magnetometer power modes

The LSM303AGR magnetometer provides two different power modes: high-resolution and low-power modes.

The tables below summarize the magnetometer RMS noise values and current consumption in different product configurations.

When the low-pass filter is enabled, the bandwidth is reduced while noise performance is improved without any increase in power consumption.

**Table 10. RMS noise of operating modes**

CFG_REG_B_M[LPF] or CFG_REG_B_M[OFF_CANC]	(CFG_REG_A_M [LP = 0]) high-resolution mode		(CFG_REG_A_M [LP = 1]) low-power mode	
	BW [Hz]	Noise RMS [mg]	BW [Hz]	Noise RMS [mg]
0 (disable)	ODR/2	4.5	ODR/2	9
1 (enable)	ODR/4	3	ODR/4	6

**Table 11. Current consumption of operating modes**

ODR (Hz)	Current consumption ( $\mu$ A) (CFG_REG_A_M [LP] = 0) high-resolution CFG_REG_B_M [OFF_CANC] = 0	Current consumption ( $\mu$ A) (CFG_REG_A_M [LP] = 1) low-power CFG_REG_B_M [OFF_CANC] = 0	Current consumption ( $\mu$ A) (CFG_REG_A_M [LP] = 0) high-resolution CFG_REG_B_M [OFF_CANC] = 1	Current consumption ( $\mu$ A) (CFG_REG_A_M [LP] = 1) low-power CFG_REG_B_M [OFF_CANC] = 1
10	100	25	120	50
20	200	50	235	100
50	475	125	575	235
100	950	250	1130	460

The following table summarizes the turn-on time of the magnetometer in the two different power modes with the offset cancellation function enabled or disabled (see [Section 4.1.2: Magnetometer offset cancellation](#)).

**Table 12. Operating mode and turn-on time**

Operating mode	Turn-on time		
	CFG_REG_A_M[LP]	CFG_REG_A_M[OFF_CANC = 0]	CFG_REG_A_M[OFF_CANC = 1]
0 (high-resolution)		9.4 ms	9.4 ms + 1/ODR
1 (low-power)		6.4 ms	6.4 ms + 1/ODR

The LSM303AGR offers single measurement mode in both high-resolution and low-power modes.

Single measurement mode is enabled by writing bits MD[1:0] to '01' in [CFG\\_REG\\_A\\_M \(60h\)](#).

In single measurement mode, once the measurement has been performed, the DRDY pin is set to high, data is available in the output register and the LSM303AGR is automatically configured in idle mode by setting the MD[1] bit to '1'.

Single measurement is independent of the programmed ODR but depends on the frequency at which the MD[1:0] bits are written by the microcontroller/application processor.

Maximum ODR frequency achievable in single mode measurement is given in the following table.

**Table 13. Maximum ODR in single measurement mode (HR and LP modes)**

Maximum ODR	Power mode (CFG_REG_A_M[LP])
100 Hz	High resolution (LP = 0)
150 Hz	Low power (LP = 1)

In single measurement mode, for ODR < 10 Hz, current consumption can be calculated with the following formula:

$$\text{Current\_consumption\_10Hz} - \text{Current\_consumption\_in\_power\_down} / (10 \text{ Hz} / \text{ODR}) + \text{Current\_consumption\_in\_power\_down}$$

Where Current\_consumption\_in\_power\_down and Current\_consumption\_10Hz can be found, respectively, in [Table 5](#) and [Table 11](#).

### 4.1.2 Magnetometer offset cancellation

Offset cancellation is the result of performing a set and reset in the magnetic sensor.

The offset cancellation technique is defined as follows:

$$H_{\text{out}} = \frac{H_n + H_{n-1}}{2}$$

where  $H_n$  and  $H_{n-1}$  are two consecutive magnetic field measurements, one after a set pulse, the other after a reset pulse.

Considering a magnetic offset ( $H_{\text{off}}$ ), the two magnetic field measurements are:

- Set:  $H_n = H + H_{\text{off}}$
- Reset:  $H_{n-1} = H - H_{\text{off}}$

The offset is cancelled according to the offset cancellation technique:

$$H_{\text{out}} = \frac{H_n + H_{n-1}}{2} = \frac{2H + H_{\text{off}} - H_{\text{off}}}{2} = H$$

In the LSM303AGR offset cancellation is enabled by setting bit `OFF_CANC = 1` (and bit `OFF_CANC_ONE_SHOT = 1` in single measurement mode) in [CFG\\_REG\\_B\\_M \(61h\)](#).

Offset cancellation is automatically managed by the device in continuous mode.

Offset cancellation has to be managed by the user in single measurement mode averaging two consecutive measurements  $H_n$  and  $H_{n-1}$ .

If offset cancellation is disabled, a set of the magnetic sensor is performed anyway.

The set pulse frequency can be configured by setting the `Set_FREQ` bit in [CFG\\_REG\\_B\\_M \(61h\)](#).

### 4.1.3 Magnetometer interrupt

In the LSM303AGR the magnetometer interrupt signal generation is based on the comparison between data and a programmable threshold.

To enable the interrupt function, in [INT\\_CTRL\\_REG\\_M \(63h\)](#) the `IEN` bit must be set to 1.

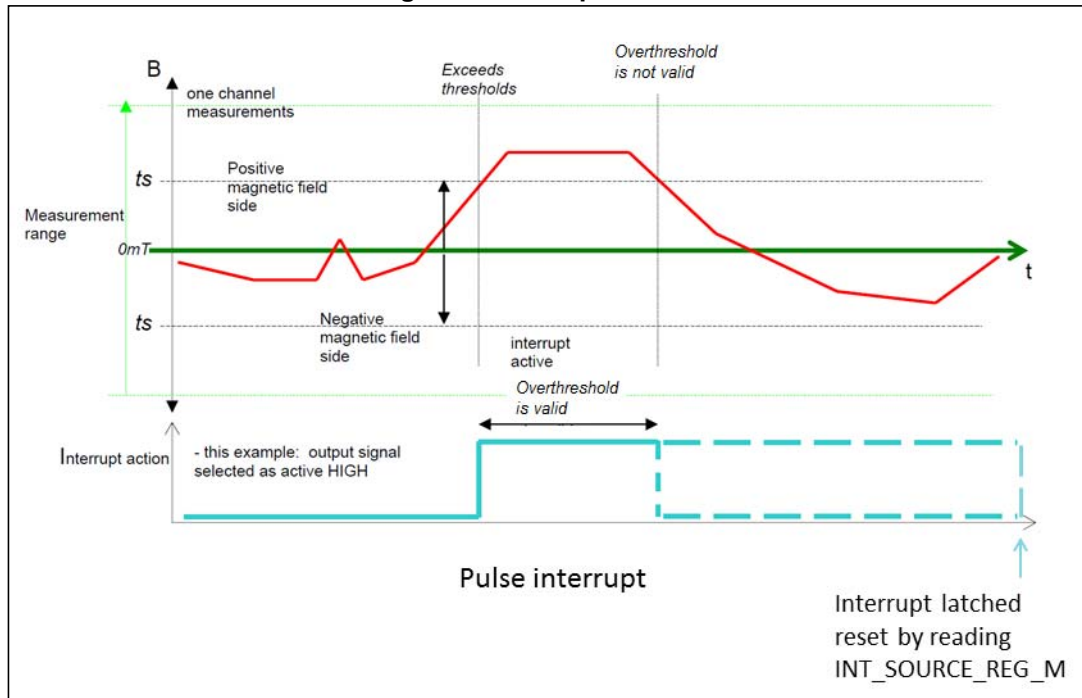
In the LSM303AGR the user can select the axis/axes in which the interrupt function can be enabled. In order to do this, the `XIEN`, `YIEN`, and `ZIEN` bits in [INT\\_CTRL\\_REG\\_M \(63h\)](#) need be set properly.

The threshold value can be programmed by setting the [INT\\_THS\\_L\\_REG\\_M \(65h\)](#) and [INT\\_THS\\_H\\_REG\\_M \(66h\)](#) registers.

The threshold is expressed in absolute value as a 15-bit unsigned number. The threshold has the same sensitivity as the magnetic data.

When magnetic data exceeds the positive or the negative threshold, the interrupt signal is generated and the information about the type of interrupt is stored in the [INT\\_SOURCE\\_REG\\_M \(64h\)](#) register. In particular, when magnetic data exceeds the positive threshold the `P_TH_S_axis` bit is set to 1, while if data exceeds the negative threshold the `N_TH_S_axis` bit is set to 1. If magnetic data lay between the positive and the negative thresholds, no interrupt signal is released.

Figure 5. Interrupt function



Two different approaches for the interrupt function are available:

- Typical: comparison is between magnetic data read by the sensor and the programmable threshold
- Advanced: comparison is made between magnetic data after hard-iron correction and the programmable threshold

These approaches are configurable by setting the INT\_on\_DataOFF bit in [CFG\\_REG\\_B\\_M \(61h\)](#).

If INT\_on\_DataOFF is set to 0 the typical approach is selected, otherwise if it is set to '1' the advanced approach is selected.

Two different interrupts are available:

- Pulsed interrupt signal: it goes high when the magnetic data exceed one of the two thresholds and goes low when the magnetic data are between the two thresholds. This kind of interrupt is selected by setting the IEL bit in [INT\\_CTRL\\_REG\\_M \(63h\)](#) to 0.
- Latched interrupt signal: it goes high when the data exceed one of the two thresholds but is reset only once the source register is read and not when the magnetic data returns between the two thresholds. This kind of interrupt is selected by setting the IEL bit in [INT\\_CTRL\\_REG\\_M \(63h\)](#) to 1.

The interrupt signal polarity can be set using the IEA bit in [INT\\_CTRL\\_REG\\_M \(63h\)](#).

If IEA is set to 1 then the interrupt signal is active high, while if it is set to 0 the interrupt signal is active low.

In order to drive the interrupt signal from the DRDY pad, the INT\_MAG\_PIN bit in [CFG\\_REG\\_C\\_M \(62h\)](#) must be set to 1.



#### 4.1.4 Magnetometer hard-iron compensation

Hard-iron distortion occurs when a magnetic object is placed near the magnetometer and appears as a permanent bias in the sensor's outputs.

The hard-iron correction consists of compensating magnetic data from hard-iron distortion.

The operation is defined as follows:

$$H_{\text{out}} = H_{\text{read}} - H_{\text{HI}}$$

where:

- $H_{\text{read}}$  is the generic uncompensated magnetic field data, as read by the sensor.
- $H_{\text{HI}}$  is the hard-iron distortion field.
- $H_{\text{out}}$  is the compensated magnetic data.

The computation of the hard-iron distortion field should be performed by an external processor. After the computation of the hard iron-distortion field has been performed, the measured magnetic data can be compensated.

The LSM303AGR offers the possibility of storing hard-iron data inside six dedicated registers from 45h to 4Ah.

Each register contains eight bits so that the hard-iron data can be expressed as a 16-bit two's complement number. The OFFSET\_axis\_REG\_H registers contain the MSBs of the hard-iron data, while the OFFSET\_axis\_REG\_L registers contain the LSBs.

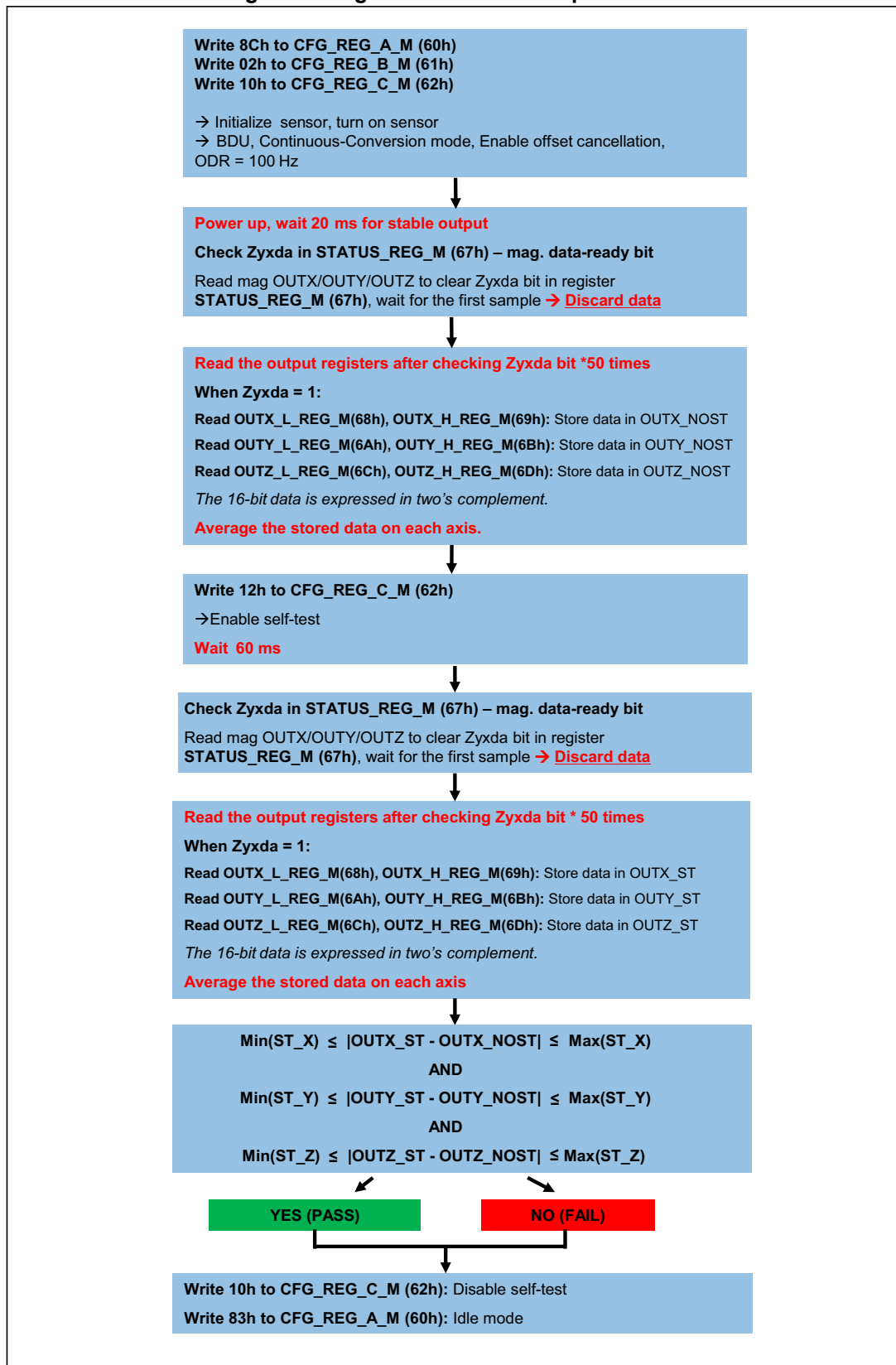
Hard-iron data have the same format and weight of the magnetic output data. The hard-iron values stored in dedicated registers are automatically subtracted from the output data.

#### 4.1.5 Magnetometer self-test

The self-test function is available for the magnetic sensor. When the magnetic self-test is enabled, a current is forced into a coil inside the device. This current generates a magnetic field that produces a variation of the magnetometer output signals. If the output signals change within the amplitude limits specified in [Table 3](#), then the sensor is working properly and the parameters of the interface chip are within the defined specifications.

The self-test procedure is described in the following figure.

Figure 6. Magnetometer self-test procedure



## 4.2 Accelerometer

### 4.2.1 Accelerometer power modes

The LSM303AGR accelerometer provides three different linear acceleration operating modes: *high-resolution mode*, *normal mode* and *low-power mode*.

The table below summarizes how to select the different operating modes.

**Table 14. Operating mode selection**

Operating mode	CTRL_REG1_A[3] (LPen bit)	CTRL_REG4_A[3] (HR bit)	BW [Hz]	Turn-on time	So @ ±2 g [mg/digit]
Low-power mode (8-bit data output)	1	0	ODR/2	1 ms	16
Normal mode (10-bit data output)	0	0	ODR/2	1.6 ms	4
High-resolution mode (12-bit data output)	0	1	ODR/9	7/ODR	1
Not allowed	1	1	--	--	--

The turn-on time to transition to another operating mode is given in [Table 15](#).

**Table 15. Turn-on time for operating mode transition**

Operating mode change	Turn-on time [s]
12-bit mode to 8-bit mode	1/ODR
12-bit mode to 10-bit mode	1/ODR
10-bit mode to 8-bit mode	1/ODR
10-bit mode to 12-bit mode	7/ODR
8-bit mode to 10-bit mode	1/ODR
8-bit mode to 12-bit mode	7/ODR

**Table 16. Current consumption of operating modes**

Operating mode [Hz]	Low-power mode (8-bit data output) [μA]	Normal mode (10-bit data output) [μA]	High resolution (12-bit data output) [μA]
1	3.7	3.7	3.7
10	4.4	5.4	5.4
25	5.6	8	8
50	7.7	12.6	12.6
100	11.7	22	22
200	20	40	40
400	36	75	75
1344	--	185	185

**Table 16. Current consumption of operating modes (continued)**

Operating mode [Hz]	Low-power mode (8-bit data output) [µA]	Normal mode (10-bit data output) [µA]	High resolution (12-bit data output) [µA]
1620	102	--	--
5376	186	--	--

### 4.2.2 Accelerometer 6D / 4D orientation detection

The LSM303AGR includes 6D / 4D orientation detection which applies only to the accelerometer.

In this configuration the interrupt is generated when the device is stable in a known direction. In 4D configuration, detection of the position of the Z-axis is disabled.

### 4.2.3 Accelerometer activity/inactivity function

The activity/inactivity recognition function allows reducing the power consumption of the accelerometer block in order to supply other smart applications and is applicable only to the accelerometer block of the device.

When the activity/inactivity recognition function is activated, accelerometer is able to automatically go to 10 Hz sampling rate and to wake up as soon as the interrupt event has been detected, increasing the output data rate and bandwidth.

With this feature the system may be efficiently switched from/to low-power mode to full performance depending on user-selectable positioning and acceleration events, thus ensuring power saving and flexibility.

The activity/inactivity recognition function is activated by writing the desired threshold in the *Act\_THS\_A (3Eh)* register. The high-pass filter is automatically enabled.

**Table 17. Activity/inactivity function control registers**

Register	LSB value
ACT_THS_A	Full scale / 128 [mg]
ACT_DUR_A	8/ODR [s]

When the acceleration becomes smaller than the threshold for at least the duration  $(8 \cdot \text{ACT\_DUR} + 1) / \text{ODR}$ , the ODR [3:0] bits of *CTRL\_REG1\_A (20h)* are bypassed (inactivity) and internally set to 10 Hz (ODR [3:0] = 0010), but the content of the *CTRL\_REG1\_A (20h)* (ODR [3:0]) bits are left untouched.

When the acceleration becomes greater than the threshold (*Act\_THS\_A (3Eh)*), *CTRL\_REG1\_A (20h)* is restored immediately (activity).

Once the activity/inactivity detection function is enabled, it is applied to the INT\_2 pin by setting the *CTRL\_REG6\_A (25h)* (P2\_ACT) bit to 1.

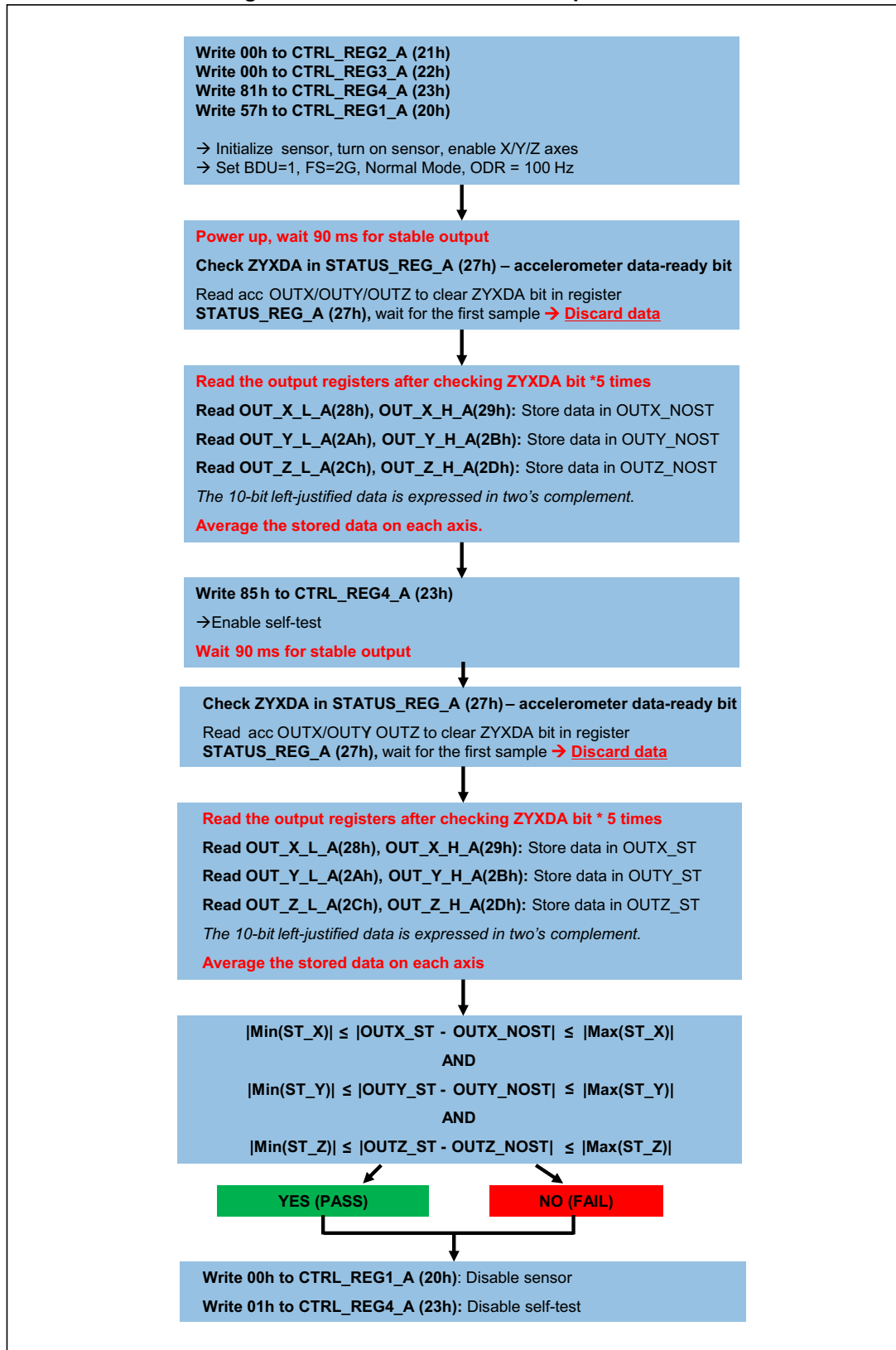
To disable the activity/inactivity detection function, set the content of the *Act\_THS\_A (3Eh)* register to 00h.

#### 4.2.4 Accelerometer self-test

The self-test allows the user to check the sensor functionality without moving it. When the self-test is enabled, an actuation force is applied to the sensor, simulating a definite input acceleration. In this case, the sensor outputs exhibit a change in their DC levels which are related to the selected full scale through the device sensitivity. When the self-test is activated, the device output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test-force. If the output signals change within the amplitude specified inside [Table 3](#), then the sensor is working properly and the parameters of the interface chip are within the defined specifications.

The self-test procedure is described in the following figure.

Figure 7. Accelerometer self-test procedure



## 4.3 IC interface

The complete measurement chain is composed of a low-noise capacitive amplifier which converts the capacitive unbalancing of the MEMS sensor into an analog voltage using an analog-to-digital converter.

The acceleration and magnetic data may be accessed through an I<sup>2</sup>C/SPI interface thus making the device particularly suitable for direct interfacing with a microcontroller.

The LSM303AGR features a data-ready signal which indicates when new sets of measured acceleration and magnetic data are available, thus simplifying data synchronization in the digital system that uses the device.

## 4.4 FIFO

The FIFO buffer applies only to the accelerometer. The LSM303AGR embeds a 32-level FIFO for each of the three output channels, X, Y and Z. This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO.

In order to enable the FIFO buffer, the FIFO\_EN bit in *CTRL\_REG5\_A (24h)* must be set to 1.

This buffer can work according to the following different modes: Bypass mode, FIFO mode, Stream mode and Stream-to-FIFO mode. Each mode is selected by the FM [1:0] bits in *FIFO\_CTRL\_REG\_A (2Eh)*. Programmable FIFO watermark level, FIFO empty or FIFO overrun events can be enabled to generate dedicated interrupts on the INT\_1\_XL pin (configuration through *CTRL\_REG3\_A (22h)*).

In the *FIFO\_SRC\_REG\_A (2Fh)* register the EMPTY bit is equal to 1 when all FIFO samples are ready and FIFO is empty.

In the *FIFO\_SRC\_REG\_A (2Fh)* register the WTM bit goes to 1 if new data is written in the buffer and *FIFO\_SRC\_REG\_A (2Fh)* (FSS [4:0]) is greater than or equal to *FIFO\_CTRL\_REG\_A (2Eh)* (FTH [4:0]). *FIFO\_SRC\_REG\_A (2Fh)* (WTM) goes to 0 if reading an X, Y, Z data slot from FIFO and *FIFO\_SRC\_REG\_A (2Fh)* (FSS [4:0]) is less than or equal to *FIFO\_CTRL\_REG\_A (2Eh)* (FTH [4:0]).

In the *FIFO\_SRC\_REG\_A (2Fh)* register the OVRN\_FIFO bit is equal to 1 if the FIFO slot is overwritten.

### 4.4.1 Bypass mode

In Bypass mode the FIFO is not operational and for this reason it remains empty. For each channel only the first address is used. The remaining FIFO levels are empty.

Bypass mode must be used in order to reset the FIFO buffer when a different mode is operating (that is, FIFO mode).

### 4.4.2 FIFO mode

In FIFO mode, the buffer continues filling data from the X, Y and Z accelerometer channels until it is full (a set of 32 samples stored). When the FIFO is full, it stops collecting data from the input channels and the FIFO content remains unchanged.

An overrun interrupt can be enabled, I1\_OVERRUN = 1 in the *CTRL\_REG3\_A (22h)* register, in order to be raised when the FIFO stops collecting data. When the overrun interrupt occurs, the first data has been overwritten and the FIFO stops collecting data from the input channels.

After the last read it is necessary to exit Bypass mode in order to reset the FIFO content. After this reset command, it is possible to restart FIFO mode just by selecting the FIFO mode configuration (FM[1:0] bits) in register *FIFO\_CTRL\_REG\_A (2Eh)*.

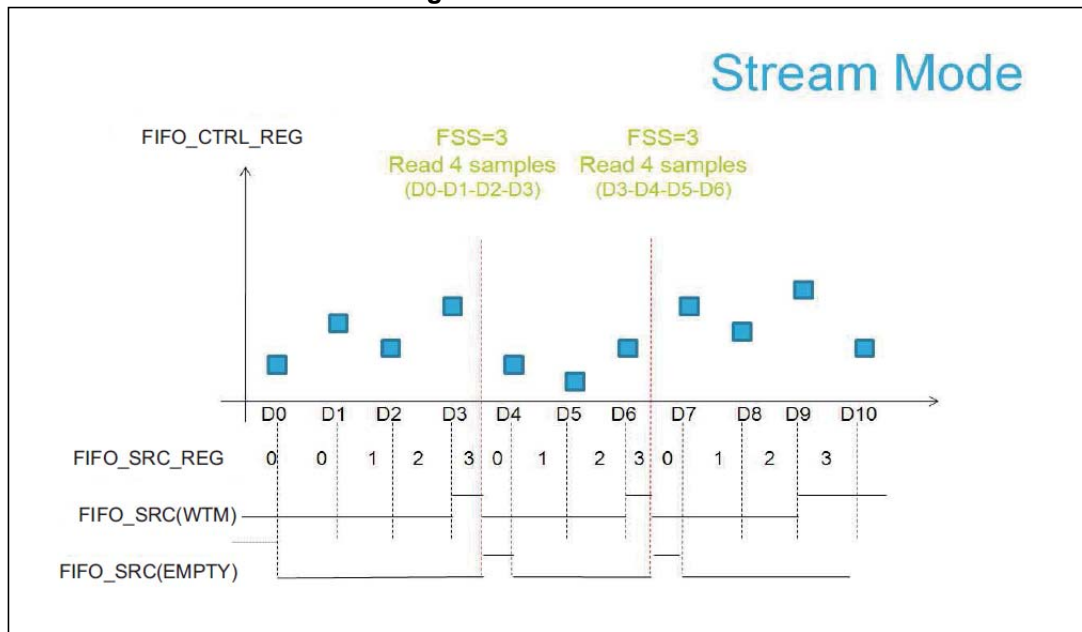
### 4.4.3 Stream mode

In Stream mode the FIFO continues filling data from the X, Y, and Z accelerometer channels until the buffer is full (a set of 32 samples stored) at which point the FIFO buffer index restarts from the beginning and older data is replaced by the current data. The oldest values continue to be overwritten until a read operation frees the FIFO slots.

An overrun interrupt can be enabled, I\_XL\_OVERRUN = 1 in the *CTRL\_REG3\_A (22h)* register, in order to read the entire contents of the FIFO at once. If, in the application, it is mandatory not to lose data and it is not possible to read at least one sample for each axis within one ODR period, a watermark interrupt can be enabled in order to read partially the FIFO and leave memory slots free for incoming data.

Setting the FTH [4:0] bit in the *FIFO\_CTRL\_REG\_A (2Eh)* register to an N value, the number of X, Y and Z data samples that should be read at the rise of the watermark interrupt is up to (N+1).

Figure 8. Stream mode





#### 4.4.4 Stream-to-FIFO mode

In Stream-to-FIFO mode, data from the X, Y and Z accelerometer channels are collected in a combination of Stream mode and FIFO mode. The FIFO buffer starts operating in Stream mode and switches to FIFO mode when the selected interrupt occurs.

When an interrupt event is configured on the INT\_1\_XL pin, the FIFO operates in Stream mode if the INT\_1\_XL pin value is equal to 0 and it operates in FIFO mode if the INT\_1\_XL pin value is equal to 1. Switching modes is dynamically performed according to the INT\_1\_XL pin value.

Stream-to-FIFO can be used in order to analyze the sampling history that generates an interrupt. The standard operation is to read the contents of FIFO when the FIFO mode is triggered and the FIFO buffer is full and stopped.

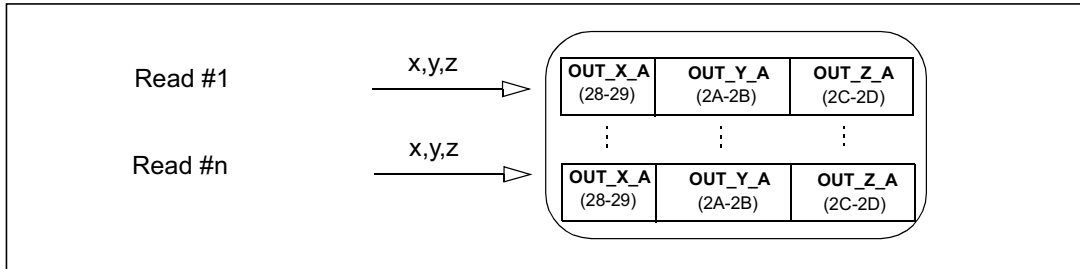
#### 4.4.5 Retrieving data from FIFO

FIFO data is read from the [OUT\\_X\\_L\\_A \(28h\)](#), [OUT\\_X\\_H\\_A \(29h\)](#), [OUT\\_Y\\_L\\_A \(2Ah\)](#), [OUT\\_Y\\_H\\_A \(2Bh\)](#), and [OUT\\_Z\\_L\\_A \(2Ch\)](#), [OUT\\_Z\\_H\\_A \(2Dh\)](#) registers. A read operation using a serial interface of the [OUT\\_X\\_L\\_A \(28h\)](#), [OUT\\_X\\_H\\_A \(29h\)](#), [OUT\\_Y\\_L\\_A \(2Ah\)](#), [OUT\\_Y\\_H\\_A \(2Bh\)](#) or [OUT\\_Z\\_L\\_A \(2Ch\)](#), [OUT\\_Z\\_H\\_A \(2Dh\)](#) output registers provides the data stored in the FIFO. Each time data is read from the FIFO, the oldest X, Y and Z data are placed in the [OUT\\_X\\_L\\_A \(28h\)](#), [OUT\\_X\\_H\\_A \(29h\)](#), [OUT\\_Y\\_L\\_A \(2Ah\)](#), [OUT\\_Y\\_H\\_A \(2Bh\)](#) and [OUT\\_Z\\_L\\_A \(2Ch\)](#), [OUT\\_Z\\_H\\_A \(2Dh\)](#) registers and both single read and read\_burst operations can be used.

### 4.4.6 FIFO multiple read (burst)

Starting from Addr 28h multiple reads can be performed. Once the read reaches Addr 2Dh, the system automatically restarts from Addr 28h.

Figure 9. FIFO multiple read



## 4.5 Temperature sensor

The LSM303AGR is supplied with an internal temperature sensor. Temperature data can be enabled by setting the TEMP\_EN[1:0] bits to 1 in the *TEMP\_CFG\_REG\_A (1Fh)* register.

To retrieve the temperature sensor data the BDU bit in *CTRL\_REG4\_A (23h)* must be set to 1.

Both the *OUT\_TEMP\_L\_A (0Ch)*, *OUT\_TEMP\_H\_A (0Dh)* registers must be read.

Temperature data is stored inside OUT\_TEMP\_H as two's complement data in 8-bit format left-justified.

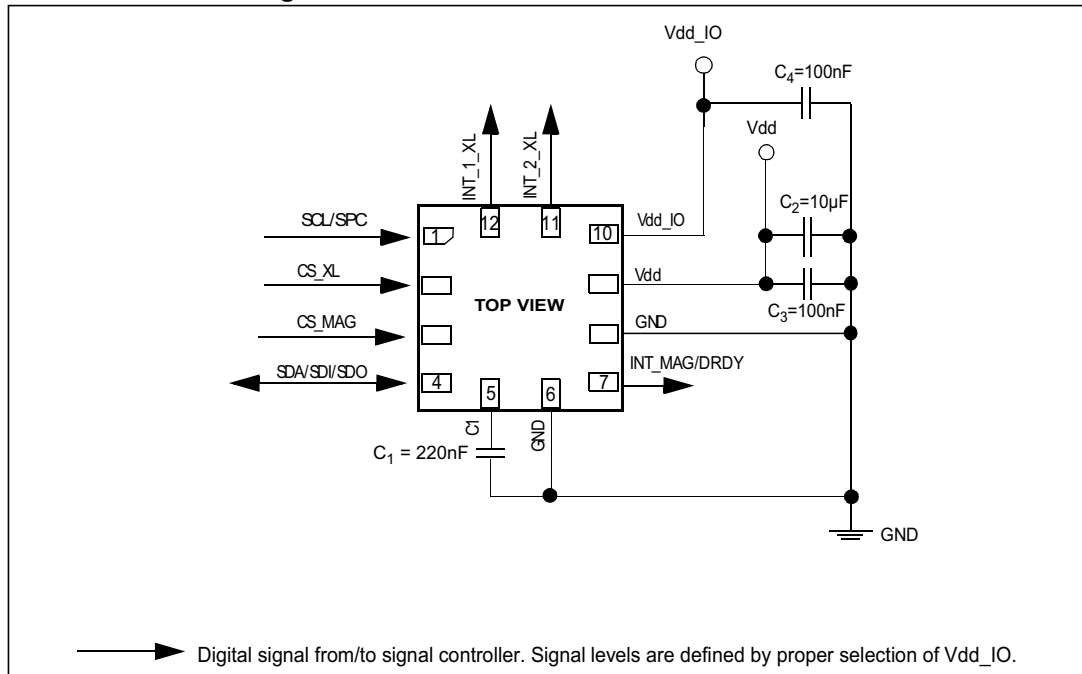
## 4.6 Factory calibration

The IC interface is factory calibrated for sensitivity (LA\_So, M\_GN), Zero-g level (LA\_TyOff) and Zero-gauss level (M\_TyOff).

The trim values are stored inside the device in nonvolatile memory. Anytime the device is turned on, the trim parameters are downloaded into the registers to be used during active operation. This allows using the device without further calibration.

## 5 Application hints

Figure 10. LSM303AGR electrical connections



The device core is supplied through the Vdd line while the I/O pads are supplied through the Vdd\_IO line. Power supply decoupling capacitors (100 nF ceramic, 10 µF aluminum) should be placed as near as possible to pin 9 of the device (common design practice).

It is possible to remove Vdd, maintaining Vdd\_IO, without blocking the communication bus, in this condition the measurement chain is powered off.

The following recommendations apply to capacitor C1:

- It must be connected as close as possible to pins 5 and 6 since very high current pulses flow from C1 to pin 5 and 6. This avoid problems caused by inductive effects due to the length of the copper strips.
- It is highly recommended to use low ESR (max 200 mOhm)

The functionality of the device and the measured acceleration data are selectable and accessible through the I<sup>2</sup>C or SPI interfaces. When using the I<sup>2</sup>C, CS must be tied high (that is, connected to Vdd\_IO).

The functions, the threshold and the timing of the three interrupt pins (INT\_1\_XL, INT\_2\_XL, and INT\_MAG) can be completely programmed by the user through the I<sup>2</sup>C/SPI interface.

### 5.1 Soldering information

The LGA package is compliant with the ECOPACK and RoHS standards. It is qualified for soldering heat resistance according to JEDEC J-STD-020.

For land pattern and soldering recommendations, consult technical note TN0018 available on [www.st.com](http://www.st.com).

## 5.2 High-current wiring effects

High current in wiring and printed circuit traces can be culprits in causing errors in magnetic field measurements for compassing.

Conductor-generated magnetic fields add to the Earth's magnetic field, leading to errors in compass heading computation.

Keep currents higher than 10 mA a few millimeters away from the sensor IC.

## 5.3 Startup sequence

The following general-purpose sequence can be used to configure the magnetometer and accelerometer:

1. Write `CFG_REG_A_M = 00h` // Mag = 10 Hz (high-resolution and continuous mode)
2. Write `CFG_REG_C_M = 01h` // Mag data-ready interrupt enable
3. Write `CTRL_REG1_A = 57h` // Accel = 100 Hz (normal mode)

## 6 Digital interfaces

The registers embedded inside the LSM303AGR may be accessed through both the I<sup>2</sup>C and SPI serial interfaces. The latter may be SW-configured to operate in 3-wire interface mode.

The serial interfaces are mapped onto the same pads. To select/exploit the I<sup>2</sup>C interface, the CS line must be tied high (that is, connected to Vdd\_IO).

**Table 18. Serial interface pin description**

Pin name	Pin description
CS_XL, CS_MAG	SPI enable I <sup>2</sup> C/SPI mode selection (1: SPI idle mode / I <sup>2</sup> C communication enabled; 0: SPI communication mode / I <sup>2</sup> C disabled)
SCL	I <sup>2</sup> C serial clock (SCL)
SPC	SPI serial port clock (SPC)
SDA	I <sup>2</sup> C serial data (SDA)
SDI	SPI serial data input (SDI)
SDO	3-wire interface serial data output (SDO)

### 6.1 I<sup>2</sup>C serial interface

The LSM303AGR I<sup>2</sup>C is a bus slave. The I<sup>2</sup>C is employed to write data into registers whose content can also be read back.

The relevant I<sup>2</sup>C terminology is given in the table below.

**Table 19. I<sup>2</sup>C terminology**

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I<sup>2</sup>C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both the lines must be connected to Vdd\_IO through an external pull-up resistor. When the bus is free, both the lines are high.

The I<sup>2</sup>C interface is compliant with fast mode (400 kHz) I<sup>2</sup>C standards as well as with the normal mode.

### 6.1.1 I<sup>2</sup>C operation

The transaction on the bus is started through a start (ST) signal. A start condition is defined as a high to low transition on the data line while the SCL line is held high. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line low so that it remains stable low during the high period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I<sup>2</sup>C embedded inside the LSM303AGR behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit subaddress (SUB) is transmitted: the 7 LSb represent the actual register address while the MSB enables address auto increment. If the MSb of the SUB field is 1, the SUB (register address) is automatically increased to allow multiple data read/writes.

The slave address is completed with a read/write bit. If the bit is 1 (read), a repeated START (SR) condition must be issued after the two subaddress bytes; if the bit is 0 (write) the master transmits to the slave with direction unchanged. [Table 24](#) explains how the SAD+read/write bit pattern is composed, listing all the possible configurations.

**Table 20. Transfer when master is writing one byte to slave**

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

**Table 21. Transfer when master is writing multiple bytes to slave**

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

**Table 22. Transfer when master is receiving (reading) one byte of data from slave**

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

**Table 23. Transfer when master is receiving (reading) multiple bytes of data from slave**

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the most significant bit (MSb) first. If a slave receiver doesn't acknowledge the slave address (that is, it is not able

to receive because it is performing some real-time function) the data line must be left high by the slave. The master can then abort the transfer. A low to high transition on the SDA line while the SCL line is high is defined as a stop condition. Each data transfer must be terminated by the generation of a stop (SP) condition.

In the presented communication format MAK is master acknowledge and NMAK is no master acknowledge.

**Default address:**

The accelerometer sensor slave address is 0011001b while magnetic sensor slave address is 0011110b.

The slave addresses are completed with a read/write bit. If the bit was 1 (read), a repeated start (SR) condition must be issued after the two subaddress bytes. If the bit is 0 (write), the master transmits to the slave with direction unchanged. *Table 24* and *Table 25* explain how the SAD+read/write bit patterns are composed, listing all the possible configurations.

**Linear acceleration sensor: the default (factory setting) 7-bit slave address is 0011001b.**

**Table 24. SAD + read/write patterns**

Command	SAD[6:0]	R/W	SAD + R/W
Read	0011001	1	00110011 (33h)
Write	0011001	0	00110010 (32h)

**Magnetic field sensor: the default (factory setting) 7-bit slave address is 0011110b.**

**Table 25. SAD + read/write patterns**

Command	SAD[6:0]	R/W	SAD + R/W
Read	0011110	1	00111101 (3Dh)
Write	0011110	0	00111100 (3Ch)

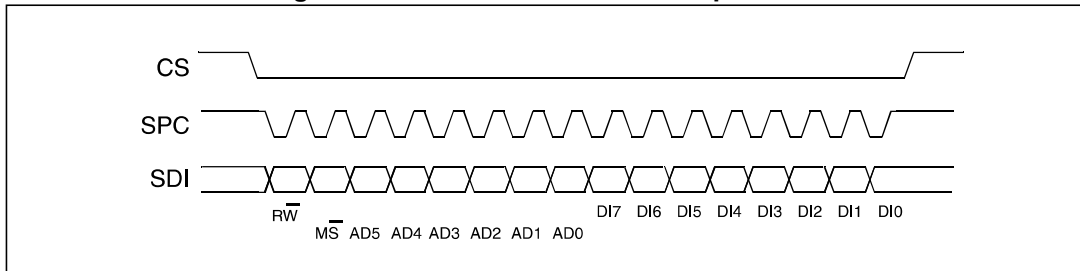
## 6.2 SPI bus interface

The LSM303AGR SPI is a bus slave. The SPI allows writing and reading the registers of the device.

The serial interface interacts with the application using 3 wires: **CS\_XL** or **CS\_MAG**, **SPC**, **SDI/O**.

### 6.2.1 Accelerometer SPI write

Figure 11. Accelerometer SPI write protocol



The SPI Write command is performed with 16 clock pulses. A multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

**bit 0:** WRITE bit. The value is 0.

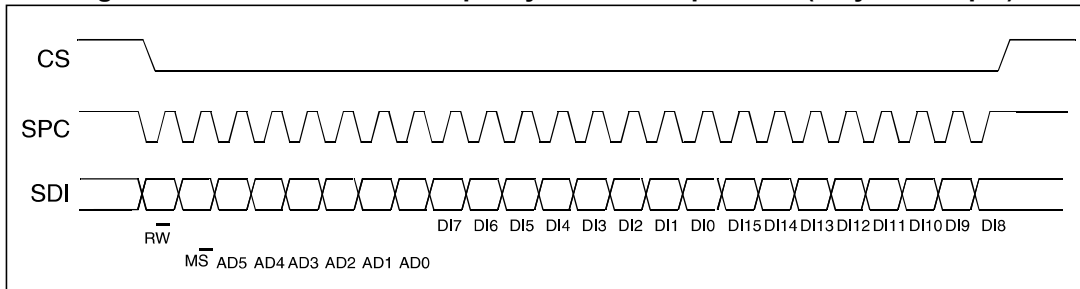
**bit 1:** MS bit. When 0 do not increment address, when 1 increment address in multiple writing.

**bit 2-7:** address AD(5:0). This is the address field of the indexed register.

**bit 8-15:** data 01(7:0) {write mode). This is the data that is written inside the device (MSb first).

**bit 16-...:** data DI(...-8). Further data in multiple byte writes.

Figure 12. Accelerometer multiple byte SPI write protocol (2-byte example)

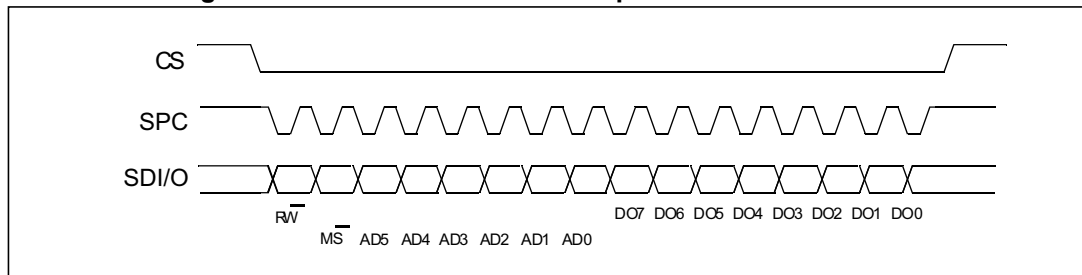




### 6.2.2 Accelerometer SPI read in 3-wire mode

3-wire mode is entered by setting the *CTRL\_REG4\_A (23h)* (SPI\_ENABLE) bit equal 1 (SPI serial interface read enable).

**Figure 13. Accelerometer SPI read protocol in 3-wire mode**



The SPI read command is performed with 16 clock pulses:

**bit 0:** READ bit. The value is 1.

**bit 1:** MS bit. When 0, does not increment the address; when 1, increments the address in multiple reads.

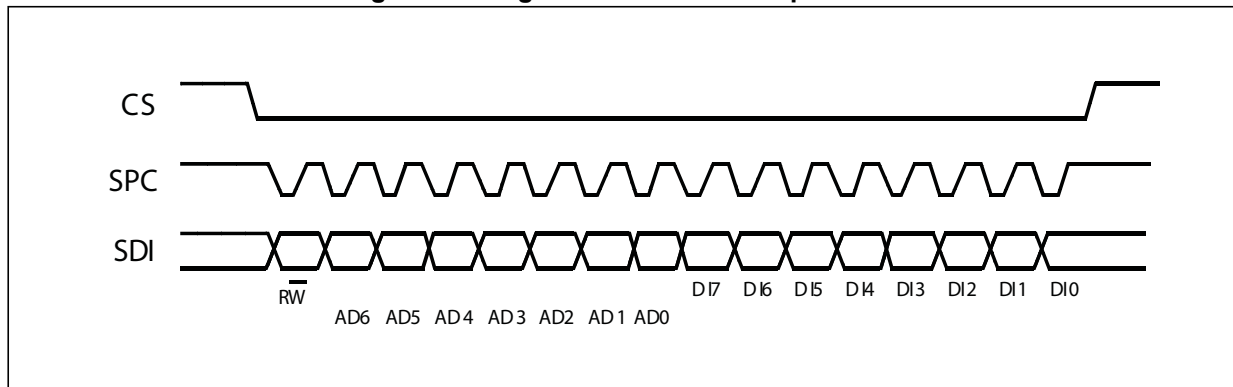
**bit 2-7:** address AD(5:0). This is the address field of the indexed register.

**bit 8-15:** data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

A multiple read command is also available in 3-wire mode.

### 6.2.3 Magnetometer SPI write

**Figure 14. Magnetometer SPI write protocol**



The SPI write command is performed with 16 clock pulses. The multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

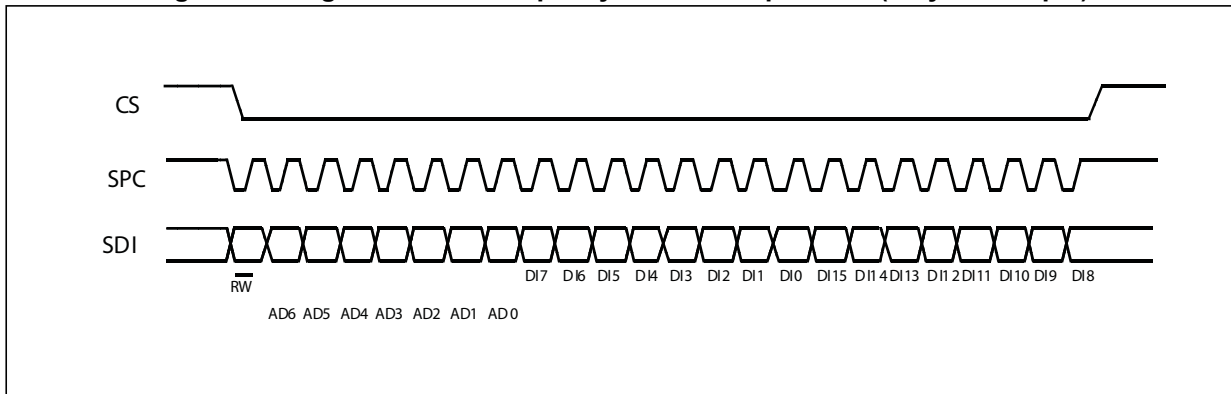
**bit 0:** WRITE bit. The value is 0.

**bit 1-7:** address AD(6:0). This is the address field of the indexed register.

**bit 8-15:** data DI(7:0) (write mode). This is the data that is written inside the device (MSb first).

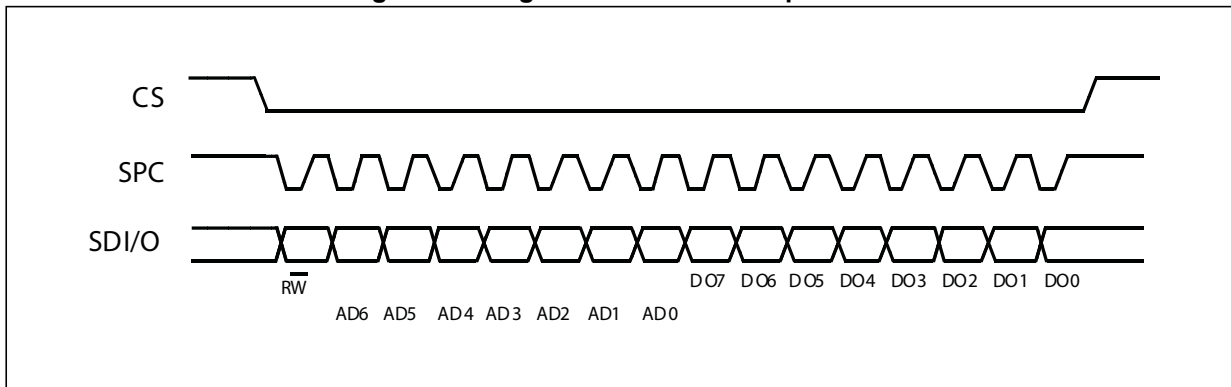
**bit 16-... :** data DI(...-8). Further data in multiple byte writes.

Figure 15. Magnetometer multiple byte SPI write protocol (2-byte example)



### 6.2.4 Magnetometer SPI read

Figure 16. Magnetometer SPI read protocol



The SPI read command is performed with 16 clock pulses:

**bit 0:** WRITE bit. The value is 1.

**bit 1-7:** address AD(6:0). This is the address field of the indexed register.

**bit 8-15:** data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

A multiple read command is available in 3-wire mode.

## 7 Register mapping

The table given below provides a list of the 8-bit registers embedded in the device and the corresponding addresses. Registers 00h through 3Fh are dedicated to the accelerometer while registers 40h through 6Fh are dedicated to the magnetometer.

**Table 26. Register address map**

Name	Type <sup>(1)</sup>	Register address		Default	Comment
		Hex	Binary		
Reserved		00 - 06			Reserved
STATUS_REG_AUX_A	R	07	000 0111		
Reserved	R	08-0B			Reserved
OUT_TEMP_L_A	R	0C	000 1100	Output	Output registers
OUT_TEMP_H_A	R	0D	000 1101	Output	
INT_COUNTER_REG_A	R	0E	000 1110		
WHO_AM_I_A	R	0F	000 1111	00110011	Dummy register
Reserved		10 - 1E			Reserved
TEMP_CFG_REG_A	R/W	1F	001 1111	00000000	
CTRL_REG1_A	R/W	20	010 0000	00000111	Accelerometer control registers
CTRL_REG2_A	R/W	21	010 0001	00000000	
CTRL_REG3_A	R/W	22	010 0010	00000000	
CTRL_REG4_A	R/W	23	010 0011	00000000	
CTRL_REG5_A	R/W	24	010 0100	00000000	
CTRL_REG6_A	R/W	25	010 0101	00000000	
REFERENCE/DATACAPTURE_A	R/W	26	010 0110	00000000	
STATUS_REG_A	R	27	010 0111	00000000	Accelerometer status register
OUT_X_L_A	R	28	010 1000	Output	Accelerometer output registers
OUT_X_H_A	R	29	010 1001	Output	
OUT_Y_L_A	R	2A	010 1010	Output	
OUT_Y_H_A	R	2B	010 1011	Output	
OUT_Z_L_A	R	2C	010 1100	Output	
OUT_Z_H_A	R	2D	010 1101	Output	
FIFO_CTRL_REG_A	R/W	2E	010 1110	00000000	FIFO registers
FIFO_SRC_REG_A	R	2F	010 1111	0010000	

Table 26. Register address map (continued)

Name	Type <sup>(1)</sup>	Register address		Default	Comment
		Hex	Binary		
INT1_CFG_A	R/W	30	011 0000	00000000	Interrupt 1 registers
INT1_SRC_A	R	31	011 0001	00000000	
INT1_THS_A	R/W	32	011 0010	00000000	
INT1_DURATION_A	R/W	33	011 0011	00000000	
INT2_CFG_A	R/W	34	011 0100	00000000	Interrupt 2 registers
INT2_SRC_A	R	35	011 0101	00000000	
INT2_THS_A	R/W	36	011 0110	00000000	
INT2_DURATION_A	R/W	37	011 0111	00000000	
CLICK_CFG_A	R/W	38	011 1000	00000000	
CLICK_SRC_A	R	39	011 1001	00000000	
CLICK_THS_A	R/W	3A	011 1010	00000000	
TIME_LIMIT_A	R/W	3B	011 1011	00000000	
TIME_LATENCY_A	R/W	3C	011 1100	00000000	
TIME_WINDOW_A	R/W	3D	011 1101	00000000	
Act_THS_A	R/W	3E	011 1110	00000000	
Act_DUR_A	R/W	3F	011 1111	00000000	
RESERVED		40-44			
OFFSET_X_REG_L_M	R/W	45	01000101	00000000	Magnetometer hard-iron registers
OFFSET_X_REG_H_M	R/W	46	01000110	00000000	
OFFSET_Y_REG_L_M	R/W	47	01000111	00000000	
OFFSET_Y_REG_H_M	R/W	48	01001000	00000000	
OFFSET_Z_REG_L_M	R/W	49	01001001	00000000	
OFFSET_Z_REG_H_M	R/W	4A	01001010	00000000	
RESERVED		4B-4C			
WHO_AM_I_M	R	4F	01001111	01000000	
RESERVED		50-5F			
CFG_REG_A_M	R/W	60	01100000	00000011	Magnetometer configuration registers
CFG_REG_B_M	R/W	61	01100001	00000000	
CFG_REG_C_M	R/W	62	01100010	00000000	
INT_CTRL_REG_M	R/W	63	01100011	11100000	Magnetometer interrupt configuration registers
INT_SOURCE_REG_M	R	64	01100100		
INT_THS_L_REG_M	R/W	65	01100101	00000000	
INT_THS_H_REG_M	R/W	66	01100110	00000000	

**Table 26. Register address map (continued)**

Name	Type <sup>(1)</sup>	Register address		Default	Comment
		Hex	Binary		
STATUS_REG_M	R	67	01100111		
OUTX_L_REG_M	R	68	01101000	output	Magnetometer output registers
OUTX_H_REG_M	R	69	01101001	output	
OUTY_L_REG_M	R	6A	01101010	output	
OUTY_H_REG_M	R	6B	01101010	output	
OUTZ_L_REG_M	R	6C	01101100	output	
OUTZ_H_REG_M	R	6D	01101101	output	
RESERVED		6E-6F			

1. R = read-only register, R/W = readable/writable register

Reserved registers must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

## 8 Register description

### 8.1 STATUS\_REG\_AUX\_A (07h)

Table 27. STATUS\_REG\_AUX register

--	TOR	--	--	--	TDA	--	--
----	-----	----	----	----	-----	----	----

Table 28. STATUS\_REG\_AUX description

TOR	Temperature data overrun. Default value: 0 (0: no overrun has occurred; 1: new temperature data has overwritten the previous data)
TDA	Temperature new data available. Default value: 0 (0: new temperature data is not yet available; 1: new temperature data is available)

### 8.2 OUT\_TEMP\_L\_A (0Ch), OUT\_TEMP\_H\_A (0Dh)

Temperature sensor data. Refer to [Section 4.5: Temperature sensor](#) for details on how to enable and read the temperature sensor output data.

### 8.3 INT\_COUNTER\_REG\_A (0Eh)

Table 29. INT\_COUNTER\_REG register

IC7	IC6	IC5	IC4	IC3	IC2	IC1	IC0
-----	-----	-----	-----	-----	-----	-----	-----

### 8.4 WHO\_AM\_I\_A (0Fh)

Table 30. WHO\_AM\_I register

0	0	1	1	0	0	1	1
---	---	---	---	---	---	---	---

Device identification register.

### 8.5 TEMP\_CFG\_REG\_A (1Fh)

Table 31. TEMP\_CFG\_REG register

TEMP_EN1	TEMP_EN0	0	0	0	0	0	0
----------	----------	---	---	---	---	---	---

Table 32. TEMP\_CFG\_REG description

TEMP_EN[1:0]	Enables temperature sensor (T). Default value: 00 (00: T disabled; 11: T enabled)
--------------	--

## 8.6 CTRL\_REG1\_A (20h)

**Table 33. CTRL\_REG1 register**

ODR3	ODR2	ODR1	ODR0	LPen	Zen	Yen	Xen
------	------	------	------	------	-----	-----	-----

**Table 34. CTRL\_REG1 description**

ODR[3:0]	Data rate selection. Default value: 0000 (0000: power-down mode; others: refer to <a href="#">Table 35</a> )
LPen	Enables low-power mode. Default value: 0 (0: normal mode, 1: low-power mode) (Refer to <a href="#">Section 4.2.1: Accelerometer power modes</a> )
Zen	Enables Z-axis. Default value: 1 (0: Z-axis disabled; 1: Z-axis enabled)
Yen	Enables Y-axis. Default value: 1 (0: Y-axis disabled; 1: Y-axis enabled)
Xen	Enables X-axis. Default value: 1 (0: X-axis disabled; 1: X-axis enabled)

**ODR[3:0]** is used to set the power mode and ODR selection. The following table indicates the frequency of each combination of ODR[3:0].

**Table 35. Data rate configuration**

ODR3	ODR2	ODR1	ODR0	Power mode selection
0	0	0	0	Power-down mode
0	0	0	1	HR / Normal / Low-power mode (1 Hz)
0	0	1	0	HR / Normal / Low-power mode (10 Hz)
0	0	1	1	HR / Normal / Low-power mode (25 Hz)
0	1	0	0	HR / Normal / Low-power mode (50 Hz)
0	1	0	1	HR / Normal / Low-power mode (100 Hz)
0	1	1	0	HR / Normal / Low-power mode (200 Hz)
0	1	1	1	HR / Normal / Low-power mode (400 Hz)
1	0	0	0	Low-power mode (1.620 kHz)
1	0	0	1	HR / Normal (1.344 kHz); Low-power mode (5.376 kHz)

## 8.7 CTRL\_REG2\_A (21h)

**Table 36. CTRL\_REG2 register**

HPM1	HPM0	HPCF2	HPCF1	FDS	HPCLICK	HPIS2	HPIS1
------	------	-------	-------	-----	---------	-------	-------

**Table 37. CTRL\_REG2 description**

HPM[1:0]	High-pass filter mode selection. Default value: 00 Refer to <a href="#">Table 38</a> for filter mode configuration
HPCF[2:1]	High-pass filter cutoff frequency selection
FDS	Filtered data selection. Default value: 0 (0: internal filter bypassed; 1: data from internal filter sent to output register and FIFO)
HPCLICK	Enables high-pass filter for CLICK function. (0: filter bypassed; 1: filter enabled)
HPIS2	Enables high-pass filter for AOI function on Interrupt 2. (0: filter bypassed; 1: filter enabled)
HPIS1	Enables high-pass filter for AOI function on Interrupt 1. (0: filter bypassed; 1: filter enabled)

**Table 38. High-pass filter mode configuration**

HPM1	HPM0	High-pass filter mode
0	0	Normal mode (reset by reading the <a href="#">REFERENCE/DATACAPTURE_A (26h)</a> register)
0	1	Reference signal for filtering
1	0	Normal mode
1	1	Autoreset on interrupt event

## 8.8 CTRL\_REG3\_A (22h)

**Table 39. CTRL\_REG3 register**

I1_CLICK	I1_AOI1	I1_AOI2	I1_DRDY1	I1_DRDY2	I1_WTM	I1_OVERRUN	--
----------	---------	---------	----------	----------	--------	------------	----

**Table 40. CTRL\_REG3 description**

I1_CLICK	CLICK interrupt on INT1 pin. Default value 0. (0: disable; 1: enable)
I1_AOI1	AOI1 interrupt on INT1 pin. Default value 0. (0: disable; 1: enable)
I1_AOI2	AOI2 interrupt on INT1 pin. Default value 0. (0: disable; 1: enable)
I1_DRDY1	DRDY1 interrupt on INT1 pin. Default value 0. (0: disable; 1: enable)



**Table 40. CTRL\_REG3 description (continued)**

I1_DRDY2	DRDY2 interrupt on INT1 pin. Default value 0. (0: disable; 1: enable)
I1_WTM	FIFO watermark interrupt on INT1 pin. Default value 0. (0: disable; 1: enable)
I1_OVERRUN	FIFO overrun interrupt on INT1 pin. Default value 0. (0: disable; 1: enable)

## 8.9 CTRL\_REG4\_A (23h)

**Table 41. CTRL\_REG4 register**

BDU	BLE <sup>(1)</sup>	FS1	FS0	HR	ST1	ST0	SPI_ENABLE
-----	--------------------	-----	-----	----	-----	-----	------------

1. The BLE function can be activated only in high-resolution mode

**Table 42. CTRL\_REG4 description**

BDU	Block data update. Default value: 0 (0: continuous update; 1: output registers not updated until MSB and LSB have been read)
BLE	Big/little endian data selection. Default value: 0 (0: data LSb at lower address; 1: data MSb at lower address) The BLE function can be activated only in high-resolution mode
FS[1:0]	Full-scale selection. Default value: 00 (00: $\pm 2 g$ ; 01: $\pm 4 g$ ; 10: $\pm 8 g$ ; 11: $\pm 16 g$ )
HR	Operating mode selection (refer to <a href="#">Section 4.2.1: Accelerometer power modes</a> )
ST[1:0]	Enables self-test. Default value: 00 (00: self-test disabled; other: see <a href="#">Table 43</a> )
SPI_ENABLE	Enables 3-wire SPI interface. Default: 0 (0: SPI 3-wire disabled; 1: SPI 3-wire enabled)

**Table 43. Self-test mode configuration**

ST1	ST0	Self-test mode
0	0	Normal mode
0	1	Self test 0
1	0	Self test 1
1	1	--

## 8.10 CTRL\_REG5\_A (24h)

**Table 44. CTRL\_REG5\_A register**

BOOT	FIFO_EN	--	--	LIR_INT1	D4D_INT1	LIR_INT2	D4D_INT2
------	---------	----	----	----------	----------	----------	----------

**Table 45. CTRL\_REG5\_A description**

BOOT	Reboot accelerometer memory content. Default value: 0 (0: normal mode; 1: reboot memory content)
FIFO_EN	Enables FIFO. Default value: 0 (0: FIFO disabled; 1: FIFO enabled)
LIR_INT1	Latch interrupt request on <i>INT1_SRC_A (31h)</i> , with <i>INT1_SRC_A (31h)</i> register cleared by reading <i>INT1_SRC_A (31h)</i> itself. Default value: 0. (0: interrupt request not latched; 1: interrupt request latched)
D4D_INT1	Enables 4D: 4D detection is enabled on INT1 pin when 6D bit on <i>INT1_CFG_A (30h)</i> is set to 1.
LIR_INT2	Latch interrupt request on <i>INT2_SRC_A (35h)</i> register, with <i>INT2_SRC_A (35h)</i> register cleared by reading <i>INT2_SRC_A (35h)</i> itself. Default value: 0. (0: interrupt request not latched; 1: interrupt request latched)
D4D_INT2	Enables 4D: 4D detection is enabled on INT2 pin when 6D bit on <i>INT2_CFG_A (34h)</i> is set to 1.

## 8.11 CTRL\_REG6\_A (25h)

**Table 46. CTRL\_REG6\_A register**

I2_CLICKen	I2_INT1	I2_INT2	BOOT_I2	P2_ACT	--	H_LACTIVE	-
------------	---------	---------	---------	--------	----	-----------	---

**Table 47. CTRL\_REG6\_A description**

I2_CLICKen	Click interrupt on INT2 pin. Default value: 0 (0: disabled; 1: enabled)
I2_INT1	Enables interrupt 1 function on INT2 pin. Default value: 0 (0: function disabled; 1: function enabled)
I2_INT2	Enables interrupt 2 function on INT2 pin. Default value: 0 (0: function disabled; 1: function enabled)
BOOT_I2	Enables boot on INT2 pin. Default value: 0 (0: disabled; 1: enabled)
P2_ACT	Enables activity interrupt on INT2 pin. Default value: 0. (0: disabled; 1: enabled)
H_LACTIVE	interrupt active. Default value: 0. (0: interrupt active-high; 1: interrupt active-low)

## 8.12 REFERENCE/DATACAPTURE\_A (26h)

**Table 48. REFERENCE/DATACAPTURE\_A register**

Ref7	Ref6	Ref5	Ref4	Ref3	Ref2	Ref1	Ref0
------	------	------	------	------	------	------	------

**Table 49. REFERENCE/DATACAPTURE\_A description**

Ref [7:0]	Reference value for interrupt generation. Default value: 0
-----------	--

## 8.13 STATUS\_REG\_A (27h)

**Table 50. STATUS\_REG\_A register**

ZYXOR	ZOR	YOR	XOR	ZYXDA	ZDA	YDA	XDA
-------	-----	-----	-----	-------	-----	-----	-----

**Table 51. STATUS\_REG\_A description**

ZYXOR	X-, Y-, and Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new set of data has overwritten the previous set)
ZOR	Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Z-axis has overwritten the previous data)
YOR	Y-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Y-axis has overwritten the previous data)
XOR	X-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the X-axis has overwritten the previous data)
ZYXDA	X-, Y- and Z-axis new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)
ZDA	Z-axis new data available. Default value: 0 (0: new data for the Z-axis is not yet available; 1: new data for the Z-axis is available)
YDA	Y-axis new data available. Default value: 0 (0: new data for the Y-axis is not yet available; 1: new data for the Y-axis is available)

**8.14 OUT\_X\_L\_A (28h), OUT\_X\_H\_A (29h)**

X-axis acceleration data. The value is expressed as two's complement left-justified. Please refer to [Section 4.2.1: Accelerometer power modes](#).

**8.15 OUT\_Y\_L\_A (2Ah), OUT\_Y\_H\_A (2Bh)**

Y-axis acceleration data. The value is expressed as two's complement left-justified. Please refer to [Section 4.2.1: Accelerometer power modes](#).

**8.16 OUT\_Z\_L\_A (2Ch), OUT\_Z\_H\_A (2Dh)**

Z-axis acceleration data. The value is expressed as two's complement left-justified. Please refer to [Section 4.2.1: Accelerometer power modes](#).

**8.17 FIFO\_CTRL\_REG\_A (2Eh)****Table 52. FIFO\_CTRL\_REG\_A register**

FM1	FM0	TR	FTH4	FTH3	FTH2	FTH1	FTH0
-----	-----	----	------	------	------	------	------

**Table 53. FIFO\_CTRL\_REG\_A description**

FM[1:0]	FIFO mode selection. Default value: 00 (see <a href="#">Table 54</a> )
TR	Trigger selection. Default value: 0 (0: trigger event allows triggering signal on INT1 1: trigger event allows triggering signal on INT2)
FTH[4:0]	Default value: 00000

**Table 54. FIFO mode configuration**

FM1	FM0	FIFO mode
0	0	Bypass mode
0	1	FIFO mode
1	0	Stream mode
1	1	Stream-to-FIFO mode

## 8.18 FIFO\_SRC\_REG\_A (2Fh)

**Table 55. FIFO\_SRC\_REG\_A register**

WTM	OVRN_FIFO	EMPTY	FSS4	FSS3	FSS2	FSS1	FSS0
-----	-----------	-------	------	------	------	------	------

**Table 56. FIFO\_SRC\_REG\_A description**

WTM	WTM bit is set high when FIFO content exceeds watermark level.
OVRN_FIFO	OVRN bit is set high when FIFO buffer is full; this means that the FIFO buffer contains 32 unread samples. At the following ODR a new sample set replaces the oldest FIFO value. The OVRN bit is set to 0 when the first sample set has been read.
EMPTY	EMPTY flag is set high when all FIFO samples have been read and FIFO is empty.
FSS [4:0]	FSS [4:0] field always contains the current number of unread samples stored in the FIFO buffer. When FIFO is enabled, this value increases at ODR frequency until the buffer is full, whereas, it decreases every time one sample set is retrieved from FIFO.

## 8.19 INT1\_CFG\_A (30h)

**Table 57. INT1\_CFG\_A register**

AOI	6D	ZHIE/ ZUPE	ZLIE/ ZDOWNE	YHIE/ YUPE	YLIE/ YDOWNE	XHIE/ XUPE	XLIE/ XDOWNE
-----	----	---------------	-----------------	---------------	-----------------	---------------	-----------------

**Table 58. INT1\_CFG\_A description**

AOI	And/Or combination of interrupt events. Default value: 0. Refer to <a href="#">Table 59</a> .
6D	6-direction detection function enabled. Default value: 0. Refer to <a href="#">Table 59</a> .
ZHIE/ ZUPE	Enables interrupt generation on Z high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)
ZLIE/ ZDOWNE	Enables interrupt generation on Z low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)
YHIE/ YUPE	Enables interrupt generation on Y high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)
YLIE/ YDOWNE	Enables interrupt generation on Y low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)
XHIE/ XUPE	Enables interrupt generation on X high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)
XLIE/ XDOWNE	Enables interrupt generation on X low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)

The content of this register is loaded at boot.

A write operation to this address is possible only after system boot.

Table 59. Interrupt mode

AOI	6D	Interrupt mode
0	0	OR combination of interrupt events
0	1	6-direction movement recognition
1	0	AND combination of interrupt events
1	1	6-direction position recognition

The difference between AOI-6D = 01 and AOI-6D = 1.

AOI-6D = 01 is movement recognition. An interrupt is generated when the orientation moves from an unknown zone to a known zone. The interrupt signal remains for a duration ODR.

AOI-6D = 11 is direction recognition. An interrupt is generated when the orientation is inside a known zone. The interrupt signal remains while the orientation is inside the zone.

## 8.20 INT1\_SRC\_A (31h)

Table 60. INT1\_SRC\_A register

0	IA	ZH	ZL	YH	YL	XH	XL
---	----	----	----	----	----	----	----

Table 61. INT1\_SRC\_A description

IA	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH	Z high. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
ZL	Z low. Default value: 0 (0: no interrupt; 1: Z low event has occurred)
YH	Y high. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
YL	Y low. Default value: 0 (0: no interrupt, 1: Y low event has occurred)
XH	X high. Default value: 0 (0: no interrupt, 1: X high event has occurred)
XL	X low. Default value: 0 (0: no interrupt, 1: X low event has occurred)

Interrupt 1 source register. Read-only register.

Reading at this address clears the *INT1\_SRC\_A (31h)* IA bit (and the interrupt signal on the INT1 pin) and allows the refresh of data in the *INT1\_SRC\_A (31h)* register if the latched option was chosen.

## 8.21 INT1\_THS\_A (32h)

**Table 62. INT1\_THS\_A register**

0	THS6	THS5	THS4	THS3	THS2	THS1	THS0
---	------	------	------	------	------	------	------

**Table 63. INT1\_THS\_A description**

THS[6:0]	Interrupt 1 threshold. Default value: 000 0000 1 LSb = 16 mg @ FS = ±2 g 1 LSb = 32 mg @ FS = ±4 g 1 LSb = 62 mg @ FS = ±8 g 1 LSb = 186 mg @ FS = ±16 g
----------	--

## 8.22 INT1\_DURATION\_A (33h)

**Table 64. INT1\_DURATION\_A register**

0	D6	D5	D4	D3	D2	D1	D0
---	----	----	----	----	----	----	----

**Table 65. INT1\_DURATION\_A description**

D[6:0]	Duration value. Default value: 000 0000 1 LSb = 1/ODR
--------	--

The **D[6:0]** bits set the minimum duration of the interrupt 2 event to be recognized. Duration steps and maximum values depend on the ODR chosen.

Duration time is measured in N/ODR, where N is the content of the duration register.

## 8.23 INT2\_CFG\_A (34h)

**Table 66. INT2\_CFG\_A register**

AOI	6D	ZHIE	ZLIE	YHIE	YLIE	XHIE	XLIE
-----	----	------	------	------	------	------	------

**Table 67. INT2\_CFG\_A description**

AOI	AND/OR combination of interrupt events. Default value: 0 (see <a href="#">Table 68</a> )
6D	6-direction detection function enabled. Default value: 0. Refer to <a href="#">Table 68</a> .
ZHIE	Enables interrupt generation on Z high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)

**Table 67. INT2\_CFG\_A description (continued)**

ZLIE	Enables interrupt generation on Z low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value lower than preset threshold)
YHIE	Enables interrupt generation on Y high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
YLIE	Enables interrupt generation on Y low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value lower than preset threshold)
XHIE	Enables interrupt generation on X high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
XLIE	Enables interrupt generation on X low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value lower than preset threshold)

The content of this register is loaded at boot.

A write operation to this address is possible only after system boot.

**Table 68. Interrupt mode**

AOI	6D	Interrupt mode
0	0	OR combination of interrupt events
0	1	6-direction movement recognition
1	0	AND combination of interrupt events
1	1	6-direction position recognition

The difference between AOI-6D = 01 and AOI-6D = 11.

AOI-6D = 01 is movement recognition. An interrupt is generated when the orientation moves from an unknown zone to a known zone. The interrupt signal remains for a duration ODR.

AOI-6D = 11 is direction recognition. An interrupt is generated when the orientation is inside a known zone. The interrupt signal remains while the orientation is inside the zone.



## 8.24 INT2\_SRC\_A (35h)

**Table 69. INT2\_SRC\_A register**

0	IA	ZH	ZL	YH	YL	XH	XL
---	----	----	----	----	----	----	----

**Table 70. INT2\_SRC\_A description**

IA	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH	Z high. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
ZL	Z low. Default value: 0 (0: no interrupt; 1: Z low event has occurred)
YH	Y high. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
YL	Y low. Default value: 0 (0: no interrupt, 1: Y low event has occurred)
XH	X high. Default value: 0 (0: no interrupt, 1: X high event has occurred)
XL	X low. Default value: 0 (0: no interrupt, 1: X low event has occurred)

Interrupt 2 source register. Read-only register.

Reading at this address clears the *INT2\_SRC\_A (35h)* IA bit (and the interrupt signal on the INT2 pin) and allows the refresh of data in the *INT2\_SRC\_A (35h)* register if the latched option was chosen.

## 8.25 INT2\_THS\_A (36h)

**Table 71. INT2\_THS\_A register**

0	THS6	THS5	THS4	THS3	THS2	THS1	THS0
---	------	------	------	------	------	------	------

**Table 72. INT2\_THS\_A description**

THS[6:0]	Interrupt 2 threshold. Default value: 000 0000 1 LSb = 16 mg @ FS = $\pm 2$ g 1 LSb = 32 mg @ FS = $\pm 4$ g 1 LSb = 62 mg @ FS = $\pm 8$ g 1 LSb = 186 mg @ FS = $\pm 16$ g
----------	--

## 8.26 INT2\_DURATION\_A (37h)

**Table 73. INT2\_DURATION\_A register**

0	D6	D5	D4	D3	D2	D1	D0
---	----	----	----	----	----	----	----

**Table 74. INT2\_DURATION\_A description**

D[6:0]	Duration value. Default value: 000 0000 1 LSb = 1/ODR <sup>(1)</sup>
--------	---

1. Duration time is measured in N/ODR, where N is the content of the duration register.

The **D[6:0]** bits set the minimum duration of the Interrupt 2 event to be recognized. Duration time steps and maximum values depend on the ODR chosen.

## 8.27 CLICK\_CFG\_A (38h)

**Table 75. CLICK\_CFG\_A register**

--	--	ZD	ZS	YD	YS	XD	XS
----	----	----	----	----	----	----	----

**Table 76. CLICK\_CFG\_A description**

ZD	Enables interrupt double-click on Z-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
ZS	Enables interrupt single-click on Z-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
YD	Enables interrupt double-click on Y-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
YS	Enables interrupt single-click on Y-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
XD	Enables interrupt double-click on X-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
XS	Enables interrupt single-click on X-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)

### 8.28 CLICK\_SRC\_A (39h)

**Table 77. CLICK\_SRC\_A register**

	IA	DClick	SClick	Sign	Z	Y	X
--	----	--------	--------	------	---	---	---

**Table 78. CLICK\_SRC\_A description**

IA	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
DClick	Enables double-click. Default value: 0 (0: double-click detection disabled, 1: double-click detection enabled)
SClick	Enables single-click. Default value: 0 (0: single-click detection disabled, 1: single-click detection enabled)
Sign	Click sign. (0: positive detection, 1: negative detection)
Z	Z click detection. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
Y	Y click detection. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
X	X click detection. Default value: 0 (0: no interrupt, 1: X high event has occurred)

### 8.29 CLICK\_THS\_A (3Ah)

**Table 79. CLICK\_THS\_A register**

-	Ths6	Ths5	Ths4	Ths3	Ths2	Ths1	Ths0
---	------	------	------	------	------	------	------

**Table 80. CLICK\_SRC\_A description**

Ths[6:0]	Click threshold. Default value: 000 0000
----------	--

### 8.30 TIME\_LIMIT\_A (3Bh)

**Table 81. TIME\_LIMIT\_A register**

-	TLI6	TLI5	TLI4	TLI3	TLI2	TLI1	TLI0
---	------	------	------	------	------	------	------

**Table 82. TIME\_LIMIT\_A description**

TLI[6:0]	Click time limit. Default value: 000 0000
----------	---

### 8.31 TIME\_LATENCY\_A (3Ch)

Table 83. TIME\_LATENCY\_A register

TLA7	TLA6	TLA5	TLA4	TLA3	TLA2	TLA1	TLA0
------	------	------	------	------	------	------	------

Table 84. TIME\_LATENCY\_A description

TLA[7:0]	Click time latency. Default value: 0000 0000
----------	--

### 8.32 TIME\_WINDOW\_A (3Dh)

Table 85. TIME\_WINDOW\_A register

TW7	TW6	TW5	TW4	TW3	TW2	TW1	TW0
-----	-----	-----	-----	-----	-----	-----	-----

Table 86. TIME\_WINDOW\_A description

TW[7:0]	Click time window
---------	-------------------

### 8.33 Act\_THS\_A (3Eh)

Table 87. Act\_THS\_A register

--	Acth6	Acth5	Acth4	Acth3	Acth2	Acth1	Acth0
----	-------	-------	-------	-------	-------	-------	-------

Table 88. Act\_THS\_A description

Acth[6:0]	<p>Sleep-to-wake, return-to-sleep activation threshold in low-power mode</p> <p>1 LSb = 16 mg @ FS = <math>\pm 2</math> g</p> <p>1 LSb = 32 mg @ FS = <math>\pm 4</math> g</p> <p>1 LSb = 62 mg @ FS = <math>\pm 8</math> g</p> <p>1 LSb = 186 mg @ FS = <math>\pm 16</math> g</p>
-----------	--

### 8.34 Act\_DUR\_A (3Fh)

Table 89. Act\_DUR\_A register

ActD7	ActD6	ActD5	ActD4	ActD3	ActD2	ActD1	ActD0
-------	-------	-------	-------	-------	-------	-------	-------

Table 90. Act\_DUR\_A description

ActD[7:0]	<p>Sleep-to-wake, return-to-sleep duration</p> <p>1 LSb = <math>(8 \times 1[\text{LSb}] + 1) / \text{ODR}</math></p>
-----------	--

**8.35 OFFSET\_X\_REG\_L\_M (45h) and OFFSET\_X\_REG\_H\_M (46h)**

These registers comprise a 16-bit register and represent X hard-iron offset in order to compensate environmental effects (data in two's complement). These values act on the magnetic output data value in order to delete the environmental offset.

**8.36 OFFSET\_Y\_REG\_L\_M (47h) and OFFSET\_Y\_REG\_H\_M (48h)**

These registers comprise a 16-bit register and represent Y hard-iron offset in order to compensate environmental effects (data in two's complement). These values act on the magnetic output data value in order to delete the environmental offset.

**8.37 OFFSET\_Z\_REG\_L\_M (49h) and OFFSET\_Z\_REG\_H\_M (4Ah)**

These registers comprise a 16-bit register and represent Z hard-iron offset in order to compensate environmental effects (data in two's complement). These values act on the magnetic output data value in order to delete the environmental offset.

**8.38 WHO\_AM\_I\_M (4Fh)**

The identification register is used to identify the device (read-only register).

0	1	0	0	0	0	0	0
---	---	---	---	---	---	---	---

**8.39 CFG\_REG\_A\_M (60h)**

The configuration register is used to configure the output data rate and the measurement configuration.

**Table 91. CFG\_REG\_A\_M register**

COMP_TEMP_EN	REBOOT	SOFT_RST	LP	ODR1	ODR0	MD1	MD0
--------------	--------	----------	----	------	------	-----	-----

**Table 92. CFG\_REG\_A\_M register description**

COMP_TEMP_EN <sup>(1)</sup>	Enables the magnetometer temperature compensation. Default value: 0 (0: temperature compensation disabled; 1: temperature compensation enabled)
REBOOT	Reboots magnetometer memory content. Default value: 0 (0: normal mode; 1: reboot memory content)
SOFT_RST	When this bit is set, the configuration registers and user registers are reset. Flash registers keep their values.
LP	Enables ow-power mode. Default: 0 (0: high-resolution mode 1: low-power mode enabled)
ODR[1:0]	Output data rate configuration (see <a href="#">Table 93: Output data rate configuration</a> )
MD[1:0]	Mode select bit. These bits select the mode of operation of the device (see <a href="#">Table 94: System mode</a> )

1. For proper operation, this bit must be set to 1.

Table 93. Output data rate configuration

ODR1	ODR0	ODR (Hz)
0	0	10 (default)
0	1	20
1	0	50
1	1	100

Table 94. System mode

MD1	MD0	Mode
0	0	Continuous mode. In continuous mode the device continuously performs measurements and places the result in the data register. The data-ready signal is generated when a new data set is ready to be read. This signal can be available on the external pin by setting the INT_MAG bit in <a href="#">CFG_REG_C_M (62h)</a> .
0	1	Single mode. When single mode is selected, the device performs a single measurement, sets DRDY high and returns to idle mode. Mode register return to idle mode bit values.
1	0	Idle mode. Device is placed in idle mode. I <sup>2</sup> C and SPI active.
1	1	Idle mode. Device is placed in idle mode. I <sup>2</sup> C and SPI active.

### 8.40 CFG\_REG\_B\_M (61h)

**Table 95. CFG\_REG\_B\_M register**

0	0	0	OFF_CANC_ONE_SHOT	INT_on_DataOFF	Set_FREQ	OFF_CANC	LPF
---	---	---	-------------------	----------------	----------	----------	-----

**Table 96. CFG\_REG\_B\_M register description**

OFF_CANC_ONE_SHOT	Enables offset cancellation in single measurement mode. The OFF_CANC bit must be set to 1 when enabling offset cancellation in single measurement mode. (0: offset cancellation in single measurement mode disabled; 1: offset cancellation in single measurement mode enabled)
INT_on_DataOFF	If 1, the interrupt block recognition checks data after the hard-iron correction to discover the interrupt.
Set_FREQ	Selects the frequency of the set pulse. (0: set pulse is released every 63 ODR; 1: set pulse is released only at power-on after PD condition)
OFF_CANC	Enables offset cancellation. (0: offset cancellation disabled; 1: offset cancellation enabled)
LPF	Enables low-pass filter (see <a href="#">Table 97</a> ) (0: digital filter disabled; 1: digital filter enabled)

**Table 97. Digital low-pass filter**

CFG_REG_B[LPF]	BW [Hz]
0 (disable)	ODR/2
1 (enable)	ODR/4

## 8.41 CFG\_REG\_C\_M (62h)

**Table 98. CFG\_REG\_C\_M register**

0	INT_MAG_PIN	I2C_DIS	BDU	BLE	0 <sup>(1)</sup>	Self_test	INT_MAG
---	-------------	---------	-----	-----	------------------	-----------	---------

1. This bit must be set to 0 for the correct operation of the device.

**Table 99. CFG\_REG\_C\_M register description**

INT_MAG_PIN	If 1, the INTERRUPT signal (INT bit inside <i>INT_SOURCE_REG_M (64h)</i> ) is driven on INT_MAG_PIN
I2C_DIS	If 1, the I <sup>2</sup> C interface is inhibited. Only the SPI interface can be used.
BDU	If enabled, reading of incorrect data is avoided when the user reads asynchronously. In fact if the read request arrives during an update of the output data, a latch is possible, reading incoherent high and low parts of the same register. Only one part is updated and the other one remains old.
BLE	If 1, an inversion of the low and high parts of the data occurs.
Self_test	If 1, the self-test is enabled.
INT_MAG	If 1, the DRDY pin is configured as a digital output.

## 8.42 INT\_CTRL\_REG\_M (63h)

The interrupt control register is used to enable and to configure the interrupt recognition.

**Table 100. INT\_CTRL\_REG\_M register**

XIEN	YIEN	ZIEN	0 <sup>(1)</sup>	0 <sup>(1)</sup>	IEA	IEL	IEN
------	------	------	------------------	------------------	-----	-----	-----

1. This bit must be set to 0 for the correct operation of the device.

**Table 101. INT\_CTRL\_REG\_M register description**

XIEN	Enables the interrupt recognition for the X-axis. Default: 0 (1: enabled; 0: disabled)
YIEN	Enables the interrupt recognition for the Y-axis. Default: 0 (1: enabled; 0: disabled)
ZIEN	Enables the interrupt recognition for the Z-axis. Default: 0 (1: enabled; 0: disabled)
IEA	Controls the polarity of the INT bit ( <i>INT_SOURCE_REG_M (64h)</i> ) when an interrupt occurs. Default: 0 If IEA = 0, then INT = 0 signals an interrupt. If IEA = 1, then INT = 1 signals an interrupt.
IEL	Controls whether the INT bit ( <i>INT_SOURCE_REG_M (64h)</i> ) is latched or pulsed. Default: 0 If IEL = 0, then INT is pulsed. If IEL = 1, then INT is latched. Once latched, INT remains in the same state until <i>INT_SOURCE_REG_M (64h)</i> is read.
IEN	Enables the interrupt. When set, enables the interrupt generation. The INT bit is in <i>INT_SOURCE_REG_M (64h)</i> . Default: 0



### 8.43 INT\_SOURCE\_REG\_M (64h)

When interrupt latched is selected, reading this register resets all the bits in this register.

**Table 102. INT\_SOURCE\_REG\_M register**

P_TH_S_X	P_TH_S_Y	P_TH_S_Z	N_TH_S_X	N_TH_S_Y	N_TH_S_Z	MROI	INT
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**Table 103. INT\_SOURCE\_REG\_M register description**

P_TH_S_X	X-axis value exceeds the threshold positive side
P_TH_S_Y	Y-axis value exceeds the threshold positive side
P_TH_S_Z	Z-axis value exceeds the threshold positive side
N_TH_S_X	X-axis value exceeds the threshold negative side
N_TH_S_Y	Y-axis value exceeds the threshold negative side
N_TH_S_Z	Z-axis value exceeds the threshold negative side
MROI	MROI flag generation is always enabled. This flag is reset by reading <a href="#">INT_SOURCE_REG_M (64h)</a> .
INT	This bit signals when the interrupt event occurs.

### 8.44 INT\_THS\_L\_REG\_M (65h)

This register contains the least significant bits of the threshold value chosen for the interrupt.

**Table 104. INT\_THS\_L\_REG\_M register**

TH7	TH6	TH5	TH4	TH3	TH2	TH1	TH0
-----	-----	-----	-----	-----	-----	-----	-----

**Table 105. INT\_THS\_L\_REG\_M register description**

TH[7:0]	Threshold value for the interrupt.
---------	------------------------------------

### 8.45 INT\_THS\_H\_REG\_M (66h)

This register contains the most significant bits of the threshold value chosen for the interrupt.

**Table 106. INT\_THS\_H\_REG\_M register**

TH15	TH14	TH13	TH12	TH11	TH10	TH9	TH8
------	------	------	------	------	------	-----	-----

**Table 107. INT\_THS\_H\_REG\_M register description**

TH[15:8]	Threshold value for the interrupt
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These registers set the threshold value for the output to generate the interrupt (INT bit in [INT\\_SOURCE\\_REG\\_M \(64h\)](#)). This threshold is common to all three (axes) output values and is unsigned unipolar. The threshold value is correlated to the current gain and it is unsigned because the threshold is considered as an absolute value, but crossing the threshold is detected for both positive and negative sides.

### 8.46 STATUS\_REG\_M (67h)

The status register is an 8-bit read-only register. This register is used to indicate device status. SR0 through SR7 indicate bit locations, with SR denoting the bits that are in the status register. SR7 denotes the first bit of the data stream.

**Table 108. STATUS\_REG\_M register**

Zyxor	zor	yor	xor	Zyxda	zda	yda	xda
-------	-----	-----	-----	-------	-----	-----	-----

**Table 109. STATUS\_REG\_M register description**

Zyxor	X-, Y-, and Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new set of data has overwritten the previous set).
zor	Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Z-axis has overwritten the previous data).
yor	Y-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Y-axis has overwritten the previous data).
xor	X-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the X-axis has overwritten the previous data).
Zyxda	X-, Y- and Z-axis new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available).
zda	Z-axis new data available. Default value: 0 (0: a new data for the Z-axis is not yet available; 1: a new data for the Z-axis is available)
yda	Y-axis new data available. Default value: 0 (0: a new data for the Y-axis is not yet available; 1: a new data for the Y-axis is available)
xda	X-axis new data available. Default value: 0 (0: a new data for the X-axis is not yet available; 1: a new data for the X-axis is available)

### 8.47 OUTX\_L\_REG\_M, OUTX\_H\_REG\_M (68h - 69h)

The data output X registers are two 8-bit registers, data output ch1 MSB register (69h) and output X LSB register (68h).

The output data represents the raw magnetic data only if OFFSET\_X\_REG is equal to zero, otherwise hard-iron calibration is included.

**Table 110. OUTX\_L\_REG\_M register**

0	0	0	0	0	0	0	0
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**Table 111. OUTX\_H\_REG\_M register**

0	0	0	0	0	0	0	0
---	---	---	---	---	---	---	---

The value of the magnetic field is expressed in two's complement. This register contains the X component of the magnetic data.

### 8.48 OUTY\_L\_REG\_M, OUTY\_H\_REG\_M (6Ah - 6Bh)

The data output Y registers are two 8-bit registers, data output ch1 MSB register (6Bh) and output Y LSB register (6Ah).

The output data represents the raw magnetic data only if OFFSET\_Y\_REG is equal to zero, otherwise hard-iron calibration is included.

**Table 112. OUTY\_L\_REG\_M register**

0	0	0	0	0	0	0	0
---	---	---	---	---	---	---	---

**Table 113. OUTY\_H\_REG\_M register**

0	0	0	0	0	0	0	0
---	---	---	---	---	---	---	---

The value of the magnetic field is expressed in two's complement. This register contains the Y component of the magnetic data.

### 8.49 OUTZ\_L\_REG\_M, OUTZ\_H\_REG\_M (6Ch - 6Dh)

The data output Z registers are two 8-bit registers, data output ch1 MSB register (6Dh) and output Z LSB register (6Ch).

The output data represents the raw magnetic data only if OFFSET\_Z\_REG is equal to zero, otherwise hard-iron calibration is included.

**Table 114. OUTZ\_L\_REG\_M register**

0	0	0	0	0	0	0	0
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**Table 115. OUTZ\_H\_REG\_M register**

0	0	0	0	0	0	0	0
---	---	---	---	---	---	---	---

The value of the magnetic field is expressed in two's complement. This register contains the Z component of the magnetic data.

## 9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 9.1 LGA-12L package information

Figure 17. LGA-12L 2 x 2 x 1 mm package outline and mechanical data

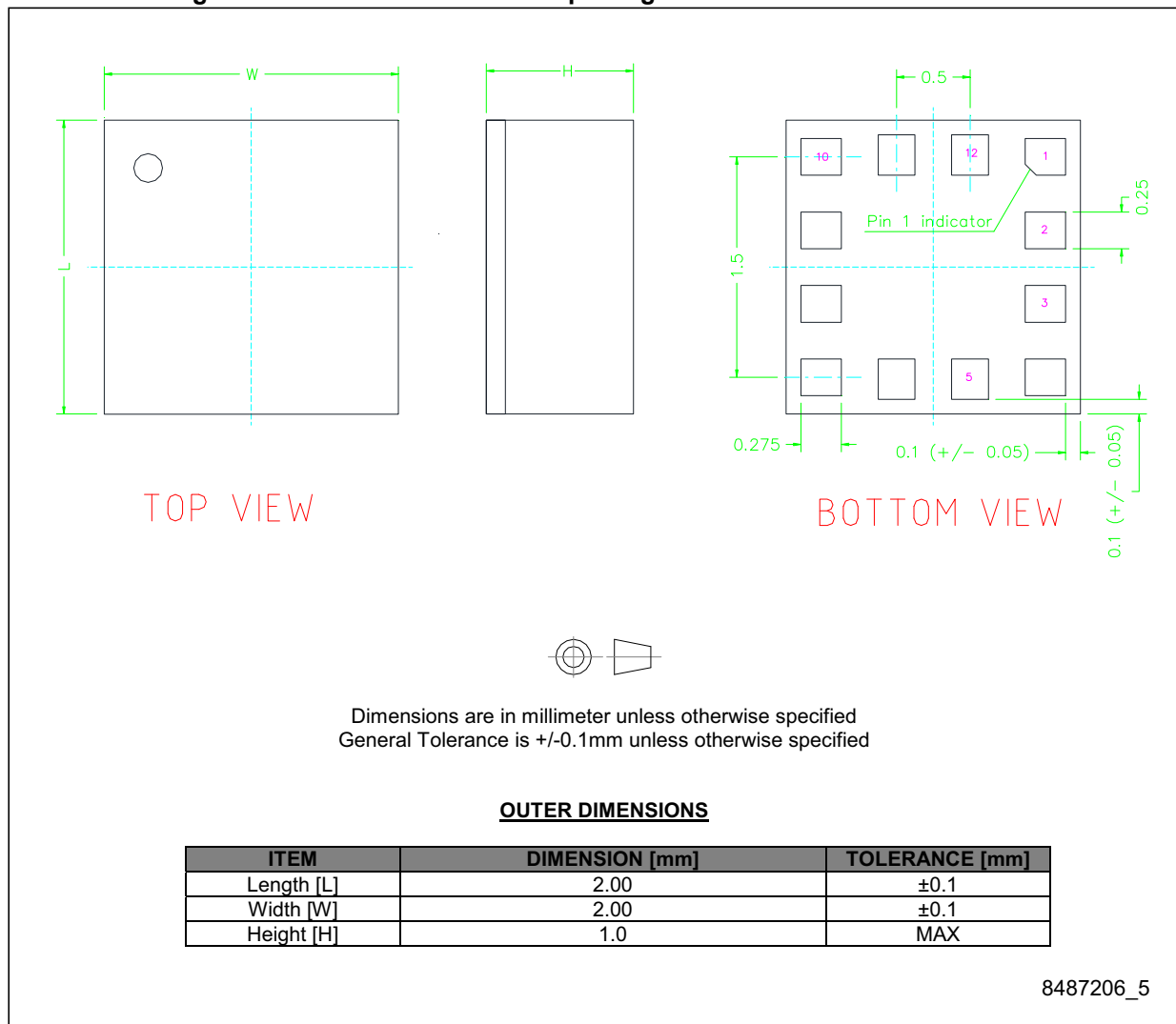




Figure 20. Reel information for carrier tape of LGA-12L package

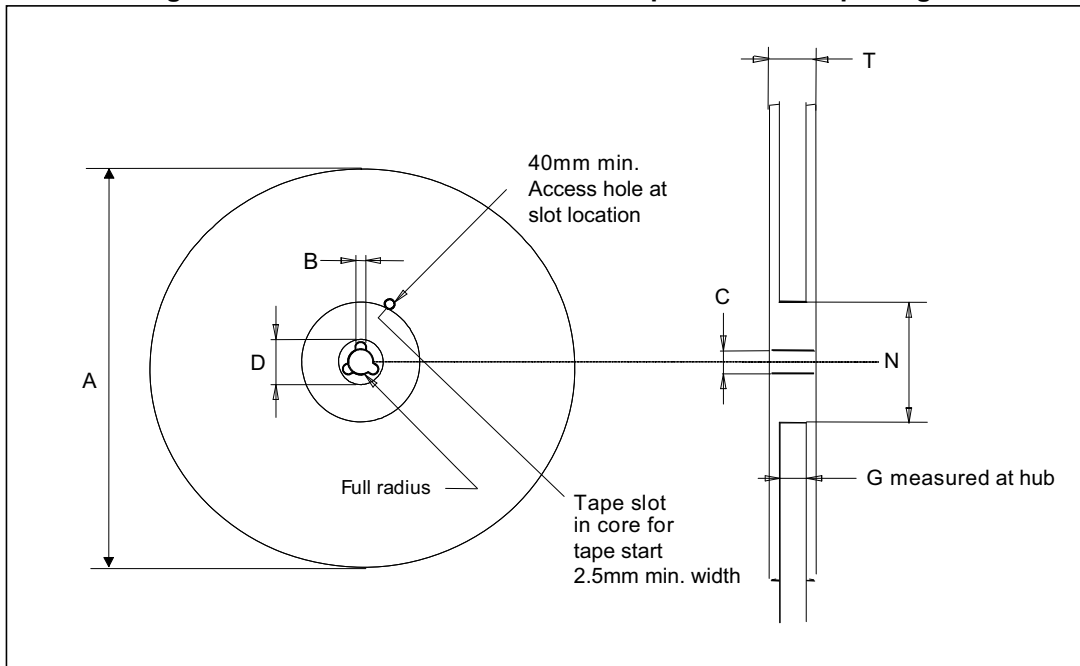


Table 116. Reel dimensions for carrier tape of LGA-12L package

Reel dimensions (mm)	
A (max)	330
B (min)	1.5
C	13 ±0.25
D (min)	20.2
N (min)	60
G	12.4 +2/-0
T (max)	18.4

## 10 Revision history

**Table 117. Document revision history**

Date	Revision	Changes
14-Mar-2016	6	Document status promoted to production data Updated <i>Features</i> Updated <i>Table 3: Sensor characteristics</i> Updated Idd_PD in <i>Table 5: Electrical characteristics</i> Updated maximum values for A <sub>POW</sub> and A <sub>UNP</sub> in <i>Table 9: Absolute maximum ratings</i> Updated <i>Section 4.1.1: Magnetometer power modes</i> Updated <i>Figure 6: Magnetometer self-test procedure</i> Updated <i>Table 16: Current consumption of operating modes</i> Updated description of BOOT bit in <i>Table 45: CTRL_REG5_A description</i> Updated <i>CFG_REG_A_M (60h)</i> Updated description of OFF_CANCEL bit in <i>Table 96: CFG_REG_B_M register description</i>
11-Apr-2016	7	Updated LA_Idd_NM in <i>Table 5: Electrical characteristics</i> Updated <i>Figure 7: Accelerometer self-test procedure</i> Added <i>Section 5.3: Startup sequence</i>
09-Aug-2016	8	Added <i>Section 9.2: LGA-12 packing information</i>
09-Sep-2016	9	Updated <i>Section 4.1.2: Magnetometer offset cancellation</i> and added OFF_CANCEL_ONE_SHOT bit to <i>CFG_REG_B_M (61h)</i>
28-Nov-2018	10	Updated <i>Table 5: Electrical characteristics</i>
29-Aug-2022	11	Updated Notes below <i>Figure 3: SPI slave timing diagram</i> and <i>Figure 4: I<sup>2</sup>C slave timing diagram</i> Updated <i>Figure 17: LGA-12L 2 x 2 x 1 mm package outline and mechanical data</i> Minor textual updates

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