STY145N65M5

N-channel 650 V, 0.012 Ω typ., 138 A MDmesh™ M5 Power MOSFET in a Max247 package

Datasheet - production data

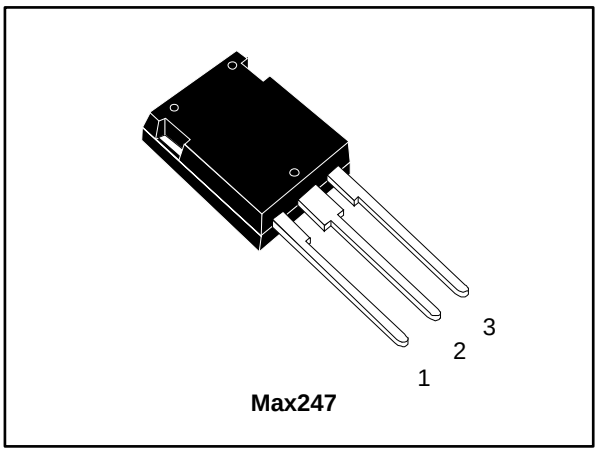
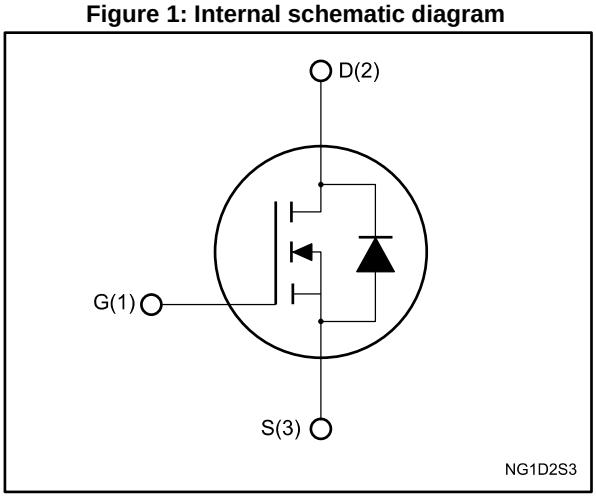


Figure 1: Internal schematic diagram



Features

Order code	V_{DS} @ T_{Jmax}	$R_{DS(on)}$ max.	I_D
STY145N65M5	710 V	0.015 Ω	138 A

- Extremely low $R_{DS(on)}$
- Low gate charge and input capacitance
- Excellent switching performance
- 100% avalanche tested

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET based on the MDmesh™ M5 innovative vertical process technology combined with the well-known PowerMESH™ horizontal layout. The resulting product offers extremely low on-resistance, making it particularly suitable for applications requiring high power and superior efficiency.

Table 1: Device summary

Order code	Marking	Package	Packaging
STY145N65M5	145N65M5	Max247	Tube

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at T_C = 25 °C	138	A
I_D	Drain current (continuous) at T_C = 100 °C	87	A
I_{DM} (1)	Drain current (pulsed)	552	A
P_{TOT}	Total dissipation at T_C = 25 °C	625	W
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	12	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	2420	mJ
dv/dt (2)	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Max. operating junction temperature	150	

Notes:

(1)Pulse width limited by safe operating area.

(2)I_{SD} ≤ 138 A, di/dt ≤ 400 A/µs; $V_{DS(peak)}$ < $V_{(BR)DSS}$, V_{DD} = 400 V.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	0.2	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	30	°C/W

2 Electrical characteristics

T_C = 25 °C unless otherwise specified

Table 4: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V			10	µA
		V_{GS} = 0 V, V_{DS} = 650 V, T_C = 125 °C			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 69 A		0.012	0.015	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS}= 100 V, f = 1 MHz, V_{GS} = 0 V	-	18500	-	pF
C_{oss}	Output capacitance		-	413	-	pF
C_{rss}	Reverse transfer capacitance		-	11	-	pF
$C_{o(er)}$ (1)	Equivalent output capacitance energy related	V_{GS} = 0, V_{DS} = 0 to 520 V	-	415	-	pF
$C_{o(tr)}$ (2)	Equivalent output capacitance time related		-	1950	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, open drain	-	0.7	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 69 A, V_{GS} = 10 V (see *Figure 15: "Test circuit for gate charge behavior"*)	-	414	-	nC
Q_{gs}	Gate-source charge		-	114	-	nC
Q_{gd}	Gate-drain charge		-	164	-	nC

Notes:

(1) $C_{o(er)}$ is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

(2) $C_{o(tr)}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(V)}$	Voltage delay time	V_{DD} = 400 V, I_D = 85 A R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 16: "Test circuit for inductive load switching and diode recovery times"* and *Figure 19: "Switching time waveform"*)	-	255	-	ns
$t_{r(V)}$	Voltage rise time		-	11	-	ns
$t_{f(i)}$	Current fall time		-	82	-	ns
$t_{C(off)}$	Crossing time		-	88	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		138	A
I_{SDM}, (1)	Source-drain current (pulsed)		-		552	A
V_{SD} (2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 138 A	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 138 A, di/dt = 100 A/µs, V_{DD} = 100 V (see *Figure 16: "Test circuit for inductive load switching and diode recovery times"*)	-	568		ns
Q_{rr}	Reverse recovery charge		-	14.5		µC
I_{RRM}	Reverse recovery current		-	51		A
t_{rr}	Reverse recovery time	I_{SD} = 138 A, di/dt = 100 A/µs, V_{DD} = 100 V, T_j = 150 °C (see *Figure 16: "Test circuit for inductive load switching and diode recovery times"*)	-	728		ns
Q_{rr}	Reverse recovery charge		-	24.5		µC
I_{RRM}	Reverse recovery current		-	67		A

Notes:

(1)Pulse width is limited by safe operating area

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.2 Electrical characteristics (curves)

Figure 2: Safe operating area

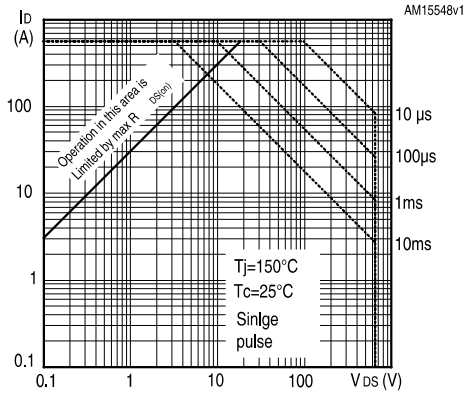


Figure 3: Thermal impedance

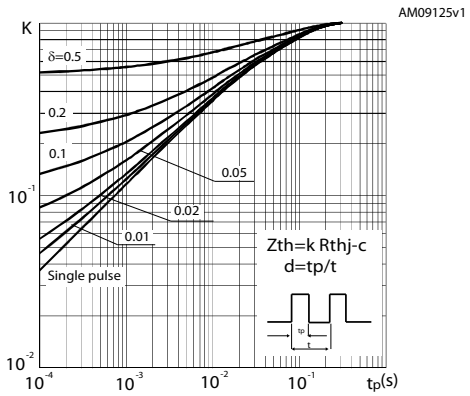


Figure 4: Output characteristics

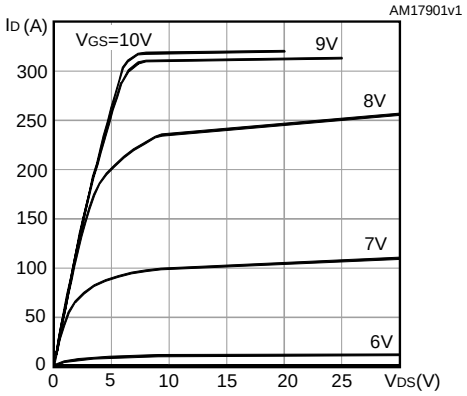


Figure 5: Transfer characteristics

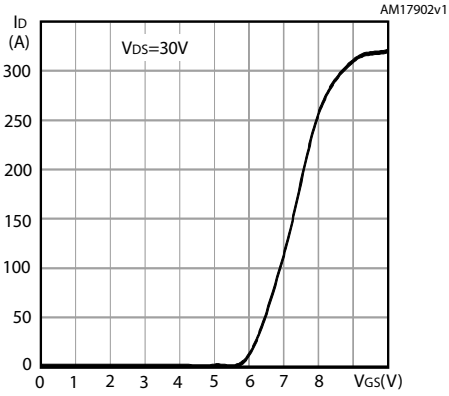


Figure 6: Gate charge vs gate-source voltage

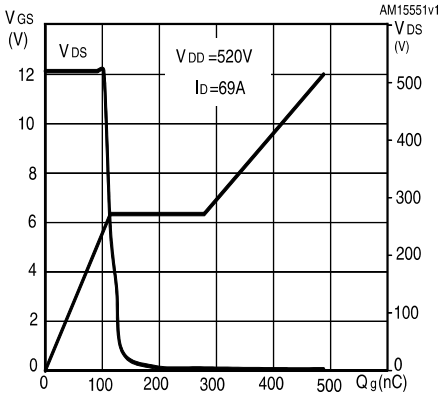


Figure 7: Static drain-source on-resistance

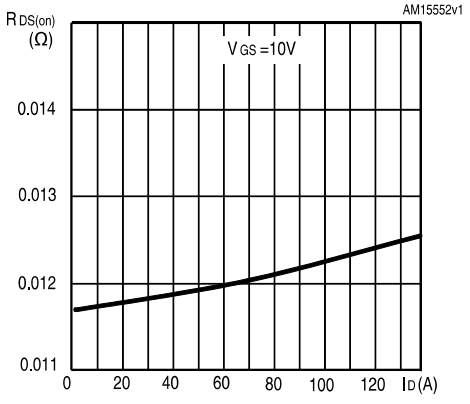


Figure 8: Capacitance variations

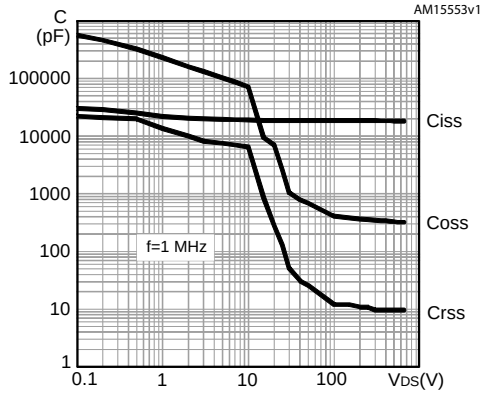


Figure 9: Normalized gate threshold voltage vs temperature

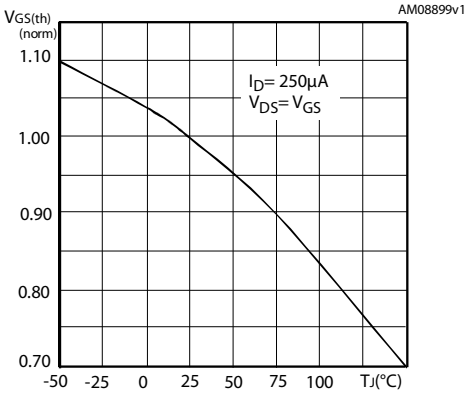


Figure 10: Normalized on-resistance vs temperature

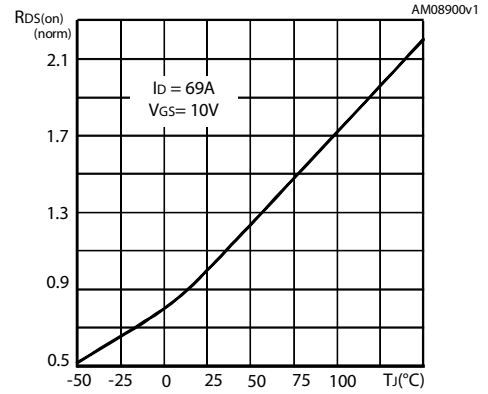


Figure 11: Normalized $V_{(BR)DSS}$ vs temperature

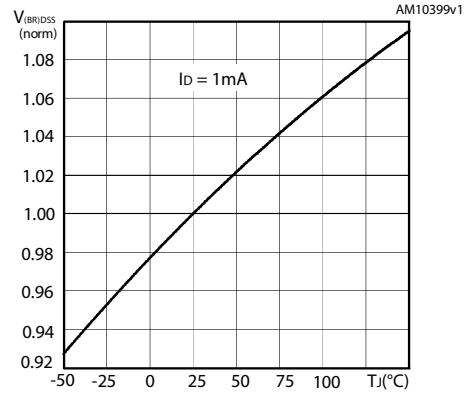


Figure 12: Output capacitance stored energy

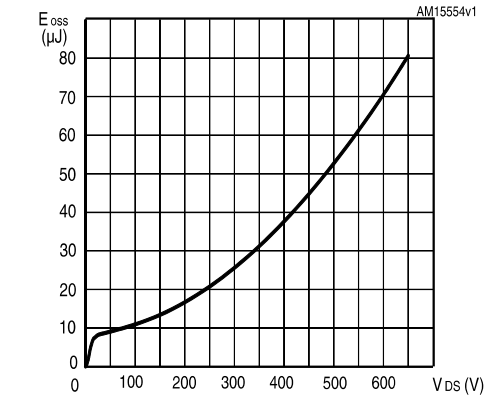
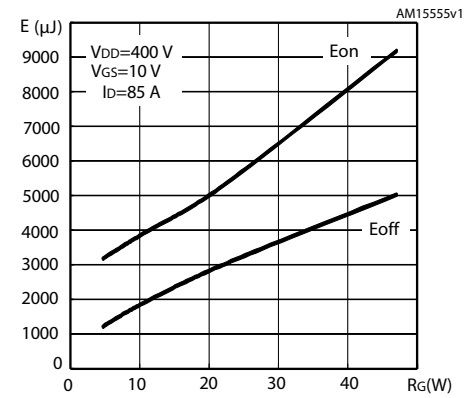


Figure 13: Switching losses vs gate resistance



The previous figure E_{on} includes reverse recovery of a SiC diode.

3 Test circuits

Figure 14: Test circuit for resistive load switching times

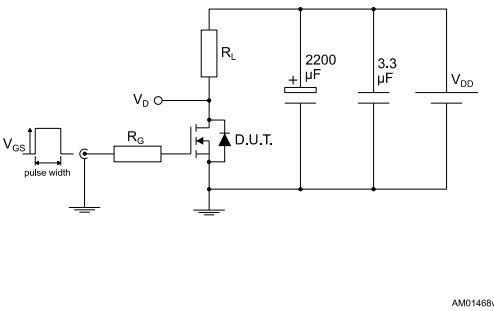


Figure 15: Test circuit for gate charge behavior

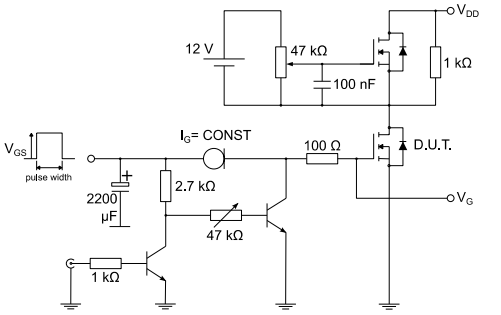


Figure 16: Test circuit for inductive load switching and diode recovery times

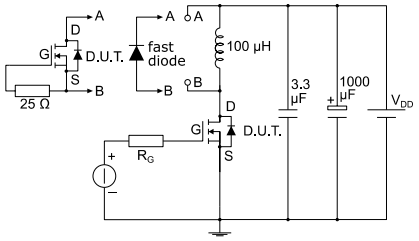


Figure 17: Unclamped inductive load test circuit

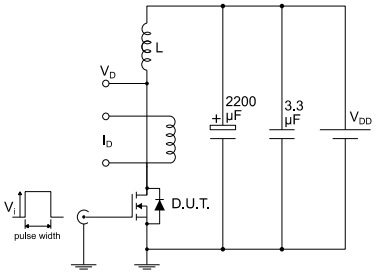


Figure 18: Unclamped inductive waveform

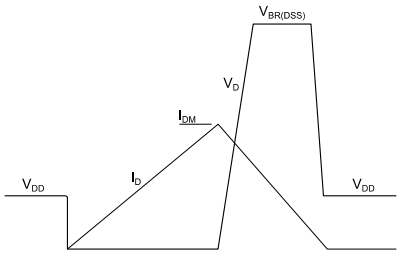
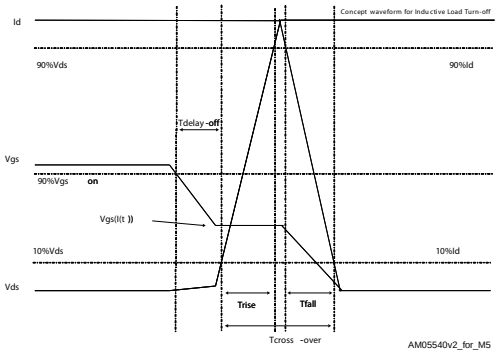


Figure 19: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 Max247 package information

Figure 20: Max247 package outline

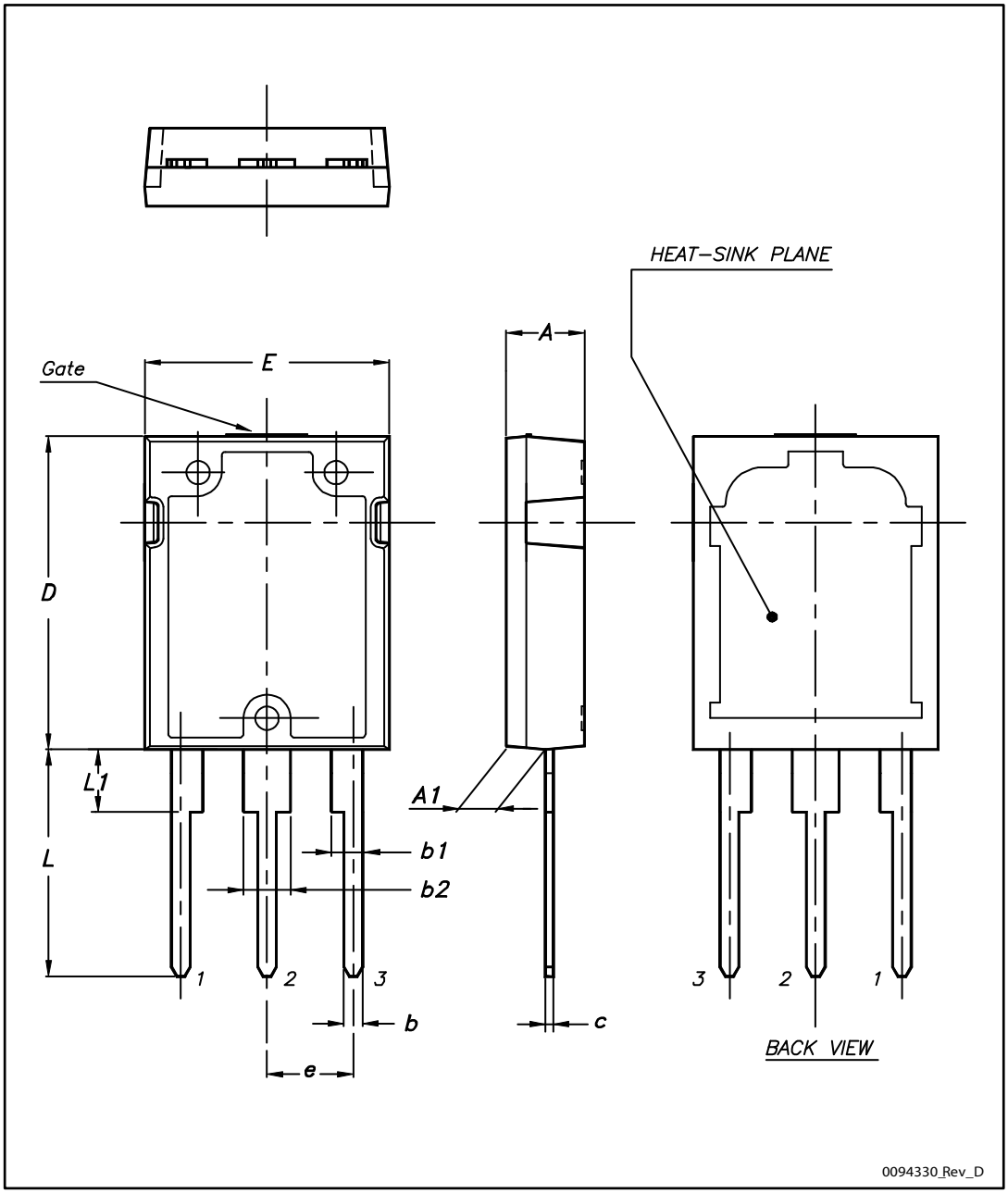


Table 8: Max247 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.70	-	5.30
A1	2.20	-	2.60
b	1.00	-	1.40
b1	2.00	-	2.40
b2	3.00	-	3.40
c	0.40	-	0.80
D	19.70	-	20.30
e	5.35	-	5.55
E	15.30	-	15.90
L	14.20	-	15.20
L1	3.70	-	4.30

5 Revision history

Table 9: Document revision history

Date	Revision	Changes
25-Sep-2012	1	First release.
17-Jan-2013	2	Modified: I_{AR} and E_{AS} values Modified: typical values on Table 5, 6 and 7
13-Nov-2015	3	Updated title, features and description on cover page. Document status promoted from preliminary to production data. Modified: *Table 2: "Absolute maximum ratings"* and *Table 3: "Thermal data"* Updated: *Figure 4: "Output characteristics"* and *Figure 5: "Transfer characteristics"* Minor text changes.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.