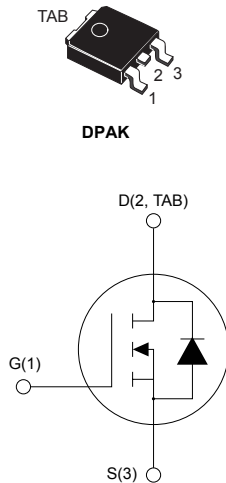


## N-channel 250 V, 140 mΩ typ., 17 A STripFET II Power MOSFET in a DPAK package



AM01475v1\_noZen



### Features

Order code	$V_{DS}$	$R_{DS(on)}$ max.	$I_D$
STD17NF25	250 V	165 mΩ	17 A

- Exceptional dv/dt capability
- 100% avalanche tested
- Low gate charge

### Applications

- Switching applications

### Description

This Power MOSFET has been developed using STMicroelectronics' unique STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the device suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

#### Product status link

[STD17NF25](#)

#### Product summary

<b>Order code</b>	STD17NF25
<b>Marking</b>	17NF25
<b>Package</b>	DPAK
<b>Packing</b>	Tape and reel

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	250	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	17	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	10	
$I_{DM}^{(1)}$	Drain current (pulsed)	68	A
$P_{TOT}$	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	90	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	10	V/ns
$T_{stg}$	Storage temperature range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating junction temperature range		$^\circ\text{C}$

1. Pulse width is limited by safe operating area.
2.  $I_{SD} \leq 17\text{ A}$ ,  $di/dt \leq 200\text{ A}/\mu\text{s}$ ,  $V_{DS}(\text{peak}) < V_{(BR)DSS}$ ,  $V_{DD} = 80\%V_{(BR)DSS}$ .

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Thermal resistance, junction-to-case	1.38	$^\circ\text{C}/\text{W}$
$R_{thJA}^{(1)}$	Thermal resistance, junction-to-ambient	50	$^\circ\text{C}/\text{W}$

1. When mounted on 1 inch<sup>2</sup> FR-4, 2 Oz copper board.

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or non-repetitive (pulse width limited by $T_J$ max.)	17	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	100	mJ

## 2 Electrical characteristics

$T_C = 25\text{ °C}$  unless otherwise specified.

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0\text{ V}$	250			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 250\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 250\text{ V}$ , $T_C = 125\text{ °C}^{(1)}$			10	
$I_{GSS}$	Gate body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$ , $I_D = 8.5\text{ A}$		140	165	m $\Omega$

1. Specified by design, not tested in production.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	1000	-	pF
$C_{oss}$	Output capacitance		-	178	-	pF
$C_{rss}$	Reverse transfer capacitance		-	28	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }200\text{ V}$ , $V_{GS} = 0\text{ V}$	-	135	-	pF
$R_g$	Gate input resistance	$f = 1\text{ MHz}$ , $I_D = 0\text{ A}$	-	2	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 200\text{ V}$ , $I_D = 17\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 13. Test circuit for gate charge behavior)	-	29.5	-	nC
$Q_{gs}$	Gate-source charge		-	4.8	-	nC
$Q_{gd}$	Gate-drain charge		-	15.6	-	nC

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 125\text{ V}$ , $I_D = 8.5\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$	-	8.8	-	ns
$t_r$	Rise time		-	17.2	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	21	-	ns
$t_f$	Fall time		-	8.8	-	ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		17	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		68	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 17\text{ A}, V_{GS} = 0\text{ V}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 17\text{ A}, di/dt = 100\text{ A}/\mu\text{s},$	-	157		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 50\text{ V}$	-	0.91		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	11.6		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 17\text{ A}, di/dt = 100\text{ A}/\mu\text{s},$	-	196		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 50\text{ V}, T_J = 150\text{ }^\circ\text{C}$	-	1.34		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	13.7		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

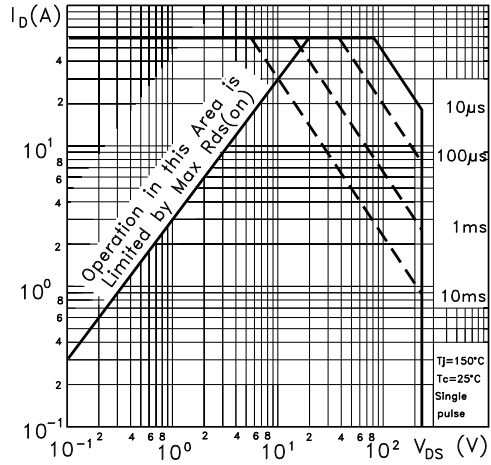


Figure 2. Thermal impedance

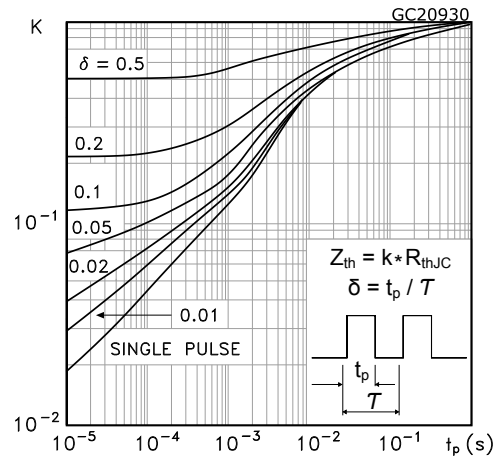


Figure 3. Output characteristics

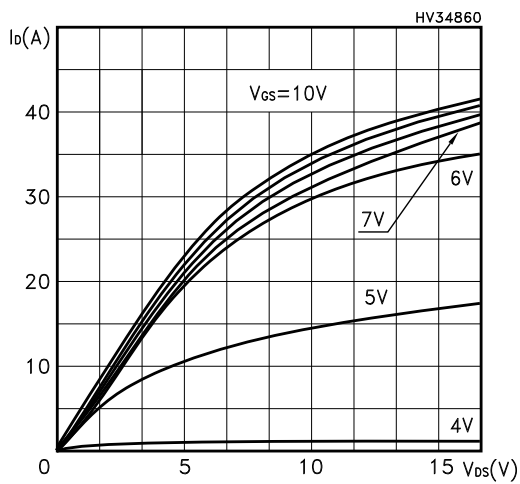


Figure 4. Transfer characteristics

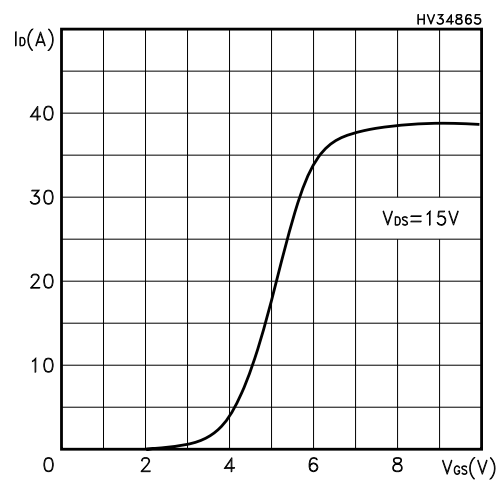


Figure 5. Normalized  $V_{(BR)DSS}$  vs temperature

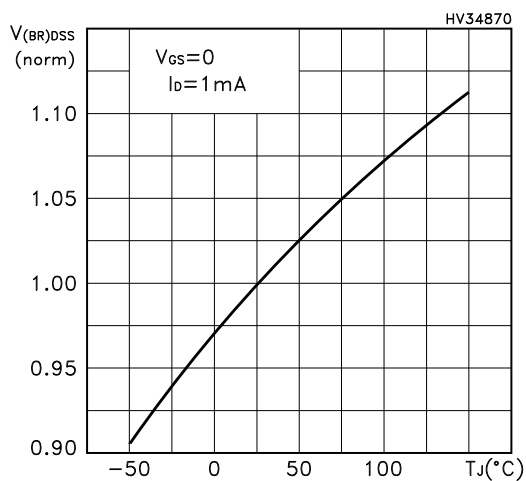
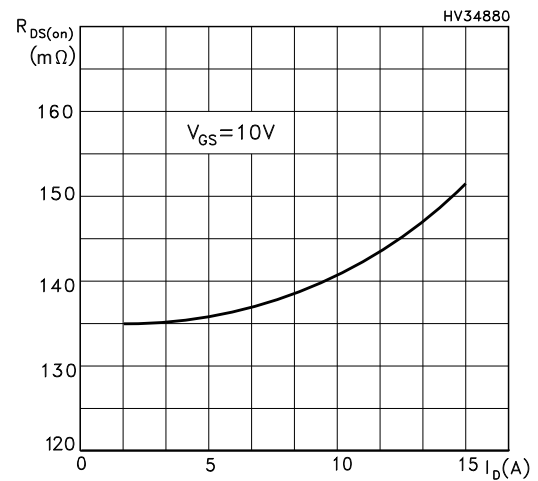
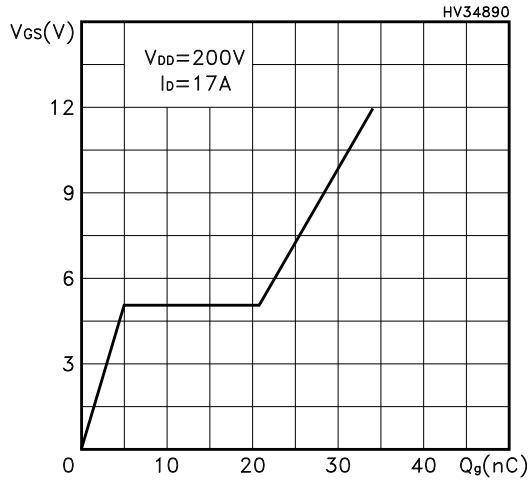


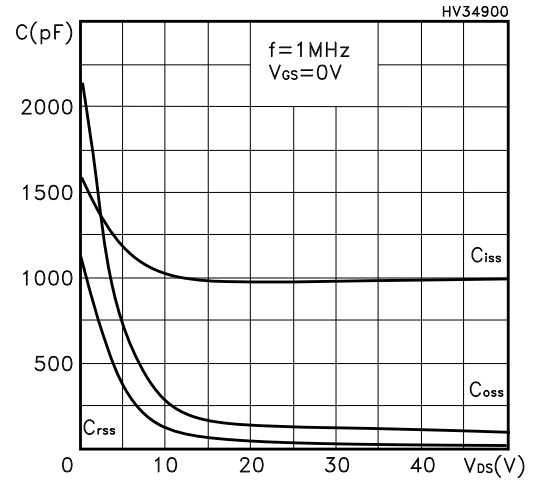
Figure 6. Static drain-source on resistance



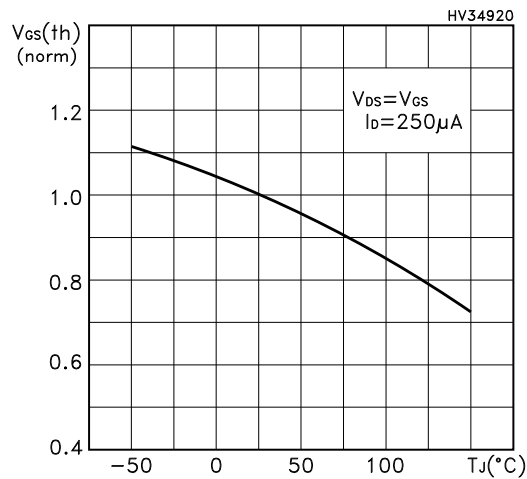
**Figure 7. Gate charge vs gate-source voltage**



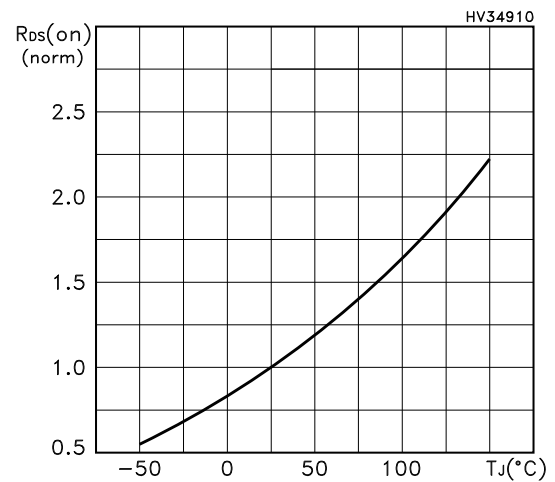
**Figure 8. Capacitance variations**



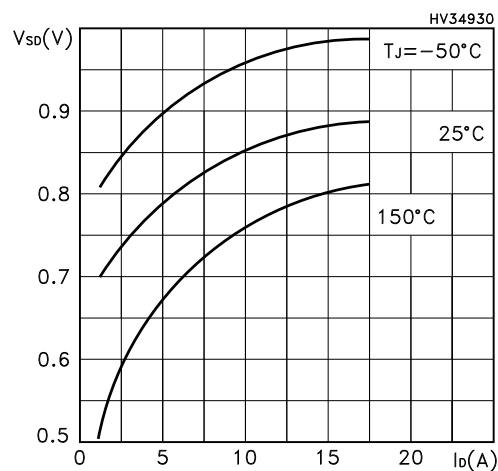
**Figure 9. Normalized gate threshold voltage vs temperature**



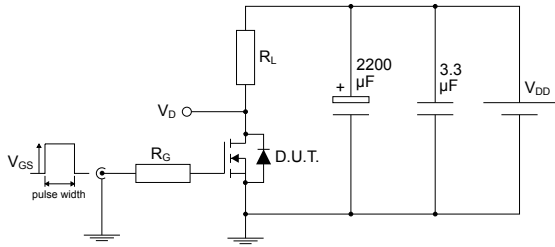
**Figure 10. Normalized on resistance vs temperature**



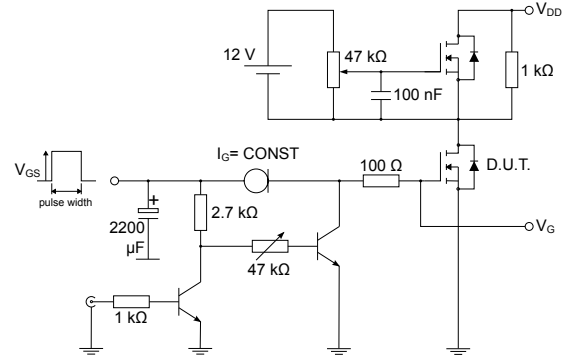
**Figure 11. Source-drain diode forward characteristics**



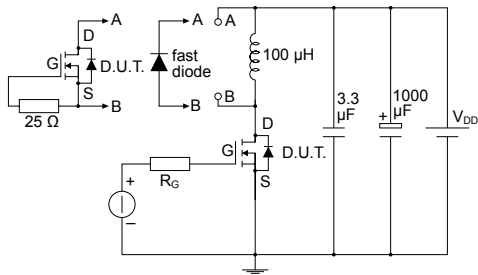
### 3 Test circuits

**Figure 12. Test circuit for resistive load switching times**


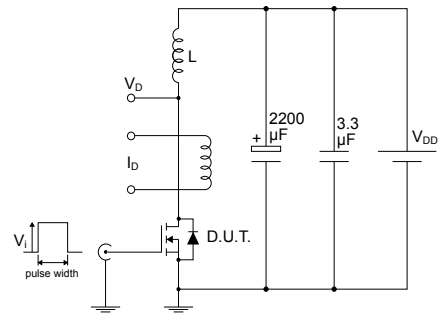
AM01468v1

**Figure 13. Test circuit for gate charge behavior**


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**Figure 14. Test circuit for inductive load switching and diode recovery times**


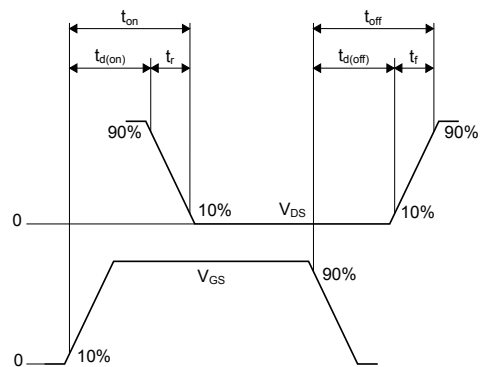
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**Figure 15. Unclamped inductive load test circuit**


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**Figure 16. Unclamped inductive waveform**


AM01472v1

**Figure 17. Switching time waveform**


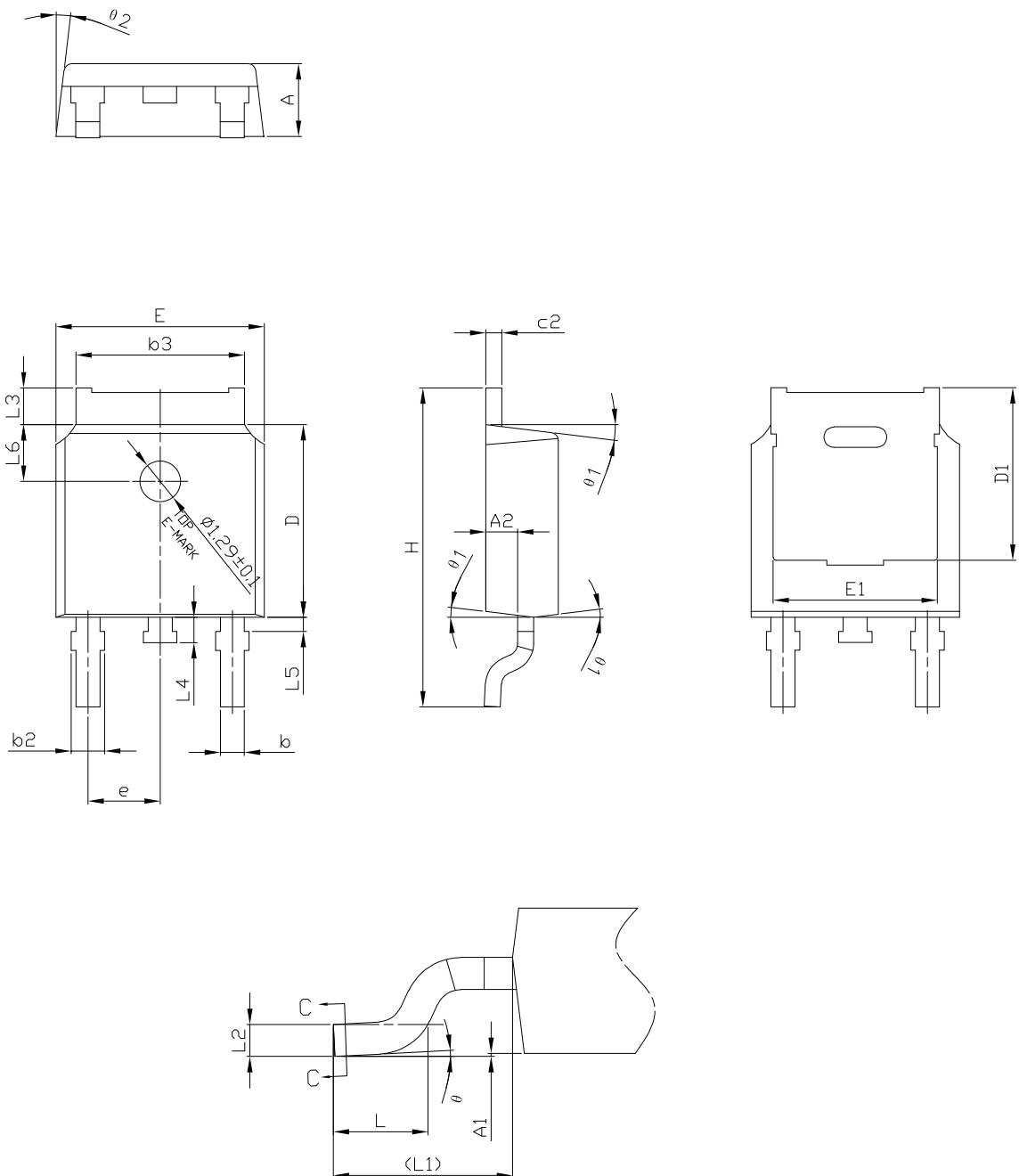
AM01473v1

## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 DPAK (TO-252) type C3 package information

Figure 18. DPAK (TO-252) type C3 package outline



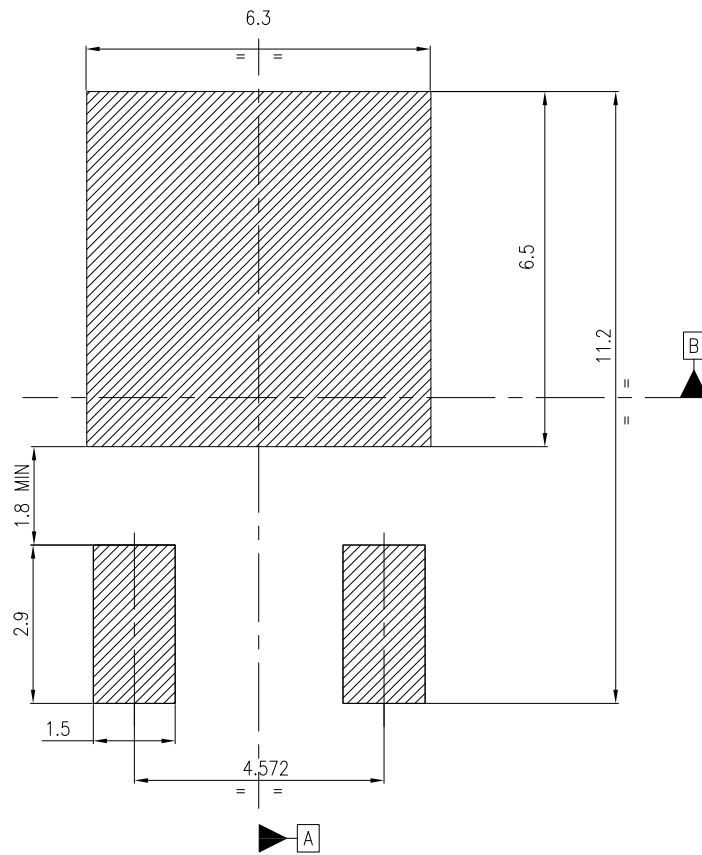
0068772\_type-C3\_rev34



**Table 8. DPAK (TO-252) type C3 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.00		0.10
A2	0.90	1.01	1.10
b	0.72		0.85
b2	0.72		1.10
b3	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.20	5.45	5.70
E	6.50	6.60	6.70
E1	5.00	5.20	5.40
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1	2.90 REF		
L2	0.51 BSC		
L3	0.90		1.25
L4	0.60	0.80	1.00
L5	0.15		0.75
L6	1.80 REF		
θ	0°		8°
θ1	5°	7°	9°
θ2	5°	7°	9°

Figure 19. DPAK (TO-252) recommended footprint (dimensions are in mm)



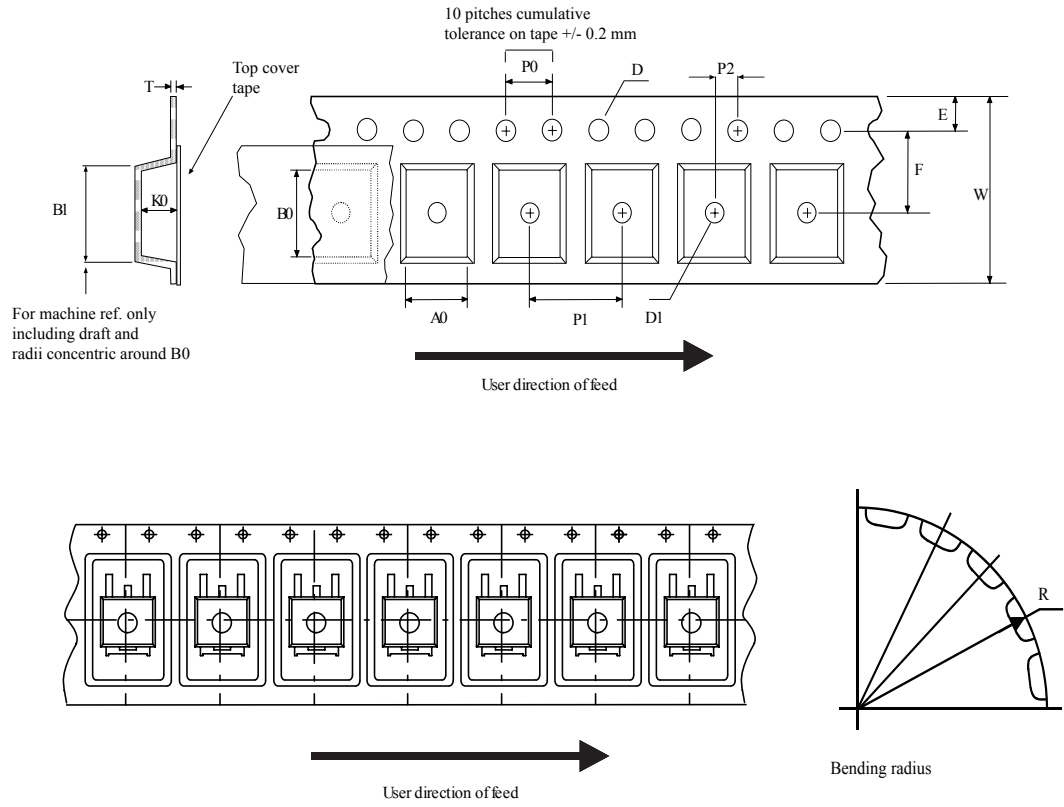
Notes:

- 1) This footprint is able to ensure insulation up to 630 Vrms (according to CEI IEC 664-1)
- 2) The device must be positioned within  $\boxed{\oplus 0.05 \text{ A B}}$

FP\_0068772\_34

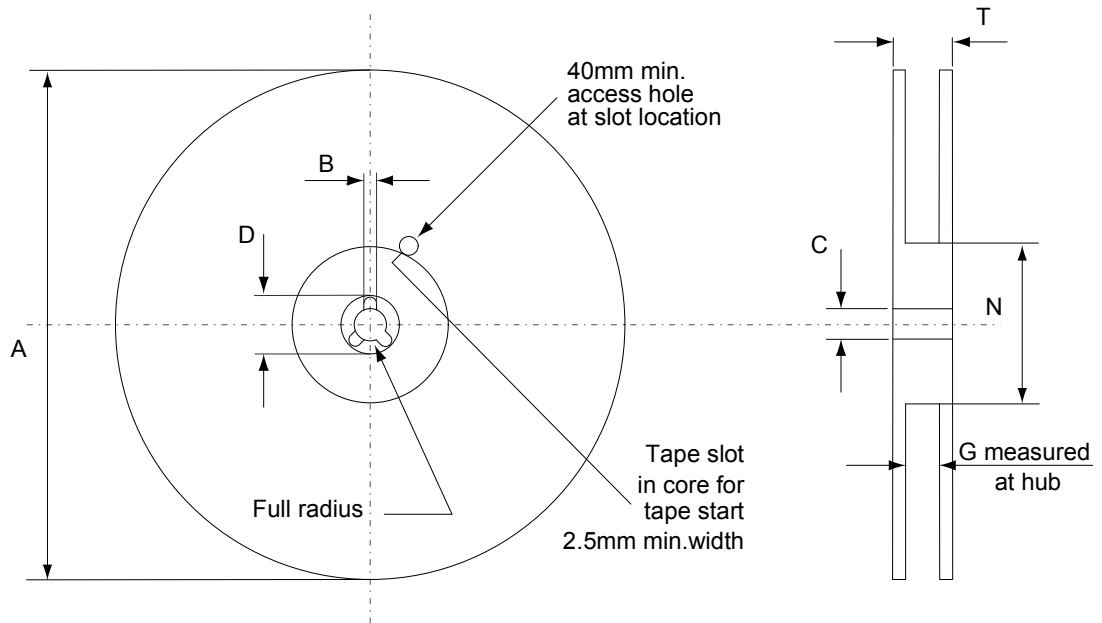
## 4.2 DPAK (TO-252) packing information

Figure 20. DPAK (TO-252) tape outline



AM08852v1

Figure 21. DPAK (TO-252) reel outline



AM06038v1

Table 9. DPAK (TO-252) tape and reel mechanical data

Dim.	Tape		Dim.	Reel	
	mm			mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

## Revision history

**Table 10. Document revision history**

Date	Revision	Changes
01-Feb-2007	1	First release.
07-Nov-2012	2	Minor text changes. The part number STI17NF25 has been moved to a separate datasheet. <i>Section 4: Package mechanical data</i> and <i>Section 5: Packaging mechanical data</i> have been updated.
28-May-2018	3	Removed maturity status indication from cover page. The document status is production data. Updated title in cover page, <i>Section 1 Electrical ratings</i> , <i>Section 2 Electrical characteristics</i> and <i>Section 4 Package information</i> . Minor text changes.
18-Jul-2023	4	The part numbers STF17NF25 and STP17NF25 have been moved to separate datasheets and the document has been updated accordingly. Removed " <i>Section 4.1 DPAK (TO-252) type A2 package information</i> " and replaced " <i>Section 4.2 DPAK (TO-252) type C2 package information</i> " with <i>Section 4.1 DPAK (TO-252) type C3 package information</i> . Minor text changes.
28-Aug-2023	5	Updated <i>Section 1 Electrical ratings</i> .

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