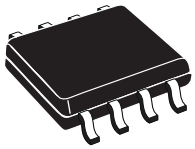
STS4DPF20L

DUAL P-CHANNEL 20V - 0.07 Ω - 4A SO-8
STripFET™ POWER MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STS4DPF20L	20 V	<0.08 Ω	4 A

- TYPICAL $R_{DS}(on)$ = 0.07 Ω
- STANDARD OUTLINE FOR EASY AUTOMATED SURFACE MOUNT ASSEMBLY
- LOW THRESHOLD DRIVE



SO-8

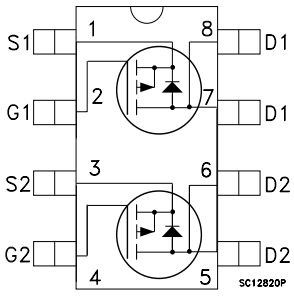
DESCRIPTION

This Power MOSFET is the latest development of STMicroelectronis unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

APPLICATIONS

- BATTERY MANAGEMENT IN NOMADIC EQUIPMENT
- POWER MANAGEMENT IN CELLULAR PHONES

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	20	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	20	V
V_{GS}	Gate- source Voltage	± 16	V
I_D	Drain Current (continuos) at T_C = 25°C Single Operation Drain Current (continuos) at T_C = 100°C Single Operation	4 2.5	A A
I_{DM}(•)	Drain Current (pulsed)	16	A
P_{tot}	Total Dissipation at T_C = 25°C Dual Operation Total Dissipation at T_C = 25°C Single Operation	1.6 2	W W

(•) Pulse width limited by safe operating area.

Note: For the P-CHANNEL MOSFET actual polarity of voltages and current has to be reversed

THERMAL DATA

Rthj-amb	(*)Thermal Resistance Junction-ambient	Single Operation Dual Operating	62.5 78	°C/W °C/W
T_j	Thermal Operating Junction-ambient		-55 to150	°C
T_{stg}	Storage Temperature		-55 to 150	°C

(*) When Mounted on 0.5 in^2 pad of 2 oz.copper

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	20			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0) Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating T_C = 125°C			1 10	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 16 V			±100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS} I_D = 250 µA	1	1.6	2.5	V
$R_{DS(on)}$	Static Drain-source On Resistance Static Drain-source On Resistance	V_{GS} = 10 V I_D = 2 A V_{GS} = 4.5 V I_D = 2 A		0.070 0.085	0.08 0.10	Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (*)	Forward Transconductance	V_{DS}= 15V I_D = 2 A		10		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		1350 490 130		pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD} = 15 V I_D = 2 A R_G = 4.7 Ω V_{GS} = 4.5 V (Resistive Load, Figure 1)		25 35		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD}= 24V I_D= 4A V_{GS}=5V (See test circuit, Figure 2)		12.5 5 3	16	nC nC nC

SWITCHING OFF

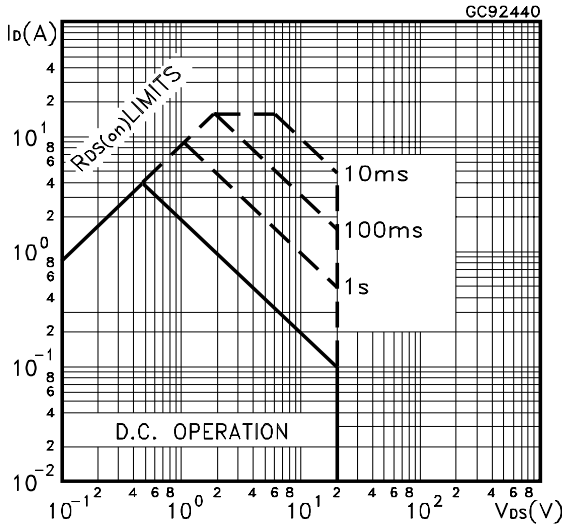
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	V_{DD} = 15 V I_D = 2 A R_G = 4.7Ω, V_{GS} = 4.5 V (Resistive Load, Figure 1)		125 35		ns ns

SOURCE DRAIN DIODE

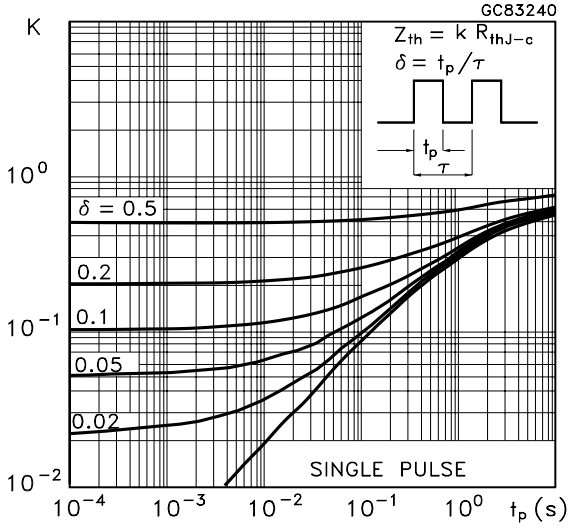
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (•)	Source-drain Current Source-drain Current (pulsed)				4 16	A A
V_{SD} (*)	Forward On Voltage	I_{SD} = 4 A V_{GS} = 0			1.2	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 4 A di/dt = 100A/µs V_{DD} = 15 V T_j = 150°C (See test circuit, Figure 3)		45 36 1.6		ns nC A

(*)Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
(•)Pulse width limited by safe operating area.

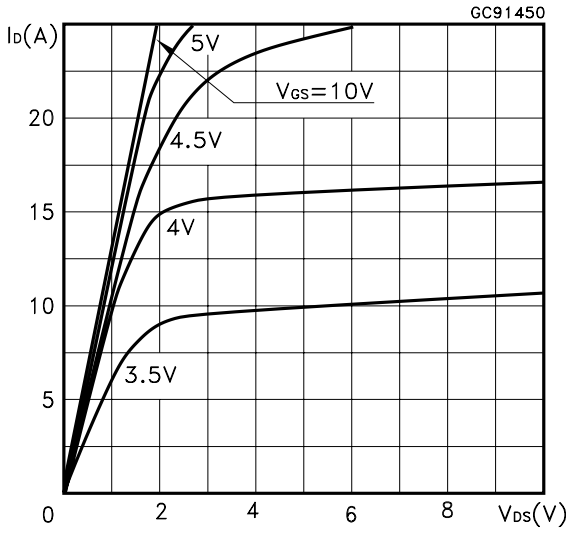
Safe Operating Area



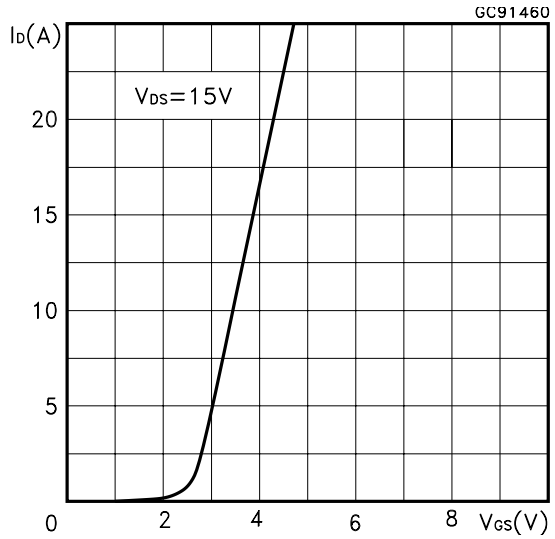
Thermal Impedance



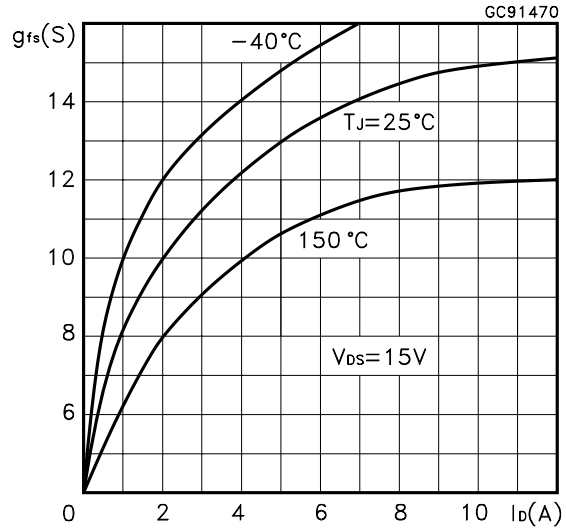
Output Characteristics



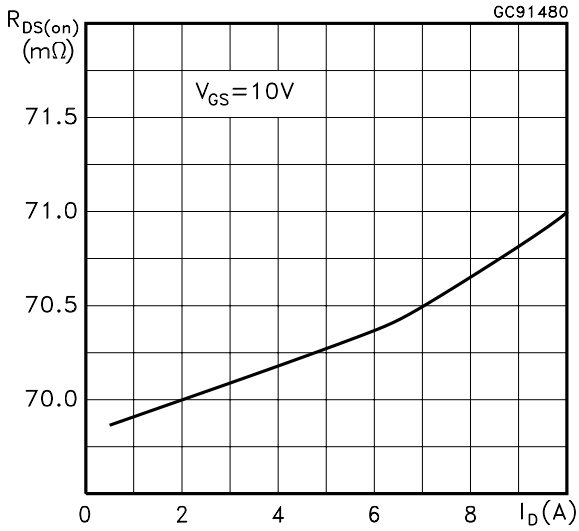
Transfer Characteristics



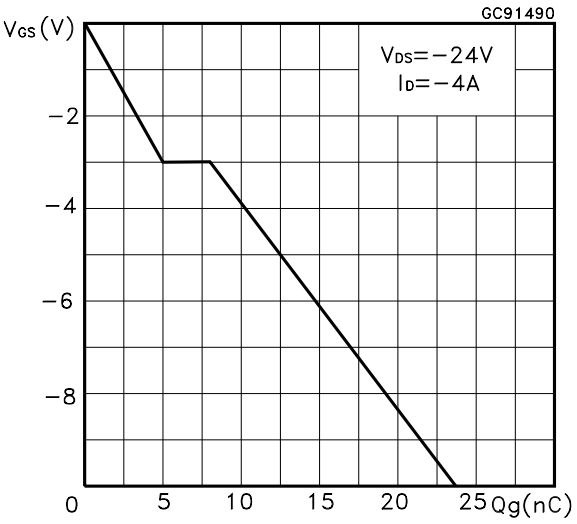
Transconductance



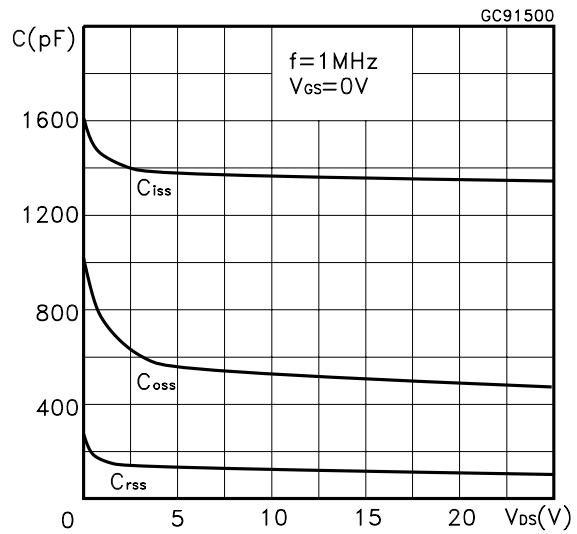
Static Drain-source On Resistance



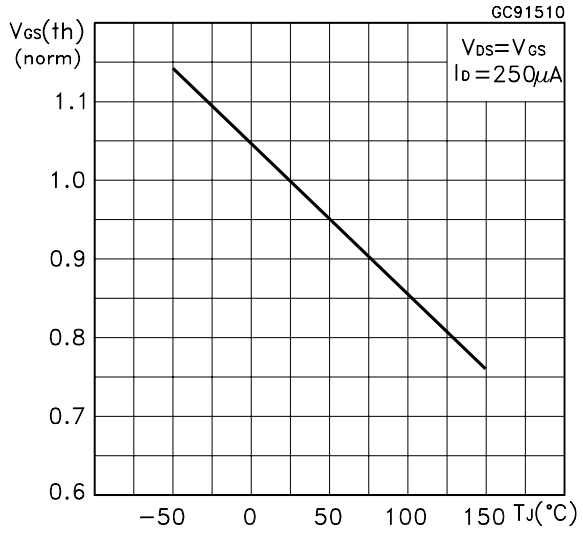
Gate Charge vs Gate-source Voltage



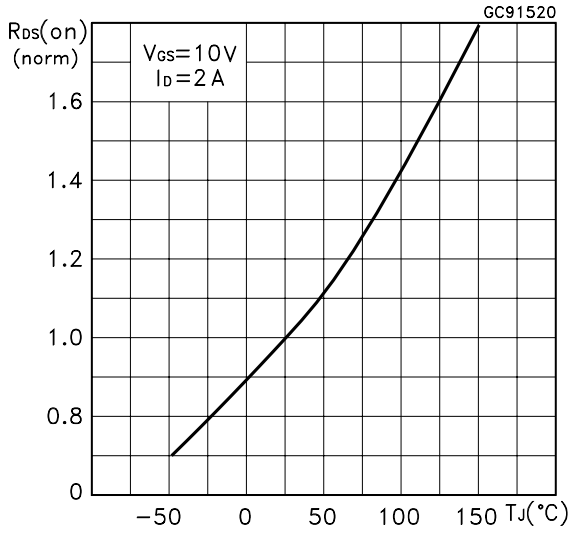
Capacitance Variations



Normalized Gate Threshold Voltage vs Temperature



Normalized on Resistance vs Temperature



Source-drain Diode Forward Characteristics

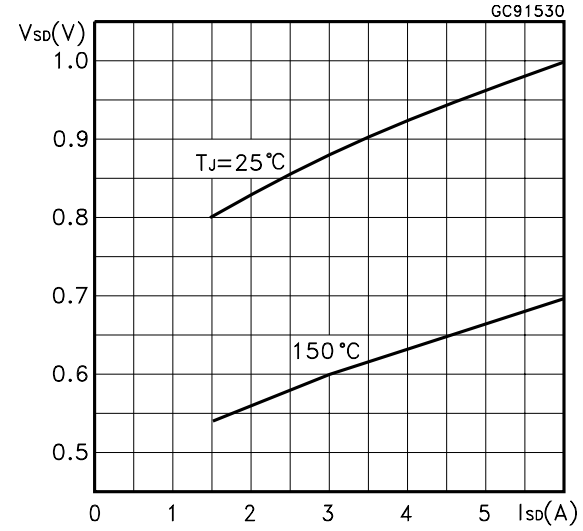


Fig. 1: Switching Times Test Circuits For Resistive Load

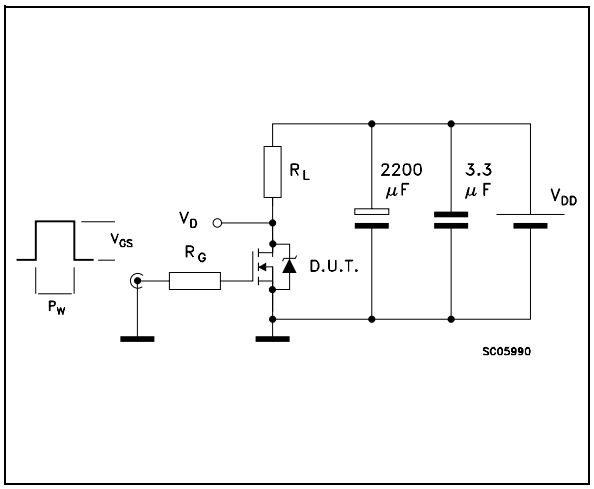


Fig. 2: Gate Charge test Circuit

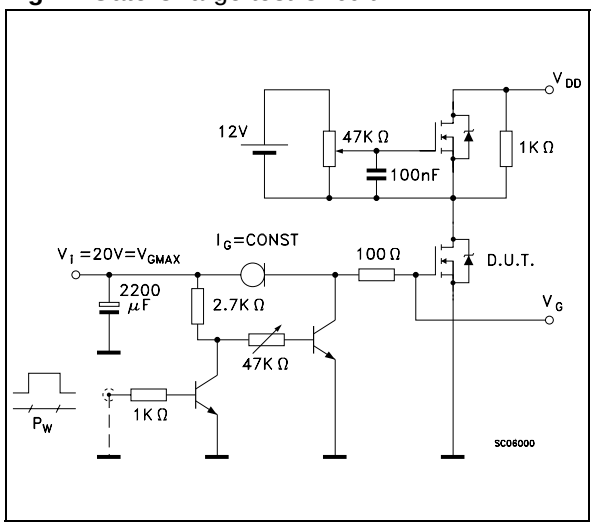
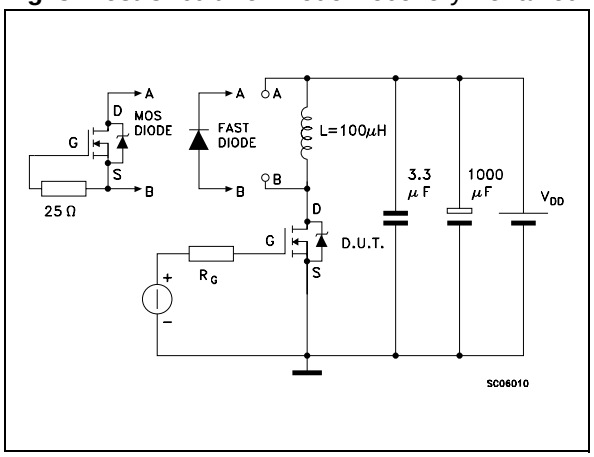
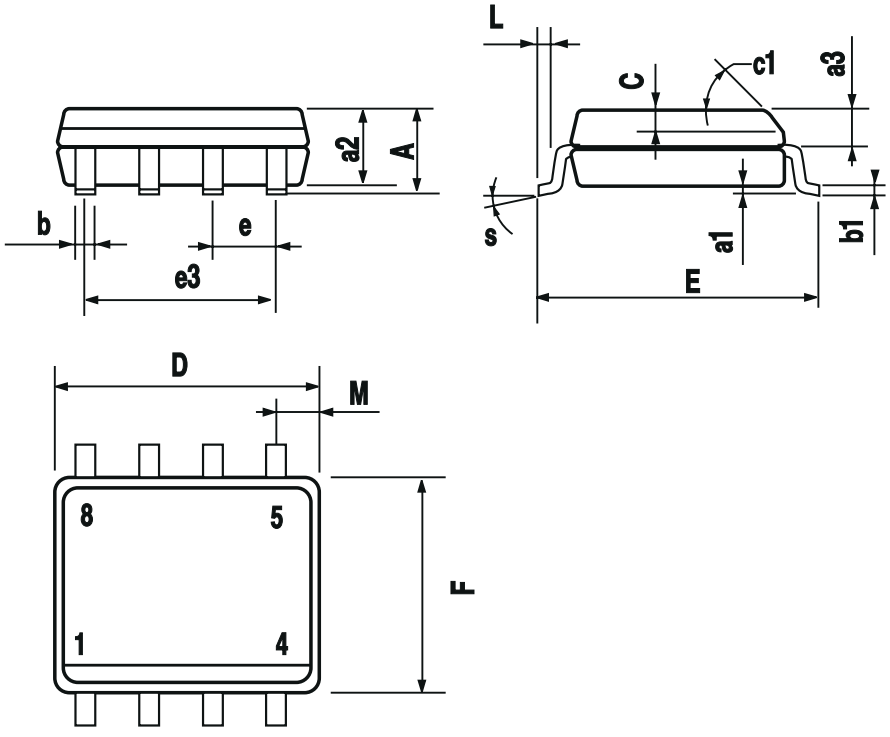


Fig. 3: Test Circuit For Diode Recovery Behaviour



SO-8 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



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