# Complementary Bias Resistor Transistors R1 = 2.2/47 kΩ, R2 = 47 kΩ

## NPN and PNP Transistors with Monolithic Bias Resistor Network

# NSVBC143JPDXV6

This series of digital transistors is designed to replace a single device and its external resistor bias network. The Bias Resistor Transistor (BRT) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space.

### Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable*
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### MAXIMUM RATINGS

($T_A$ = 25°C both polarities $Q_1$ (PNP) & $Q_2$ (NPN), unless otherwise noted)

| Rating | Symbol | Max | Unit |
|---|---|---|---|
| Collector-Base Voltage | $V_{CBO}$ | 50 | Vdc |
| Collector-Emitter Voltage | $V_{CEO}$ | 50 | Vdc |
| Collector Current – Continuous | $I_C$ | 100 | mAdc |
| Input Forward Voltage | $V_{IN(fwd)}$ | 12 | Vdc |
| Input Reverse Voltage | $V_{IN(rev)}$ | 5 | Vdc |

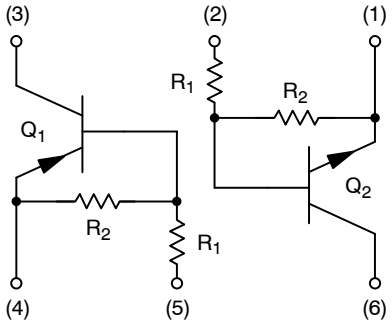
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| NSVBC143JPDXV6T5G | SOT−563 | 8,000/Tape & Reel |
| NSVBC143JPDXV6T1G | SOT−563 | 4,000/Tape & Reel |

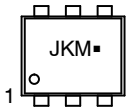
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

### PIN CONNECTIONS




### MARKING DIAGRAM

SOT−563
CASE 463A




JK = Specific Device Code
M = Date Code*
▪ = Pb-Free Package

## THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| **NSVBC143JPDXV6 (SOT−563) ONE JUNCTION HEATED** | | | |
| Total Device Dissipation<br>$T_A$ = 25°C (Note 1)<br>Derate above 25°C (Note 1) | $P_D$ | <br>357<br>2.9 | <br>mW<br>mW/°C |
| Thermal Resistance,<br>Junction to Ambient (Note 1) | $R_{\theta JA}$ | <br>350 | °C/W |
| **NSVBC143JPDXV6 (SOT−563) BOTH JUNCTION HEATED** (Note 2) | | | |
| Total Device Dissipation<br>$T_A$ = 25°C (Note 1)<br>Derate above 25°C (Note 1) | $P_D$ | <br>500<br>4.0 | <br>mW<br>mW/°C |
| Thermal Resistance,<br>Junction to Ambient (Note 1) | $R_{\theta JA}$ | <br>250 | °C/W |
| Junction and Storage Temperature Range | $T_J$, $T_{stg}$ | −55 to +150 | °C |

1. FR−4 @ Minimum Pad.
2. Both junction heated values assume total power is sum of two equally powered channels.

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C both polarities $Q_1$ (PNP) & $Q_2$ (NPN), unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Collector-Base Cutoff Current ($V_{CB}$ = 50 V, $I_E$ = 0) | $I_{CBO}$ | – | – | 100 | nAdc |
| Collector-Emitter Cutoff Current ($V_{CE}$ = 50 V, $I_B$ = 0) | $I_{CEO}$ | – | – | 500 | nAdc |
| Emitter-Base Cutoff Current ($V_{EB}$ = 6.0 V, $I_C$ = 0) | $I_{EBO}$ | – | – | 0.2 | mAdc |
| Collector-Base Breakdown Voltage ($I_C$ = 10 μA, $I_E$ = 0) | $V_{(BR)CBO}$ | 50 | – | – | Vdc |
| Collector-Emitter Breakdown Voltage (Note 3) ($I_C$ = 2.0 mA, $I_B$ = 0) | $V_{(BR)CEO}$ | 50 | – | – | Vdc |
| **ON CHARACTERISTICS** | | | | | |
| DC Current Gain (Note 3) ($I_C$ = 5.0 mA, $V_{CE}$ = 10 V) | $h_{FE}$ | 80 | 140 | – | |
| Collector-Emitter Saturation Voltage (Note 3) ($I_C$ = 10 mA, $I_B$ = 0.3 mA) | $V_{CE(sat)}$ | – | – | 0.25 | V |
| Input Voltage (Off)<br>($V_{CE}$ = 5.0 V, $I_C$ = 100 μA) (NPN)<br>($V_{CE}$ = 5.0 V, $I_C$ = 100 μA) (PNP) | $V_{i(off)}$ | –<br>– | 1.2<br>0.6 | 0.8<br>0.5 | Vdc |
| Input Voltage (On)<br>($V_{CE}$ = 0.3 V, $I_C$ = 2.0 mA) (NPN)<br>($V_{CE}$ = 0.3 V, $I_C$ = 5.0 mA) (PNP) | $V_{i(on)}$ | 3.0<br>1.1 | 1.6<br>0.8 | –<br>– | Vdc |
| Output Voltage (On)<br>($V_{CC}$ = 5.0 V, $V_B$ = 3.5 V, $R_L$ = 1.0 kΩ) (NPN)<br>($V_{CC}$ = 5.0 V, $V_B$ = 2.5 V, $R_L$ = 1.0 kΩ) (PNP) | $V_{OL}$ | –<br>– | –<br>– | 0.2<br>0.2 | Vdc |
| Output Voltage (Off)<br>($V_{CC}$ = 5.0 V, $V_B$ = 0.5 V, $R_L$ = 1.0 kΩ) | $V_{OH}$ | 4.9 | – | – | Vdc |
| Input Resistor (NPN)<br>Input Resistor (PNP) | R1 | 32.9<br>1.5 | 47<br>2.2 | 61.1<br>2.9 | kΩ |
| Resistor Ratio (NPN)<br>Resistor Ratio (PNP) | $R_1/R_2$ | 0.8<br>0.038 | 1.0<br>0.047 | 1.2<br>0.056 | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulsed Condition: Pulse Width = 300 ms, Duty Cycle ≤ 2%.

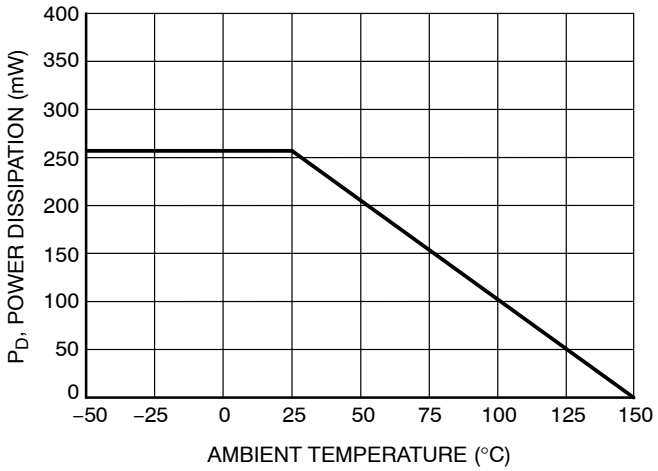



**Figure 1. Derating Curve**

## TYPICAL CHARACTERISTICS – NPN TRANSISTOR

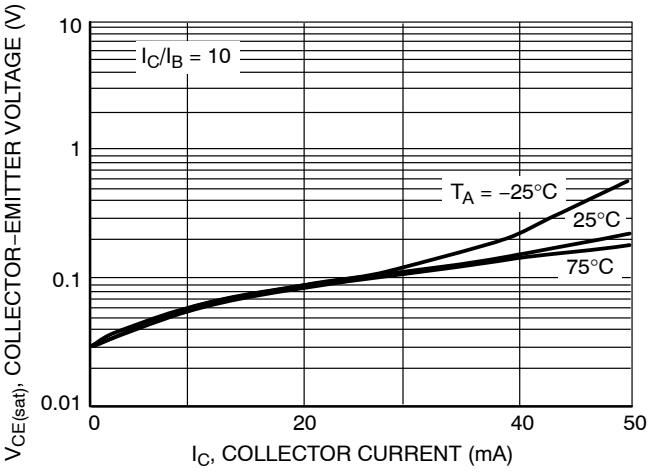



**Figure 2. $V_{CE(sat)}$ vs. $I_C$**

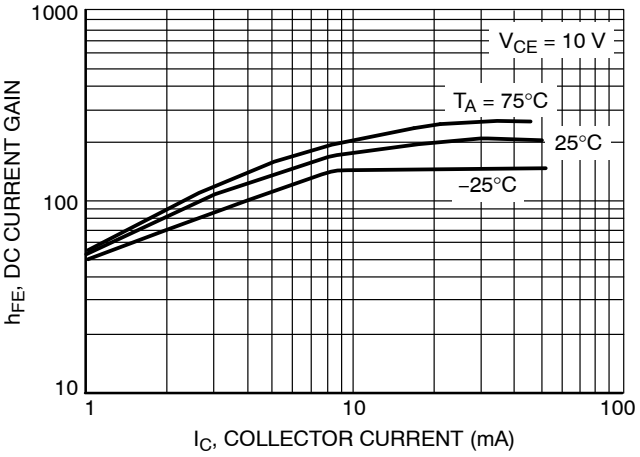



**Figure 3. DC Current Gain**

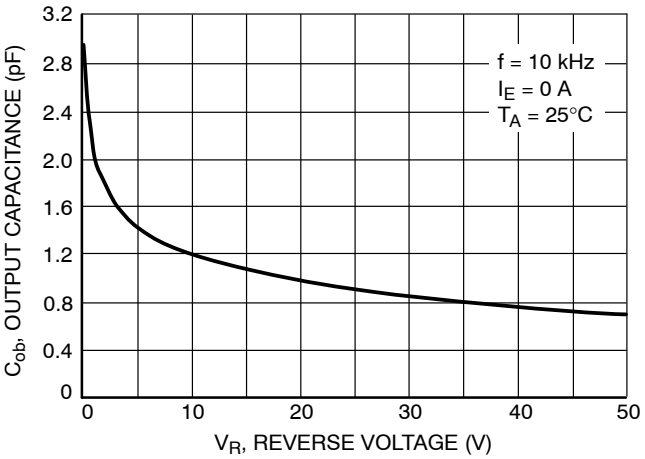



**Figure 4. Output Capacitance**

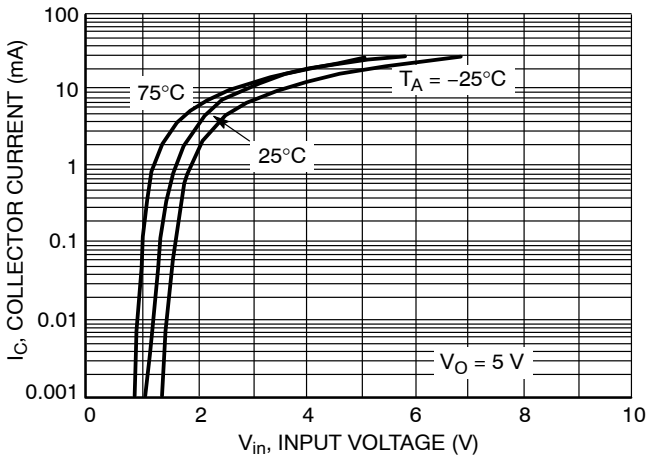



**Figure 5. Output Current vs. Input Voltage**

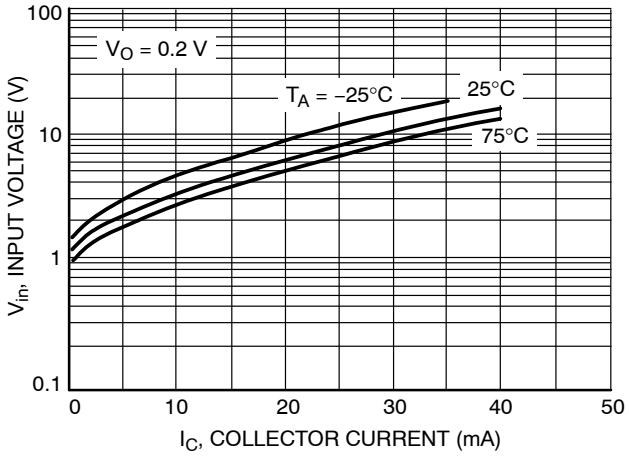



**Figure 6. Input Voltage vs. Output Current**

## TYPICAL CHARACTERISTICS – PNP TRANSISTOR

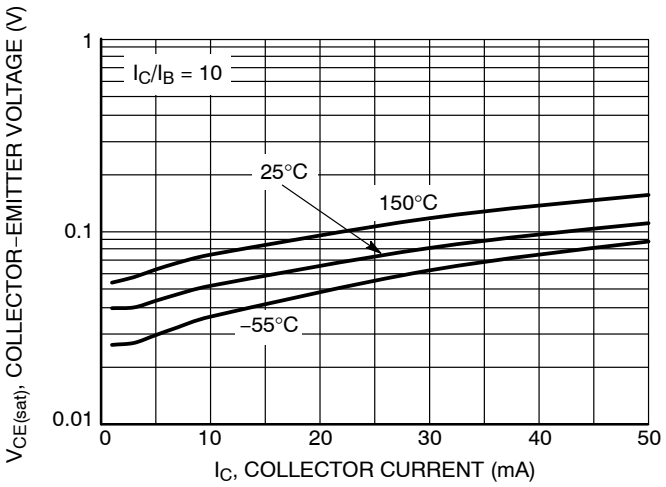



**Figure 7. $V_{CE(sat)}$ vs. $I_C$**

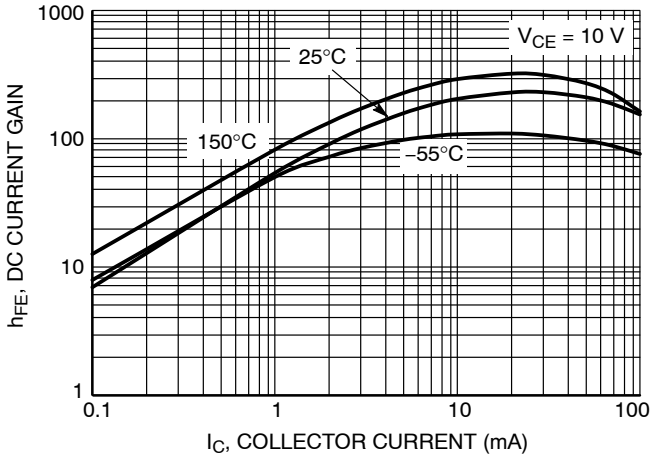



**Figure 8. DC Current Gain**

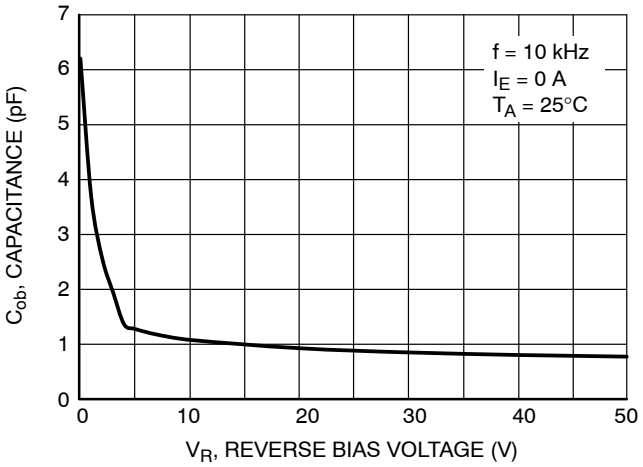



**Figure 9. Output Capacitance**

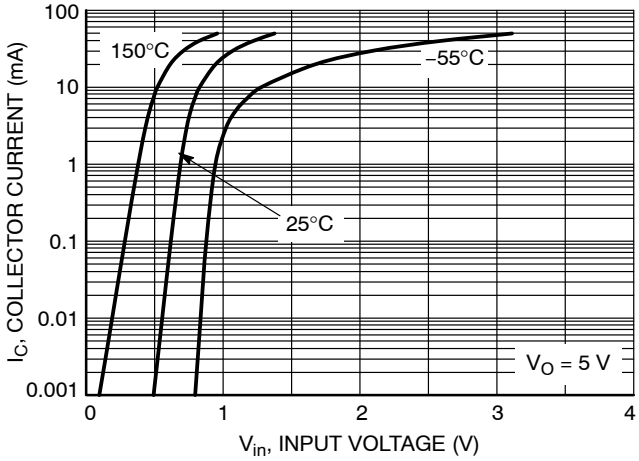



**Figure 10. Output Current vs. Input Voltage**

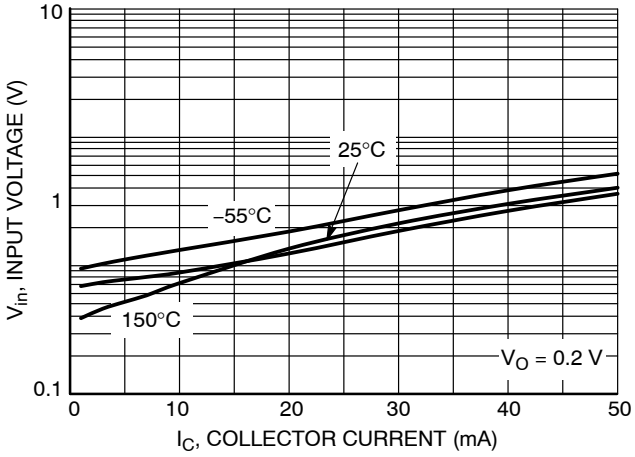
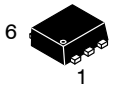



**Figure 11. Input Voltage vs. Output Current**

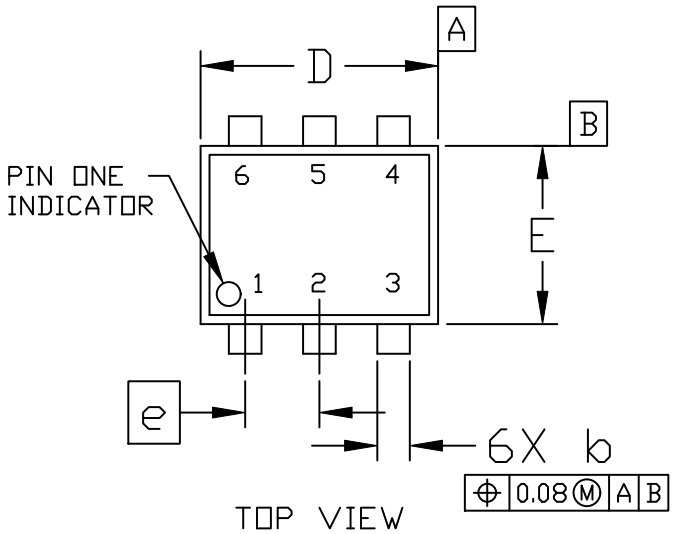



**SCALE 4:1**

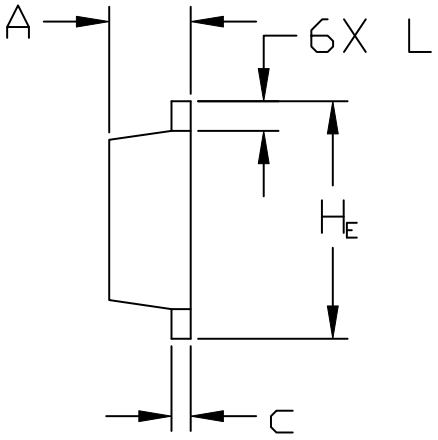
**SOT−563, 6 LEAD**
CASE 463A
ISSUE H

DATE 26 JAN 2021

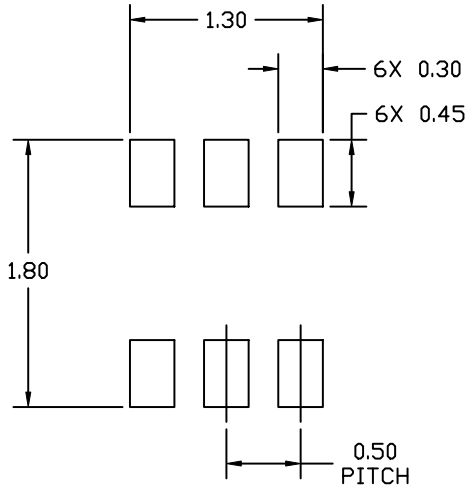
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.




TOP VIEW




SIDE VIEW




RECOMMENDED MOUNTING FOOTPRINT*

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 0.50 | 0.55 | 0.60 |
| b | 0.17 | 0.22 | 0.27 |
| c | 0.08 | 0.13 | 0.18 |
| D | 1.50 | 1.60 | 1.70 |
| E | 1.10 | 1.20 | 1.30 |
| e | 0.50 BSC | | |
| L | 0.10 | 0.20 | 0.30 |
| $H_E$ | 1.50 | 1.60 | 1.70 |

**SOT−563, 6 LEAD**
CASE 463A
ISSUE H

DATE 26 JAN 2021

STYLE 1:
PIN 1. EMITTER 1
2. BASE 1
3. COLLECTOR 2
4. EMITTER 2
5. BASE 2
6. COLLECTOR 1

STYLE 2:
PIN 1. EMITTER 1
2. EMITTER 2
3. BASE 2
4. COLLECTOR 2
5. BASE 1
6. COLLECTOR 1

STYLE 3:
PIN 1. CATHODE 1
2. CATHODE 1
3. ANODE/ANODE 2
4. CATHODE 2
5. CATHODE 2
6. ANODE/ANODE 1

STYLE 4:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 5:
PIN 1. CATHODE
2. CATHODE
3. ANODE
4. ANODE
5. CATHODE
6. CATHODE

STYLE 6:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. ANODE
6. CATHODE

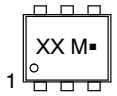
STYLE 8:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 9:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 10:
PIN 1. CATHODE 1
2. N/C
3. CATHODE 2
4. ANODE 2
5. N/C
6. ANODE 1

STYLE 11:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

**GENERIC MARKING DIAGRAM***




XX = Specific Device Code
M = Month Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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|---|---|---|
| DESCRIPTION: | SOT−563, 6 LEAD | PAGE 2 OF 2 |

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