60 Volt, 12 Amp Full-Function Active ORing Solution

Description

The PI2127 *Cool-ORing*® is a complete full-function Active ORing solution with a high-speed ORing MOSFET controller and a very low on-state resistance MOSFET designed for use in redundant power system architectures. The PI2127 *Cool-ORing* solution is offered in an extremely small, thermally enhanced 7mm x 8mm LGA package and can be used in high side, medium voltage Active ORing applications. The PI2127 enables extremely low power loss with fast dynamic response to fault conditions, critical for high availability systems.

The PI2127, with its 8.5mΩ internal MOSFET provides very high efficiency and low power loss during steady state operation, while achieving high-speed turn-off of the internal MOSFET during input power source fault conditions that cause reverse current flow. The PI2127 provides an active low fault flag output to the system during reverse current, excessive forward over-current and UVLO fault conditions.

Features

- Integrated High Performance 12A, 8.5mΩ MOSFET
- Very small, high density fully-optimized solution with simple PCB layout
- Fast dynamic response to power source failures, with 80ns reverse current turn-off delay time
- Accurate sensing capability to indicate system fault conditions (-6mV reverse threshold)
- Internal charge pump
- Active low fault flag output

Applications

- N+1 Redundant Power Systems
- Servers & High End Computing
- Telecom Systems
- High-side Active ORing

Package Information

The PI2127 is offered in the following package:

- 17-pin 7mm x 8mm thermally enhanced LGA package, achieving <10°C/W $R_{\theta J\text{-}PCB}$

Typical Application:

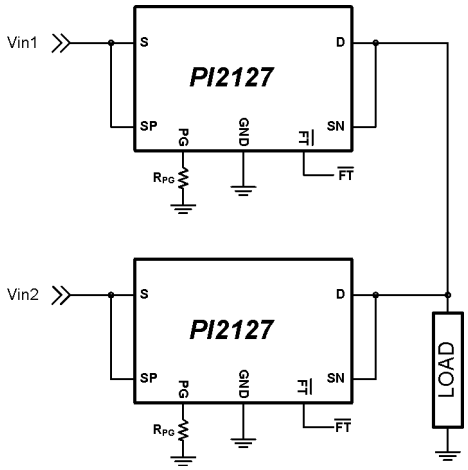


Figure 1: PI2127 High Side Active ORing

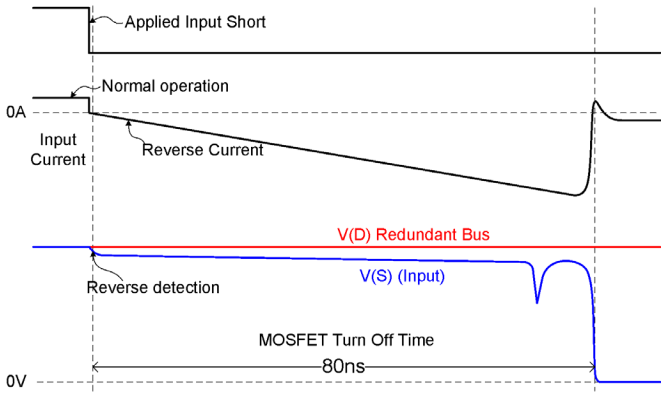
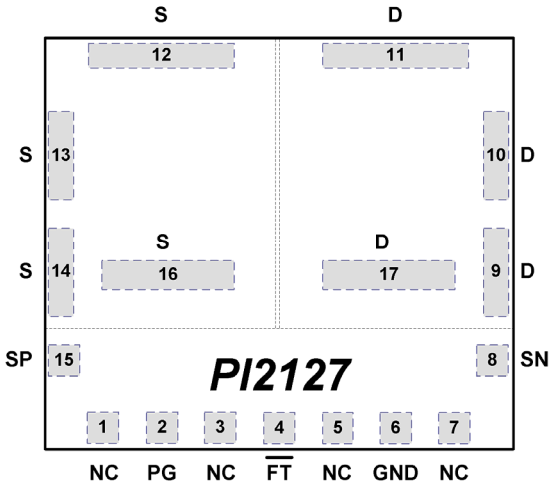


Figure 2: PI2127 response time to an input short fault condition

Pin Description

Pin Name	Pin Number	Description
NC	1, 3, 5, 7	**Not Connected:** Leave pins floating.
PG	2	**Control Circuitry Return:** This pin is the floating return path for the controller circuitry. Connect this pin via a resistor to the low side return (ground).
$\overline{FT}$	4	**Fault Status Output:** This open collector pin pulls low to indicate one of the several potential fault conditions may exist. The Fault pin will pull low after a reverse or forward fault has been detected with a defined delay time (8µs). In addition, the $\overline{FT}$ pin will pull low when the controller input voltage is below the VC under-voltage threshold $V_{S\text{-}PG}$ < 7V (V_{SUVF}). When $V_{S\text{-}PG}$ > 7.15V (V_{SUVR}) and 6mV < $V_{SP\text{-}SN}$ < 275mV this pin clears (High). Leave this pin open if unused.
GND	6	$\overline{FT}$ **Return:** This pin is the return (ground) for the open collector fault circuitry. Connect this pin to logic ground.
SN	8	**Negative Sense Input:** Connect SN pin to the trace between D pin (outside of the PI2127 foot print) and the output load. The polarity of the voltage difference between SP and SN provides an indication of current flow direction through the MOSFET.
D	9, 10, 11, 17	Drain: The Drain of the internal N-channel MOSFET and fault level shift circuit. Connect this pin to the output load.
S	12, 13, 14 16	Source-The source of the internal N-channel MOSFET and bias for the control circuitry. Connect this pin to the input power source bus voltage.
SP	15	**Positive Sense Input:** Connect SP pin to the trace between S pin (outside of the PI2127 foot print) and the input source. The polarity of the voltage difference between SP and SN provides an indication of current flow direction through the MOSFET.

Package Pin-Out



17-pin LGA (7mm x 8mm)
Top view

Absolute Maximum Ratings

Note: Unless otherwise specified, all voltage nodes are referenced to "PG"

Drain-to-Source Voltage (V_{DS})	60V @ 25°C
Source Current (Is) Continuous	12A
Source Current (Is) Pulsed (10µs) (1)	100A
Source Current (Is) Pulsed (300ns) (1)	150A
Single Pulse Avalanche Current (T_{AV}<11µs) (1)	33A
Junction-to-Ambient Thermal Resistance ($R_{\theta J-A}$)	45°C/W (0LFM)
Junction-to-PCB Thermal Resistance ($R_{\theta J-PCB}$)	10°C/W
S (Source),	-0.3V to 13V / 10mA
SP	-0.3V to 17.3V / 10mA
SN, D (Drain)	-0.3V to 60V / 10mA
GND	-50V to +0.3V / 10mA
$\overline{FT}$ to GND	-0.3V to 20V / 10mA
D (Drain) to GND	-0.3V to 60V / 10mA
Storage Temperature	-65°C to 150°C
Operating Junction Temperature	-40°C to 140°C
Internal MOSFET Operating Junction Temperature	-40°C to 150°C
Soldering Temperature for 20 seconds	260°C
ESD Rating	CDM Class IV

Electrical Specifications

Unless otherwise specified: -40°C < T_J < 125°C, V_{S-PG} =10.5V, V_{PG}=V_{GND}=0V, V_D=V_S

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Control Circuit Supply (S to PG)						
Operating Supply Range	V_{S-PG}	8.5		10.5	V	No VC limiting Resistor
Quiescent Current	I_{VC}		1.5	2.0	mA	Normal operation, no fault
Clamp Voltage	V_{S-CLM}	11	11.7	12.5	V	I_S=3mA
Clamp Resistance	R_S			10	Ω	Delta I_S=10mA
Under-Voltage Rising Threshold	V_{SUVR}	6.1	7.15	8.5	V	
Under-Voltage Falling Threshold	V_{SUVF}	6	7.00	7.9	V	
Under-Voltage Hysteresis	V_{SUV-HS}	100	150	200	mV	

Electrical Specifications

Unless otherwise specified: -40°C < T_J < 125°C, V_{S-PG} =10.5V, V_{PG}=V_{GND}=0V, V_D=V_S

Parameter	Symbol	Min	Typ	Max	Units	Conditions
DIFFERENTIAL AMPLIFIER AND COMPARATORS (Continued)						
Common Mode Input Voltage	V_{CM}	-3		3	V	SP to S and SN to S
Differential Operating Input Voltage[1]	V_{SP-SN}	-80		400	mV	SP-SN
SP Input Bias Current	I_{SP}	35	55	75	µA	V_{SP} = V_{SN} = V_S
SN Input Bias Current	I_{SN}	35	55	75	µA	V_{SP} = V_{SN} = V_S
SN Current During Fault Condition[3]	I_{SN-FLT}		5	7.5	mA	V_{SN} = 60V, V_{SP} = V_S =V_D=0V
MOSFET Turn On Threshold	V_{FET-ON}	+1	+6	+11	mV	V_{SP-PG} = 10.5V, @ 25°C
Reverse Comparator Threshold	V_{RVS-TH}	-11	-6	-2	mV	V_{SP-PG} = 10.5V, @ 25°C
Reverse to On Hysteresis	V_{RVS-HY}	10	12	14	mV	V_{SP-PG} = 10.5V, @ 25°C
Reverse Fault to MOSFET Turn-off Time	t_{RVS}		80	150	ns	V_{SP-SN} = ± 50mV step
Forward Comparator Threshold	V_{FWD-TH}	250	275	300	mV	
Forward Comparator Hysteresis	V_{FWD-HY}	15	25	35	mV	
Internal N-Channel MOSFET						
Drain-to-Source Breakdown Voltage	BV_{DSS}	60			V	V_S=V_{GND}=V_{FT}=V_{SP}=0V I_D=2mA , Tj=25°C; V_{SN}=10.5V
Source Current Continuous	I_S			12	A	In ON state, Tj=25°C
D Pin Current During Fault [3] (including level-shift circuitry)	I_{D-FLT}			4	mA	V_D=60V; V_{GND}=V_{FT}=V_S=V_{SP}=0V, Tj=25°C, V_{SN}=10.5V
Drain-to-Source On Resistance	R_{DSon}		8.5	11	mΩ	In ON state, Is=10A, Tj=25°C
Body Diode Forward Voltage	V_{F-BD}		0.75	1.0	V	In OFF state, Is=4A, Tj=25°C
Fault						
Fault Output Low Voltage	$V_{\overline{FT}}$		0.2	0.5	V	I_{FT}=2mA, V_{S-PG} ≥ 4.5V
Fault Output High, Leakage Current	I_{FT}			10	µA	V_{FT}=14V
Fault Delay time	T_{FT-DLY}	4	8	16	µs	V_{SP-SN} = ± 50mV step

Note 1*:* These parameters are not production tested but are guaranteed by design, characterization, and correlation with statistical process control.

Note 2: Current sourced by a pin is reported with a negative sign.

Note 3: Current flow during input short fault condition. See the Fault Circuit description in the Application Information section for more detail

Functional Description:

The PI2127 integrated *Cool-ORing* product takes advantage of two different technologies combining an 8.5mΩ on-state resistance ($R_{DS(on)}$) N-channel MOSFET with high density control circuitry. This combination provides superior density, minimizing PCB space to achieve an ideal ORing diode function, significantly reducing power dissipation and eliminating the need for heat sinking, while minimizing design complexity.

The PI2127's 8.5mΩ on-state resistance MOSFET used in the conduction path enables a dramatic reduction in power dissipation versus the performance of a diode used in conventional ORing applications due to its high forward voltage drop.
Due to the inherent characteristics of the MOSFET, current will flow in the forward and reverse directions while the gate remains above the gate threshold voltage. Ideal ORing applications should not allow reverse current flow, so the controller has to be capable of very fast and accurate detection of reverse current caused by input power source failures, and very fast turn off of the gate of the MOSFET. Once the gate voltage falls below the gate threshold, the MOSFET is off and the body diode will be reverse biased preventing reverse current flow and subsequent excessive voltage droop on the redundant bus.

Differential Amplifier:

The PI2127 integrates a high-speed low offset voltage differential amplifier to sense the difference between the Sense Positive (SP) pin voltage and Sense Negative (SN) pin voltage with high sensitivity to fault current. The amplifier output is connected to the Reverse and Forward comparators.

Reverse Current Comparator: RVS

The reverse current comparator provides the critical function in the controller, detecting negative voltage caused by reverse current. Gate drive is enabled when SP is 6mV higher than SN. When the SN pin is 6mV higher than the SP pin, the reverse comparator will force the gate discharge circuit to turn off the MOSFET in typically 80ns and assert the Fault ($\overline{FT}$) low to report a fault condition.

The reverse comparator will hold the gate low until the SP pin is 6mV higher than the SN pin. The reverse comparator hysteresis is shown in Figure 3.

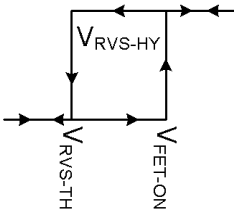


Figure 3: Reverse comparator hysteresis: V_{SP} - V_{SN}

Forward Voltage Comparator: FWD

The FWD comparator detects when a forward voltage condition exists and SP is above 275mV (typical) positive with respect to SN. When SP-SN is more than 275mV, the FWD comparator will assert the Fault ($\overline{FT}$) low to report a fault condition.

Internal Voltage Regulator:

The PI2127 control circuitry and the gate driver are biased through the S pin. An internal regulator clamps the S voltage (V_{S-PG}) to 11.7V. The internal regulator circuit has a comparator to monitor S input with respect to the PG pin and pulls the MOSFET GATE low when V_{S-PG} is lower than the Under-Voltage Threshold.

Fault Indication: $\overline{FT}$

The $\overline{FT}$ pin is an open collector NPN that will be pulled low during following fault conditions.

		Typical Condition	Indication of possible faults
1	Reverse:	V_{SP}-V_{SN} ≤ -6mV	Input supply shorted (MOSFET turned OFF)
2	Forward:	V_{SP}-V_{SN} ≥ +275mV	Open FET, Gate short, Gate open, or High current (MOSFET turned ON)
3	Forward	V_{SP}-V_{SN} ≤ +6mV	Shorted FET on power-up (MOSFET turned OFF)
4	UVLO	4.5V < V_{S-PG}<7.15V	Controller not ready (MOSFET turned OFF)

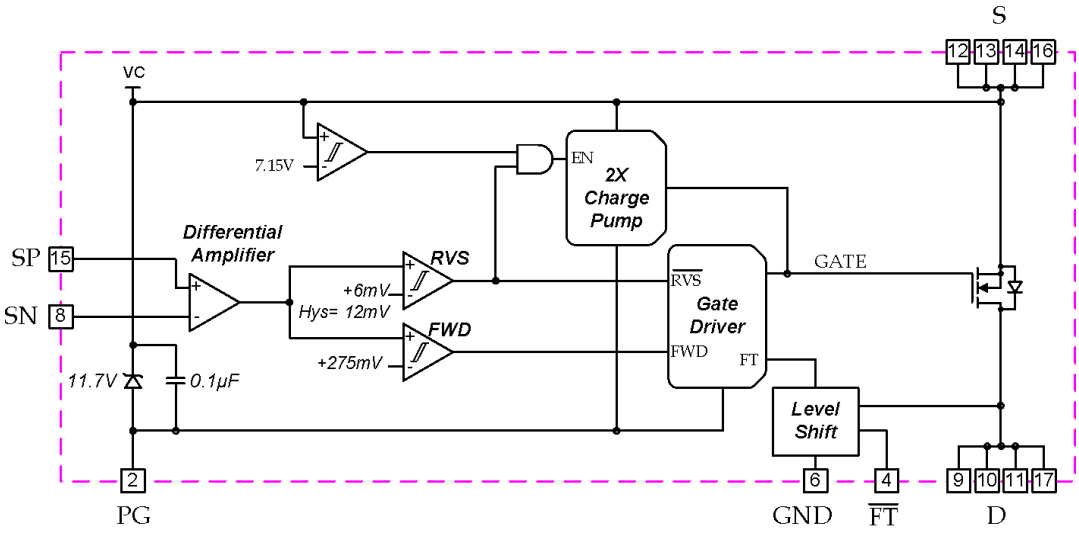


Figure 4: PI2127 Internal Block Diagram

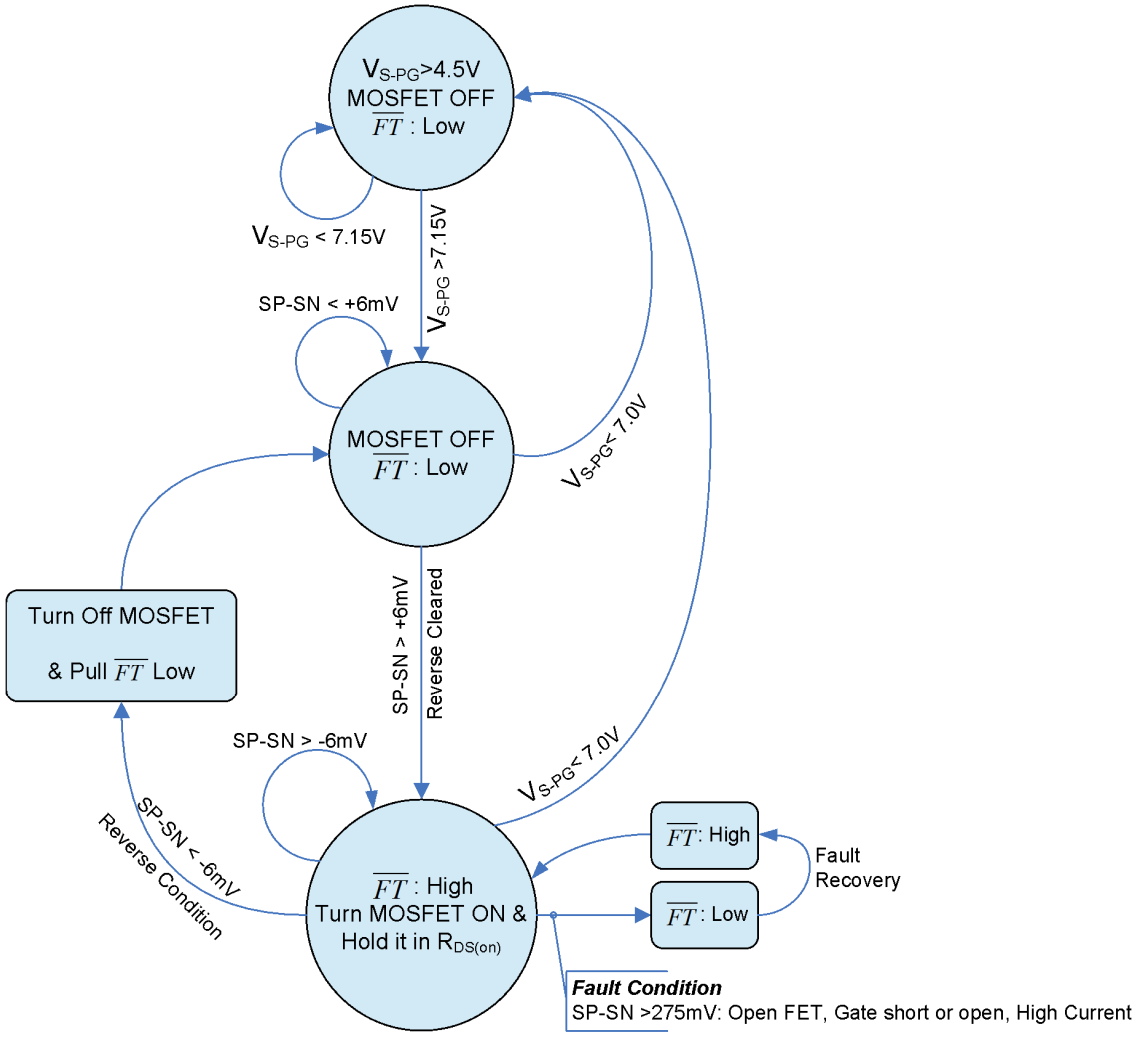


Figure 5: PI2127 State Diagram

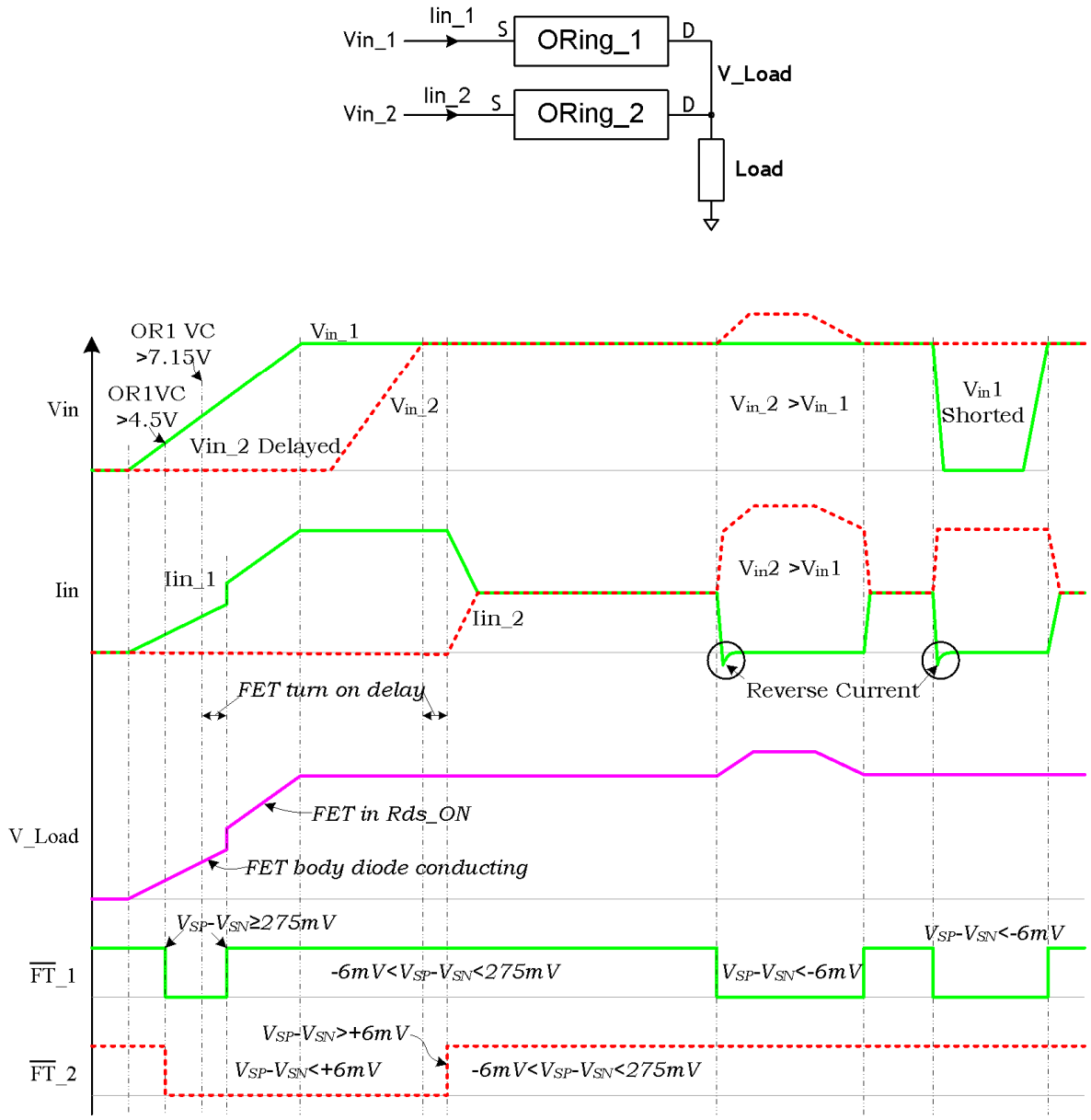


Figure 6: PI2127 Timing Diagram.

Typical Characteristics:

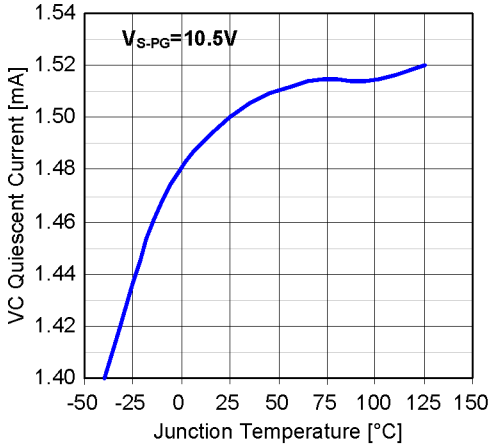


Figure 7: Controller bias current vs. temperature

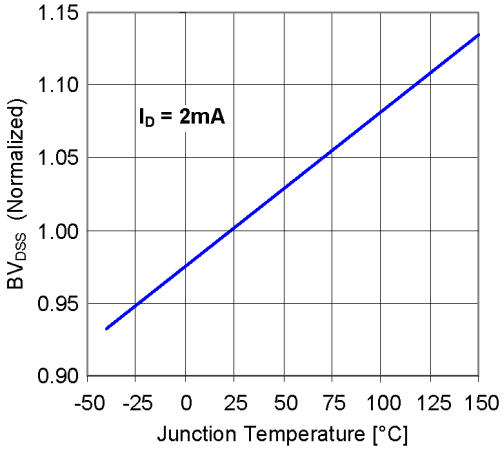


Figure 10: Internal MOSFET drain to source breakdown voltage vs. temperature.

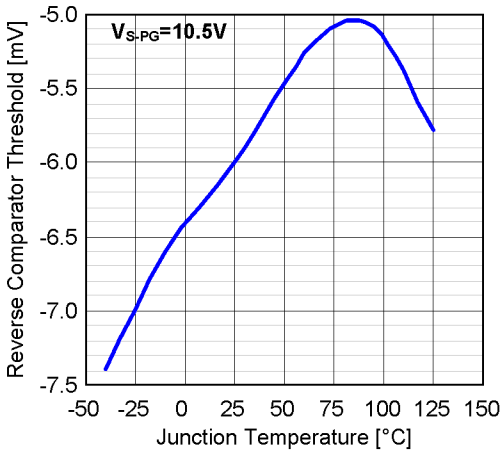


Figure 8: Reverse comparator threshold vs. temperature.

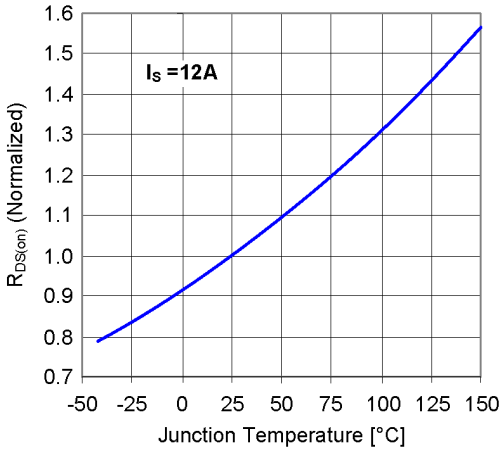


Figure 11: Internal MOSFET on-state resistance vs. temperature.

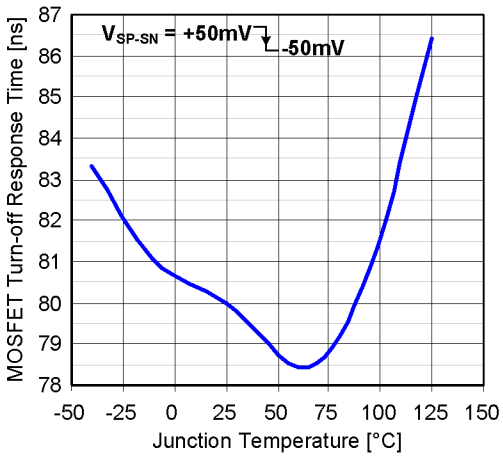


Figure 9: Reverse Fault to MOSFET Turn-off Response Time vs. temperature.

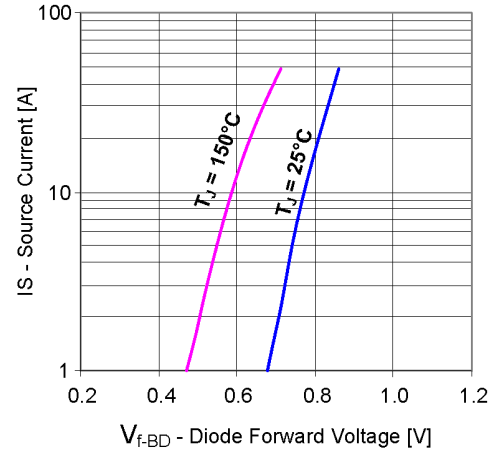


Figure 12: Internal MOSFET source to drain diode forward voltage (pulsed ≤300µs).

Thermal Characteristics:

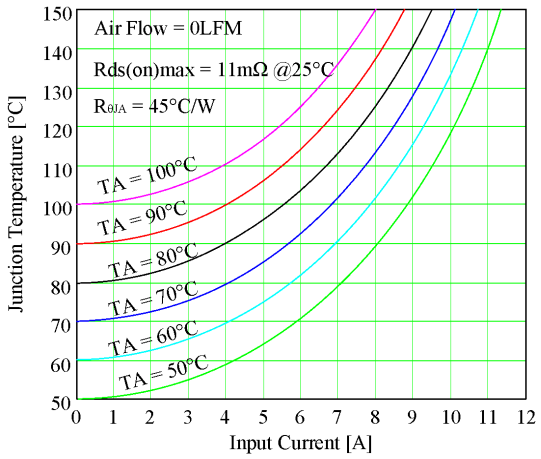


Figure 13: MOSEFT Junction Temperature vs. Input Current for a given ambient temperature (0LFM)

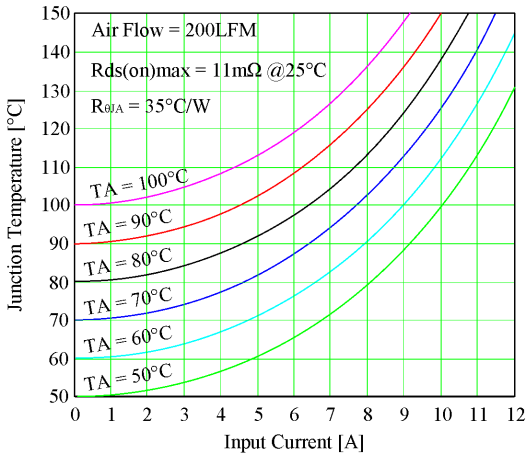


Figure 16: MOSFET Junction Temperature vs. Input Current for a given ambient temperature (200LFM)

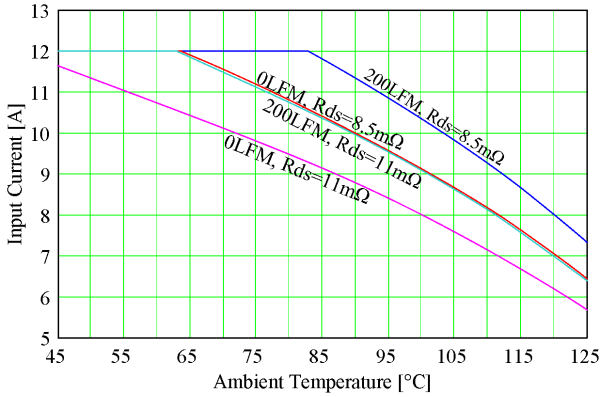


Figure 14: PI2127 input current de-rating based on the MOSFET maximum T_J=150°C vs. ambient temperature

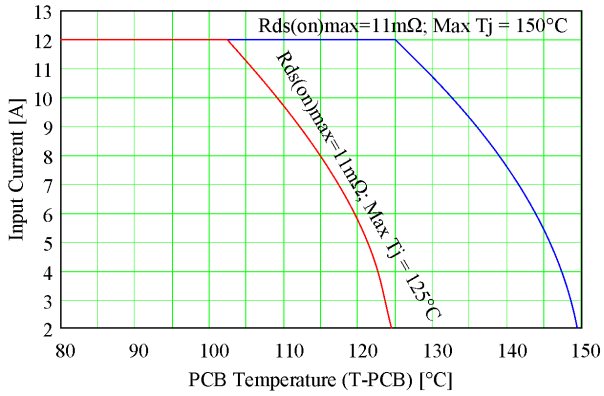


Figure 17: PI2127 input current de-rating vs. PCB temperature, for the MOSFET maximum T_J at 125°C and 150°C

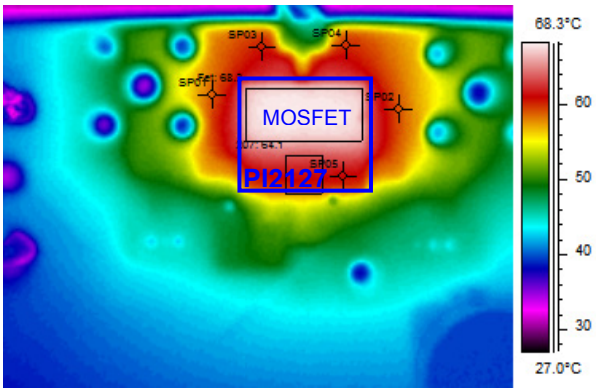


Figure 15: PI2127 mounted on PI2127-EVAL1Thermal Image picture, Iout=12A, T_A=25°C, Air Flow=0LFM

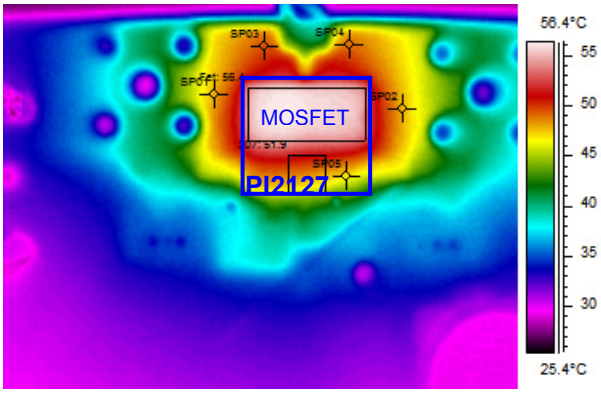


Figure 18: PI2127 mounted on PI2127-EVAL1 Thermal Image picture, Iout=10A, T_A=25°C, Air Flow=200LFM

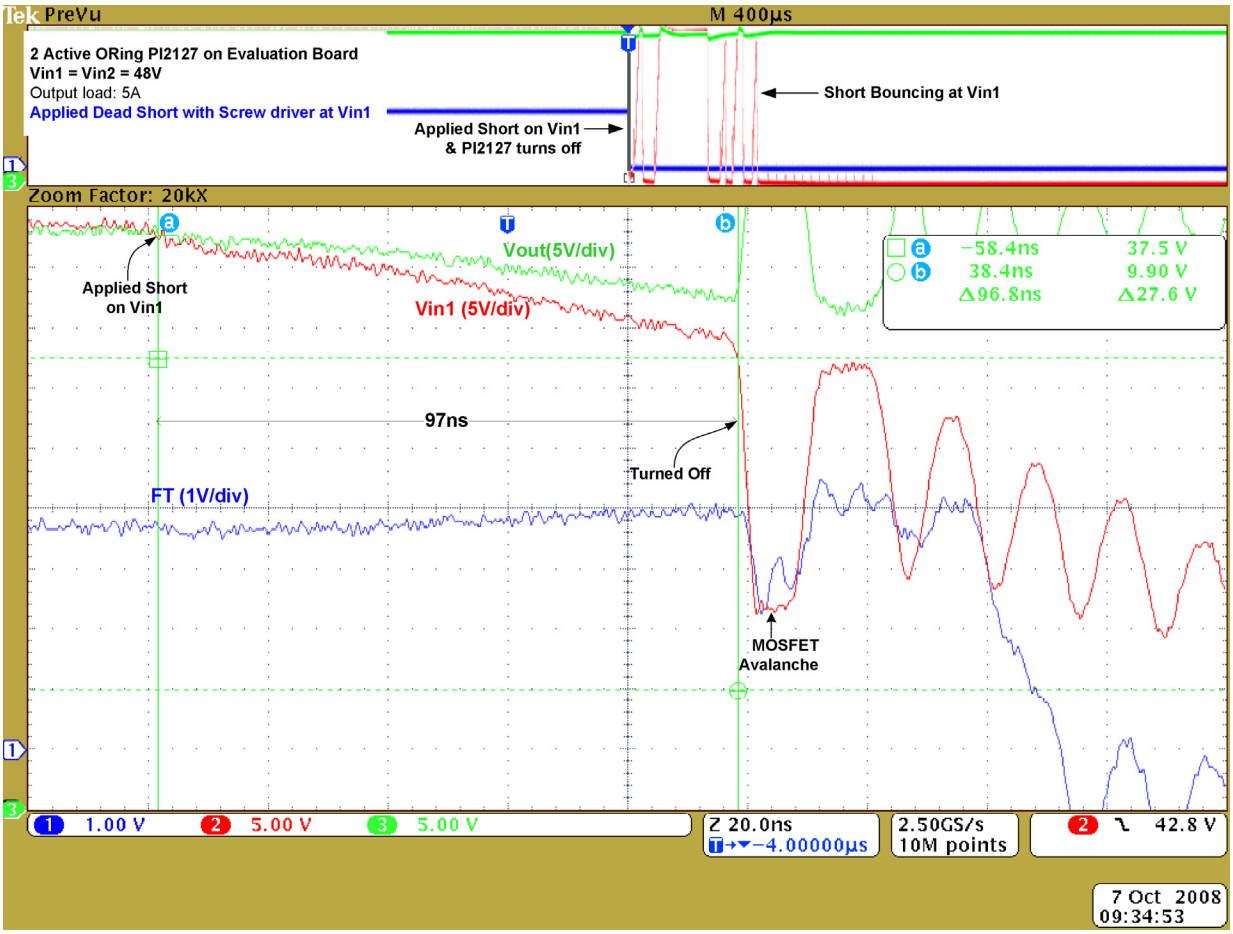


Figure 19: Plot of PI2127 response time to reverse current detection

Application Information

The PI2127 is designed to replace high side ORing diodes in high current, medium voltage redundant power architectures. Replacing a traditional diode with a PI2127 will result in significant power dissipation reduction as well as board space reduction, efficiency improvement and additional protection features.

This section describes in detail the procedure to follow when designing with the PI2127 Active ORing solution.

Control Circuitry Bias:

The PI2127 control circuitry and the gate driver for the internal MOSFET are biased through the S pin. An internal regulator clamps the S pin voltage (V_{S-PG}) to 11.7V typically.

A bias resistor (R_{PG}) is required if the voltage at the S pin is higher than the minimum Voltage Clamp (V_{S-CLM}). R_{PG} should be connected between PG pin and ground (V_S return).

Minimize the resistor value for low S voltage levels to avoid a voltage drop that may reduce V_{S-PG} lower than required.

Select the value of R_{PG} using the following equations:

$$R_{PG} = \frac{V_{S-\min} - V_{S-PGMax}}{I_{VC\max} + 0.1mA}$$

R_{PG} maximum power dissipation:

$$Pd_{RPG} = \frac{(V_{S-\max} - V_{S-PGMin})^2}{R_{PG}}$$

Where:

$V_{S-\min}$: S pin minimum applied voltage

$V_{S-\max}$: S pin maximum applied voltage

$V_{S-PGMax}$: Controller maximum clamp voltage, 12.5V

$V_{S-PGMin}$: Controller minimum clamp voltage, 11V

$I_{VC\max}$: Controller maximum bias current, use 2.0mA

$0.1mA$: 0.1mA is added for margin

Example: 40V <$V_{S\text{-}PG}$ <50V

$$R_{PG} = \frac{V_{S\min} - V_{S-PGMax}}{IC_{\max} + 0.1mA} = \frac{40V - 12.5V}{2.1mA} = 13.1k\Omega$$

$$PdR_{PG} = \frac{(V_{S-\max} - V_{S-PGMin})^2}{R_{PG}} = \frac{(50V - 11V)^2}{13.1k\Omega} = 116mW$$

Alternative Bias Circuit with Device Enable:
Constant current circuit

In a wide operating input voltage range the size of R_{PG} may be become large to support power dissipation. A simple constant current circuit can be used instead of R_{PG} to reduce power dissipation and can be used as a device enable.

As shown in Figure 20, the constant current circuit consists of an NPN transistor (Q1), Zener diode D_Z, current limit resistor (R_{LIMIT}) and Zener bias resistor (R_Z). R_{LIMIT} and R_Z can be very low power resistors and Q1 is a signal transistor where its Collector-Emitter Voltage (V_{CEO}) is equal or greater than the input operating voltage and supports 2.5mA at the operating input voltage.

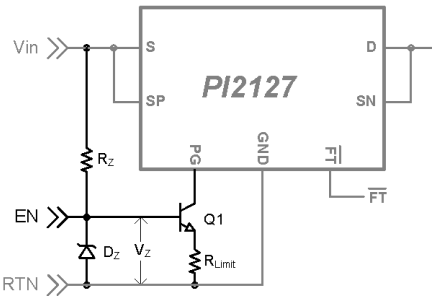


Figure 20: Constant current bias circuit

Pulling the Q1 base (EN) to the system return (RTN) will turn off the transistor and the controller return (PG pin) will float and eventually the MOSFET will be turned off. An open collector device can be used to enable and disable the PI2127.

The constant current circuit should guarantee current greater than the PI2127 maximum Quiescent current (I_{VC}), 2.0mA.

R_{LIMIT} can be calculated from the following equation:

$$R_{LIMIT} = \frac{V_{Z\_MIN} - V_{BE}(on)}{I_{VC\_MAX}}$$

Where:

V_{Z_MIN}: Minimum Zener diode voltage

$V_{BE}(on)$: Q1 Base-Emitter On maximum voltage, for default use $V_{BE}(on)$ =0.7V

Zener Diode Selection:

Select a Zener diode with a low reverse current requirement to minimize R_Z. Zener diodes with higher break down voltage will have lower reverse current and reduce Q1 collector current variation. Zener diodes with a breakdown voltage of 6V and higher will require low bias current for accurate voltage breakdown.

R_Z maximum value can be calculated with the following equation:

Note that the surface mount resistors have limited operating voltage capability. Be sure to pick a resistor package that can meet the maximum operating voltage (Vin).

$$R_Z = \frac{V_{in\_MIN} - V_{Z\_MAX}}{I_Z + I_{B\_MAX}}$$

Where:

V_{in_MIN}: Min input voltage

V_{Z_MAX}: Zener diode maximum breakdown voltage

I_Z: Zener diode required reverse current

I_{B_MAX}: Q1 required maximum base current which calculated from the following equation:

$$I_{B\_MAX} = \frac{I_{C\_MAX}}{h_{FE\_MIN}}$$

I_{C_MAX}: Q1 maximum expected collector current.

h_{FE_MIN}: Q1 minimum gain.

Internal N-Channel MOSFET BV_{DSS}:

The PI2127's internal N-Channel MOSFET breakdown voltage (BV_{DSS}) is rated for 60V at 25°C and will degrade to 55.5V at -40°C, refer to Figure 10. Drain to source voltage should not exceed BV_{DSS} in nominal operation. During a fast switching transient the MOSFET can tolerate voltages higher than its BV_{DSS} rating under avalanche conditions, refer to the Absolute Maximum Ratings table.

In Active ORing applications when one of the input power sources is shorted, a large reverse current is

sourced from the load through the MOSFET. Depending on the output impedance of the system and the parasitic inductance, the reverse current in the MOSFET may exceed the source pulsed current rating (150A) just before the PI2127 MOSFET is turned off.

The peak current during an input short condition is calculated as follows, assuming that the output has very low impedance and it is not a limiting factor:

$$I_{PEAK} = \frac{V_S * t_{RVS}}{L_{PARASITIC}}$$

Where:

I_{PEAK} : Peak current in PI2127 MOSFET before it is turned off.

V_S : Input voltage or load voltage at S pin before input short condition did occur.

t_{RVS} : Reverse fault to MOSFET turn-off time.

$L_{PARASITIC}$:Circuit parasitic inductance

The high peak current during an input short and before the MOSFET turns off, stores energy in the circuit parasitic inductance, and as soon as the MOSFET turns off, the stored energy will be released and this will produce a high negative voltage and ringing at the MOSFET source. At the same time the energy stored at the drain side of the internal MOSFET will be released and produce a voltage higher than the load voltage. This event will create a high voltage difference between the drain and source of the MOSFET. ***The MOSFET will avalanche, but this avalanche will not affect the MOSFET performance because the PI2127 has a fast response time to the input fault condition and the stored energy will be well below the MOSFET avalanche capability***.

MOSFET avalanche during input short is calculated as follows:

$$E_{AS} = \frac{1}{2} * \frac{1.3 * BV_{DSS}}{1.3 * BV_{DSS} - V_S} * L_{PARASITIC} * I_{PEAK}{}^2$$

Where:

E_{AS} : Avalanche energy

BV_{DSS} : MOSFET breakdown voltage (60V)

Power dissipation:

In Active ORing circuits the MOSFET is always on in steady state operation and the power dissipation is derived from the total source current and the on-state resistance of the MOSFET.

The PI2127 internal MOSFET power dissipation can be calculated with the following equation:

$$Pd_{MOSFET} = Is^2 * R_{DS(on)}$$

Where:

Is: Source Current

Pd_{MOSFET} :MOSFET power dissipation

$R_{DS(on)}$: MOSFET on-state resistance

Note: For the worst case condition, calculate with maximum rated $R_{DS(on)}$ at the MOSFET maximum operating junction temperature because $R_{DS(on)}$ is temperature dependent. Refer to Figure 11 for normalized $R_{DS(on)}$ values over temperature. The PI2127 maximum $R_{DS(on)}$ at 25°C is 11mΩ and will increase by 43% at 125°C junction temperature.

The Junction Temperature rise is a function of power dissipation and thermal resistance.

$$Trise = R_{\theta JA} * Pd_{MOSFET} = R_{\theta JA} * Is^2 * R_{DS(on)}$$

Where:

$R_{\theta JA}$: Junction-to-Ambient thermal resistance (45°C/Watt)

This may require iteration to get to the final junction temperature. Figure 13 and Figure 16 show the PI2127 internal MOSFET final junction temperature curves versus conducted current at maximum $R_{DS(on)}$, given ambient temperatures and air flow.

Fault Circuit:

$\overline{FT}$ is an open collector pin and should be pulled up to the logic voltage via a resistor (10KΩ).
An internal level shift circuit is implemented to change the PI2127 controller fault output reference from the PG pin voltage level to the GND pin voltage level. The level shift circuit is biased from the D pin to stay active when the bias voltage at S pin is not available. In the event of an input short fault condition, the S pin will be pulled low (ground) and the PI2127 control circuit will lose its bias voltage. If the output voltage is supplied from a redundant source, then the level shifter stays biased and the $\overline{FT}$ pin will be pulled low to indicate that the MOSFET is in the OFF condition.

During start-up and before the output voltage is established, the $\overline{FT}$ pin will be floating until the approximately 4.5V is present at the S pin or at D pin. Thereafter the $\overline{FT}$ pin is pulled low and stays low until the PI2127 controller bias voltage V_{S-PG} increases above the controller Under-Voltage Threshold (V_{SUVR}) and no fault conditions are present. Once this

happens, the MOSFET is turned on and the $\overline{FT}$ pin will be high resistance to indicate that the MOSFET is in $R_{DS(on)}$ with no fault conditions existing.

Note that in case of an input fault condition, where the S pin is at ground and the output (D pin and SN pin) are at a high voltage there will be two current paths, one path from D pin to GND and the other path from SN pin to SP.

The current path from D pin to GND and S pins is due to the level shift circuit and will draw current from the output as a function of the voltage between D pin and GND (V_{D-GND}) based on the following equation:

$$I_{D-FLT} = \frac{V_{D-GND} - 0.5V}{15k\Omega}$$

Where:

I_{D-FLT}: Maximum D pin current during input short fault condition

V_{D-GND}: Voltage difference between the D pin and ground.

The current path from SN pin to S pin is a function of the SN voltage based on the following equation:

$$I_{SN\_FLT} = \frac{V_{SN-GND} - 12V}{R_{PAR}}$$

Where:

I_{SN_FLT}: SN current during input short fault condition

V_{SN-GND}: Voltage difference between SN pin (or load voltage) and ground.

R_{PAR}: Resistance of the internal path, 10KΩ typical and 8kΩ minimum

The level shift circuit worst case power dissipation during input short is:

$$Pd = \frac{(V_{D-GND} - 0.5V)^2}{15k\Omega}$$

The thermal resistance and power dissipation of the level shift circuit will limit the voltage applied at the D pin during a shorted input condition. When the PCB temperature exceeds 110°C, the applied voltage must be derated according to Figure 21. The plot in Figure 21 is calculated using the worst case power dissipation during an input short with $R_{\theta J-PCB}$= 100°C/W.

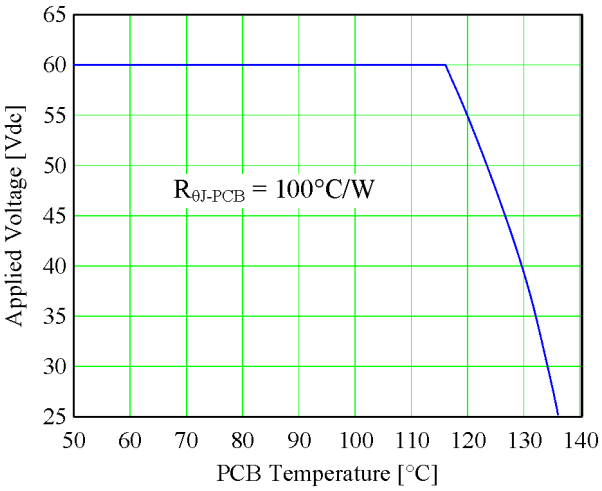


Figure 21: Level shift circuit applied voltage de-rating (valid during an input short fault condition as a function of PCB Temperature)

Typical Application Example:

Requirement:

Redundant Bus Voltage = 40V ±5V

Maximum Load Current = 9A (assume through each redundant path)

Maximum Ambient Temperature = 60°C, no air flow (0LFM)

The current flow parasitic inductance for each ORing device is 60nH.

Solution:

A single PI2127 for each redundant 40V power source should be used, configured as shown in the circuit schematic in Figure 23.

R_{PG} selection:

35V <$V_{S\text{-}PG}$ <45V

$$R_{PG} = \frac{V_{S\min} - V_{S-PGMax}}{IC_{\max} + 0.1mA} = \frac{35V - 12.5V}{2.1mA} = 10.71k\Omega$$

The closest 1% resistor available is 10.5kΩ

$$PdR_{PG} = \frac{(V_{S-\max} - V_{S-PGMin})^2}{R_{PG}} = \frac{(45V - 11V)^2}{10.5k\Omega} = 110mW$$

The selected resistor should be capable of supporting the total power at maximum operating temperature, 60°C. An 0805 (2012) will support the power requirement.

$\overline{FT}$ pin:

Connect $\overline{FT}$ pin to the logic input and to the logic power supply via a resistor, as required for the proper input level of the supervisor functions.

Power Dissipation and Junction Temperature:

First use Figure 13 (Junction Temperature vs. Input Current) to find the final junction temperature for 9A load current at 60°C ambient temperature. In Figure 13 (illustrated in Figure 22) draw a vertical line from 9A to intersect the 60°C ambient temperature line. At the intersection draw a horizontal line towards the Y-axis (Junction Temperature). The Junction Temperature at maximum load current (9A) and 60°C ambient is 115°C.

$R_{DS(on)}$ is 11mΩ maximum at 25°C and will increase as the Junction temperature increases. From Figure 11, at 115°C $R_{DS(on)}$ will increase by 38%, then

$R_{DS(on)} = 11m\Omega * 1.38 = 15.18m\Omega$ maximum at 115°C

Maximum power dissipation is:

$$Pd_{\max} = Iin^2 * R_{DS(on)} = (9A)^2 * 15.18m\Omega = 1.23W$$

Recalculate T_J:

$$T_{J\max} = 60°C + \left(\frac{45°C}{W} * (9A)^2 * 15.18m\Omega\right) = 115.3°C$$

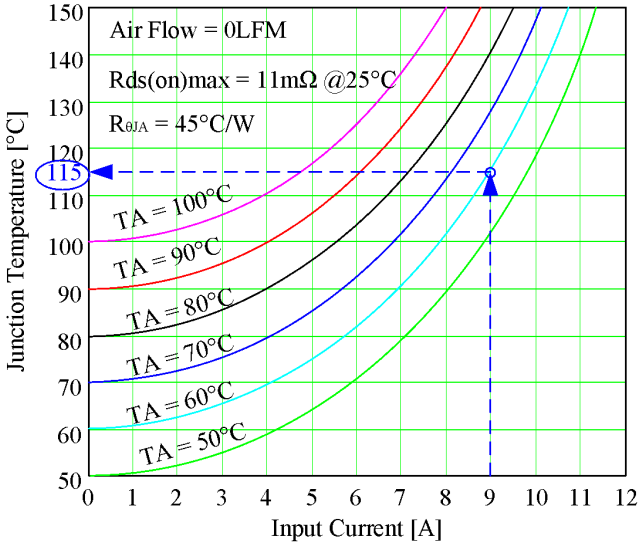


Figure 22: Example 1 final MOSFET junction temperature at 9A/60°C T_A

Reverse Current Threshold:

The following procedure demonstrates how to calculate the minimum required reverse current in the internal MOSFET to generate a reverse fault condition and turn off the internal MOSFET.

At maximum junction temperature (115°C) and maximum $R_{DS(on)}$:

$$Is.reverse = \frac{V_{RVS-TH}}{R_{DS(on)}} = \frac{-6mV}{15.18m\Omega} = -395mA$$

Peak current under input short is:

At typical response time:

$$I_{PEAK} = \frac{V_S * t_{RVS}}{L_{PARASITIC}} = \frac{45V * 80ns}{60nH} = 60A$$

At maximum response time:

$$I_{PEAK} = \frac{V_S * t_{RVS}}{L_{PARASITIC}} = \frac{45V * 150ns}{60nH} = 112.5A$$

Avalanche Energy:

$$E_{AS} = \frac{1}{2} * \frac{1.3 * BV_{DSS}}{1.3 * BV_{DSS} - V_S} * L_{PARASITIC} * I_{PEAK}{}^2$$

$$E_{AS} = \frac{1}{2} * \frac{1.3 * 60}{1.3 * 60V - 45V} * 60nH * 112.5A^2 = 897\mu J$$

The avalanche energy is well below the total MOSFET specified peak current of 150A for 300ns and below the rated avalanche energy. The specified energy can be calculated from Single Pulse Avalanche Current as specified in the Absolute Maximum Ratings table:

$$\frac{1}{2} \cdot 1.3 * BV_{DSS} \cdot I_{AS} \cdot t_{AV} = \frac{1}{2} 1.3 \cdot 60V \cdot 33A \cdot 11\mu s = 14mJ$$

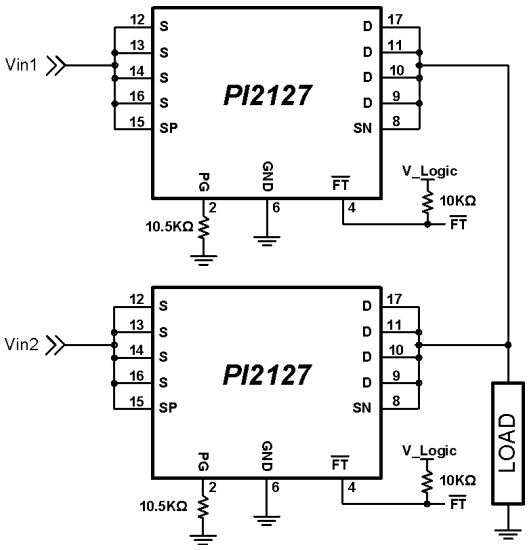


Figure 23 : Two PI2127 in High Side ORing configuration

VC bias through Constant current circuit

Select an NPN transistor with V_{CEO} equal or higher than the input voltage (Vin) plus any expected transient voltage and capable of handling the expected maximum power dissipation. Any NPN transistor with V_{CEO} ≥ 60V in a small footprint is suitable. An exemplary NPN is the BC846 from NXP Semiconductors:

From the BC846 datasheet:

NPN general-purpose transistor
V_{CEO} = 65V Collector-Emitter maximum voltage
I_C = 100mA maximum collector current
h_{FE} = 110 minimum at I_C=2mA
V_{BE} = 0.580V to 0.70V Base-Emitter voltage at I_C = 2mA and 25°C
$R_{\theta J-A}$ = 500°C/W Junction to ambient thermal resistance.

Select Zener Diode: A Zener diode with low bias current and V_Z=10 in small foot print is suitable for this application. An exemplary Zener diode is the MM3Z10VST1 the from ON Semiconductor

From the MM3Z10VST1 datasheet:
10V, 200mW Zener Diode
V_Z = 9.80V to 10.2V Zener voltage range
I_R = 10µA will hold the Zener breakdown voltage at 9.8V

$$R_{LIMIT} = \frac{V_{Z\_MIN} - V_{BE}(on)}{I_{VC\_MAX}} = \frac{9.8V - 0.7V}{2.1mA} = 4.33k\Omega$$

Or 4.32kΩ 1%

$$I_{B\_MAX} = \frac{I_{C\_MAX}}{h_{FE\_MIN}} = \frac{3mA}{110} = 27.27\mu A$$

R_Z Calculation:

Use 120µA as minimum for the Zener diode reverse leakage current and Q2 base current combined.

$$R_Z = \frac{V_{in\_MIN} - V_{Z\_MAX}}{I_Z + I_{B\_MAX}} = \frac{40V - 10.2V}{120\mu A} = 248k\Omega$$

Select R_Z= 249kΩ 1%

Maximum Q1 collector current:

$$I_{C\_MAX} = \frac{V_{Z\_MAX} - V_{BE\_MIN}}{R_{LIMIT\_MIN}} = \frac{10.2V - 0.50V}{4.32k\Omega * 0.98} = 2.29mA$$

Maximum Q2 power dissipation

$$Pd_{Q1} = I_{C\_MAX} * [Vin_{MAX} - V_{VC-CLM} - (V_{Z\_MIN} - V_{EB\_MAX})]$$

$$Pd_{Q1} = 2.29mA * [45V - 11V - (9.8V - 0.7V)] = 57mW$$

Transistor temperature rise

$$T_{RISEQ1} = Pd_{Q1} * R_{\theta J-A} = 57mW * 500\frac{°C}{W} = 28.50°C$$

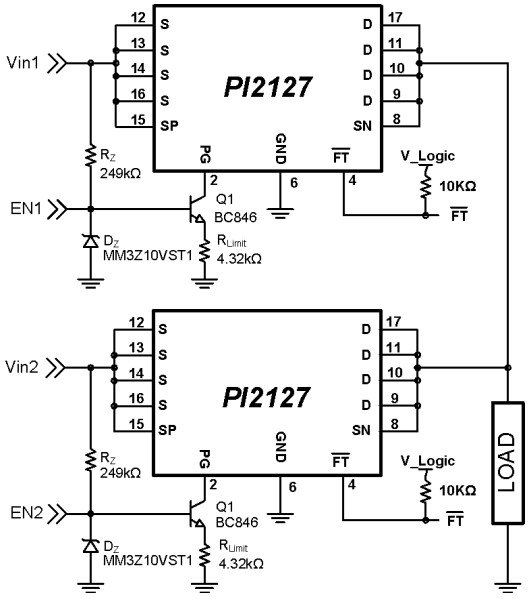


Figure 24: PI2127 in high side +48V application, VC is biased through constant current circuit.

Layout Recommendation:

Use the following general guidelines when designing printed circuit boards. An example of the typical land pattern for the PI2127 is shown in Figure 25:

- Make sure to have a solid ground (return) plane to reduce circuit parasitic.
- Connect all S pads together with a wide trace to reduce trace parasitics to accommodate the high current input, and also connect all D pads together with a wide trace to accommodate the high current output.
- Connect the SP pin to the S pins and connect the SN pin to D pins as shown in Figure 25.
- Use 1oz of copper or thicker if possible to reduce trace resistance and reduce power dissipation.

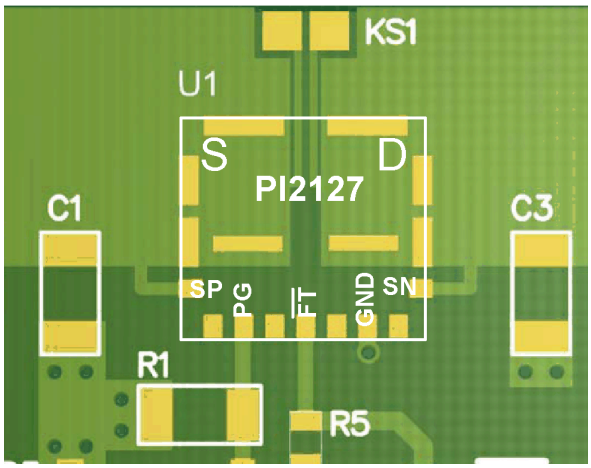
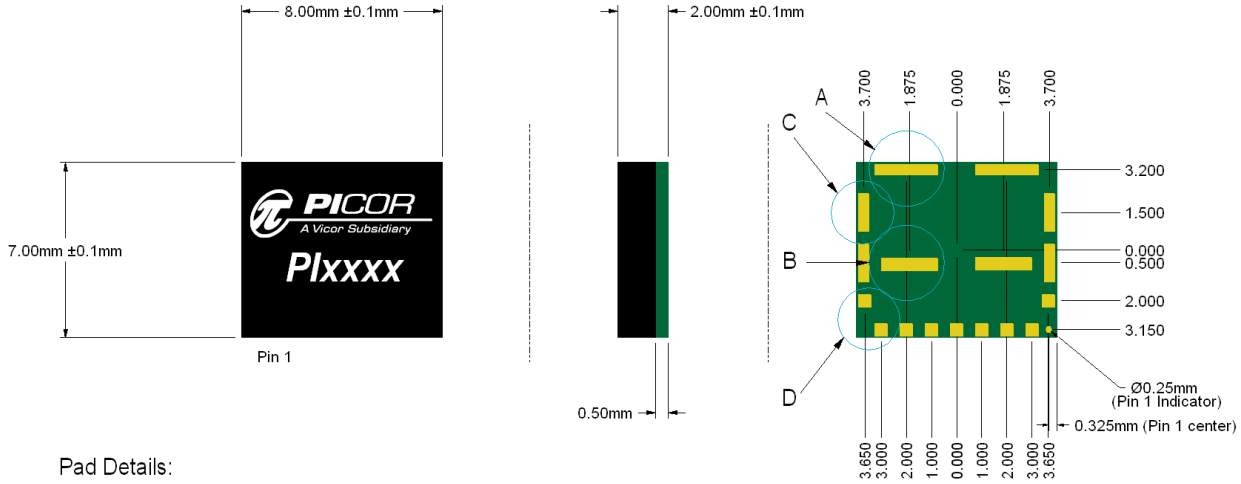
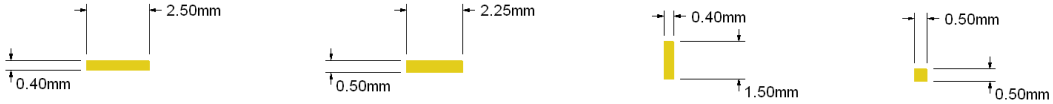


Figure 25: PI2127 layout recommendation

Package Drawing:



Pad Details:
Pad D is copper defined, all others are soldermask defined.

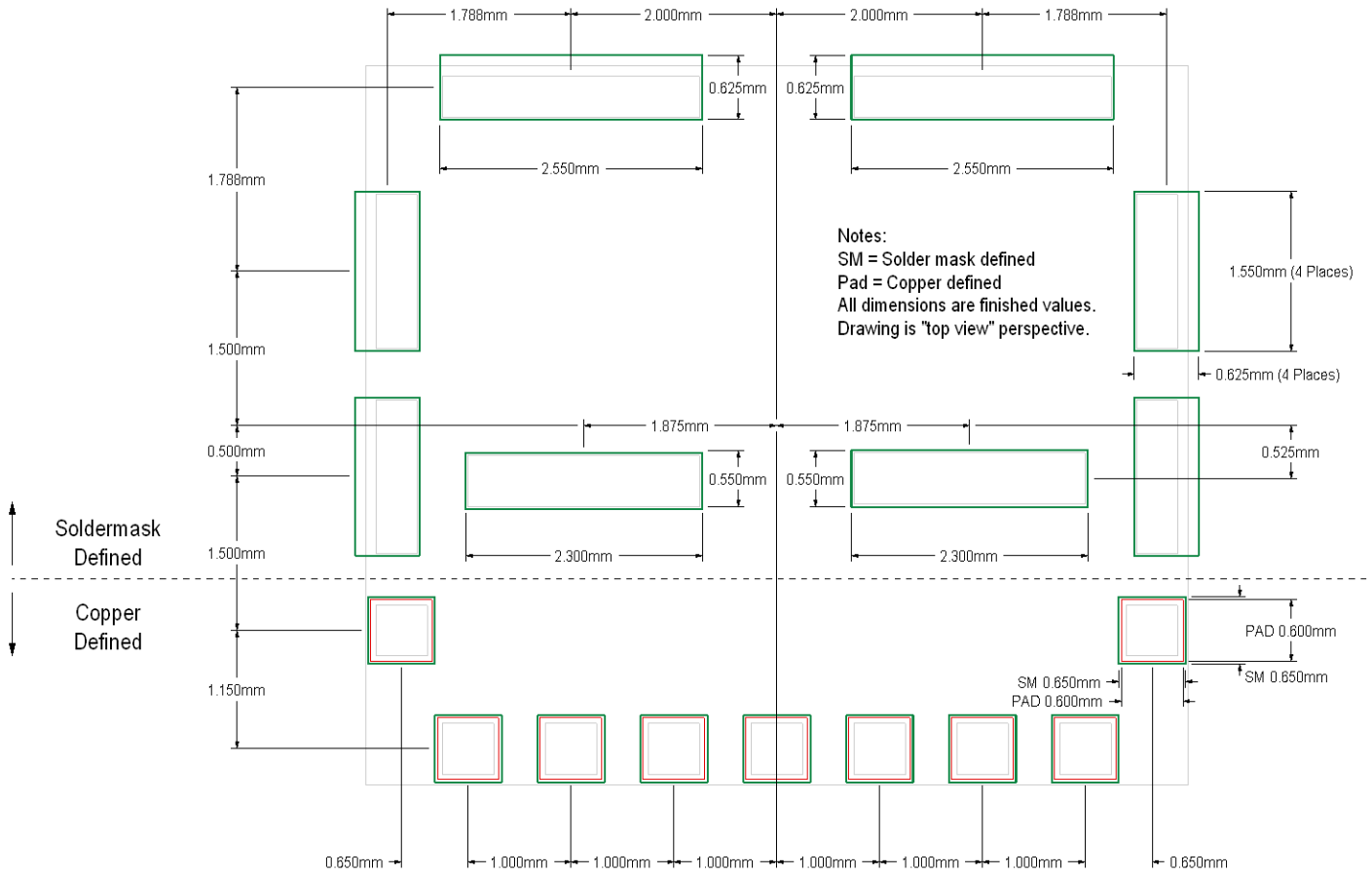


Pad A: (2 Places) Pad B: (2 Places) Pad C: (4 Places) Pad D: (9 Places)

Ordering Information

Part Number	Package	Transport Media
PI2127-01-LGIZ	7mm x 8mm 17-pin LGA	T&R

Footprint Recommendation:



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