EVALUATION KIT AVAILABLE

DS1856

Dual, Temperature-Controlled Resistors with Internally Calibrated Monitors and Password Protection

General Description

The DS1856 dual, temperature-controlled, nonvolatile (NV) variable resistors with three monitors consists of two 256-position, linear, variable resistors; three analog monitor inputs (MON1, MON2, MON3); and a direct-to-digital temperature sensor. The device provides an ideal method for setting and temperature-compensating bias voltages and currents in control applications using minimal circuitry. The variable resistor settings are stored in EEPROM memory and can be accessed over the 2-wire serial bus.

Relative to other members of the family, the DS1856 is essentially a DS1859 with a DS1852-friendly memory map. In particular, the DS1856 can be configured so the 128 bytes of internal Auxiliary EEPROM memory is mapped into Main Device Table 00h and Table 01h, maintaining compatibility between both the DS1858/DS1859 and the DS1852. The DS1856 also features password protection equivalent to the DS1852, further enhancing compatibility between the two.

Applications

Optical Transceivers

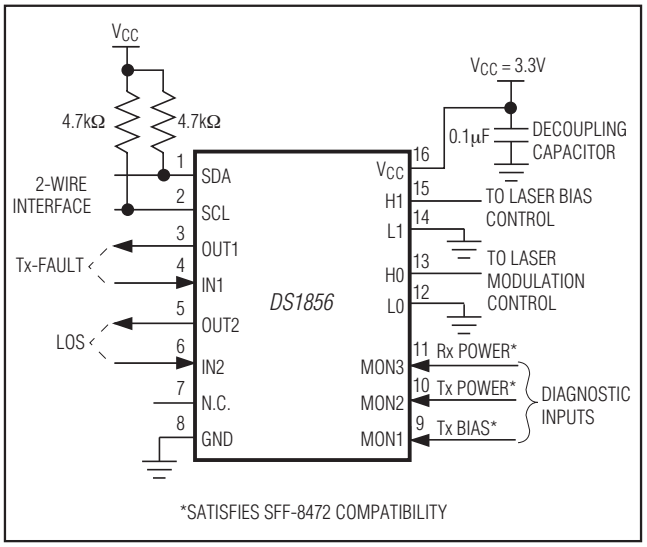
Optical Transponders

Instrumentation and Industrial Controls

RF Power Amps

Diagnostic Monitoring

Typical Operating Circuit



Visit www.maximintegrated.com/products/patents for product patent marking information.

Features

- **SFF-8472 Compatible**
- **Five Monitored Channels (Temperature, VCC, MON1, MON2, MON3)**
- **Three External Analog Inputs (MON1, MON2, MON3) That Support Internal and External Calibration**
- **Scalable Dynamic Range for External Analog Inputs**
- **Internal Direct-to-Digital Temperature Sensor**
- **Alarm and Warning Flags for All Monitored Channels**
- **Two Linear, 256-Position, Nonvolatile Temperature-Controlled Variable Resistors**
- **Resistor Settings Changeable Every 2°C**
- **Three Levels of Security**
- **Access to Monitoring and ID Information Configurable with Separate Device Addresses**
- **2-Wire Serial Interface**
- **Two Buffers with TTL/CMOS-Compatible Inputs and Open-Drain Outputs**
- **Operates from a 3.3V or 5V Supply**
- **-40°C to +95°C Operating Temperature Range**

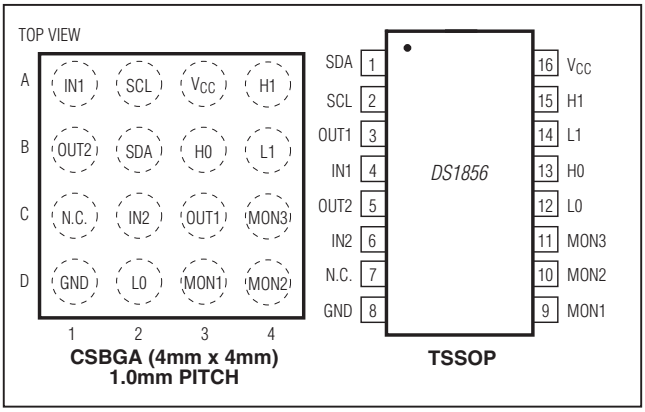
Ordering Information

PART	RES0/RES1 RESISTANCE (kΩ)	PIN-PACKAGE
DS1856E-050	50/50	16 TSSOP
DS1856E-050/T&R	50/50	16 TSSOP
DS1856B-050	50/50	16 CSBGA

Ordering Information continued at end of data sheet.

+Denotes lead-free package.
T&R denotes tape-and-reel package.
Note: *All devices are specified over the -40°C to +95°C temperature range.*

Pin Configurations



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

Rev 1; 2/06

ABSOLUTE MAXIMUM RATINGS

Voltage Range on V_{CC} Relative to Ground .....-0.5V to +6.0V
Voltage Range on Inputs Relative to Ground*.....-0.5V to (V_{CC} + 0.5V)
Voltage Range on Resistor Inputs Relative to Ground*.....-0.5V to (V_{CC} + 0.5V)
Current into Resistors.....5mA

Operating Temperature Range .....-40°C to +95°C
Programming Temperature Range .....0°C to +70°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature .....See IPC/JEDEC J-STD-020A

**Not to exceed 6.0V.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 1)	2.85		5.50	V
Input Logic 1 (SDA, SCL)	V_{IH}	(Note 2)	0.7 x Vcc		V_{CC} + 0.3	V
Input Logic 0 (SDA, SCL)	V_{IL}	(Note 2)	-0.3		+0.3 x V_{CC}	V
Resistor Inputs (L0, L1, H0, H1)			-0.3		V_{CC} + 0.3	V
Resistor Current	I_{RES}		-3		+3	mA
High-Impedance Resistor Current	I_{ROFF}			0.001	0.1	µA
Input Logic Levels (IN1, IN2)		Input logic 1	1.6			V
		Input logic 0			0.9	

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.85V to 5.5V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	(Note 3)		1	2	mA
Input Leakage	I_{IL}		-200		+200	nA
Low-Level Output Voltage (SDA, OUT1, OUT2)	V_{OL1}	3mA sink current	0		0.4	V
	V_{OL2}	6mA sink current	0		0.6	
Full-Scale Input (MON1, MON2, MON3)		At factory setting (Note 4)	2.4875	2.5	2.5125	V
Full-Scale V_{CC} Monitor		At factory setting (Note 5)	6.5208	6.5536	6.5864	V
I/O Capacitance	$C_{I/O}$				10	pF
Digital Power-On Reset	POD		1.0		2.2	V
Analog Power-On Reset	POA		2.0		2.6	V

ANALOG RESISTOR CHARACTERISTICS

(V_{CC} = 2.85V to 5.5V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Position 00h Resistance (50kΩ)	T_A = +25°C	0.65	1.0	1.35	kΩ
Position FFh Resistance (50kΩ)	T_A = +25°C	40	50	60	kΩ
Position 00h Resistance (30kΩ)	T_A = +25°C	0.165	0.275	0.400	kΩ
Position FFh Resistance (30kΩ)	T_A = +25°C	22.5	30	37.5	kΩ
Position 00h Resistance (20kΩ)	T_A = +25°C	0.20	0.40	0.55	kΩ
Position FFh Resistance (20kΩ)	T_A = +25°C	15	20	25	kΩ
Position 00h Resistance (10kΩ)	T_A = +25°C	0.075	0.125	0.200	kΩ
Position FFh Resistance (10kΩ)	T_A = +25°C	7.5	10	12.5	kΩ
Position 00h Resistance (2.5kΩ)	T_A = +25°C	0.1	0.175	0.250	kΩ
Position FFh Resistance (2.5kΩ)	T_A = +25°C	2.0	2.50	3.0	kΩ
Absolute Linearity	(Note 6)	-2		+2	LSB
Relative Linearity	(Note 7)	-1		+1	LSB
Temperature Coefficient	(Note 8)		50		ppm/°C

ANALOG VOLTAGE MONITORING

(V_{CC} = 2.85V to 5.5V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Resolution	ΔVMON			610		µV
Supply Resolution	ΔV_{CC}			1.6		mV
Input/Supply Accuracy (MON1, MON2, MON3, V_{CC})	A_{CC}	At factory setting		0.25	0.5	% FS (full scale)
Update Rate for MON1, MON2, MON3, Temp, or V_{CC}	t_{frame}			47	60	ms
Input/Supply Offset (MON1, MON2, MON3, V_{CC})	V_{OS}	(Note 14)		0	5	LSB

DIGITAL THERMOMETER

(V_{CC} = 2.85V to 5.5V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Thermometer Error	T_{ERR}	-40°C to +95°C			±3.0	°C

NONVOLATILE MEMORY CHARACTERISTICS

(V_{CC} = 2.85V to 5.5V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EEPROM Writes		+70°C (Note 14)	50,000			Writes

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.85V to 5.5V, T_A = -40°C to +95°C, unless otherwise noted. See Figure 6.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency (Note 9)	f_{SCL}	Fast mode	0		400	kHz
		Standard mode	0		100	
Bus Free Time Between STOP and START Condition (Note 9)	t_{BUF}	Fast mode	1.3			µs
		Standard mode	4.7			
Hold Time (Repeated) START Condition (Notes 9, 10)	$t_{HD:STA}$	Fast mode	0.6			µs
		Standard mode	4.0			
LOW Period of SCL Clock (Note 9)	t_{LOW}	Fast mode	1.3			µs
		Standard mode	4.7			
HIGH Period of SCL Clock (Note 9)	t_{HIGH}	Fast mode	0.6			µs
		Standard mode	4.0			
Data Hold Time (Notes 9, 11, 12)	$t_{HD:DAT}$	Fast mode	0		0.9	µs
		Standard mode	0			
Data Setup Time (Note 9)	$t_{SU:DAT}$	Fast mode	100			ns
		Standard mode	250			
START Setup Time (Note 9)	$t_{SU:STA}$	Fast mode	0.6			µs
		Standard mode	4.7			
Rise Time of Both SDA and SCL Signals (Note 13)	t_R	Fast mode	$20 + 0.1C_B$		300	ns
		Standard mode	$20 + 0.1C_B$		1000	
Fall Time of Both SDA and SCL Signals (Note 13)	t_F	Fast mode	$20 + 0.1C_B$		300	ns
		Standard mode	$20 + 0.1C_B$		300	
Setup Time for STOP Condition	$t_{SU:STO}$	Fast mode	0.6			µs
		Standard mode	4.0			
Capacitive Load for Each Bus Line	C_B	(Note 13)			400	pF
EEPROM Write Time	t_W			10	20	ms

Note 1: All voltages are referenced to ground.

Note 2: I/O pins of fast-mode devices must not obstruct the SDA and SCL lines if V_{CC} is switched off.

Note 3: SDA and SCL are connected to V_{CC} and all other input signals are connected to well-defined logic levels.

Note 4: Full scale is user programmable. The maximum voltage that the MON inputs read is approximately full scale, even if the voltage on the inputs is greater than full scale.

Note 5: This voltage defines the maximum range of the analog-to-digital converter voltage, not the maximum V_{CC} voltage.

Note 6: Absolute linearity is the difference of measured value from expected value at DAC position. The expected value is a straight line from measured minimum position to measured maximum position.

Note 7: Relative linearity is the deviation of an LSB DAC setting change vs. the expected LSB change. The expected LSB change is the slope of the straight line from measured minimum position to measured maximum position.

Note 8: See the *Typical Operating Characteristics*.

Note 9: A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT}$ > 250ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{RMAX} + t_{SU:DAT}$ = 1000ns + 250ns = 1250ns before the SCL line is released.

Note 10: After this period, the first clock pulse is generated.

Note 11: The maximum $t_{HD:DAT}$ only has to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

Note 12: A device must internally provide a hold time of at least 300ns for the SDA signal (see the $V_{IH\ MIN}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.

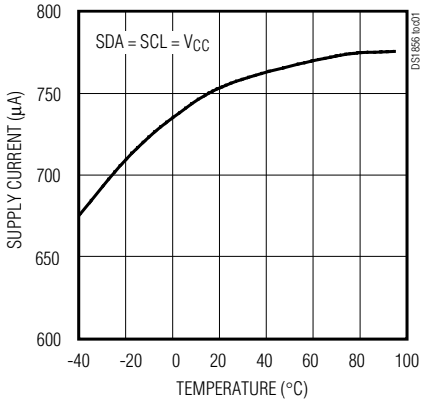
Note 13: C_B—total capacitance of one bus line, timing referenced to 0.9 x V_{CC} and 0.1 x V_{CC}.

Note 14: Guaranteed by design.

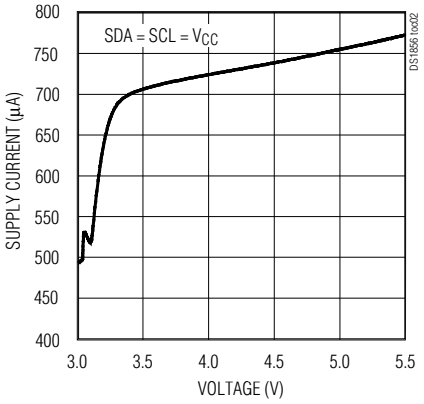
Typical Operating Characteristics

(V_{CC} = 5.0V, T_A = +25°C, for both 50kΩ and 20kΩ versions, unless otherwise noted.)

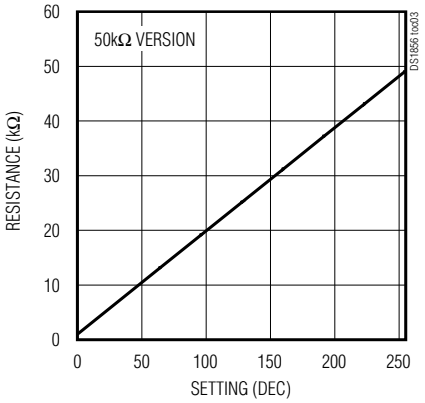
SUPPLY CURRENT vs. TEMPERATURE



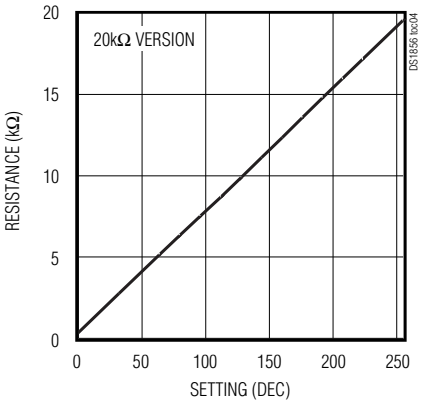
SUPPLY CURRENT vs. VOLTAGE



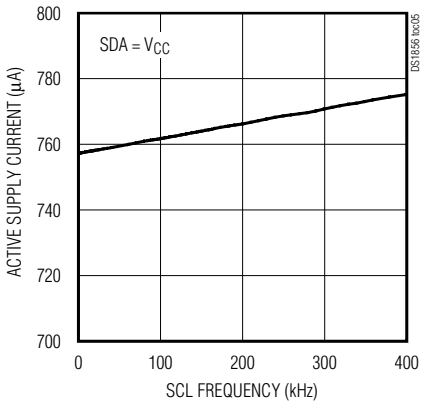
RESISTANCE vs. SETTING



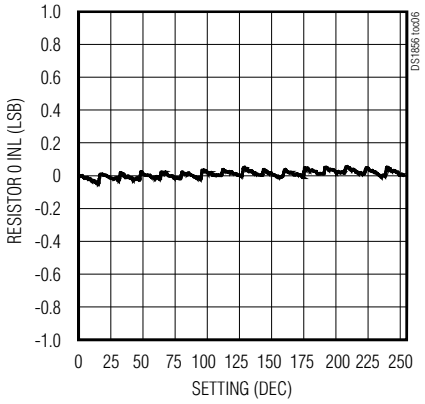
RESISTANCE vs. SETTING



ACTIVE SUPPLY CURRENT vs. SCL FREQUENCY



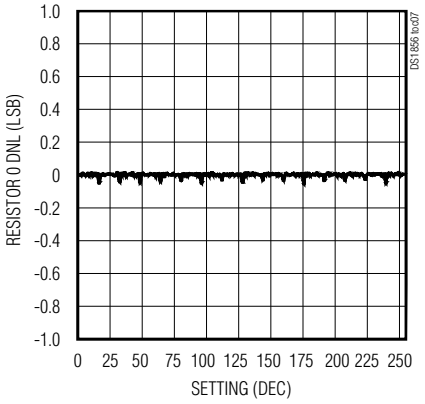
RESISTOR 0 INL (LSB)



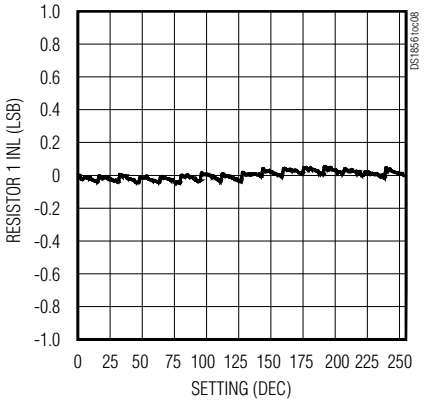
Typical Operating Characteristics (continued)

(V_{CC} = 5.0V, T_A = +25°C, for both 50kΩ and 20kΩ versions, unless otherwise noted.)

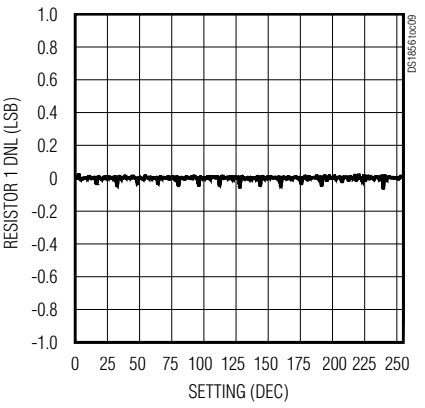
RESISTOR 0 DNL (LSB)



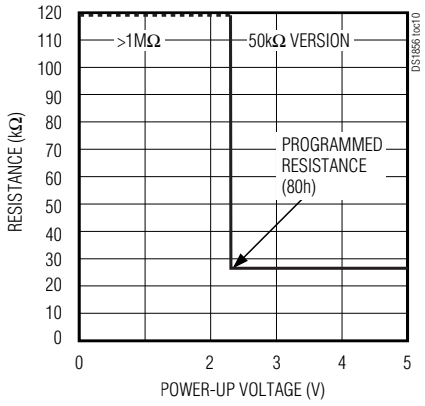
RESISTOR 1 INL (LSB)



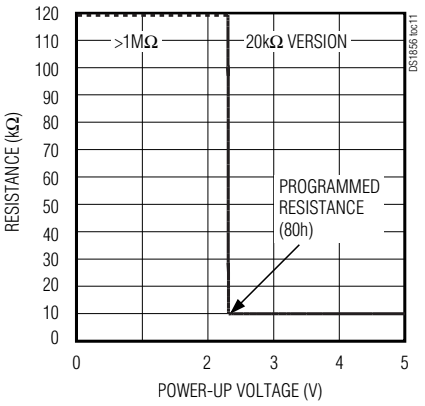
RESISTOR 1 DNL (LSB)



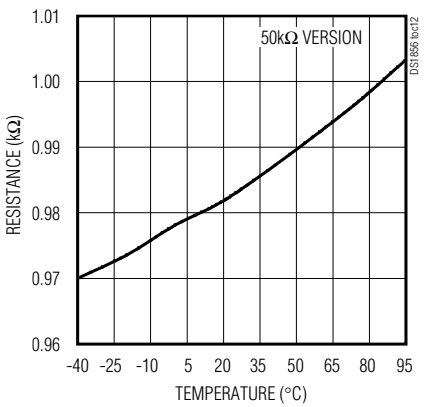
RESISTANCE vs. POWER-UP VOLTAGE



RESISTANCE vs. POWER-UP VOLTAGE



POSITION 00h RESISTANCE vs. TEMPERATURE

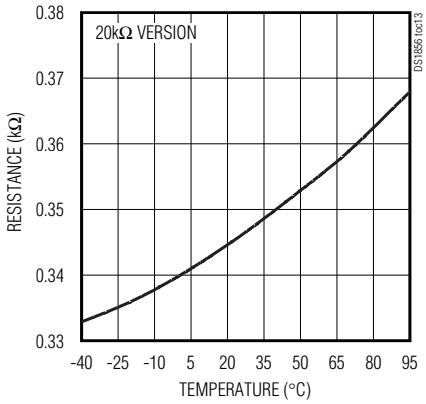


Dual, Temperature-Controlled Resistors with Internally Calibrated Monitors and Password Protection

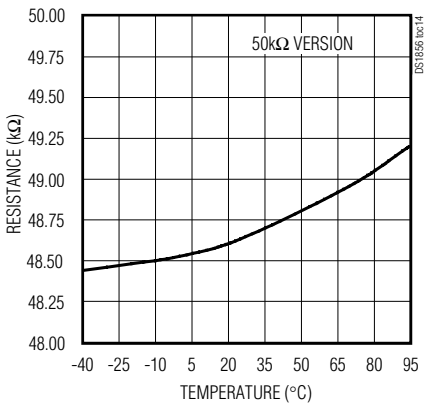
Typical Operating Characteristics (continued)

(V_{CC} = 5.0V, T_A = +25°C, for both 50kΩ and 20kΩ versions, unless otherwise noted.)

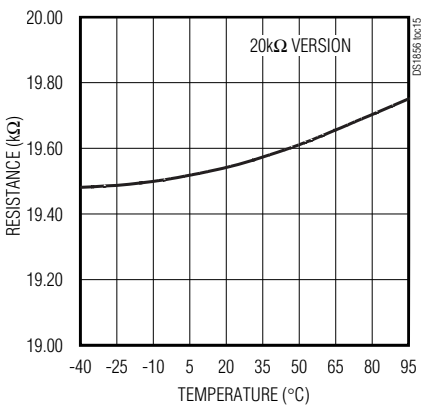
POSITION 00h RESISTANCE vs. TEMPERATURE



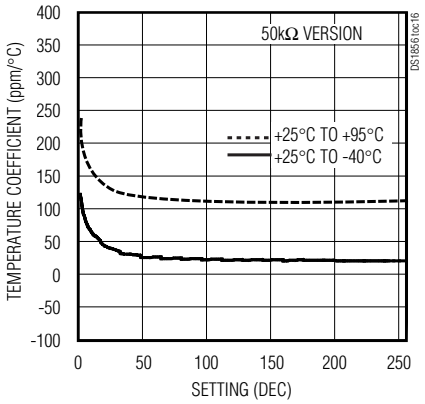
POSITION FFh RESISTANCE vs. TEMPERATURE



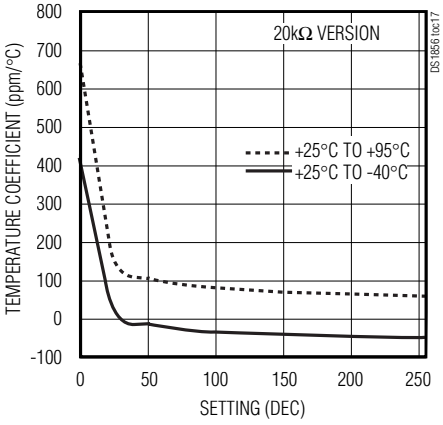
POSITION FFh RESISTANCE vs. TEMPERATURE



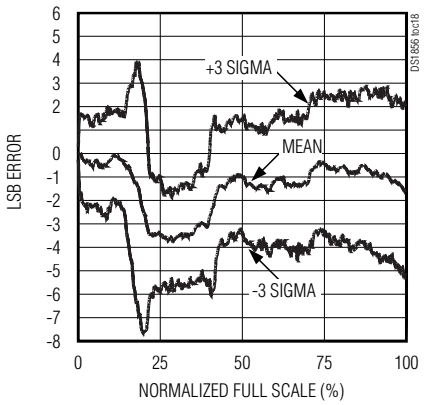
TEMPERATURE COEFFICIENT vs. SETTING



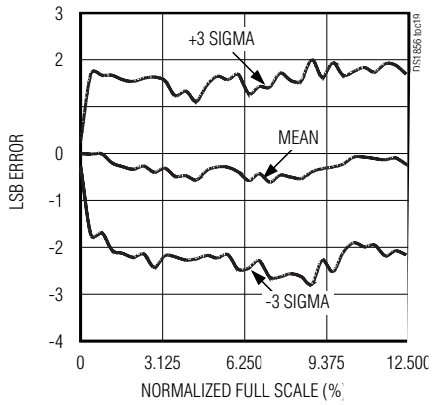
TEMPERATURE COEFFICIENT vs. SETTING



LSB ERROR vs. FULL-SCALE INPUT



LSB ERROR vs. FULL-SCALE INPUT



Pin Description

PIN	BALL	NAME	FUNCTION
1	B2	SDA	2-Wire Serial Data I/O Pin. Transfers serial data to and from the device.
2	A2	SCL	2-Wire Serial Clock Input. Clocks data into and out of the device.
3	C3	OUT1	Open-Drain Buffer Output
4	A1	IN1	TTL/CMOS-Compatible Input to Buffer
5	B1	OUT2	Open-Drain Buffer Output
6	C2	IN2	TTL/CMOS-Compatible Input to Buffer
7	C1	N.C.	No Connection
8	D1	GND	Ground
9	D3	MON1	External Analog Input
10	D4	MON2	External Analog Input
11	C4	MON3	External Analog Input
12	D2	L0	Low-End Resistor 0 Terminal. It is not required that the low-end terminals be connected to a potential less than the high-end terminals of the corresponding resistor. Voltage applied to any of the resistor terminals cannot exceed the power-supply voltage, V_{CC}, or go below ground.
13	B3	H0	High-End Resistor 0 Terminal. It is not required that the high-end terminals be connected to a potential greater than the low-end terminals of the corresponding resistor. Voltage applied to any of the resistor terminals cannot exceed the power-supply voltage, V_{CC}, or go below ground.
14	B4	L1	Low-End Resistor 1 Terminal
15	A4	H1	High-End Resistor 1 Terminal
16	A3	V_{CC}	Supply Voltage

Detailed Description

The user can read the registers that monitor the V_{CC}, MON1, MON2, MON3, and temperature analog signals. After each signal conversion, a corresponding bit is set that can be monitored to verify that a conversion has occurred. The signals also have alarm and warning flags that notify the user when the signals go above or below the user-defined value. Interrupts can also be set for each signal.

The position values of each resistor can be independently programmed. The user can assign a unique value to each resistor for every 2°C increment over the -40°C to +102°C range.

Two buffers are provided to convert logic-level inputs into open-drain outputs. Typically, these buffers are used to implement transmit (Tx) fault and loss-of-signal (LOS) functionality. Additionally, OUT1 can be asserted in the event that one or more of the monitored values go beyond user-defined limits.

Dual, Temperature-Controlled Resistors with Internally Calibrated Monitors and Password Protection

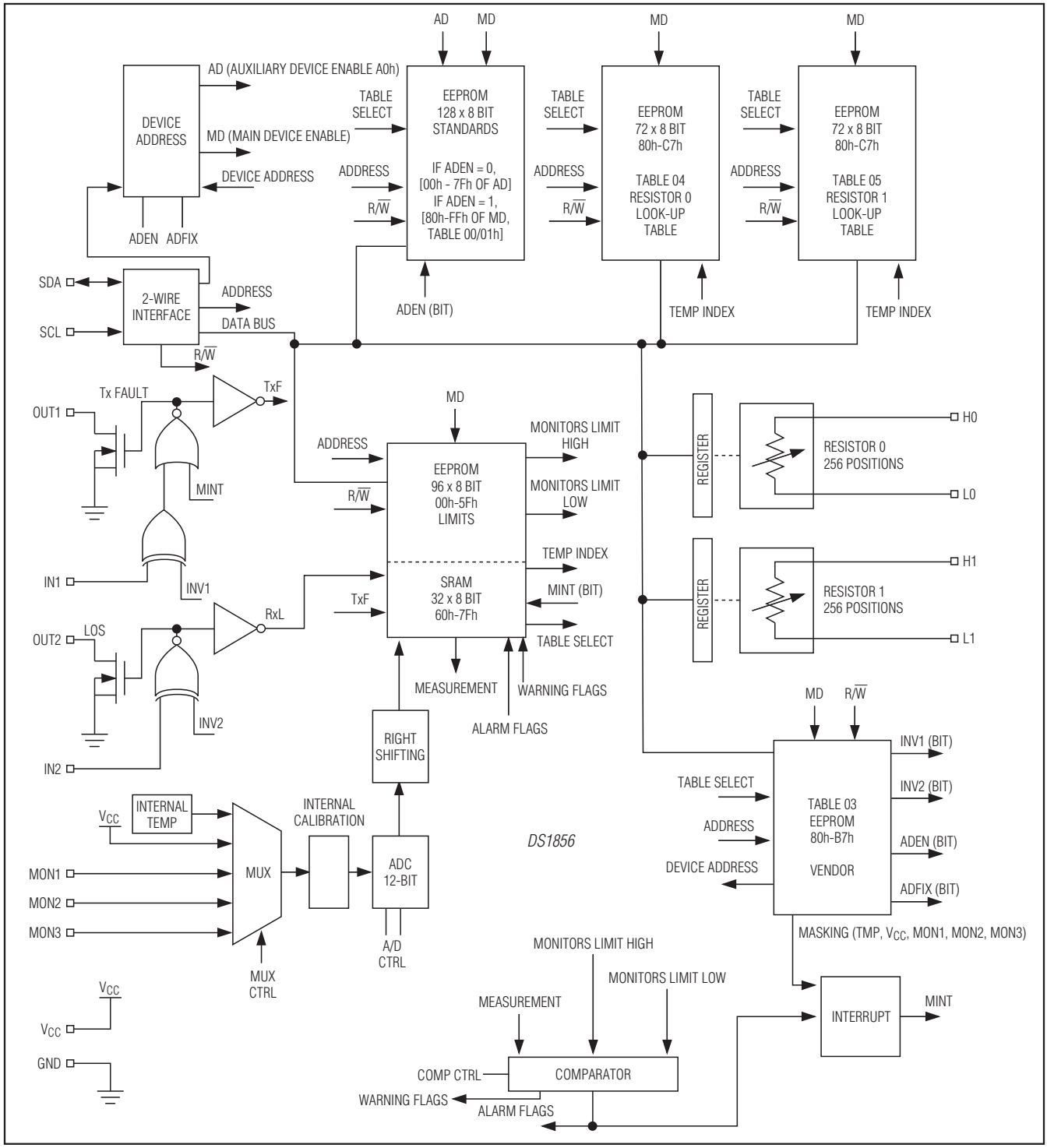


Figure 1. Block Diagram

Table 1. Scales for Monitor Channels at Factory Setting

SIGNAL	+FS SIGNAL	+FS (hex)	-FS SIGNAL	-FS (hex)
Temperature	+127.984°	7FFC	-128°C	8000
V_{CC}	6.5528V	FFF8	0V	0000
MON1	2.4997V	FFF8	0V	0000
MON2	2.4997V	FFF8	0V	0000
MON3	2.4997V	FFF8	0V	0000

Table 2. Signal Comparison

SIGNAL	FORMAT
V_{CC}	Unsigned
MON1	Unsigned
MON2	Unsigned
MON3	Unsigned
Temperature	Two's complement

Monitored Signals

Each signal (V_{CC}, MON1, MON2, MON3, and temperature) is available as a 16-bit value with 12-bit accuracy (left-justified) over the serial bus. See Table 1 for signal scales and Table 2 for signal format. The four LSBs should be masked when calculating the value. The 3 LSBs are internally masked with 0s.

The signals are updated every frame rate (t_{frame}) in a round-robin fashion.

The comparison of all five signals with the high and low user-defined values are done automatically. The corresponding flags are set to 1 within a specified time of the occurrence of an out-of-limit condition.

Calculating Signal Values

The LSB = 100µV for V_{CC}, and the LSB = 38.147µV for the MON signals when using factory default settings.

Monitor/V_{CC} Bit Weights

MSB	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
LSB	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

V_{CC} Conversion Examples

MSB (BIN)	LSB (BIN)	VOLTAGE (V)
10000000	10000000	3.29
11000000	11111000	4.94

Table 3. Look-Up Table Address for Corresponding Temperature Values

TEMPERATURE (°C)	CORRESPONDING LOOK-UP TABLE ADDRESS
<-40	80h
-40	80h
-38	81h
-36	82h
-34	83h
—	—
+98	C5h
+100	C6h
+102	C7h
>+102	C7h

Monitor Conversion Example

MSB (BIN)	LSB (BIN)	VOLTAGE (V)
11000000	00000000	1.875
10000000	10000000	1.255

To calculate V_{CC}, convert the unsigned 16-bit value to decimal and multiply by 100µV.

To calculate MON1, MON2, or MON3, convert the unsigned 16-bit value to decimal and multiply by 38.147µV.

To calculate the temperature, treat the two's complement value binary number as an unsigned binary number, then convert to decimal and divide by 256. If the result is greater than or equal to 128, subtract 256 from the result.

Temperature: high byte: -128°C to +127°C signed; low byte: 1/256°C.

Temperature Bit Weights

S	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}

Temperature Conversion Examples

MSB (BIN)	LSB (BIN)	TEMPERATURE (°C)
01000000	00000000	+64
01000000	00001111	+64.059
01011111	00000000	+95
11110110	00000000	-10
11011000	00000000	-40

Table 4. ADEN Address Configuration

ADEN (ADDRESS ENABLE)	NO. OF SEPARATE DEVICE ADDRESSES	ADDITIONAL INFORMATION
0	2	See Figure 2
1	1 (Main Device Only)	See Figure 3

Table 5. ADEN and ADFIX Bits

ADEN	ADFIX	AUXILIARY ADDRESS	MAIN ADDRESS
0	0	A0h	A2h
0	1	A0h	EEPROM (Table 03, 8Ch)
1	0	—	A2h
1	1	—	EEPROM (Table 03, 8Ch)

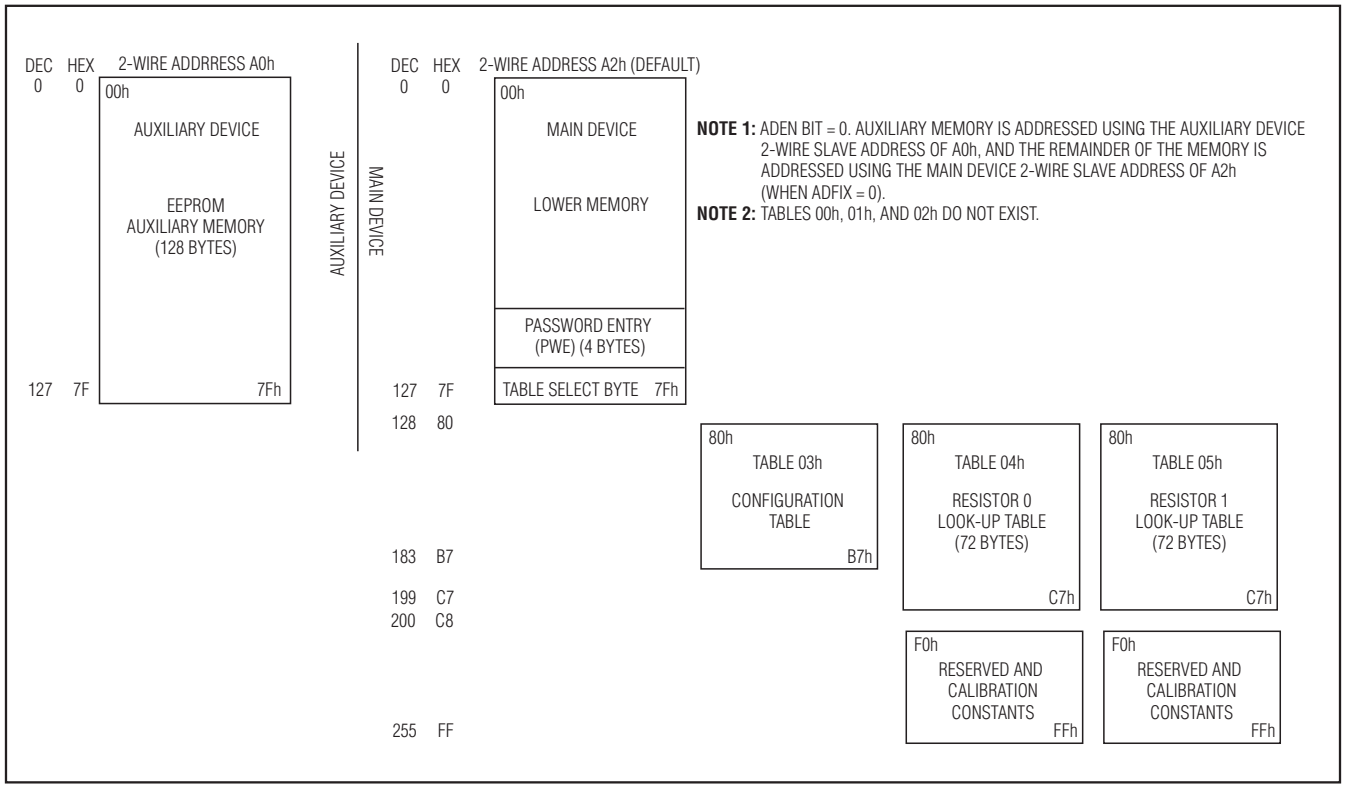


Figure 2. Memory Organization, ADEN = 0

Variable Resistors

The value of each variable resistor is determined by a temperature-addressed look-up table, which can assign a unique value (00h to FFh) to each resistor for every 2°C increment over the -40°C to +102°C range (see Table 3). See the *Temperature Conversion* section for more information.

The variable resistors can also be used in manual mode. If the TEN bit equals 0, the resistors are in manual mode and the temperature indexing is disabled. The user sets the resistors in manual mode by writing to addresses 82h and 83h in Table 03 to control resistors 0 and 1, respectively.

Memory Description

The memory of the DS1856 is divided into two areas referred to as the Main Device and the Auxiliary Device. The Main Device comprises all of the DS1856 specific memory while the Auxiliary Device consists of 128 bytes of general-purpose EEPROM and is especially useful in GBIC applications. Main and Auxiliary

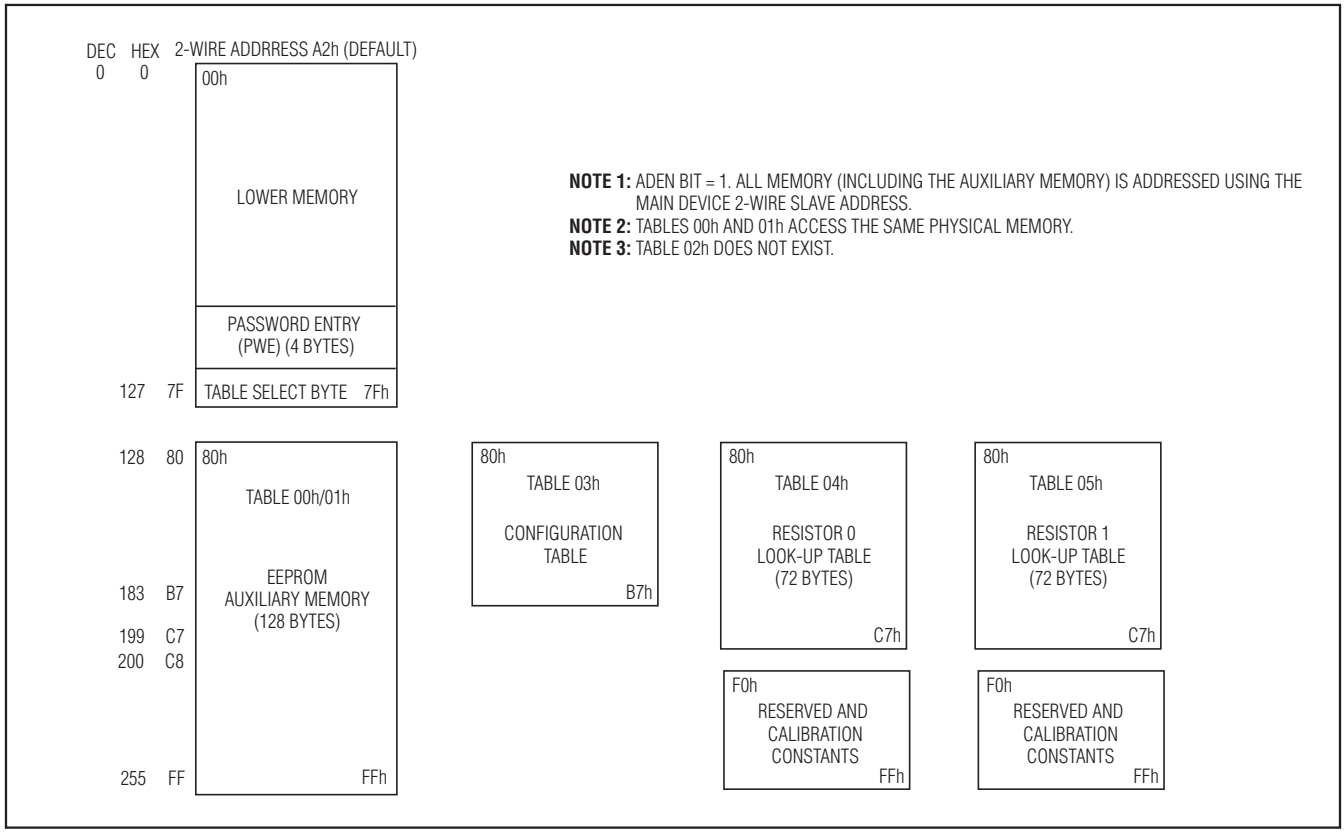


Figure 3. Memory Organization, ADEN = 1

memories can be accessed by two separate 2-wire slave addresses (see Table 4). The Main Device address is A2h (or determined by the value in Table 03, byte 8Ch, when ADFIX = 1) and the Auxiliary Device address is A0h (fixed). A configuration bit, ADEN (Table 03, byte 89h, bit 5), determines whether the DS1856 uses one or two 2-wire slave addresses. This feature can be used to save component count in SFF applications or other applications where both GBIC and monitoring functions are implemented and two device addresses are needed.

The memory organization for ADEN = 0 is shown in Figure 2. In this configuration, the 128 bytes of Auxiliary Device EEPROM are located at memory locations 00h to 7Fh and accessed using the Auxiliary Device 2-wire slave address of A0h (fixed). The remainder of the DS1856's memory is accessed using the Main Device address.

The memory organization of the second configuration, ADEN = 1, is shown in Figure 3. In this configuration, all of the DS1856's memory including the Auxiliary memory is accessed using only the Main Device address. The Auxiliary Device memory is mapped into Table 00 and Table 01 in the Main Device. Both tables map to the same block of physical memory. This is done to improve the compatibility between previous members of this IC family such as the DS1858/DS1859 and the DS1852. In this configuration, the DS1856 ignores communication using the Auxiliary Device address.

The value of the Main Device address can be changed to a value other than the default value of A2h (see data sheet Table 5). There can be up to 128 devices sharing a common 2-wire bus, with each device having its own unique address. To change the Main Device address, first write the desired value to the Chip Address byte (Table 03, byte 8Ch). Then, enable the new address by setting ADFIX to a 1. Subsequent 2-wire communication must be performed using the new Main Device address. When ADFIX = 0, the Chip Address byte is ignored, and the Main Device address is set to A2h.

The DS1856 2-wire interface uses 8-bit addressing, which allows up to 256 bytes to be addressed traditionally on a given 2-wire slave address. However, since the Main Device contains more than 256 bytes, a table scheme is used. The lower 128 bytes of the Main Device, memory locations 00h to 7Fh, function as expected and are independent of the currently selected table. Byte 7Fh is the Table Select byte. This byte determines which memory table will be accessed by the 2-wire interface when address locations 80h to FFh are accessed. Memory locations 80h to FFh are accessible only through the Main Device address. The Auxiliary Device address has no access to the tables, but the Auxiliary Device memory can be mapped into the Main Device's memory space (by setting ADEN = 1). Valid values for the Table Select byte are shown in the table below.

Table 6. Table Select Byte

TABLE SELECT BYTE	TABLE NAME
00	Auxiliary Device Memory (When ADEN = 1)
01	
02	Does Not Exist
03	Configuration
04	Resistor 0 Look-up Table
05	Resistor 1 Look-up Table

Before attempting to read and write any of the bits or bytes mentioned in this section, it is important to look at the memory map provided in a subsequent section to verify what level of password is required. Password protection is described in the following section.

Password Protection

The DS1856 uses two 4-byte passwords to achieve three levels of access to various memory locations. The three levels of access are:

User Access: This is the default state after power-up. It allows read access to standard monitoring and status functions.

Level 1 Access: This allows access to customer data table (Tables 00 and 01) in addition to everything granted by User access. This level is granted by entering Password 1 (PW1).

Level 2 Access: This allows access to all memory, settings, and features, in addition to everything granted by Level 1 and User access. This level is granted by entering Password 2 (PW2).

To obtain a particular level of access, the corresponding password must be entered in the Password Entry (PWE) bytes located in the Main Device at 7Bh to 7Eh. The value entered is compared to both the PW1 and PW2 settings located in Table 03, bytes B0h to B3h and Table 03, bytes B4h to B7h, respectively, to determine if access should be granted. Access is granted until the password is changed or until power is cycled.

Writing PWE can be done with any level of access, although PWE can never be read.

Writing PW1 and PW2 requires PW2 access. However, PW1 and PW2 can never be read, even with PW2 access.

On power-up, PWE is set to all 1s (FFFFh). As long as neither of the passwords are ever changed to FFFFh, then User access is the power-up default. Likewise, password protection can be intentionally disabled by setting the PW2 password to FFFFh.

Memory Map

The following table is the legend used in the memory map to indicate the access level required for read and write access.

Each table in the following memory map begins with a higher level view of a particular portion of the memory showing information such as row (8 bytes) and byte names. The tables are then followed, where applicable, by an Expanded Bytes table, which shows bit names and values. Furthermore, both tables use the permission legend to indicate the access required on a row, byte, and bit level.

The memory map is followed by a *Register Description* section, which describes bytes and bits in further detail.

Table 7. Password Permission

PERMISSION	READ	WRITE
<0>	At least one byte in the row is different than the rest of the row, so look at each byte separately for permissions.	
<1>	all	PW2
<2>	all	NA
<3>	all	all (The part also writes to this byte.)
<4>	PW2	PW2 + mode_bit
<5>	all	all
<6>	NA	all
<7>	PW1	PW1
<8>	PW2	PW2
<9>	NA	PW2
<10>	PW2	NA
<11>	all	PW1

Memory Map

LOWER MEMORY															
Row (hex)	Row Name	Word 0				Word 1				Word 2				Word 3			
		Byte 0/8		Byte 1/9		Byte 2/A		Byte 3/B		Byte 4/C		Byte 5/D		Byte 6/E		Byte 7/F	
00	<1>Threshold$_0$	Temp Alarm Hi				Temp Alarm Lo				Temp Warn Hi				Temp Warn Lo			
08	<1>Threshold$_1$	V_{CC} Alarm Hi				V_{CC} Alarm Lo				V_{CC} Warn Hi				V_{CC} Warn Lo			
10	<1>Threshold$_2$	Mon1 Alarm Hi				Mon1 Alarm Lo				Mon1 Warn Hi				Mon1 Warn Lo			
18	<1>Threshold$_3$	Mon2 Alarm Hi				Mon2 Alarm Lo				Mon2 Warn Hi				Mon2 Warn Lo			
20	<1>Threshold$_4$	Mon3 Alarm Hi				Mon3 Alarm Lo				Mon3 Warn Hi				Mon3 Warn Lo			
28	<1>user ROM	EE		EE		EE		EE		EE		EE		EE		EE	
30	<1>user ROM	EE		EE		EE		EE		EE		EE		EE		EE	
38	<1>user ROM	EE		EE		EE		EE		EE		EE		EE		EE	
40	<1>user ROM	EE		EE		EE		EE		EE		EE		EE		EE	
48	<1>user ROM	EE		EE		EE		EE		EE		EE		EE		EE	
50	<1>user ROM	EE		EE		EE		EE		EE		EE		EE		EE	
58	<1>user ROM	EE		EE		EE		EE		EE		EE		EE		EE	
60	<2>Values$_0$	Temp Value				Vcc Value				Mon1 Value				Mon2 Value			
68	<0>Values$_1$	<2>Mon3 Value				<2>*Reserved*				<2>*Reserved*				<0>Status		<3>Update	
70	<2>Alrm Wrn	Alarm$_1$		Alarm$_0$		*Reserved*		*Reserved*		Warn$_1$		Warn$_0$		*Reserved*		*Reserved*	
78	<0>Table Select	<6>*Reserved*		<6>*Reserved*		<6>*Reserved*		<6>PWE msb				<6>PWE lsb				<5>Tbl Sel	
EXPANDED BYTES																	
Byte (hex)	Byte Name	Bit7		Bit6		Bit5		Bit4		Bit3		Bit2		Bit1		Bit0	
		bit$_{15}$	bit$_{14}$	bit$_{13}$	bit$_{12}$	bit$_{11}$	bit$_{10}$	bit$_9$	bit$_8$	bit$_7$	bit$_6$	bit$_5$	bit$_4$	bit$_3$	bit$_2$	bit$_1$	bit$_0$
	User EE	EE		EE		EE		EE		EE		EE		EE		EE	
	Temp Alarm	S	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}
	Temp Warn	S	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}
	Volt Alarm	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	Volt Warn	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
28	User ROM	EE		EE		EE		EE		EE		EE		EE		EE	
30	User ROM	EE		EE		EE		EE		EE		EE		EE		EE	
38	User ROM	EE		EE		EE		EE		EE		EE		EE		EE	
40	User ROM	EE		EE		EE		EE		EE		EE		EE		EE	
48	User ROM	EE		EE		EE		EE		EE		EE		EE		EE	
50	User ROM	EE		EE		EE		EE		EE		EE		EE		EE	
58	User ROM	EE		EE		EE		EE		EE		EE		EE		EE	

Memory Map (continued)

60	Temp Value	S	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}
62	V_{CC} Value	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
64	Mon1 Value	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
66	Mon2 Value	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
68	Mon3 Value	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
6E	Status	<2>Rhiz		<11>SoftHiz		<2>*Reserved*		<2>*Reserved*		<2>*Reserved*		<2>TxF		<2>RxL		<2>Rdyb	
6F	Update	Temp Rdy		V_{CC} Rdy		Mon1 Rdy		Mon2 Rdy		Mon3 Rdy		*Reserved*		*Reserved*		*Reserved*	
70	$Alarm_1$	Temp Hi		Temp Lo		V_{CC} Hi		V_{CC} Lo		Mon1 Hi		Mon1 Lo		Mon2 Hi		Mon2 Lo	
71	$Alarm_0$	Mon3 Hi		Mon3 Lo		*Reserved*		*Reserved*		*Reserved*		*Reserved*		*Reserved*		Mint	
74	$Warn_1$	Temp Hi		Temp Lo		V_{CC} Hi		V_{CC} Lo		Mon1 Hi		Mon1 Lo		Mon2 Hi		Mon2 Lo	
75	$Warn_0$	Mon3 Hi		Mon3 Lo		*Reserved*		*Reserved*		*Reserved*		*Reserved*		*Reserved*		*Reserved*	
7B	PWE msb	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}
7D	PWE lsb	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
7F	Tbl Sel	2^7		2^6		2^5		2^4		2^3		2^2		2^1		2^0	

AUXILIARY (VALID WHEN ADEN = 0)									
Row (hex)	Row Name	Word 0		Word 1		Word 2		Word 3	
		Byte 0/8	Byte 1/9	Byte 2/A	Byte 3/B	Byte 4/C	Byte 5/D	Byte 6/E	Byte 7/F
00–7F	<1>EE	EE	EE	EE	EE	EE	EE	EE	EE
TABLE 00/01 (VALID WHEN ADEN = 1)									
Row (hex)	Row Name	Word 0		Word 1		Word 2		Word 3	
		Byte 0/8	Byte 1/9	Byte 2/A	Byte 3/B	Byte 4/C	Byte 5/D	Byte 6/E	Byte 7/F
80–FF	<7>EE	EE	EE	EE	EE	EE	EE	EE	EE

Memory Map (continued)

TABLE 03 (CONFIGURATION)

Row (hex)	Row Name	Word 0		Word 1		Word 2		Word 3	
		Byte 0/8	Byte 1/9	Byte 2/A	Byte 3/B	Byte 4/C	Byte 5/D	Byte 6/E	Byte 7/F
80	$^{<0>}Config_0$	$^{<8>}$Mode	$^{<4>}$Tindex	$^{<4>}$Res0	$^{<4>}$Res1	$^{<8>}$*Reserved*	$^{<8>}$*Reserved*	$^{<8>}$*Reserved*	$^{<8>}$*Reserved*
88	$^{<8>}Config_1$	Int Enable	Config	*Reserved*	*Reserved*	chip addr	*Reserved*	$Rshift_1$	$Rshift_0$
90	$^{<8>}Scale_0$	*Reserved*		Vcc Scale		Mon1 Scale		Mon2 Scale	
98	$^{<8>}Scale_1$	Mon3 Scale		*Reserved*		*Reserved*		*Reserved*	
A0	$^{<8>}Offset_0$	*Reserved*		Vcc Offset		MON1 Offset		MON2 Offset	
A8	$^{<8>}Offset_1$	MON3 Offset		*Reserved*		*Reserved*		Internal Temp Offset*	
B0	$^{<9>}$Pwd Value	PW1 msb		PW1 lsb		PW2 msb		PW2 lsb	

EXPANDED BYTES

Byte (hex)	Byte Name	Bit7		Bit6		Bit5		Bit4		Bit3		Bit2		Bit1		Bit0	
		bit_{15}	bit_{14}	bit_{13}	bit_{12}	bit_{11}	bit_{10}	bit_9	bit_8	bit_7	bit_6	bit_5	bit_4	bit_3	bit_2	bit_1	bit_0
80	Mode	*Reserved*		*Reserved*		*Reserved*		*Reserved*		*Reserved*		*Reserved*		TEN		AEN	
81	Tindex	2^7		2^6		2^5		2^4		2^3		2^2		2^1		2^0	
82	Res0	2^7		2^6		2^5		2^4		2^3		2^2		2^1		2^0	
83	Res1	2^7		2^6		2^5		2^4		2^3		2^2		2^1		2^0	
88	Int Enable	Temp		Vcc		Mon1		Mon2		Mon3		*Reserved*		*Reserved*		*Reserved*	
89	Config	*Reserved*		*Reserved*		ADEN		ADFIX		*Reserved*		*Reserved*		Inv 1		Inv 2	
8C	Chip Addr	2^7		2^6		2^5		2^4		2^3		2^2		2^1		2^0	
8E	$Rshift_1$	*Reserved*		$Mon1^2$		$Mon1^1$		$Mon1^0$		*Reserved*		$Mon2^2$		$Mon2^1$		$Mon2^0$	
8F	$Rshift_0$	*Reserved*		$Mon3^2$		$Mon3^1$		$Mon3^0$		*Reserved*		*Reserved*		*Reserved*		*Reserved*	
92	V_{CC} Scale	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
94	Mon1 Scale	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
96	Mon2 Scale	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
98	Mon3 Scale	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
A2	V_{CC} Offset	S	S	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2
A4	Mon1 Offset	S	S	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2
A6	Mon2 Offset	S	S	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2
A8	Mon3 Offset	S	S	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2
AE	Temp Offset*	S	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}
B0	PW1 msb	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}
B2	PW1 lsb	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
B4	PW2 msb	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}
B6	PW2 lsb	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

**The final result must be XOR'ed with BB40h.*

Memory Map (continued)

TABLE 04 (LOOKUP TABLE FOR RESISTOR 0)									
Row (hex)	Row Name	Word 0		Word 1		Word 2		Word 3	
		Byte 0/8	Byte 1/9	Byte 2/A	Byte 3/B	Byte 4/C	Byte 5/D	Byte 6/E	Byte 7/F
80	<8>LUT								
88	<8>LUT								
90	<8>LUT								
98	<8>LUT								
A0	<8>LUT								
A8	<8>LUT								
B0	<8>LUT								
B8	<8>LUT								
C0	<8>LUT								
C8		*Empty*	*Empty*	*Empty*	*Empty*	*Empty*	*Empty*	*Empty*	*Empty*
D0		*Empty*	*Empty*	*Empty*	*Empty*	*Empty*	*Empty*	*Empty*	*Empty*
D8		*Empty*	*Empty*	*Empty*	*Empty*	*Empty*	*Empty*	*Empty*	*Empty*
E0		*Empty*	*Empty*	*Empty*	*Empty*	*Empty*	*Empty*	*Empty*	*Empty*
E8		*Empty*	*Empty*	*Empty*	*Empty*	*Empty*	*Empty*	*Empty*	*Empty*
F0		*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*
F8	<10>Res0 data	Resistor 0 Calibration Constants (see data sheet Table 8)							
EXPANDED BYTES									
Byte (hex)	Byte Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
80–C7	Res0	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
F8–FF	Res0 data	Resistor 0 Calibration Constants (see data sheet Table 8 for weighting)							

Memory Map (continued)

TABLE 05 (LOOKUP TABLE FOR RESISTOR 1)									
Row (hex)	Row Name	Word 0		Word 1		Word 2		Word 3	
		Byte 0/8	Byte 1/9	Byte 2/A	Byte 3/B	Byte 4/C	Byte 5/D	Byte 6/E	Byte 7/F
80	<8>LUT								
88	<8>LUT								
90	<8>LUT								
98	<8>LUT								
A0	<8>LUT								
A8	<8>LUT								
B0	<8>LUT								
B8	<8>LUT								
C0	<8>LUT								
C8		*Empty*	*Empty*	*Empty*	*Empty*	*Empty*	*Empty*	*Empty*	*Empty*
D0		*Empty*	*Empty*	*Empty*	*Empty*	*Empty*	*Empty*	*Empty*	*Empty*
D8		*Empty*	*Empty*	*Empty*	*Empty*	*Empty*	*Empty*	*Empty*	*Empty*
E0		*Empty*	*Empty*	*Empty*	*Empty*	*Empty*	*Empty*	*Empty*	*Empty*
E8		*Empty*	*Empty*	*Empty*	*Empty*	*Empty*	*Empty*	*Empty*	*Empty*
F0		*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*
F8	<10>Res1 data	Resistor 1 Calibration Constants (see data sheet Table 8)							
EXPANDED BYTES									
Byte (hex)	Byte Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
80–C7	Res1	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
F8–FF	Res1 data	Resistor 1 Calibration Constants (see data sheet Table 8 for weighting)							

Register Descriptions

Name of Row

- *Name of Byte*..... <Read/Write><Volatile><Power-On-Value>
- *Name of Byte*..... <Read/Write><Nonvolitile><Factory-Default-Setting>

$Threshold_0$

- *Temp High Alarm* ..... <R-all/W-pw2><NV><7FFFh> Temperature measurements above this two's complement threshold set its corresponding alarm bit. Measurements below this threshold clear the alarm bit.
- *Temp Low Alarm*..... <R-all/W-pw2><NV><8000h> Temperature measurements below this two's complement threshold set its corresponding alarm bit. Measurements above this threshold clear the alarm bit.
- *Temp High Warning* . <R-all/W-pw2><NV><7FFFh> Temperature measurements above this two's complement threshold set its corresponding warning bit. Measurements below this threshold clear the warning bit.
- *Temp Low Warning* .. <R-all/W-pw2><NV><8000h> Temperature measurements below this two's complement threshold set its corresponding warning bit. Measurements above this threshold clear the warning bit.

$Threshold_1$

- V_{CC} *High Alarm*..... <R-all/W-pw2><NV><FFFFh> Voltage measurements of the V_{CC} input above this unsigned threshold set its corresponding alarm bit. Measurements below this threshold clear the alarm bit.
- V_{CC} *Low Alarm*..... <R-all/W-pw2><<NV><0000h> Voltage measurements of the V_{CC} input below this unsigned threshold set its corresponding alarm bit. Measurements above this threshold clear the alarm bit.
- V_{CC} *High Warning*.... <R-all/W-pw2><NV><FFFFh> Voltage measurements of the V_{CC} input above this unsigned threshold set its corresponding warning bit. Measurements below this threshold clear the warning bit.
- V_{CC} *Low Warning*..... <R-all/W-pw2><<NV><0000h> Voltage measurements of the V_{CC} input below this unsigned threshold set its corresponding warning bit. Measurements above this threshold clear the warning bit.

$Threshold_2$

- *Mon1 High Alarm*..... <R-all/W-pw2><NV><FFFFh> Voltage measurements of the Mon1 input above this unsigned threshold set its corresponding alarm bit. Measurements below this threshold clear the alarm bit.
- *Mon1 Low Alarm* ..... <R-all/W-pw2><NV><0000h> Voltage measurements of the Mon1 input below this unsigned threshold set its corresponding alarm bit. Measurements above this threshold clear the alarm bit.
- *Mon1 High Warning*. <R-all/W-pw2><NV><FFFFh> Voltage measurements of the Mon1 input above this unsigned threshold set its corresponding warning bit. Measurements below this threshold clear the warning bit.
- *Mon1 Low Warning*.. <R-all/W-pw2><NV><0000h> Voltage measurements of the Mon1 input below this unsigned threshold set its corresponding warning bit. Measurements above this threshold clear the warning bit.

Register Descriptions (continued)

Threshold$_3$

- *Mon2 High Alarm*..... <R-all/W-pw2><NV><FFFFh> Voltage measurements of the Mon2 input above this unsigned threshold set its corresponding alarm bit. Measurements below this threshold clear the alarm bit.
- *Mon2 Low Alarm*..... <R-all/W-pw2><NV><0000h> Voltage measurements of the Mon2 input below this unsigned threshold set its corresponding alarm bit. Measurements above this threshold clear the alarm bit.
- *Mon2 High Warning*. <R-all/W-pw2><NV><FFFFh> Voltage measurements of the Mon2 input above this unsigned threshold set its corresponding warning bit. Measurements below this threshold clear the warning bit.
- *Mon2 Low Warning*.. <R-all/W-pw2><NV><0000h> Voltage measurements of the Mon2 input below this unsigned threshold set its corresponding warning bit. Measurements above this threshold clear the warning bit.

Threshold$_4$

- *Mon3 High Alarm*..... <R-all/W-pw2><NV><FFFFh> Voltage measurements of the Mon3 input above this unsigned threshold set its corresponding alarm bit. Measurements below this threshold clear the alarm bit.
- *Mon3 Low Alarm*..... <R-all/W-pw2><NV><0000h> Voltage measurements of the Mon3 input below this unsigned threshold set its corresponding alarm bit. Measurements above this threshold clear the alarm bit.
- *Mon3 High Warning*. <R-all/W-pw2><NV><FFFFh> Voltage measurements of the Mon3 input above this unsigned threshold set its corresponding warning bit. Measurements below this threshold clear the warning bit.
- *Mon3 Low Warning*.. <R-all/W-pw2><NV><0000h> Voltage measurements of the Mon3 input below this unsigned threshold set its corresponding warning bit. Measurements above this threshold clear the warning bit.

User ROM

- *User ROM*..... <R-all/W-pw2><NV><00h> Nonvolatile EEPROM memory.

A2D Value$_0$

- *Temp Meas*..... <R-all><W-NA><0000h> The signed two's complement Direct-to-Temperature measurement.
- *V_{CC} Meas*..... <R-all><W-NA><0000h> Unsigned voltage measurement.
- *Mon1 Meas*..... <R-all><W-NA><0000h> Unsigned voltage measurement.
- *Mon2 Meas*..... <R-all><W-NA><0000h> Unsigned voltage measurement.

Register Descriptions (continued)

A2D Value$_1$

- *Mon3 Meas*..... <R-all><W-NA><0000h> Unsigned voltage measurement.
- *Reserved*..... <R-all><W-NA><0000h>
- *Status*..... <R-all><W-see bits><conditional>
  a) Rhiz..... <R-all><W-NA><1b> High when resistor outputs are high impedance.
  b) Soft Hiz..... <R-all><W-all><0b> Setting this bit will make resistor outputs high impedance.
  c) Reserved ..... <R-all><W-NA><0b>
  d) TxF ..... <R-all><W-NA><conditional> Reflects the logic level to be output on pin Out1.
  e) RxL ..... <R-all><W-NA><conditional> Reflects the logic level to be output on pin Out2.
  f) Rdyb..... <R-all><W-NA>< V_{CC} dependant > Ready Bar. When the supply is above the Power-On-Analog (POA) trip point, this bit is active LOW. Thus, this bit reads a logic One if the supply is below POA or too low to communicate over the 2-wire bus.
- *Update*..... <R-all/W-all><00h> Status of completed conversions. At Power-On, these bits are cleared and will be set as each conversion is completed. These bits can be cleared so that a completion of a new conversion may be verified.
  a) Temp Rdy ..... Temperature conversion is ready.
  b) V_{CC} Rdy..... V_{CC} conversion is ready.
  c) Mon1 Rdy..... Mon1 conversion is ready.
  d) Mon2 Rdy..... Mon2 conversion is ready.
  e) Mon3 Rdy..... Mon3 conversion is ready.

Status

- *Alarm$_0$* ..... <R-all><W-NA><10h> High Alarm Status bits.
  a) Temp Hi..... High Alarm Status for Temperature measurement.
  b) Temp Lo ..... Low Alarm Status for Temperature measurement.
  c) V_{CC} Hi ..... High Alarm Status for V_{CC} measurement.
  d) V_{CC} Lo..... Low Alarm Status for V_{CC} measurement. This bit is set when theV_{CC} supply is below the POA trip point value. It clears itself when a V_{CC} measurement is completed and the value is above the low threshold.
  e) MON1 Hi..... High Alarm Status for MON1 measurement.
  f) MON1 Lo ..... Low Alarm Status for MON1 measurement.
  g) MON2 Hi..... High Alarm Status for MON2 measurement.
  h) MON2 Lo ..... Low Alarm Status for MON2 measurement.
- *Alarm$_1$* ..... <R-all><W-NA><00h> Low Alarm Status bits.
  a) MON3 HI..... High Alarm Status for MON3 measurement.
  b) MON3 Lo ..... Low Alarm Status for MON3 measurement.
  c) Mint ..... Maskable Interrupt. If an alarm is present and the alarm is enabled then this bit is high. Otherwise this bit is a zero.
- *Reserved*..... <R-all><W-NA><00h>.
- *Warning$_0$* ..... <R-all><W-NA><00h> High Warning Status bits.
  a) Temp Hi..... High Warning Status for Temperature measurement.
  b) Temp Lo ..... Low Warning Status for Temperature measurement.
  c) V_{CC} Hi ..... High Warning Status for V_{CC} measurement.

Register Descriptions (continued)

d) V_{CC} Lo ..... Low Warning Status for V_{CC} measurement. This bit is set when the V_{CC} supply is below the POA trip point value. It clears itself when a V_{CC} measurement is completed and the value is above the low threshold.
e) MON1 Hi..... High Warning Status for MON1 measurement.
f) MON1 Lo ..... Low Warning Status for MON1 measurement.
g) MON2 Hi..... High Warning Status for MON2 measurement.
h) MON2 Lo ..... Low Warning Status for MON2 measurement.

- *$Warning_1$* ..... <R-all><W-NA><00h> Low warning Status bits.
  a) MON3 HI..... High Warning Status for MON3 measurement.
  b) MON3 Lo..... Low Warning Status for MON3 measurement.

Table Select

- *Reserved*..... <R-NA><W-all><00h>
- *PWE*..... <R-NA><W-all><FFFFFFFFh> Password Entry. There are two passwords for the DS1856. The lower level password (PW1) has all the access of a normal user plus those made available with PW1. The higher level password (PW2) has all of the access of PW1 plus those made available with PW2. The value of the password reside in EE inside of PW2 memory.
- *TBL Sel*..... <R-all/W-all><00h> Table Select. The upper memory tables of the DS1856 are accessible by writing the correct table value in this register. If the device is configured to have a Table 01h then writing a 00h ora 01h in this byte will access that table.

$Config_0$

- *Mode*..... <R-pw2/W-pw2><NV><03h>
  a) TEN..... At Power-On this bit is HIGH, which enables autocontrol of the LUT. If this bit is written to a ZERO then the resistor values are writeable by the user and the LUT recalls are disabled. This allows the user to interactively test their modules by manually writing resistor values. The resistors will update with the new value at the end of the write cycle. Thus both registers (Res0 and Res1) should be written in the same write cycle. The 2-wire Stop condition is the end of the write cycle.
  b) AEN ..... At Power-On this bit is HIGH, which enables autocontrol of the LUT. If this bit is cleared to a ZERO then the temperature calculated index value (T index) is writeable by the user and the updates of calculated indexes are disabled. This allows the user to interactively test their modules by controlling the indexing for the look-up tables. The recalled values from the LUTs will appear in the resistor registers after the next completion of a temperature conversion (just like it would happen in auto mode). Both pots will update at the same time (just like it would happen in auto mode).
- *T Index*..... <R-pw2><W-pw2+AENb><00h> Holds the calculated index based on the Temperature Measurement. This index is used for the address during Look-up of Tables 4 and 5.

Register Descriptions (continued)

- *Res0* ..... <R-pw2><W-pw2+TENb><FFh> The base value used for Resistor 0 and recalled from Table 4 at the memory address found in T Index. This register is updated at the end of the Temperature conversion.
- *Res1* ..... <R-pw2><W-pw2+TENb><FFh> The base value used for Resistor 1 and recalled from Table 5 at the memory address found in T Index. This register is updated at the end of the Temperature conversion.
- *Reserved*..... <R-pw2><W-pw2><00h> SRAM.

$Config_1$

- *Int Enable*..... <R-pw2/W-pw2><NV><F8h> Configures the maskable interrupt for the Out1 pin.
  a) Temp Enable..... Temperature measurements, outside of the threshold limits, are enabled to create an active interrupt on the Out1 pin.
  b) V_{CC} Enable..... V_{CC} measurements, outside of the threshold limits, are enabled to create an active interrupt on the Out1 pin.
  c) MON1 Enable.... MON1 measurements, outside of the threshold limits, are enabled to create an active interrupt on the Out1 pin.
  d) MON2 Enable.... MON2 measurements, outside of the threshold limits, are enabled to create an active interrupt on the Out1 pin.
  e) MON3 Enable.... MON3 measurements, outside of the threshold limits, are enabled to create an active interrupt on the Out1 pin.
  f) Reserved ..... EE.
- *Config*..... <R-pw2/W-pw2><NV><00h> Configure the memory location and the polarity of the digital outputs.
  a) Reserved ..... EE.
  b) ADEN ..... Auxiliary Device ENable. 128 bytes of EE are addressable depending on the value of this bit. When set to a 1, the memory is located in or as Table 01h. When set to a 0, the memory is addressed by using a Device address of A0h and the locations in memory are 00h to 7Fh.
  c) ADFIX ..... Device Fixable Address. When this bit is set to a 1, the main memory of the DS1856 is a Device Address equal to the value found in byte *chip_address.* When this bit is set to a 0 the main memory of the DS1856 is a Device Address of A2h.
  d) Inv1 ..... Enable the inversion of the relationship between IN1 and OUT1.
  e) Inv2 ..... Enable the inversion of the relationship between IN2 and OUT2.
- *Chip Address*..... This value becomes the Device address for the main memory when *ADFIX* bit is set.
- *Right Shift$_1$* ..... Allows for right-shifting the final answer of some voltage measurements. This allows for scaling the measurements to the smallest full-scale voltage and then right-shifting the final result so the reading is weighted to the correct lsb.
- *Right Shift$_0$* ..... Allows for right-shifting the final answer of some voltage measurements. This allows for scaling the measurements to the smallest full-scale voltage and then right-shifting the final result so the reading is weighted to the correct lsb.

Register Descriptions (continued)

Scale$_0$

- *V_{CC} Scale*..... <R-pw2/W-pw2><NV><6.5535V> Controls the Scaling or Gain of the V_{CC} measurements.
- *MON1 Scale*..... <R-pw2/W-pw2><NV><2.500V> Controls the Scaling or Gain of the MON1 measurements.
- *MON2 Scale*..... <R-pw2/W-pw2><2.500V> Controls the Scaling or Gain of the MON2 measurements.

Scale$_1$

- *MON3 Scale*..... <R-pw2/W-pw2><NV><2.500V> Controls the Scaling or Gain of the MON3 measurements.

Offset$_0$

- *V_{CC} Offset*..... <R-pw2/W-pw2><NV><0000h> Allows for offset control of V_{CC} measurement if desired.
- *MON1 Offset*..... <R-pw2/W-pw2><NV><0000h> Allows for offset control of MON1 measurement if desired.
- *MON2 Offset*..... <R-pw2/W-pw2><NV><0000h> Allows for offset control of MON2 measurement if desired.

Offset$_1$

- *MON3 Offset*..... <R-pw2/W-pw2><NV><0000h> Allows for offset control of MON3 measurement if desired.
- *Temp Offset*..... <R-pw2/W-pw2><NV><0000h> Allows for offset control of Temp measurement if desired.

PWD Value

- *Password 1*..... <R-NA/W-pw2><NV><FFFFFFFFh> The PWE value is compared against the value written to this location to enable PW1 access. At power-on, the PWE value is set to all ones. Thus writing these bytes to all ones grants PW1 access on power-up without writing the password entry.
- *Password 2*..... <R-NA/W-pw2><NV><FFFFFFFFh> The PWE value is compared against the value written to this location to enable PW2 access. At power-on, the PWE value is set to all ones. Thus writing these bytes to all ones grants PW2 access on power-up without writing the password entry.

LUT

- *Res0*..... The unsigned value for Resistor 0.
- *Res1*..... The unsigned value for Resistor 1.

Programming the Look-up Table (LUT)

The following equation can be used to determine which resistor position setting, 00h to FFh, should be written in the LUT to achieve a given resistance at a specific temperature.

$$pos(\alpha,R,C)=\frac{R-u\ x\left[1+v\ x\ (C-25)+w\ x\ (C-25)^2\right]}{(x)\ x\left[1+y\ x\ (C-25)+z\ x\ (C-25)^2\right]}-\alpha$$

R = the resistance desired at the output terminal

C = temperature in degrees Celsius

u, v, w, x_1, x_0, y, z, and α are calculated values found in the corresponding look-up tables. The variable x from the equation above is separated into x_1 (the MSB of x) and x_0 (the LSB of x). Their addresses and LSB values are given below. The variable y is assigned a value. All other variables are unsigned. Resistor 0 variables are found in Table 04, and Resistor 1 variables are found in Table 05.

When shipped from the factory, all other memory locations in the LUTs are programmed to FFh.

Table 8. Calibration Constants

ADDRESS	VARIABLE	LSB
F8h	u	2^0
F9h	v	20E-6
FAh	w	100E-9
FBh	x_1	2^1
FCh	x_0	2^{-7}
FDh	y	2E-6 (signed)
		8E-6 (signed) for -025 version
		4E-6 (signed) for -030 version
FEh	z	10E-9
FFh	α	2^{-2}

Internal Calibration

The DS1856 has two methods for scaling an analog input to a digital result. The two methods are gain and offset. Each of the inputs (V_{CC}, MON1, MON2, and MON3) has a unique register for the gain and the offset found in Table 03h, 92h to 99h, and A2h to A9h.

To scale the gain and offset of the converter for a specific input, you must first know the relationship between the analog input and the expected digital result. The input that would produce a digital result of all zeros is the null value (normally this input is GND). The input that would produce a digital result of all ones is the full-scale (FS) value. The FS value is also found by multiplying an all-ones digital answer by the weighted LSB (e.g., since the digital reading is a 16-bit register, let us assume that the LSB of the lowest weighted bit is 50µV, then the FS value is 65,535 x 50µV = 3.27675V).

A binary search is used to scale the gain of the converter. This requires forcing two known voltages to the input pin. It is preferred that one of the forced voltages is the null input and the other is 90% of FS. Since the LSB of the least significant bit in the digital reading register is known, the expected digital results are also known for both inputs (null/LSB = CNT1 and 90%FS/LSB = CNT2).

The user might not directly force a voltage on the input. Instead they have a circuit that transforms light, frequency, power, or current to a voltage that is the input to the DS1856. In this situation, the user does not need to know the relationship of voltage to expected digital result but instead knows the relationship of light, frequency, power, or current to the expected digital result.

An explanation of the binary search used to scale the gain is best served with the following example pseudocode:

```
/* Assume that the null input is 0.5V. */
/* In addition, the requirement for LSB is 50µV. */
        FS = 65535 x 50E-6;          /* 3.27675 */
        CNT1 = 0.5 / 50E-6;          /* 10000 */
        CNT2 = 0.90 x FS / 50E-6;    /* 58981.5 */
/* Thus the null input 0.5V and the 90% of FS input is 2.949075V. */
        Set the trim-offset-register to zero;
        Set Right-Shift register to zero (typically zero. See the Right-Shifting section);
        gain_result = 0h;
        Clamp = FFF8h/2^(Right_Shift_Register);
        For n = 15 down to 0
        begin
```

```
                gain_result = gain_result + 2^n;
                Force the 90% FS input (2.949075V);
                Meas2 = read the digital result from
                the part;
        If Meas2 >= Clamp then
                gain_result = gain_result – 2^n;
        Else
                Force the null input (0.5V);
                Meas1 = read the digital result from
                the part;
                if (Meas2 – Meas1) > (CNT2 –
                CNT1) then
                gain_result = gain_result – 2^n;
        end;
        Set the gain register to gain_result;
```

The gain register is now set and the resolution of the conversion will best match the expected LSB. The next step is to calibrate the offset of the DS1856. With the correct gain value written to the gain register, again force the null input to the pin. Read the digital result from the part (Meas1). The offset value is equal to the negative value of Meas1.

$$\text{Offset\_Register} = \left[\frac{\text{Meas1}}{4} \right]$$

The calculated offset is now written to the DS1856 and the gain and offset scaling is now complete.

Right-Shifting A/D Conversion Result (Scalable Dynamic Ranging)

The right-shifting method is used to regain some of the lost ADC range of a calibrated system. If a system is calibrated so the maximum expected input results in a digital output value of less than 7FFFh (1/2 FS), then it is a candidate for using the right-shifting method.

If the maximum desired digital output is less than 7FFFh, then the calibrated system is using less than 1/2 of the ADC's range. Similarly, if the maximum desired digital output is less than 1FFFh, then the calibrated system is only using 1/8 of the ADC's range. For example, if using a zero for the right-shift during internal calibration and the maximum expected input results in a maximum digital output less than 1FFCh, only 1/8 of the ADC's range is used. If left like this, the three MS bits of the ADC will never be used. In this example, a value of 3 for the right-shifting maximizes the ADC range. No resolution is lost since this is a 12-bit converter that is left justified. The value can be right-shifted four times without losing resolution. Table 9 shows when the right-shifting method can be used.

Temperature Conversion

The direct-to-digital temperature sensor measures temperature through the use of an on-chip temperature measurement technique with a -40°C to +102°C operating range. Temperature conversions are initiated upon power-up, and the most recent conversion is stored in memory locations 60h and 61h of the Main Device, which are updated every t_{frame}. Temperature conversions do not occur during an active read or write to memory.

The value of each resistor is determined by the temperature-addressed look-up table. The look-up table assigns a unique value to each resistor for every 2°C increment with a 1°C hysteresis at a temperature transition over the operating temperature range (see Figure 4).

Table 9. Right Shifting

OUTPUT RANGE USED WITH ZERO RIGHT-SHIFTS	NUMBER OF RIGHT-SHIFTS NEEDED
0h....FFFFh	0
0h....7FFFh	1
0h....3FFFh	2
0h....1FFFh	3
0h....0FFFh	4

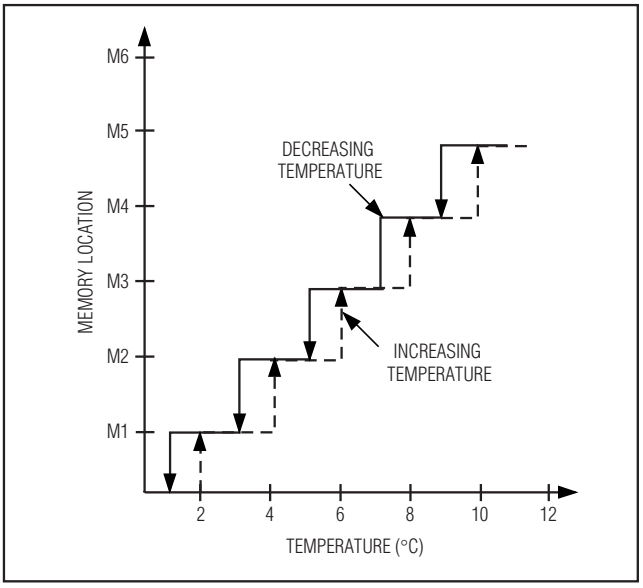


Figure 4. Look-Up Table Hysteresis

Power-Up and Low-Voltage Operation

During power-up, the device is inactive until V_{CC} exceeds the digital power-on-reset voltage (POD). At this voltage, the digital circuitry, which includes the 2-wire interface, becomes functional. However, EEPROM-backed registers/settings cannot be internally read (recalled into shadow SRAM) until V_{CC} exceeds the analog power-on-reset voltage (POA), at which time the remainder of the device becomes fully functional. Once V_{CC} exceeds POA, the RDYB bit in byte 6Eh of the Main Device memory is timed to go from a 1 to a 0 and indicates when analog-to-digital conversions begin. If V_{CC} ever dips below POA, the RDYB bit reads as a 1 again. Once a device exceeds POA and the EEPROM is recalled, the values remain active (recalled) until V_{CC} falls below POD.

For 2-wire device addresses sourced from EEPROM (ADFIX = 1), the device address defaults to A2h until V_{CC} exceeds POA and the EEPROM values are recalled. The Auxiliary Device (A0h) is always available within this voltage window (between POD and the EEPROM recall) regardless of the programmed state of ADEN.

Furthermore, as the device powers up, the V_{CC}lo alarm flag (bit 4 of 70h in Main Device) defaults to a 1 until the first V_{CC} analog-to-digital conversion occurs and sets or clears the flag accordingly.

2-Wire Operation

Clock and Data Transitions: The SDA pin is normally pulled high with an external resistor or device. Data on the SDA pin may only change during SCL-low time periods. Data changes during SCL-high periods will indicate a START or STOP condition depending on the conditions discussed below. See the timing diagrams in Figures 5 and 6 for further details.

START Condition: A high-to-low transition of SDA with SCL high is a START condition that must precede any other command. See the timing diagrams in Figures 5 and 6 for further details.

STOP Condition: A low-to-high transition of SDA with SCL high is a STOP condition. After a read or write sequence, the stop command places the DS1856 into a low-power mode. See the timing diagrams in Figures 5 and 6 for further details.

Acknowledge: All address and data bytes are transmitted through a serial protocol. The DS1856 pulls the SDA line low during the ninth clock pulse to acknowledge that it has received each word.

Standby Mode: The DS1856 features a low-power mode that is automatically enabled after power-on, after a STOP command, and after the completion of all internal operations.

Device Addressing: The DS1856 must receive an 8-bit device address, the slave address byte, following a START condition to enable a specific device for a read or write operation. The address is clocked into this part MSB to LSB. The address byte consists of either A2h or the value in Table 03, 8Ch for the Main Device or A0h for the Auxiliary Device, then the R/$\overline{W}$ bit. This byte must match the address programmed into Table 03, 8Ch or A0h (for the Auxiliary Device). If a device address match occurs, this part will output a zero for one clock cycle as an acknowledge and the corresponding block of memory is enabled (see the *Memory Organization* section). If the R/$\overline{W}$ bit is high, a read operation is initiated. If the R/$\overline{W}$ is low, a write operation is initiated (see the *Memory Organization* section). If the address does not match, this part returns to a low-power mode.

Write Operations

After receiving a matching address byte with the R/$\overline{W}$ bit set low, if there is no write protect, the device goes into the write mode of operation (see the *Memory Organization* section). The master must transmit an 8-bit EEPROM memory address to the device to define the address where the data is to be written. After the byte has been received, the DS1856 transmits a zero for one clock cycle to acknowledge the address has been received. The master must then transmit an 8-bit data word to be written into this address. The DS1856 again transmits a zero for one clock cycle to acknowledge the receipt of the data. At this point, the master must terminate the write operation with a STOP condition. The DS1856 then enters an internally timed write process t_W to the EEPROM memory. All inputs are disabled during this byte write cycle.

Page Write

The DS1856 is capable of an 8-byte page write. A page is any 8-byte block of memory starting with an address evenly divisible by eight and ending with the starting address plus seven. For example, addresses 00h through 07h constitute one page. Other pages would be addresses 08h through 0Fh, 10h through 17h, 18h through 1Fh, etc.

A page write is initiated the same way as a byte write, but the master does not send a STOP condition after the first byte. Instead, after the slave acknowledges the data byte has been received, the master can send up to seven more bytes using the same nine-clock sequence. The master must terminate the write cycle with a STOP condition or the data clocked into the DS1856 will not be latched into permanent memory.

The address counter rolls on a page during a write. The counter does not count through the entire address space as during a read. For example, if the starting address is 06h and 4 bytes are written, the first byte goes into address 06h. The second goes into address 07h. The third goes into address 00h (not 08h). The fourth goes into address 01h. If 9 bytes or more are written before a STOP condition is sent, the first bytes sent are overwritten. Only the last 8 bytes of data are written to the page.

Acknowledge Polling: Once the internally timed write has started and the DS1856 inputs are disabled, acknowledge polling can be initiated. The process involves transmitting a START condition followed by the device address. The R/$\overline{W}$ bit signifies the type of operation that is desired. The read or write sequence will only be allowed to proceed if the internal write cycle has completed and the DS1856 responds with a zero.

Read Operations

After receiving a matching address byte with the R/$\overline{W}$ bit set high, the device goes into the read mode of operation. There are three read operations: current address read, random read, and sequential address read.

Current Address Read

The DS1856 has an internal address register that maintains the address used during the last read or write operation, incremented by one. This data is maintained as long as V_{CC} is valid. If the most recent address was the last byte in memory, then the register resets to the first address.

Once the device address is clocked in and acknowledged by the DS1856 with the R/$\overline{W}$ bit set to high, the current address data word is clocked out. The master does not respond with a zero, but does generate a STOP condition afterwards.

Single Read

A random read requires a dummy byte write sequence to load in the data byte address. Once the device and data address bytes are clocked in by the master and acknowledged by the DS1856, the master must generate another START condition. The master now initiates a current address read by sending the device address with the R/$\overline{W}$ bit set high. The DS1856 acknowledges the device address and serially clocks out the data byte.

Sequential Address Read

Sequential reads are initiated by either a current address read or a random address read. After the master receives the first data byte, the master responds with an acknowledge. As long as the DS1856 receives this acknowledge after a byte is read, the master can clock out additional data words from the DS1856. After reaching address FFh, it resets to address 00h.

The sequential read operation is terminated when the master initiates a STOP condition. The master does not respond with a zero.

The following section provides a detailed description of the 2-wire theory of operation.

2-Wire Serial-Port Operation

The 2-wire serial-port interface supports a bidirectional data transmission protocol with device addressing. A device that sends data on the bus is defined as a transmitter, and a device that receives data as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are slaves. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The DS1856 operates as a slave on the 2-wire bus. Connections to the bus are made through the open-drain I/O lines SDA and SCL. The following I/O terminals control the 2-wire serial port: SDA, SCL. Timing diagrams for the 2-wire serial port can be found in Figures 5 and 6. Timing information for the 2-wire serial port is provided in the *AC Electrical Characteristics* table for 2-wire serial communications.

The following bus protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain high.

Start data transfer: A change in the state of the data line from high to low while the clock is high defines a START condition.

Stop data transfer: A change in the state of the data line from low to high while the clock line is high defines the STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the high period of the clock signal. The data on the line can be changed during the low period of the clock signal. There is one clock pulse per bit of data. Figures 5 and 6 detail how data transfer is accomplished on the 2-wire bus. Depending on the state of the R/$\overline{W}$ bit, two types of data transfer are possible.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

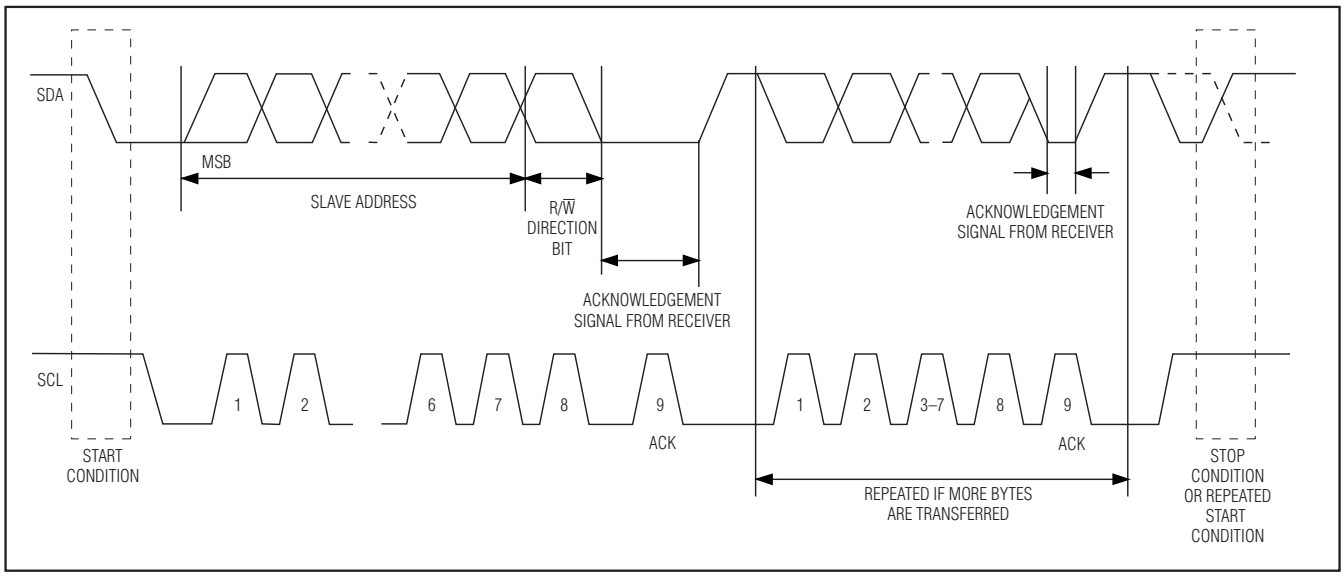


Figure 5. 2-Wire Data Transfer Protocol

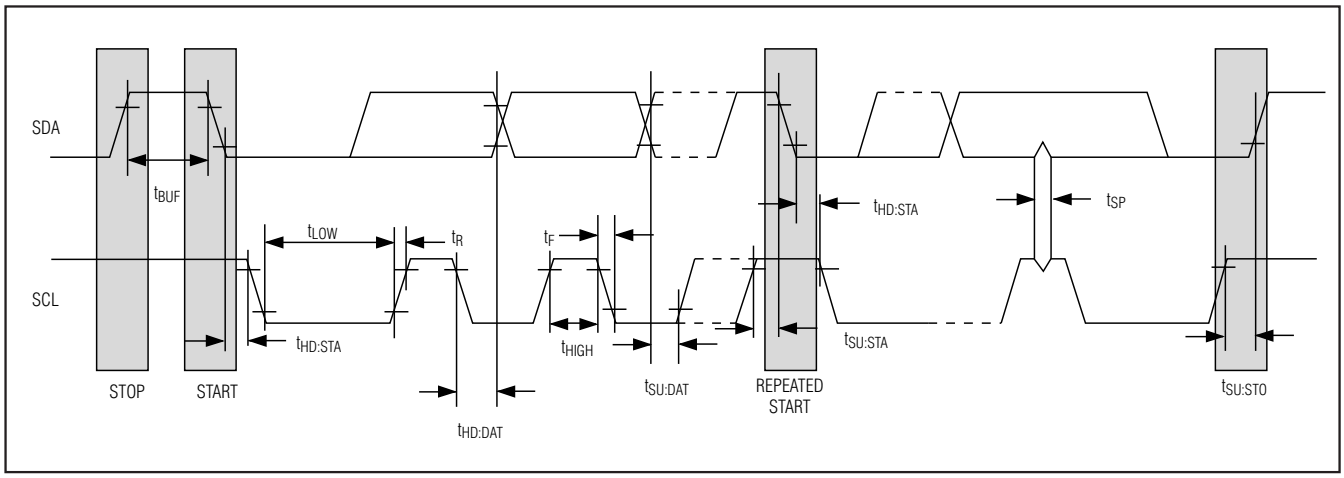


Figure 6. 2-Wire AC Characteristics

Within the bus specifications, a standard mode (100kHz clock rate) and a fast mode (400kHz clock rate) are defined. The DS1856 works in both modes.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the byte has been received. The master device must generate an extra clock pulse, which is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable low during the high period of the acknowledge-related clock pulse. Setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line high to enable the master to generate the STOP condition.

1) **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the command/control byte. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte.
2) **Data transfer from a slave transmitter to a master receiver.** The master transmits the first byte (the command/control byte) to the slave. The slave then returns an acknowledge bit. Next follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a not acknowledge can be returned.

The master device generates all serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released.

The DS1856 can operate in the following two modes:

1) **Slave Receiver Mode:** Serial data and clock are received through SDA and SCL, respectively. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after the slave (device) address and direction bit have been received.
2) **Slave Transmitter Mode:** The first byte is received and handled as in the slave receiver mode. However, in this mode the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the DS1856, while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

Dual, Temperature-Controlled Resistors with Internally Calibrated Monitors and Password Protection

Ordering Information (continued)

PART	RES0/RES1 RESISTANCE (kΩ)	PIN-PACKAGE
DS1856B-050	50/50	16 CSBGA
DS1856B-050/T&R	50/50	16 CSBGA
DS1856B-050+	50/50	16 CSBGA
DS1856B-050+T&R	50/50	16 CSBGA
DS1856E-050	50/50	16 TSSOP
DS1856E-050/T&R	50/50	16 TSSOP
DS1856E-020	20/20	16 TSSOP
DS1856E-020/T&R	20/20	16 TSSOP
DS1856B-020	20/20	16 CSBGA
DS1856B-020/T&R	20/20	16 CSBGA
DS1856B-020+	20/20	16 CSBGA
DS1856B-020+T&R	20/20	16 CSBGA
DS1856B-030	30/10	16 CSBGA
DS1856E-030+	30/10	16 TSSOP
DS1856E-030+T&R	30/10	16 TSSOP
DS1856B-030+	30/10	16 CSBGA
DS1856B-030+T&R	30/10	16 CSBGA
DS1856E-002	10/2.5	16 TSSOP
DS1856E-002/T&R	10/2.5	16 TSSOP
DS1856B-002	10/2.5	16 CSBGA
DS1856B-002/T&R	10/2.5	16 CSBGA
DS1856B-025	2.5/2.5	16 CSBGA

+Denotes lead-free package.
T&R denotes tape-and-reel package.
***Note:** All devices are specified over the -40°C to +95°C temperature range.*

Chip Information

TRANSISTOR COUNT: 51,061
SUBSTRATE CONNECTED TO GROUND

Package Information

For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.