TEXAS INSTRUMENTS

DRV3245Q-Q1
SLVSEE3B –NOVEMBER 2017–REVISED OCTOBER 2019

DRV3245Q-Q1 3-Phase Automotive Gate Driver Unit (GDU) With High Performance Sensing, Protection and Diagnostics

1 Features

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 1: –40°C to +125°C, T_A
- SafeTI™ semiconductor component
  - Developed according to the applicable requirements of ISO 26262
- 4.5-V to 45-V operating voltage
- Programmable peak gate drive currents up to 1A
- Charge-pump gate driver for 100% Duty Cycle
- Current-shunt amplifiers and phase comparators
  - A / C Device: 3 current-shunt amplifiers[1] and 3-phase comparators with status through SPI

[1] C device : Low-drift offset high-precision amplifiers

  - B Device: 2 current-shunt amplifiers and 3-phase comparators with real-time monitor through digital pins
- 3-PWM or 6-PWM input control up to 20 kHz
- Single PWM-mode commutation capability
- Supports both 3.3-V and 5-V digital interface
- Serial peripheral interface (SPI)
- Thermally-enhanced 48-Pin HTQFP
- Protection features:
  - Internal regulators, battery voltage monitor
  - SPI CRC
  - Clock monitor
  - Analog built-in self test
  - Programmable dead-time control
  - MOSFET shoot-through prevention
  - MOSFET V_{DS} overcurrent monitors
  - Gate-source voltage real time monitor
  - Overtemperature warning and Shutdown

2 Applications

- 12-V automotive motor-control applications
  - Electrical power steering (EPS, EHPS)
  - Electrical brake and brake assist
  - Transmissions and pumps

3 Description

The DRV3245Q-Q1 device is a FET gate driver IC for three-phase motor-drive applications designed according to the applicable requirements of ISO 26262 for functional safety applications. The device provides three half-bridge drivers each capable of driving a high-side and low-side N-channel MOSFET while also providing sophisticated protection and monitoring of the FETs. A charge-pump driver enables 100% duty cycle and supports low battery voltages during cold-crank operation. The integration of current-sense amplifiers, integrated phase comparators, and SPI-based configuration of the driver and its peripherals enable reduction of the bill of materials (BOM) and space on the printed circuit board (PCB) because of the elimination of most external and passive components.

The DRV3245Q-Q1 device also integrates diagnostics and protection for each internal block and provides support for common system diagnostic checks each of which can be instantiated and reported through SPI. This flexibility of the integrated features allows the device to integrate seamlessly into a variety of safety architectures.

Device Information [1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV3245Q-Q1	HTQFP (48)	7.00 mm × 7.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
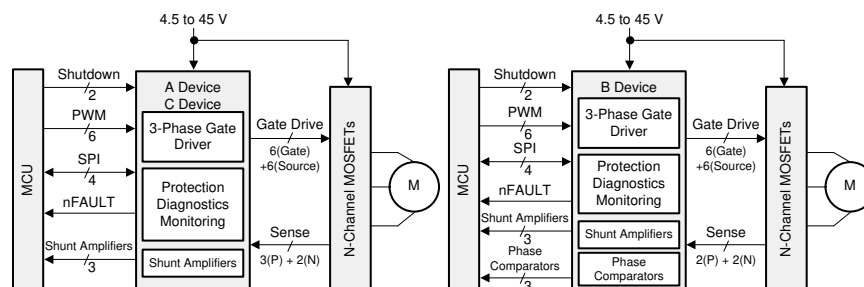
Simplified Schematic

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2018) to Revision B	**Page**

- Added DRV3245C device 1

Changes from Original (November 2017) to Revision A	**Page**

- Changed the device status from: *Advance Information* to: *Production Data* 1

Product Folder Links: *DRV3245Q-Q1*

5 Device and Documentation Support

5.1 Device Support

5.1.1 Device Nomenclature

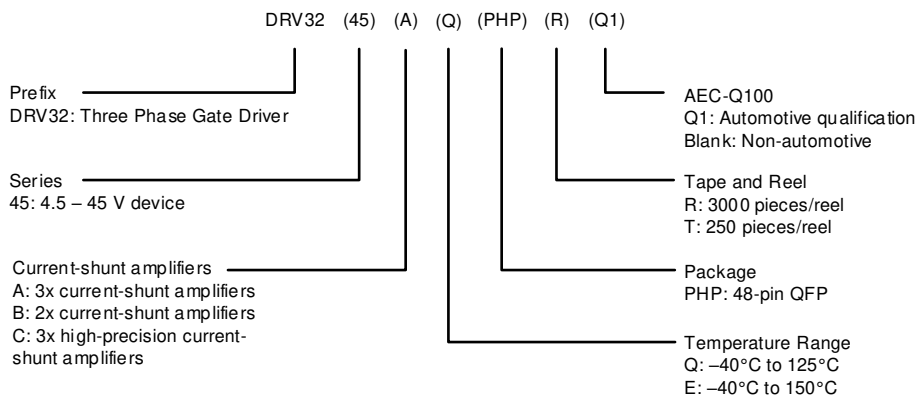Figure 1 shows a legend for reading the complete orderable device name for the DRV3245Q-Q1 device

DRV32 (45) (A) (Q) (PHP) (R) (Q1)

Prefix
DRV32: Three Phase Gate Driver

Series
45: 4.5 – 45 V device

Current-shunt amplifiers
A: 3x current-shunt amplifiers
B: 2x current-shunt amplifiers
C: 3x high-precision current-shunt amplifiers

AEC-Q100
Q1: Automotive qualification
Blank: Non-automotive

Tape and Reel
R: 3000 pieces/reel
T: 250 pieces/reel

Package
PHP: 48-pin QFP

Temperature Range
Q: –40°C to 125°C
E: –40°C to 150°C

Figure 1. Device Nomenclature

5.2 Documentation Support

For related documentation see the following:
• Texas Instruments, *PowerPAD™ Thermally Enhanced Package* application report
• Texas Instruments, *PowerPAD™ Made Easy* application report
• Texas Instruments, *Sensored 3-Phase BLDC Motor Control Using MSP430* application report
• Texas Instruments, *Understanding IDRIVE and TDRIVE in TI Motor Gate Drivers* application report

5.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

5.4 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

5.5 Trademarks

SafeTI, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

5.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.7 Glossary

SLYZ022 — *TI Glossary*.

   This glossary lists and explains terms, acronyms, and definitions.

6   Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV3245AQPHPRQ1	ACTIVE	HTQFP	PHP	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DR3245AQ	Samples
DRV3245BQPHPRQ1	ACTIVE	HTQFP	PHP	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DR3245BQ	Samples
DRV3245CQPHPRQ1	ACTIVE	HTQFP	PHP	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DR3245CQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV3245AQPHPRQ1	HTQFP	PHP	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
DRV3245BQPHPRQ1	HTQFP	PHP	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
DRV3245CQPHPRQ1	HTQFP	PHP	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV3245AQPHPRQ1	HTQFP	PHP	48	1000	350.0	350.0	43.0
DRV3245BQPHPRQ1	HTQFP	PHP	48	1000	350.0	350.0	43.0
DRV3245CQPHPRQ1	HTQFP	PHP	48	1000	350.0	350.0	43.0

PHP (S−PQFP−G48)   PowerPAD™ PLASTIC QUAD FLATPACK
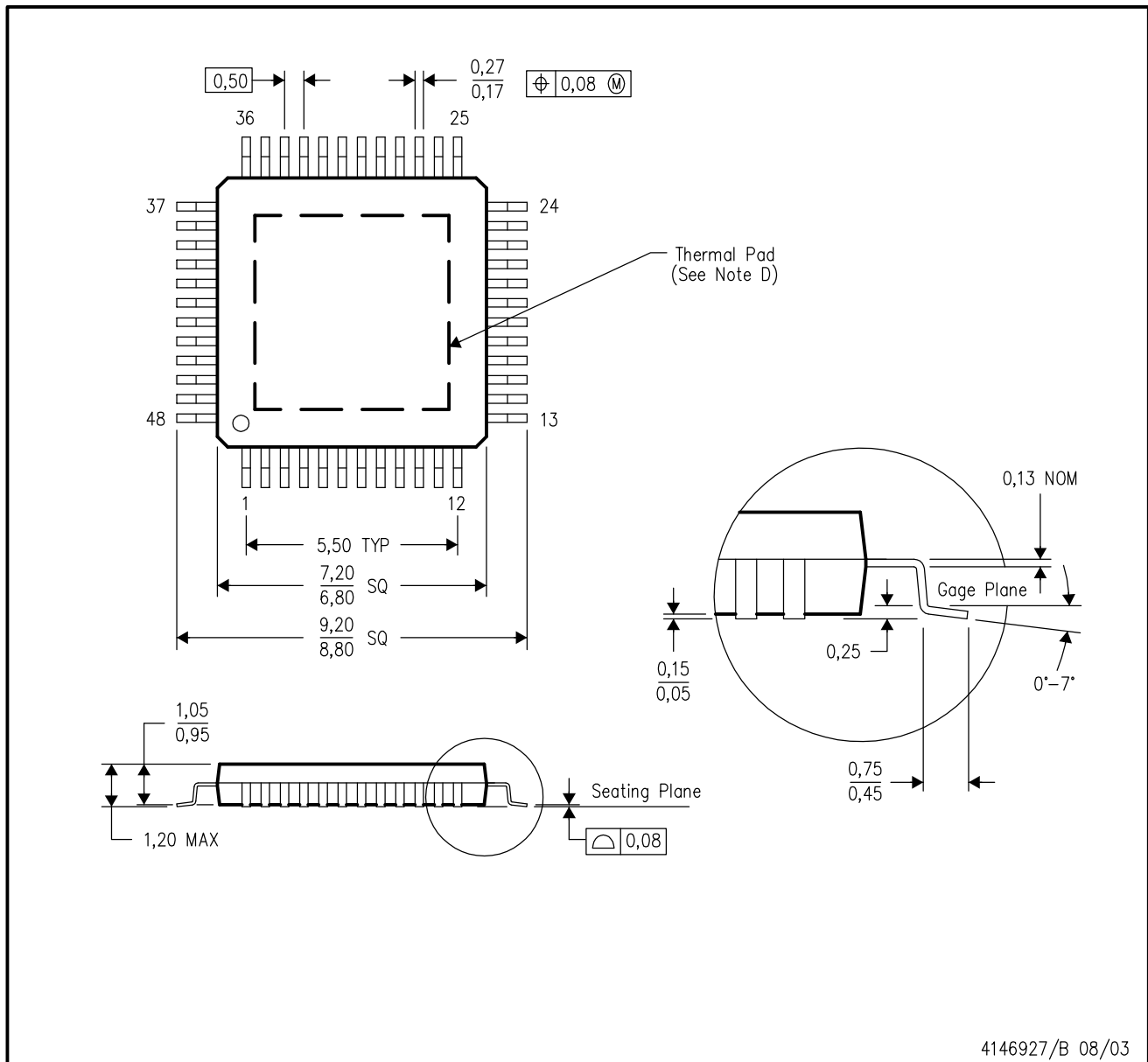
Thermal Pad
(See Note D)

0,50

0,27
0,17

⊕ 0,08 Ⓜ

36   25

37   24

48   13

1   12

5,50 TYP

7,20
6,80 SQ

9,20
8,80 SQ

0,13 NOM

Gage Plane

0,15
0,05

0,25

0°−7°

0,75
0,45

1,05
0,95

1,20 MAX

Seating Plane

◁ 0,08

4146927/B 08/03

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion
         D.   This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad
              Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding
              recommended board layout.   This document is available at www.ti.com <http://www.ti.com>.
         E.   Falls within JEDEC MS−026

PowerPAD is a trademark of Texas Instruments.

TEXAS
INSTRUMENTS
www.ti.com

PHP (S−PQFP−G48)   PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.
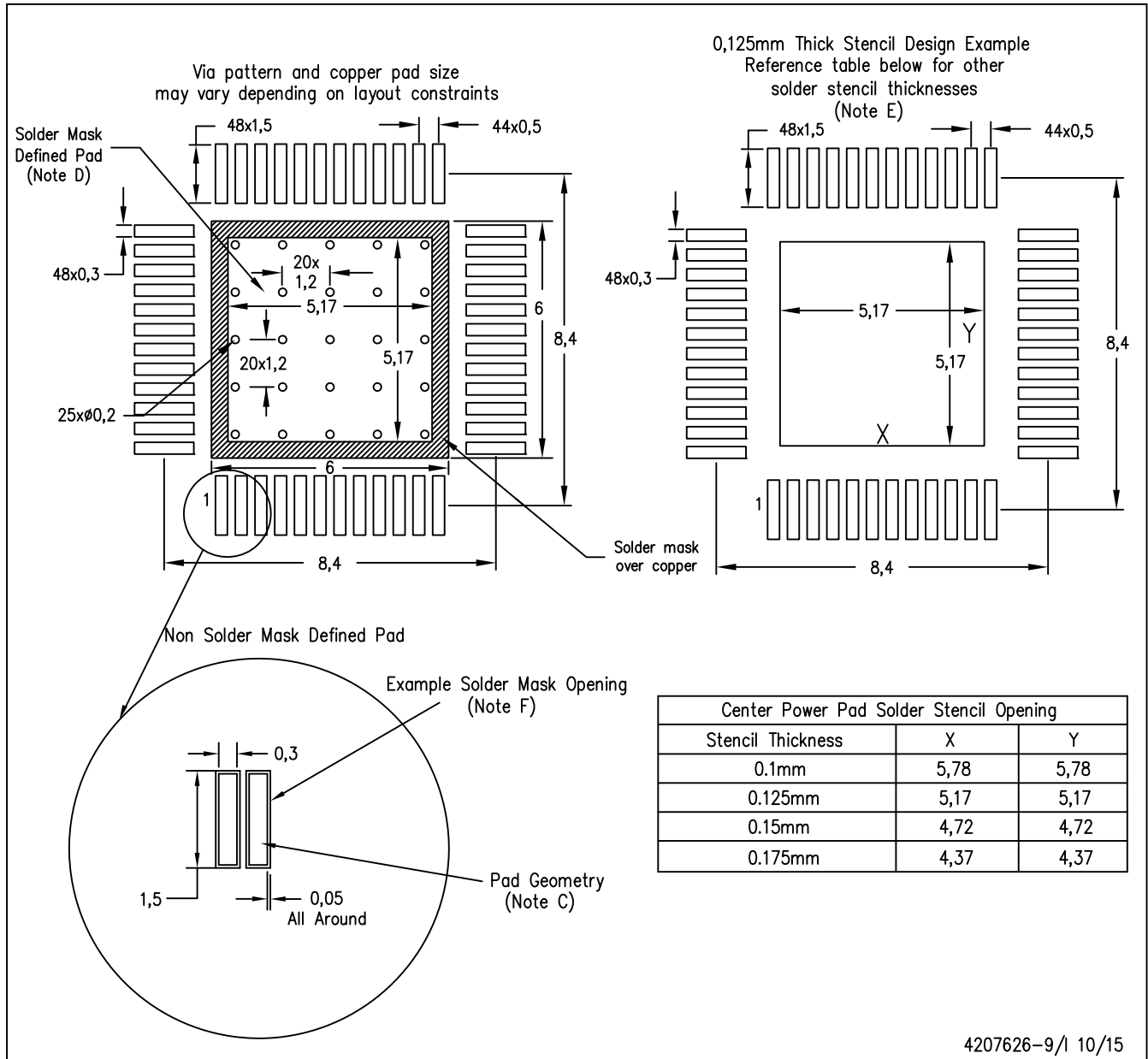

Top View
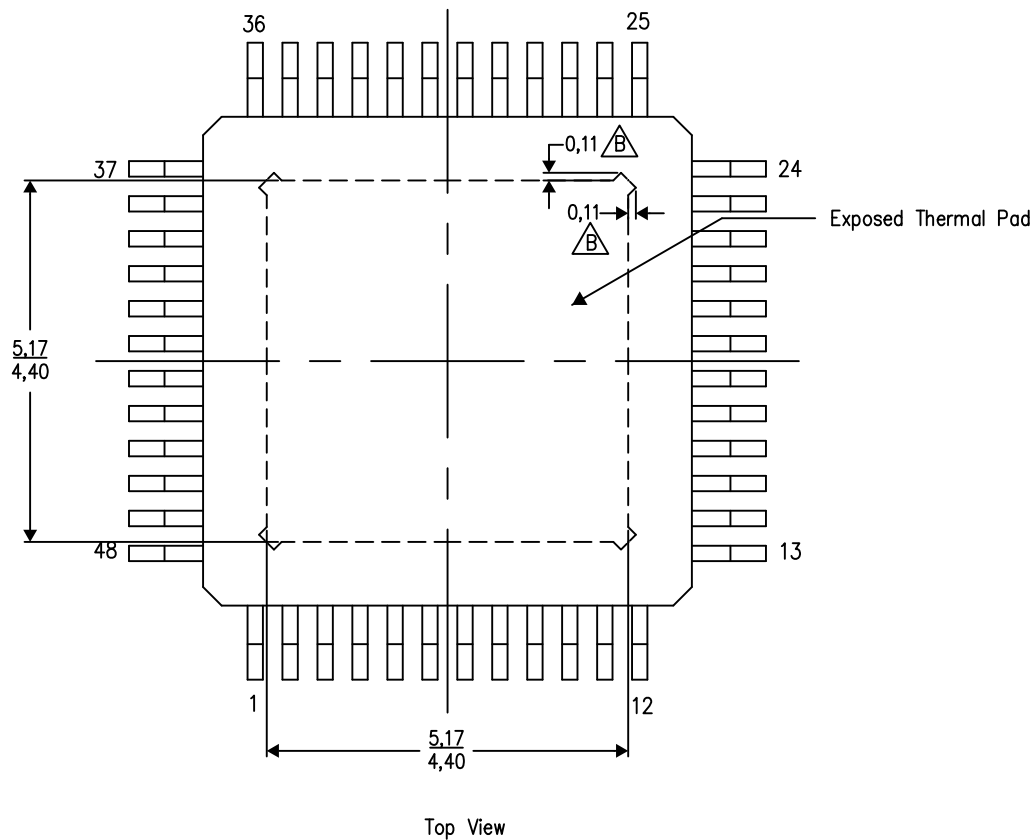
Exposed Thermal Pad Dimensions

4206329−7/P 03/15

NOTE: A. All linear dimensions are in millimeters

  B. Tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

TEXAS
INSTRUMENTS
www.ti.com

PHP (S–PQFP–G48)   PowerPAD™ PLASTIC QUAD FLATPACK

Via pattern and copper pad size
may vary depending on layout constraints

0,125mm Thick Stencil Design Example
Reference table below for other
solder stencil thicknesses
(Note E)

Solder Mask
Defined Pad
(Note D)

48x1,5   44x0,5

48x0,3

20x
1,2

5,17

20x1,2   5,17

25x⌀0,2

6

8,4

6

1

8,4

Solder mask
over copper

48x1,5   44x0,5

48x0,3

5,17

Y

5,17

X

8,4

1

8,4

Non Solder Mask Defined Pad

Example Solder Mask Opening
(Note F)

0,3

1,5

0,05
All Around

Pad Geometry
(Note C)

Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	5,78	5,78
0.125mm	5,17	5,17
0.15mm	4,72	4,72
0.175mm	4,37	4,37

4207626–9/I 10/15

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Publication IPC–7351 is recommended for alternate designs.
         D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad
             Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets
             for specific thermal information, via requirements, and recommended board layout. These documents are available at
             www.ti.com <http://www.ti.com>.
         E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
         F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting
             options for vias placed in the thermal pad.
PowerPAD is a trademark of Texas Instruments

TEXAS
INSTRUMENTS
www.ti.com

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated