

# Mercury+ XU1 SoC Module

## User Manual

### Purpose

The purpose of this document is to present the characteristics of Mercury+ XU1 SoC module to the user, and to provide the user with a comprehensive guide to understanding and using the Mercury+ XU1 SoC module.

### Summary

This document first gives an overview of the Mercury+ XU1 SoC module followed by a detailed description of its features and configuration options. In addition, references to other useful documents are included.

Product Information	Code	Name
Product	ME-XU1	Mercury+ XU1 SoC Module

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Written by	DIUN	Design Engineer	04.05.2016
Verified by	GLAC	Design Expert	12.05.2016
Approved by	SJOK	Product Manager	06.09.2022

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## Document History

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# 1 Overview

## 1.1 General

### 1.1.1 Introduction

The Mercury+ XU1 SoC module combines the Xilinx Zynq® UltraScale+ MPSoC (Multiprocessor System-on-Chip) device with USB 3.0, PCIe® Gen2 ×4, two USB 2.0 PHYs, two Gigabit Ethernet PHYs, DDR4 SDRAM with Error Correction Code (ECC), eMMC flash, multi-gigabit transceivers, high-speed LVDS I/O, and is available in industrial temperature range, forming a complete and powerful embedded processing system.

The use of the Mercury+ XU1 SoC module, in contrast to building a custom MPSoC hardware, significantly reduces development effort and redesign risk and improves time-to-market for the embedded system.

Together with Mercury+ base boards, the Mercury+ XU1 SoC module allows the user to quickly build a system prototype and start with application development.

The Enclustra Build Environment [17] is available for the Mercury+ XU1 SoC module. This build system allows the user to quickly set up and run Linux on any Enclustra SoC module. It allows the user to choose the desired target and download all the required binaries, such as bitstream and FSBL (First Stage Boot Loader). It downloads and compiles all required software, such as U-Boot, Linux, and BusyBox based root file system.

### 1.1.2 Warranty

Please refer to the General Business Conditions, available on the Enclustra website [1].

#### Warning!

*Please note that the warranty of an Enclustra module is voided if the FPGA fuses are blown. This operation is done at own risk, as it is irreversible. Enclustra cannot test the module in case of a warranty product return.*

### 1.1.3 RoHS

The Mercury+ XU1 SoC module is designed and produced according to the Restriction of Hazardous Substances (RoHS) Directive (2011/65/EC).

### 1.1.4 Disposal and WEEE

The Mercury+ XU1 SoC module must be properly disposed of at the end of its life.

The Waste Electrical and Electronic Equipment (WEEE) Directive (2002/96/EC) is not applicable for the Mercury+ XU1 SoC module.

### 1.1.5 Safety Recommendations and Warnings

Mercury+ modules are not designed to be "ready for operation" for the end-user. These can only be used in combination with suitable base boards. Proper configuration of the hardware before usage is required.

Ensure that the power supply is disconnected from the board before inserting or removing the Mercury+ XU1 SoC module, connecting interfaces, or connecting jumpers.

Touching the capacitors of the DC-DC converters can lead to voltage peaks and permanent damage; over-voltage on power or signal lines can also cause permanent damage to the module.

### 1.1.6 Electrostatic Discharge

Electronic boards are sensitive to electrostatic discharge (ESD). Please ensure that the product is handled with care and only in an ESD-protected environment.

### 1.1.7 Electromagnetic Compatibility

The Mercury+ XU1 SoC module is a Class A product (as defined in IEC 61000-3-2 standard) and is not intended for use in domestic environments. The product may cause electromagnetic interference, for which appropriate measures must be taken.

## 1.2 Features

- Xilinx Zynq® UltraScale+™ MPSoC
  - XCZU6CG/XCZU6EG/XCZU9EG/XCZU15EG device
  - FFVC900 package
  - Dual-/Quad-core ARM® Cortex™-A53 MPCore™ up to 1.5 GHz
  - Dual-core ARM® Cortex™-R5 MPCore™ up to 600 MHz
  - Mali-400 MP2 GPU (not for CG variants)
  - Xilinx 16nm FinFET+ FPGA fabric
- 294 user I/Os
  - 14 ARM peripheral I/Os (SPI, SDIO, CAN, I2C, UART)
  - 200 FPGA I/Os (single-ended, differential or analog)
    - 152 HP I/Os (up to 1.8 V)
      - 148 I/Os up to 1.8 V
      - 4 I/Os up to 3.3 V (routed via level shifters)
    - 48 HD I/Os (up to 3.3 V)
  - 80 MGT signals (clock and data)
    - 60 GTH MGT signals
    - 20 GTR MGT signals
- *Speedgrade 1 devices*: 12 GTH MGTs @ 12.5 Gbit/sec and 6 reference input clock differential pairs
- *Other devices*: 12 GTH MGTs @ 16.375 Gbit/sec and 6 reference input clock differential pairs
- 4 GTR MGTs @ 6 Gbit/sec and 2 reference input clock differential pairs
- PCIe Gen2 ×4 (Xilinx built-in PCIe hard block using GTR lines)
- Up to 4 GB DDR4 SDRAM with ECC
- 64 MB quad SPI flash
- 16 GB eMMC flash
- 2 × Gigabit Ethernet PHY (one PHY shared with one of the USB PHYs)
- 2 × USB 2.0 PHYs
  - PHY0 configured as host or device
  - PHY1 configured as host (shared with one of the Gigabit Ethernet PHYs)
- USB 3.0 (Xilinx built-in USB 3.0 hard block using GTR lines)
- Real-time clock
- CAN, UART, SPI, I2C, SDIO/MMC
- 5 to 15 V supply voltage

Starting with revision 3 modules, 4 additional GTH transceivers and 2 differential clock pairs may be routed to the module connector, by using the "G1" assembly variants. Please refer to Section 2.9.2 for details on the assembly variants and MGT connectivity.



## 1.3 Deliverables

- Mercury+ XU1 SoC module
- Mercury+ XU1 SoC module documentation, available via download:
  - Mercury+ XU1 SoC Module User Manual (this document)
  - Mercury+ XU1 SoC Module Reference Design [2]
  - Mercury+ XU1 SoC Module IO Net Length Excel Sheet [3]
  - Mercury+ XU1 SoC Module FPGA Pinout Excel Sheet [4]
  - Mercury+ XU1 SoC Module FPGA Pinout Assembly Variants Excel Sheet [5]
  - Mercury+ XU1 SoC Module User Schematics (PDF) [6]
  - Mercury+ XU1 SoC Module Known Issues and Changes [7]
  - Mercury+ XU1 SoC Module Footprint (Altium, Eagle, Orcad and PADS) [8]
  - Mercury+ XU1 SoC Module 3D Model (PDF) [9]
  - Mercury+ XU1 SoC Module STEP 3D Model [10]
  - Mercury Mars Module Pin Connection Guidelines [11]
  - Mercury Master Pinout [12]
  - Mercury Heatsink Application Note [21]
  - Enclustra Build Environment [17] (Linux build environment; refer to Section 1.4.2 for details)
  - Enclustra Build Environment How-To Guide [18]
  - Petalinux BSP and Documentation [19]

## 1.4 Accessories

### 1.4.1 Reference Design

The Mercury+ XU1 SoC module reference design features an example configuration for the Zynq UltraScale+ MPSoC device, together with an example top level HDL file for the user logic.

A number of software applications are available for the reference design, that show how to initialize the peripheral controllers and how to access the external devices. Pre-compiled binaries are included in the archive, so that the user can easily check that the hardware is functional.

The reference design can be downloaded from Github: <https://github.com/enclustra>.

### 1.4.2 Enclustra Build Environment

The Enclustra Build Environment (EBE) [17] enables the user to quickly set up and run Linux on any Enclustra SoC module or system board. It allows the user to choose the desired target, and download all the required binaries, such as bitstream and FSBL. It downloads and compiles all required software, such as U-Boot, Linux, and BusyBox based root file system.

The Enclustra Build Environment features a graphical user interface (GUI) and a command line interface (CLI) that facilitates the automatic build flow.

The Enclustra Build Environment How-To Guide [18] describes in more detail how to use the EBE to customize the provided software for the user application. The document provides information on the configuration options for U-boot, Linux kernel and Buildroot, debugging possibilities for Linux applications, customization of device trees and integration of existing or new kernel drivers.

### 1.4.3 Petalinux BSP

The Enclustra Petalinux BSPs enable the user to quickly set up a Petalinux project and to run Linux on the Enclustra SoC module or system board.

The documentation [19] describes the build process in detail and allows a user without Petalinux knowledge to build and run the desired design on the target hardware.

#### **1.4.4 Enclustra Heat Sink**

For Mercury modules an Enclustra heat sink is available for purchase along with the product. Please refer to section 2.11.6 for further information on the available cooling options.

#### **1.4.5 Mercury+ PE1 Base Board**

The Mercury+ PE1 is a versatile PCIe® x4 base board equipped with a multitude of I/O interfaces for use with the Mercury/Mercury+ family of FPGA and SoC modules, providing a head start for building custom FPGA and SoC based hardware systems.

It is compatible with a multitude of FMC boards from different suppliers to use in data acquisition systems, motor control, display and camera interfaces, software defined radio and more. The board is equally well suited for rapid prototyping and for building FPGA systems without designing custom hardware.

For more information visit

<https://www.enclustra.com/en/products/base-boards/mercury-pe1-200-300-400/>.

Please note that the available features depend on the equipped Mercury module type and on the selected base board variant.

#### **1.4.6 Mercury+ PE3 Base Board**

The Mercury+ PE3 is a versatile PCIe® x8 base board equipped with a multitude of I/O interfaces for use with the Mercury/Mercury+ family of FPGA and SoC modules, providing a head start for building custom FPGA and SoC based hardware systems.

This high performance base board provides a versatile set of I/O connectivity options, specialized for high-speed communication and video applications, including SFP+, QSFP+, HDMI, USB Type-C and Firefly. The board is equally well suited for rapid prototyping and for building FPGA systems without designing custom hardware.

For more information visit <https://www.enclustra.com/en/products/base-boards/mercury-pe3/>.

Please note that the available features depend on the equipped Mercury module type and on the selected base board variant.

#### **1.4.7 Mercury+ ST1 Base Board**

The Mercury+ ST1 board is a compact, low-cost base board equipped with a multitude of I/O interfaces for use with the Mercury/Mercury+ family of FPGA and SoC modules.

It provides a versatile set of I/O connectivity options, specialized for video applications, including MIPI, HDMI and SFP+. The board is equally well suited for rapid prototyping and for building FPGA systems without designing custom hardware.

For more information visit <https://www.enclustra.com/en/products/base-boards/mercury-st1/>.

Please note that the available features depend on the equipped Mercury module type and on the selected base board variant.

### **1.5 Xilinx Tool Support**

The MPSoC devices equipped on the Mercury+ XU1 SoC module are supported by the Vivado HL Design Edition software, for which a paid license is required. Please contact Xilinx for further information.

# 2 Module Description

## 2.1 Block Diagram

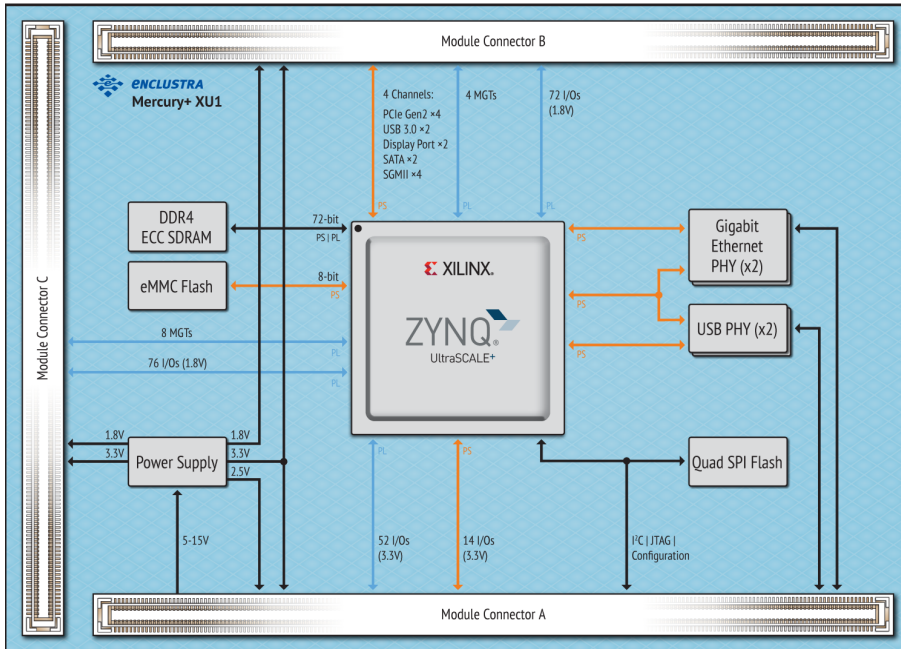


Figure 1: Hardware Block Diagram

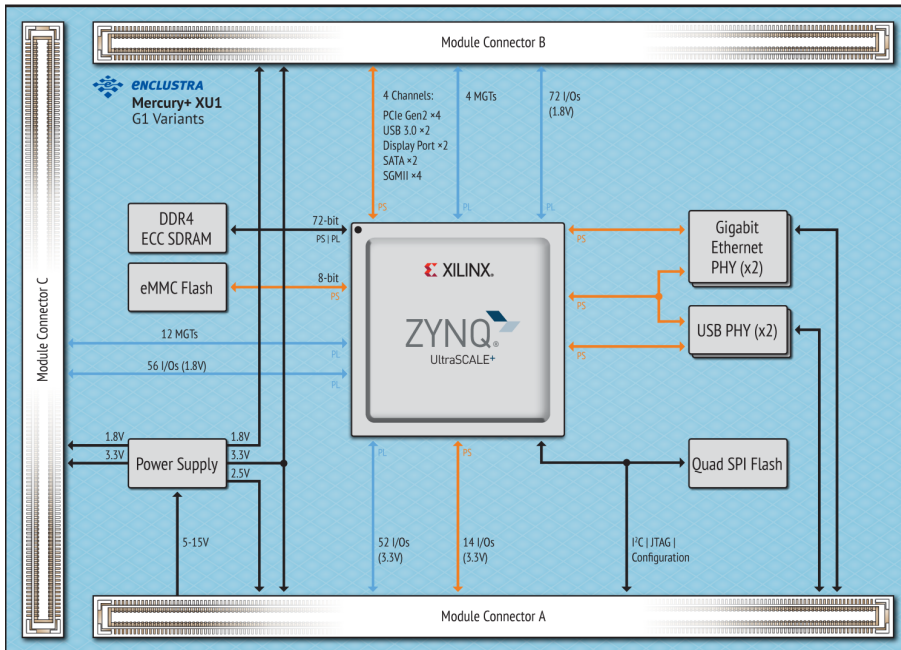


Figure 2: Hardware Block Diagram - G1 Variants

The main component of the Mercury+ XU1 SoC module is the Xilinx Zynq UltraScale+ MPSoC device. Most of its I/O pins are connected to the Mercury+ module connector, making up to 214 regular user I/Os available to the user. Further, up to twenty MGT pairs are available on the module connector, making possible the implementation of several high-speed protocols such as PCIe Gen2  $\times 4$  and USB 3.0 (simultaneous usage of all the interfaces is limited to the available hardware resources i.e. number of transceivers and lane mapping).

The "G1" module variants offer 16 GTH MGT lines on the module connector at the trade-off of having only 194 regular I/Os (instead of 214). Section 2.9.2 describes in more detail the module assembly variants and routing options around the Processing System (PS) and Programmable Logic (PL) transceivers and I/Os.

The MPSoC device can boot from the on-board QSPI flash, from the eMMC flash or from an external SD card. For development purposes, a JTAG interface is connected to Mercury module connector.

The available standard configurations include a 16 GB eMMC flash, a 64 MB quad SPI flash and 2 GB or 4 GB DDR4 SDRAM.

Further, the module is equipped with two Gigabit Ethernet PHYs and two USB 2.0 PHYs, making it ideal for communication applications.

A real-time clock is available on the Xilinx Zynq UltraScale+ MPSoC device.

On-board clock generation is based on a 33.33 MHz crystal oscillator. In addition, two oscillators delivering 100 MHz and 27 MHz reference clocks for the MGT GTR lines, are equipped on the module.

The module's internal supply voltages are generated from a single input supply of 5 - 15 V DC. Some of these voltages are available on the Mercury module connectors to supply circuits on the base board.

Five LEDs are connected to the MPSoC pins for status signaling.

## 2.2 Module Configuration and Product Models

Table 1 describes the available standard module configurations. Custom configurations are available; please contact Enclustra for further information.

Product Model	MPSoC	DDR4 SDRAM	DDR4 ECC	GTH MGTs	Temperature Range
ME-XU1-6CG-1E-D11E-G1	XCZU6CG-1FFVC900E	2 GB	✓	16	0 to +85° C
ME-XU1-6CG-1E-D11E	XCZU6CG-1FFVC900E	2 GB	✓	12	0 to +85° C
ME-XU1-6EG-1I-D11E-G1	XCZU6EG-1FFVC900I	2 GB	✓	16	-40 to +85° C
ME-XU1-6EG-1I-D11E	XCZU6EG-1FFVC900I	2 GB	✓	12	-40 to +85° C
ME-XU1-9EG-1E-D11E-G1	XCZU9EG-1FFVC900E	2 GB	✓	16	0 to +85° C
ME-XU1-9EG-2I-D12E	XCZU9EG-2FFVC900I	4 GB	✓	12	-40 to +85° C
ME-XU1-9EG-2I-D12E-G1	XCZU9EG-2FFVC900I	4 GB	✓	16	-40 to +85° C
ME-XU1-9EG-3E-D12E	XCZU9EG-3FFVC900E	4 GB	✓	12	0 to +85° C
ME-XU1-15EG-1E-D12E-G1	XCZU15EG-1FFVC900E	4 GB	✓	16	0 to +85° C
ME-XU1-15EG-2I-D12E	XCZU15EG-2FFVC900I	4 GB	✓	12	-40 to +85° C
ME-XU1-15EG-2I-D12E-G1	XCZU15EG-2FFVC900I	4 GB	✓	16	-40 to +85° C

Table 1: Standard Module Configurations

Starting with revision 3 modules, 4 additional GTH transceivers and 2 differential clock pairs may be routed to the module connector, by using the "G1" assembly variants. Please refer to Section 2.9.2 for details on the assembly variants and MGT connectivity.

The product model indicates the module type and main features. Figure 3 describes the fields within the product model.

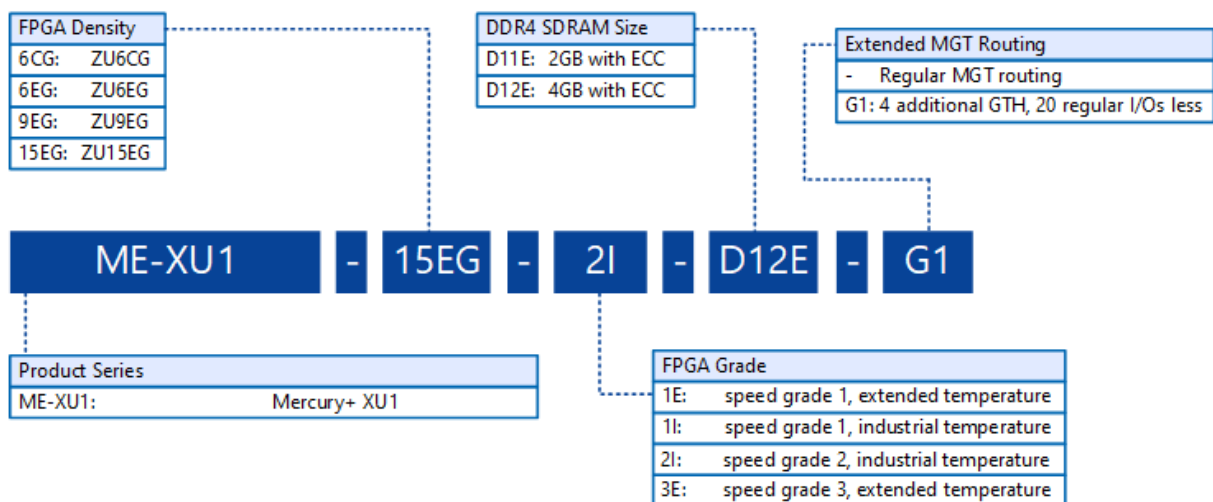


Figure 3: Product Model Fields

Please note that for the first revision modules or early access modules, the product model may not respect entirely this naming convention. Please contact Enclustra for details on this aspect.

## 2.3 EN-Numbers and Part Names

Every module is uniquely labeled, showing the EN-number and serial number. An example is presented in Figure 4.

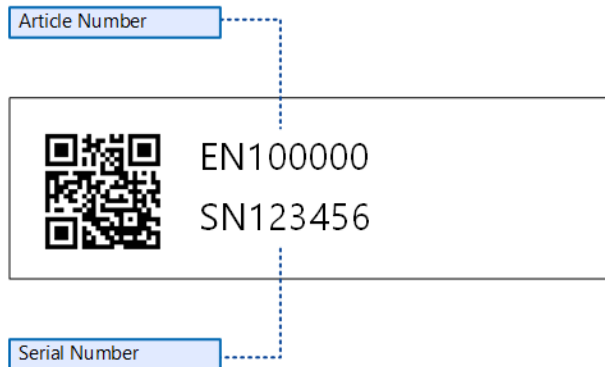


Figure 4: Module Label

The correspondence between EN-number and part name is shown in Table 2. The part name represents the product model, followed by the revision; the R suffix and number represent the revision number.

The revision changes and product known issues are described in the Mercury+ XU1 SoC Module Known Issues and Changes document [7].

EN-Number	Part Name
EN105136	ME-XU1-6CG-1E-D11E-G1-R4.2
EN105137	ME-XU1-6CG-1E-D11E-R4.2
EN105138	ME-XU1-6EG-1I-D11E-G1-R4.2
EN105139	ME-XU1-6EG-1I-D11E-R4.2
EN105142	ME-XU1-9EG-1E-D11E-G1-R4.2
EN105144	ME-XU1-9EG-2I-D12E-R4.2
EN105143	ME-XU1-9EG-2I-D12E-G1-R4.2
EN105145	ME-XU1-9EG-3E-D12E-R4.2
EN105132	ME-XU1-15EG-1E-D12E-G1-R4.2
EN105134	ME-XU1-15EG-2I-D12E-R4.2
EN105133	ME-XU1-15EG-2I-D12E-G1-R4.2

Table 2: EN-Numbers and Part Names

## 2.4 Top and Bottom Views

### 2.4.1 Top View



Figure 5: Module Top View

### 2.4.2 Bottom View

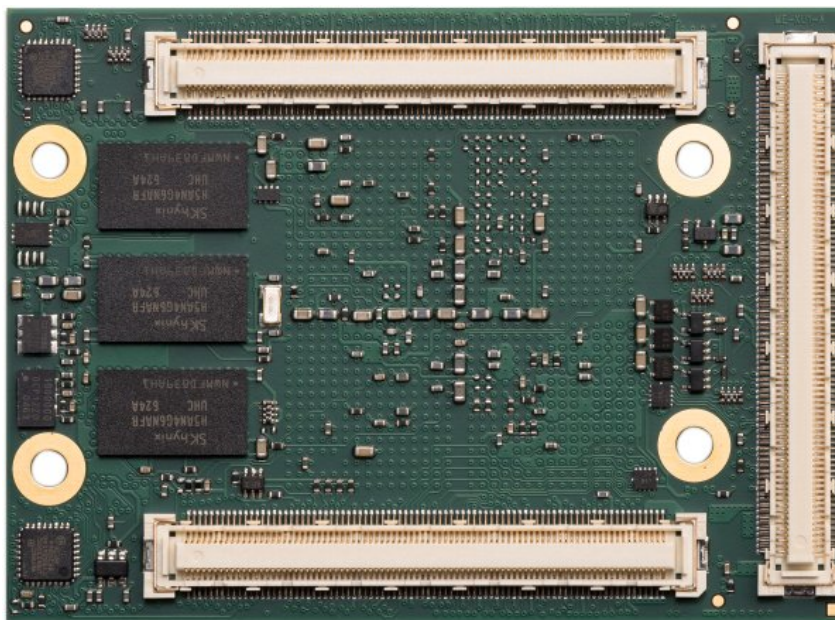


Figure 6: Module Bottom View

Please note that depending on the hardware revision and configuration, the module may look slightly different than shown in this document.





## 2.6 Module Footprint

Figure 9 shows the dimensions of the module footprint on the base board.

Enclustra offers Mercury and Mercury+ modules of various geometries having widths of 56, 64, 65, 72 or 74 mm and having different topologies for the mounting holes. If different module types shall be fixed on the base board by screws, additional mounting holes may be required to accommodate different modules. The footprints of the module connectors for the base board design are available for different PCB design tools (Altium, PADS, Eagle, Orcad) [8] and include the required information on the module sizes and holes.

The maximum component height under the module is dependent on the connector type - refer to Section 2.8 for detailed connector information.

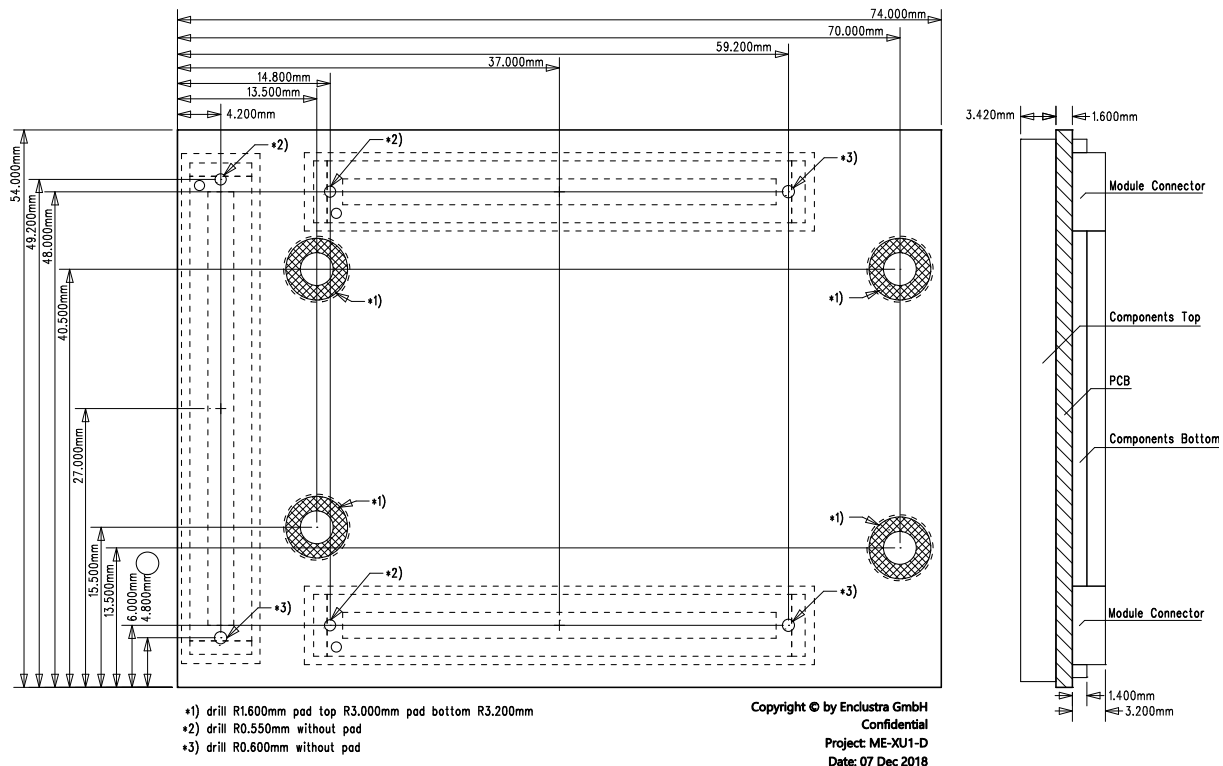


Figure 9: Module Footprint - Top View

### Warning!

*It is possible to mount the Mercury+ XU1 SoC module the wrong way round on the base board - always check that the mounting holes on the base board are aligned with the mounting holes of the Mercury+ XU1 SoC module.*

## 2.7 Mechanical Data

Table 3 describes the mechanical characteristics of the Mercury+ XU1 SoC module. A 3D model (PDF) and a STEP 3D model are available [9], [10].

Symbol	Value
Size	74 × 54 mm
Component height top	3.42 mm
Component height bottom	1.4 mm
Weight	34 g

Table 3: Mechanical Data

## 2.8 Module Connector

Three Hirose FX10 168-pin 0.5 mm pitch headers with a total of 504 pins have to be integrated on the base board. Up to four M3 screws may be used to mechanically fasten the module to the base board. Do not use excessive force to tighten the screws, as this could damage the module.

The pinout of the module connector is found in the Mercury Master Pinout Excel Sheet [12]. The connector is available in different packaging options and different stacking heights. Some examples are presented in Table 4. Please refer to the connector datasheet for more information.

Reference	Type	Description
Mercury module connector	FX10A-168S-SV	Hirose FX10, 168-pin, 0.5 mm pitch
Base board connector	FX10A-168P-SV(71)	Hirose FX10, 168-pin, 0.5 mm pitch, 4 mm stacking height
Base board connector	FX10A-168P-SV1(71)	Hirose FX10, 168-pin, 0.5 mm pitch, 5 mm stacking height

Table 4: Module Connector Types

Figure 10 indicates the pin numbering for the Mercury module connectors from the top view of the base board. The connector pins are numbered as follows:

- Connector A: from J800-1 to J800-168
- Connector B: from J801-1 to J801-168
- Connector C: from J900-1 to J900-168

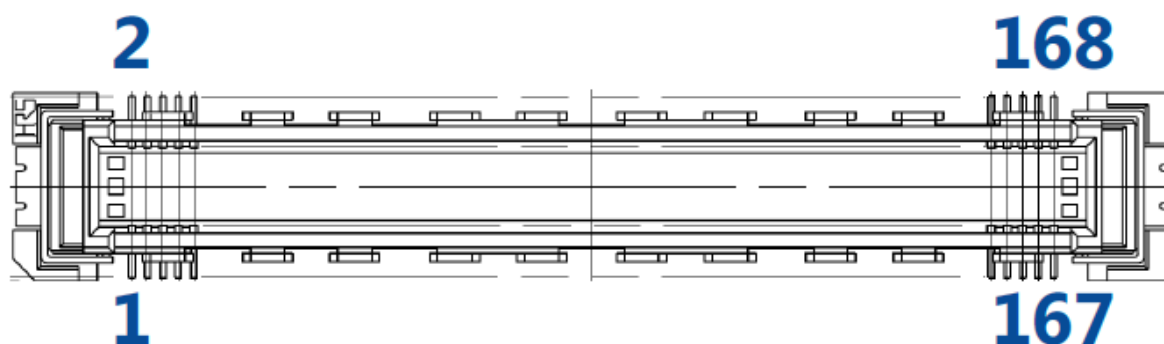


Figure 10: Pin Numbering for the Module Connector

## Warning!

*Do not use excessive force to latch a Mercury module into the Mercury connectors on the base board, as this could damage the module and the base board; always make sure that the module is correctly oriented before mounting it into the base board.*

## 2.9 User I/O

### 2.9.1 Pinout

Information on the Mercury+ XU1 SoC module pinout can be found in the Enclustra Mercury Master Pinout [12], and in the additional document Enclustra Module Pin Connection Guidelines [11].

## Warning!

*Please note that the pin types on the schematics symbol of the module connector and in the Master Pinout document are for reference only. On the Mercury+ XU1 SoC module it may be possible that the connected pins do not have the targeted functions (such as primary clocks, differential pins, MGT signals, etc).*

The naming convention for the user I/Os is:

IO\_B<BANK>\_L<PAIR><\_SPECIAL\_FUNCTION>\_<PACKAGE\_PIN>\_<POLARITY>.

For example, IO\_B64\_L18\_AD2\_AH4\_P is located on pin AH4 of I/O bank 64, pair 18, it is a System Monitor differential auxiliary analog input capable pin and it has positive polarity, when used in a differential pair.

The global clock capable pins are marked with "GC" (HP I/O banks) or with "HDGC" (HD I/O banks) in the signal name. For details on their function and usage, please refer to the Xilinx documentation.

Table 5 includes information related to the total number of I/Os available in each I/O bank and possible limitations.

Signal Name	Signals	Pairs	Differential	Single-ended	I/O Bank
IO_B64_<...>	52	24	In/Out	In/Out	64 (HP) <sup>1</sup>
IO_B65_<...>	50	24	In/Out	In/Out	65 (HP) <sup>1</sup>
IO_B66_<...>	50	24	In/Out	In/Out	66 (HP) <sup>1</sup>
IO_B47_<...>	24	12	In/Out (no LVDS/LVPECL outputs supported; internal differential termination not supported)  Refer to Section 2.9.3 for details.	In/Out	47 (HD) <sup>1</sup>
IO_B48_<...>	24	12	In/Out (no LVDS/LVPECL outputs supported; internal differential termination not supported)  Refer to Section 2.9.3 for details.	In/Out	48 (HD) <sup>1</sup>
<b>Total</b>	<b>200</b>	<b>96</b>	-	-	-

Table 5: User I/Os

Please note that on the “G1” variants with 16 GTH transceivers, not all I/Os listed in Table 5 are available on the module connector. Certain user I/Os on the module connectors can be connected to various MP-SoC I/Os, depending on the product variant. Section 2.9.2 lists and describes the connectivity for these pins for each assembly variant. The multi-use signals on the module connector are not named according to the naming convention described above.

The multi-gigabit transceiver (MGT) are described in section 2.10.

## 2.9.2 I/O Pin Exceptions

The I/O pin exceptions are pins with special functions or restrictions (for example, when used in combination with certain Mercury boards they may have a specific role).

### PCIe Reset Signal (PERST#)

Table 6 lists the I/O pin exceptions on the Mercury+ XU1 SoC module related to the PCIe reset connection.

I/O Name	Module Connector Pin	Description
PS_MIO42_PERST#	A-104	When the pin has a low value, ETH0_TXD3_PERST# pin (MIO30) is pulled to ground via a 1 kΩ resistor for PCIe PERST# connection implementation

Table 6: I/O Pin Exceptions - PERST#

When the Mercury+ XU1 SoC module is used in combination with a Mercury+ PE1 base board as a PCIe device, the low value of the PERST# signal coming from the PCIe edge connector on the module connector pin A-104 (PS\_MIO42\_PERST#) pulls the ETH0\_TXD3\_PERST# (MIO30) to ground via a 1 kΩ resistor.

MIO30 is the default pin used for the reset signal of the PCIe PS built-in block, therefore it was chosen for the reset implementation. The Ethernet controller 0 is disabled when the PCIe hard block is used; note that any other valid position for PERST# would have resulted in having the Ethernet controller disabled.

<sup>1</sup>HD = high density pins, HP = high performance pins; Refer to the Zynq UltraScale+ MPSoC Overview [26] for details.

In situations in which PCIe functionality is not required, PS\_MIO42\_PERST# pin can be used in the same manner as a regular MIO pin.

For root complex applications the PERST# signal can be placed on any unused MIO pin (the restriction on MIO30/42 does not apply in this case).

### ***I/O Pins with Level Shifter***

There are four signals on the Mercury+ XU1 SoC module that are routed from the FPGA banks to the module connector via level shifters - these are presented in Table 7.

<b>I/O Name</b>	<b>Module Connector Pin</b>	<b>Description</b>
IO_B64_AG4_LS	A-88	These pins have a level shifter from VCC_IO_B64 to VCC_CFG_MIO
IO_B64_AJ1_LS	A-90	
IO_B64_AH11_LS	A-92	
IO_B64_AG9_LS	A-94	

*Table 7: I/O Pin Exceptions - Level Shifters*

The level shifters used for the I/O pins mentioned in Table 7 are NXP NTB0104 and the maximum achievable data rate on these pins is 40 Mbit/sec. Please note that the level shifter requires the VCC\_IO\_B64 to be more or equal to 1.2 V; refer to the level shifter datasheet for details. For VCC\_IO\_B64 voltages below 1.2 V, the level shifted signals are not operational.

### ***Assembly Options and Migration between Modules***

Starting with revision 3 modules, 4 additional GTH transceivers and 2 differential clock pairs may be routed to the module connector, by using the "G1" assembly variants. This option may be useful when the user application requires 16 GTH transceivers and less regular I/Os.

Table 8 presents the assembly variants for different product configurations. The signals on the module connector are routed to different types of I/Os, depending on the product variant. To find out where exactly these pins are routed, refer to the naming conventions for regular user I/Os (Section 2.9.1) and for MGT signals (Section 2.10). Table 8 is also available in a separate file, FPGA Pinout Assembly Variants Excel Sheet [5].

Figures 11 and 12 depict the assembly variants information. The default option is marked in bold.

Design support files such as the Mercury Master Pinout [12], Mercury+ XU1 SoC Module User Schematics [6], and Mercury+ XU1 SoC Module FPGA Pinout Assembly Variants Excel Sheet [5] offer additional information on assembly options and migration guidelines. In the user schematics, this information is depicted in the "Assembly Variants" section at the end of the PDF file (MGT\_SEL).

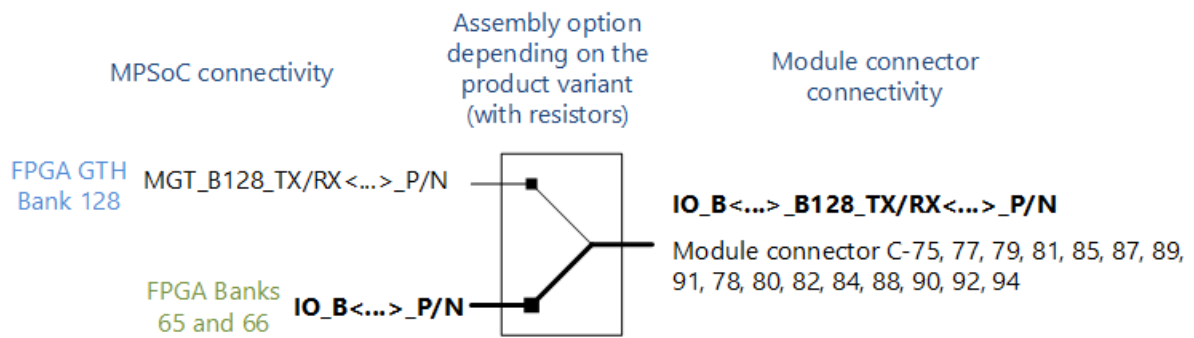


Figure 11: Assembly Options for MGT TX/RX Signals

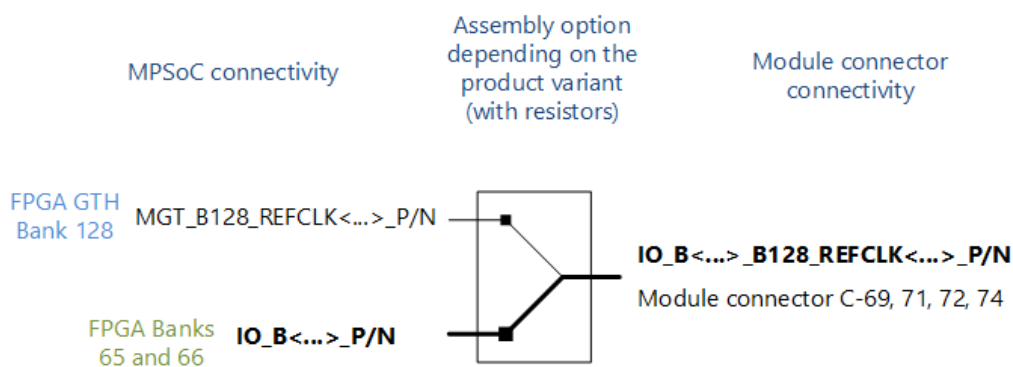


Figure 12: Assembly Options for MGT REFCLK Signals

Module Variant		Standard Assembly Variant	"G1" Assembly Variant
Compatibility		ME-XU1-R1/R2	ME-XU7/ME-XU8
Signal Name	Pin	MPSoC Pin Connectivity	
IO_B66_Y10_B128_REFCLK0_F25_P	C-69	IO_B66_Y10	MGT_B128_REFCLK0_F25_P
IO_B66_N11_B128_REFCLK0_F26_N	C-71	IO_B66_N11	MGT_B128_REFCLK0_F26_N
IO_B66_L5_AD14_U2_B128_TX0_G27_P	C-75	IO_B66_L5_AD14_U2_P	MGT_B128_TX0_G27_P
IO_B66_L5_AD14_U3_B128_TX0_G28_N	C-77	IO_B66_L5_AD14_U3_N	MGT_B128_TX0_G28_N
IO_B66_L4_AD7_V2_B128_TX1_E27_P	C-79	IO_B66_L4_AD7_V2_P	MGT_B128_TX1_E27_P
IO_B66_L4_AD7_V1_B128_TX1_E28_N	C-81	IO_B66_L4_AD7_V1_N	MGT_B128_TX1_E28_N
IO_B66_L3_AD15_W2_B128_TX2_C27_P	C-85	IO_B66_L3_AD15_W2_P	MGT_B128_TX2_C27_P
IO_B66_L3_AD15_W1_B128_TX2_C28_N	C-87	IO_B66_L3_AD15_W1_N	MGT_B128_TX2_C28_N
IO_B66_L11_GC_V7_B128_TX3_A27_P	C-89	IO_B66_L11_GC_V7_P	MGT_B128_TX3_A27_P
IO_B66_L11_GC_V6_B128_TX3_A28_N	C-91	IO_B66_L11_GC_V6_N	MGT_B128_TX3_A28_N
IO_B65_AE7_B128_REFCLK1_D25_P	C-72	IO_B65_AE7_P	MGT_B128_REFCLK1_D25_P
IO_B65_AE1_B128_REFCLK1_D26_N	C-74	IO_B65_AE1_N	MGT_B128_REFCLK1_D26_N
IO_B65_L5_AD14_AA12_B128_RX0_H29_P	C-78	IO_B65_L5_AD14_AA12_P	MGT_B128_RX0_H29_P
IO_B65_L5_AD14_AA11_B128_RX0_H30_N	C-80	IO_B65_L5_AD14_AA11_N	MGT_B128_RX0_H30_N
IO_B65_L4_AD7_AC11_B128_RX1_F29_P	C-82	IO_B65_L4_AD7_AC11_P	MGT_B128_RX1_F29_P

Continued on next page...

Module Variant		Standard Assembly Variant	"G1" Assembly Variant
Compatibility		ME-XU1-R1/R2	ME-XU7/ME-XU8
Signal Name	Pin	MPSoC Pin Connectivity	
IO_B65_L4_AD7_AD11_B128_RX1_F30_N	C-84	IO_B65_L4_AD7_AD11_N	MGT_B128_RX1_F30_N
IO_B65_L11_GC_AC7_B128_RX2_D29_P	C-88	IO_B65_L11_GC_AC7_P	MGT_B128_RX2_D29_P
IO_B65_L11_GC_AD7_B128_RX2_D30_N	C-90	IO_B65_L11_GC_AD7_N	MGT_B128_RX2_D30_N
IO_B65_L3_AD15_AD12_B128_RX3_B29_P	C-92	IO_B65_L3_AD15_AD12_P	MGT_B128_RX3_B29_P
IO_B65_L3_AD15_AE12_B128_RX3_B30_N	C-94	IO_B65_L3_AD15_AE12_N	MGT_B128_RX3_B30_N

Table 8: Assembly Options for MGT Signals and Migration Guidelines

### 2.9.3 Differential I/Os

When using differential pairs, a differential impedance of 100  $\Omega$  must be matched on the base board, and the two nets of a differential pair must have the same length.

The information regarding the length of the signal lines from the MPSoC device to the module connector is available in Mercury+ XU1 SoC Module IO Net Length Excel Sheet [3]. This enables the user to match the total length of the differential pairs on the base board if required by the application.

#### Warning!

*Please note that the trace length of various signals may change between revisions of the Mercury+ XU1 SoC module. Please use the information provided in the Mercury+ XU1 SoC Module IO Net Length Excel Sheet [3] to check which signals are affected. The differential signals will still be routed differentially in subsequent product revisions.*

The I/Os in the HD banks (47, 48) can be used only as differential inputs when LVDS/LVPECL standards are used; LVDS/LVPECL outputs are not supported.

Internal differential termination is not supported for the HD pins; all differential signal pairs from both HD banks may optionally be equipped with 100  $\Omega$  differential termination resistors on the module. Refer to Section 2.9.6 for details.

### 2.9.4 I/O Banks

Table 9 describes the main attributes of the Programmable Logic (PL) and Processing System (PS) I/O banks, and indicates which peripherals are connected to each I/O bank. All I/O pins within a particular I/O bank must use the same I/O (VCC\_IO) and reference (VREF) voltages.

Bank	Connectivity	VCC_IO	VREF
MGT Bank 228	Module connector	0.9 V	-
MGT Bank 229	Module connector	0.9 V	-
MGT Bank 230	Module connector	0.9 V	-
MGT Bank 128 <sup>2</sup>	Module connector <sup>2</sup>	0.9 V	-

Continued on next page...

Bank	Connectivity	VCC_IO	VREF
Bank 64	Module connector	User selectable VCC_IO_B64	User selectable $0.5 \times VCC\_IO\_B64$
Bank 65	Module connector <sup>2</sup>	User selectable VCC_IO_B65	User selectable $0.5 \times VCC\_IO\_B65$
Bank 66	Module connector <sup>2</sup>	User selectable VCC_IO_B66	User selectable $0.5 \times VCC\_IO\_B66$
Bank 47	Module connector	User selectable VCC_IO_B47	-
Bank 48	Module connector	User selectable VCC_IO_B48	-
Bank 503	FPGA PS Configuration	User selectable VCC_CFG_MIO	-
PS DDR Bank 504	DDR4 SDRAM	1.2 V	-
PS Bank 500	eMMC and QSPI flash devices, I2C, LEDs	1.8 V	-
PS Bank 501	Gigabit Ethernet PHY 0, module connector	User selectable VCC_CFG_MIO	-
PS Bank 502	USB PHY 0, and Gigabit Ethernet PHY 1 / USB PHY 1 (shared lines)	1.8 V	-
PS GTR Bank 505	Module connector, GTR oscillators	VCC_0V85	-

Table 9: I/O Banks

### 2.9.5 VCC\_IO Usage

The VCC\_IO voltages for the I/O banks located on the module connector are configurable by applying the required voltage to the VCC\_IO\_B[x], respectively VCC\_CFG\_[x] pins. All VCC\_IO\_B[x] or VCC\_CFG\_[x] pins of the same bank must be connected to the same voltage.

For compatibility with other Enclustra Mercury modules, it is recommended to use a single I/O voltage per module connector.

<sup>2</sup>The MGTs in bank 128 are available on the module connector only on "G1" assembly variants. On these variants, certain I/Os from banks 65 and 66 are not routed to the module connector. Please check the assembly variants description in Section 2.9.2.



Signal Name	MPSoC Pins	Supported Voltages	Connector A Pins	Connector B Pins	Connector C Pins
VCC_CFG_MIO	VCCO_PSIO1_501, VCCO_PSIO3_503	1.8 V - 3.3 V $\pm$ 5%	74, 77	-	-
VCC_IO_B64	VCCO_64	1.0 V <sup>3</sup> - 1.8 V $\pm$ 5%	-	-	76, 116, 158
VCC_IO_B65	VCCO_65	1.0 V - 1.8 V $\pm$ 5%	-	64, 88, 140	-
VCC_IO_B66	VCCO_66	1.0 V <sup>4</sup> - 1.8 V $\pm$ 5%	-	67, 95, 143	-
VCC_IO_B47	VCCO_47	1.2 V - 3.3 V $\pm$ 5% <sup>5</sup>	41	-	-
VCC_IO_B48	VCCO_48	1.2 V - 3.3 V $\pm$ 5% <sup>5</sup>	38	-	-

Table 10: VCC\_IO Pins

If the Mercury+ XU1 SoC module is used in combination with a base board having only two module connectors, the VCC\_IO\_B64 pin that powers I/O bank 64 is connected to the on-board generated 1.8 V supply voltage.

#### Warning!

*Use only VCC\_IO voltages compliant with the equipped MPSoC device; any other voltages may damage the equipped MPSoC device, as well as other devices on the Mercury+ XU1 SoC module.*

*Do not leave a VCC\_IO pin floating, as this may damage the equipped MPSoC device, as well as other devices on the Mercury+ XU1 SoC module.*

#### Warning!

*Do not power the VCC\_IO pins when PWR\_GOOD and PWR\_EN signals are not active. If the module is not powered, you need to make sure that the VCC\_IO voltages are disabled (for example, by using a switch on the base board, which uses PWR\_GOOD as enable signal). Figure 13 illustrates the VCC\_IO power requirements.*

<sup>3</sup>There are limitations on the I/Os from bank 64 routed via level shifters when VCC\_IO\_B64 is less than 1.2 V. Refer to Section 2.9.2 for details.

<sup>4</sup>When using voltages lower than 1.8 V for VCC\_IO\_B66, the I2C bus on FPGA bank 66 is not operational (I2C on PL side is available starting with revision 2).

<sup>5</sup>For voltages of 3.3 V for VCC\_IO\_B47 and VCC\_IO\_B48 the tolerance range is -5% to +3%.

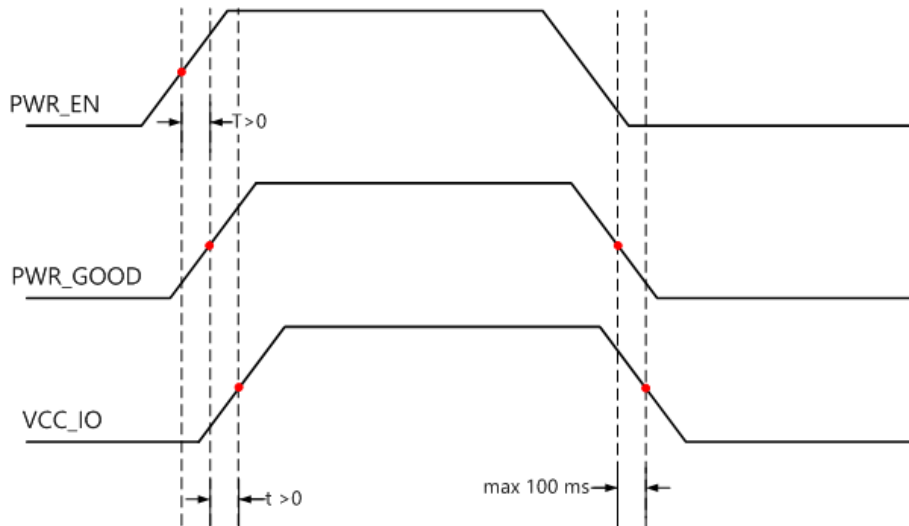


Figure 13: Power-Up Sequence - VCC\_IO in Relation with PWR\_GOOD and PWR\_EN Signals

## 2.9.6 Signal Terminations

### Differential Inputs

Internal differential termination is not supported for the HD pins (banks 47, 48). All differential signal pairs from both HD banks may optionally be equipped with 100  $\Omega$  differential termination resistors on the module.

The resistor identifiers for each differential input pair can be retrieved from the Mercury+ XU1 SoC Module User Schematics [6].

### Single-Ended Outputs

There are no series termination resistors on the Mercury+ XU1 SoC module for single-ended outputs. If required, series termination resistors may be equipped on the base board (close to the module pins).

## 2.9.7 Multiplexed I/O (MIO) Pins

Details on the MIO/EMIO terminology are available in the Zynq UltraScale+ MPSoC Technical Reference Manual [22].

Some of the MIO pins on the Mercury+ XU1 SoC module are connected to on-board peripherals, while others are available as GPIOs; the suggested functions below are for reference only - always verify your MIO pinout with the Xilinx device handbook.

Table 11 gives an overview over the MIO pin connections on the Mercury+ XU1 SoC module. Only the pins marked with "user functionality" are available on the module connector.

MIO Group	Default Function	Second Function	Connection
0-5	QSPI flash	Trace interface	QSPI flash, debug connector <sup>6</sup>
6	QSPI feedback clock	Trace interface (cont.)	Debug connector <sup>6</sup>
7-9	-	Trace interface (cont.)	Debug connector <sup>6</sup>
10-11	I2C	-	On-board I2C bus and module and debug connectors <sup>6</sup> via level shifter
12	I2C interrupt	PJTAG interface	On-board I2C bus, debug connector <sup>6</sup>
13-15	eMMC flash	PJTAG interface (cont.)	eMMC flash, debug connector <sup>6</sup>
16-22	eMMC flash (cont.)	-	eMMC flash
23	USB PHY 1 reset	-	USB 2.0 PHY 1
24	LED0	Debug UART TX <sup>7</sup>	LEDs, debug connector <sup>6</sup>
25	LED1	Debug UART RX <sup>7</sup>	
26-29, 31-37	Ethernet 0	-	Gigabit Ethernet PHY 0
30	Ethernet 0 (cont.)	PS PCIe block PERST# signal <sup>8</sup>	Gigabit Ethernet PHY 0 and module connector via series resistor
38	UART RX <sup>7</sup>	User functionality	Module connector
39	UART TX <sup>7</sup>		
40-41, 43-44	User functionality	-	Module connector
42	User functionality	PS PCIe block PERST# signal <sup>8</sup>	Module connector
45-51	SD card	User functionality	Module connector
52-63	USB 0	-	USB 2.0 PHY 0
64-75	Ethernet 1	USB 1	Gigabit Ethernet PHY 1, USB 2.0 PHY 1
76-77	Ethernet MDIO	-	Gigabit Ethernet PHY 1 and PHY 0 via level shifter

Table 11: MIO Pins Connections Overview

<sup>6</sup>Starting with revision 3, the PJTAG, TRACE, and debug UART interfaces to debug connector are not supported anymore. Please refer to Section 2.25 for details.

<sup>7</sup>UART RX is an MPSoC input; UART TX is an MPSoC output.

<sup>8</sup>Used for PCIe PERST# connection implementation. Refer to Section 2.9.2 for details.

## 2.9.8 Analog Inputs

The Zynq UltraScale+ MPSoC devices contain a system monitor in the PL and an additional system monitor block in the PS. These are used to sample analog inputs and to collect information on the internal voltages and temperatures.

The system monitor block in the PL provides a 10-bit ADC, which supports up to 17 external analog lines (1 dedicated differential input, 16 auxiliary differential inputs). The auxiliary analog lines of the MPSoC device are available on the module connector; these I/Os have the abbreviation "AD" followed by the ADC channel in the signal name. The ADC lines are always used differentially; for single-ended applications, the \*\_N line must be connected to GND. The dedicated channel is not available on the module connector.

The analog input signals can be connected to any normal I/O FPGA bank, provided that all analog pins belong to the same bank. Note that the HD I/O banks have a limited number of analog inputs and they must be connected directly to the SYSMONE4 primitive instead of to the Xilinx System Management Wizard IP core.

For detailed information on the ADC and system monitor, refer to the UltraScale Architecture System Monitor document [23], Zynq UltraScale+ MPSoC Technical Reference Manual [22] and System Management Wizard Product Guide [25].

Table 12 presents the ADC Parameters for the PL System Monitor. The PS System Monitor is only used for monitoring the on-chip power supply voltages and die temperature.

Parameter	Value (PL Sysmon)
VCC_ADC	1.8 V
VREF_ADC	Internal
ADC Range	0-1 V
Sampling Rate per ADC	0.2 MSPS
Total number of channels available on the module connector	16 (only auxiliary inputs)

Table 12: System Monitor (PL) Parameters

## 2.10 Multi-Gigabit Transceiver (MGT)

There are two types of multi-gigabit transceivers available on the Mercury+ XU1 SoC module: GTH transceivers (connected to the PL) and GTR transceivers (connected to the PS).

### GTH Transceivers

There are 12 GTH MGTs available on the Mercury+ XU1 SoC module organized in three FPGA banks - Table 13 describes the connections.

The naming convention for the GTH MGT I/Os is:  
MGT\_B<BANK>\_<FUNCTION>\_<PACKAGE\_PIN>\_<POLARITY>.

For example, MGT\_B228\_TX2\_M5\_N is located on pin M5 of MGT I/O bank 228, it is a transmit pin and it has negative polarity.

Starting with revision 3 modules, 4 additional GTH transceivers and 2 differential clock pairs may be routed to the module connector, by using the "G1" assembly variants. Please refer to Section 2.9.2 for

details on the assembly variants and MGT connectivity.

Signal Name	Signal Description	Pairs	I/O Bank
MGT_B228_RX<...>	MGT receivers	4	228
MGT_B228_TX<...>	MGT transmitters	4	
MGT_B228_REFCLK<...>	MGT reference input clocks	2	
MGT_B229_RX<...>	MGT receivers	4	229
MGT_B229_TX<...>	MGT transmitters	4	
MGT_B229_REFCLK<...>	MGT reference input clocks	2	
MGT_B230_RX<...>	MGT receivers	4	230
MGT_B230_TX<...>	MGT transmitters	4	
MGT_B230_REFCLK<...>	MGT reference input clocks	2	
MGT_B128_RX<...> <sup>9</sup>	MGT receivers	4	128
MGT_B128_TX<...> <sup>9</sup>	MGT transmitters	4	
MGT_B128_REFCLK<...> <sup>9</sup>	MGT reference input clocks	2	
<b>Total</b>		<b>30 (40 on "G1" assembly variants)</b>	

Table 13: MGT Pairs

Eight of the GTH pairs and four corresponding clocks are routed to module connector C, while four GTH pairs and two reference input clock differential pairs are routed to module connector B. On "G1" assembly variant, four additional GTH pairs may be routed to module connector C - refer to Section 2.9.2 for details.

The GTH MGTs on the MPSoC device support data rates of 12.5 Gbit/sec on speedgrade 1 devices and of 16.375 Gbit/sec on the other devices. Hirose has removed the bandwidth limitation to 15 Gbit/sec from the past, therefore the maximum MPSoC performance may be achieved.

### **GTR Transceivers**

There are four GTR MGT pairs and two reference input clock differential pairs on the Mercury+ XU1 SoC module connected to I/O bank 505; these are routed to module connector B.

The naming convention for the GTR MGT I/Os is:  
MGTPS\_<FUNCTION>\_<PACKAGE\_PIN>\_<POLARITY>.

For example, MGTPS\_RX2\_M30\_N is located on pin M30 of PS GTR bank (bank 505), it is a receive pin and it has negative polarity.

All Mercury+ XU1 SoC module variants support the implementation of a PCIe Gen2 ×4 interface.

Please note that when the PCIe hard block is used, it is not possible to use the Ethernet 0 interface. Ethernet PHY 0 is connected to ETH 0 controller from the PS I/O bank 501; one of the Ethernet TX data signals is shared with the PCIe reset signal (PERST#). Refer to Sections 2.9.2 and 2.9.7 for details on the PERST# connection.

<sup>9</sup>"G1" assembly option available starting with revision 3.

The GTR pairs support data rates of 6 Gbit/sec and can be used for the implementation of several interfaces such as PCIe Gen2  $\times 4$ , USB 3.0, DisplayPort, SATA, or Ethernet SGMII. Please refer to the Zynq UltraScale+ MPSoC Technical Reference Manual [22] and to the Zynq UltraScale+ MPSoC Overview [26] for details.

A 100 MHz LVDS oscillator and a 27 MHz CMOS oscillator provide reference clock inputs to the PS GTR bank 505. Please refer to Section 2.12 for details.

### Warning!

*The maximum data rate on the MGT lines on the Mercury+ XU1 SoC module depends on the routing path for these signals. Adequate signal integrity over the full signal path must be ensured when using MGTs at high performance rates.*

### Warning!

*No AC coupling capacitors are placed on the Mercury+ XU1 SoC module on the MGT lines - make sure capacitors are mounted, if required, on the base board (close to the module pins), to prevent MGT lines from being damaged.*

## 2.11 Power

### 2.11.1 Power Generation Overview

The Mercury+ XU1 SoC module uses a 5 - 15 V DC power input for generating the on-board supply voltages (0.72/0.85/0.9 V, 0.85/0.9 V, 0.9 V, 1.2 V, 1.8 V, 2.5 V, 3.3 V, and 5.0 V). Some of these voltages (1.8 V, 2.5 V, 3.3 V) are accessible on the module connector.

On revision 3 the Mercury+ XU1 SoC module suffered a major redesign around the power circuitry in order to support all MPSoC device speedgrades, increase performance and support power converter synchronization for noise-sensitive applications. The power converter synchronization is not supported anymore starting from revision 4.2 due to the usage of a new generation of power converters.

Table 14 describes the power supplies generated on the module.

Voltage Supply Name	Voltage Value	Rated Current	Voltage Source	Shut down via PWR_EN	Influences PWR_GOOD
VCC_INT	0.72 V <sup>10</sup> /0.85 V/0.9 V (PL core supply)	35 A <sup>11</sup>	VCC_MOD	Yes	Yes
VCC_PSINT	0.85 V/0.9 V (PS core supply)	6 A <sup>11</sup>	VCC_MOD	Yes	Yes
VCC_0V85 <sup>12</sup>	0.85 V (GTR transceiver supply)	0.5 A	VCC_1V2	Yes	No
VCC_0V9	0.9 V	6 A <sup>13</sup>	VCC_MOD <sup>13</sup>	Yes	Yes
VCC_1V2	1.2 V	6 A <sup>14</sup>	VCC_MOD <sup>14</sup>	Yes	Yes
VCC_BAT_FPGA <sup>15</sup>	1.2 V	10 mA	VCC_BAT	No	No
VCC_1V8	1.8 V	3 A <sup>16</sup>	VCC_MOD <sup>16</sup>	Yes	Yes
VCC_2V5	2.5 V	0.5 A	VCC_3V3	Yes <sup>17</sup>	No
VCC_3V3	3.3 V	6 A <sup>18</sup>	VCC_MOD	No	Yes
VCC_5V0	5.0 V	0.15 A	VCC_MOD	No	No

Table 14: Generated Power Supplies

In the standard configuration the PL core supply is 0.85 V. For configurations, in which a speedgrade -3E MPSoC device is equipped, an assembly option is available to switch the PL core operating voltage to 0.9 V. Similarly, in situations in which a speedgrade -2LE or -1LI device is used, an assembly option is available to switch the PL core operating voltage to 0.72 V.

In the standard configuration the PS core supply is 0.85 V. For configurations, in which a speedgrade -3E MPSoC device is equipped, an assembly option is available to switch the PS core operating voltage to 0.9 V.

PS and PL operation at 0.9 V is not supported on modules revision 1 and 2 - please refer to the Mercury+ XU1 SoC Module Known Issues and Changes document [7] for details.

Please refer to the Enclustra Module Pin Connection Guidelines for general rules on the power pins [11].

<sup>10</sup>Support for 0.72 V core voltage has been added starting with revision 3.

<sup>11</sup>On modules revision 1 and 2 the PL and PS core supplies were combined in a single power rail rated 20 A.

<sup>12</sup>Starting with revision 3 modules, an LDO is used to generate the GTR transceiver supply, when a -1LI, -2LE, or -3E speedgrade MPSoC device is used. For the other speedgrades, VCC\_INT is used.

<sup>13</sup>On modules revision 1 and 2 the VCC\_0V9 supply is rated 2 A and is using VCC\_3V3 as input.

<sup>14</sup>On modules revision 1 and 2 the 1.2 V supply required for the MPSoC device, DDR components and Gigabit Ethernet PHYs is separated into two separate power rails VCC\_1V2 and VCC\_1V2M both rated 2 A and using VCC\_3V3 as voltage input.

<sup>15</sup>Starting with revision 2 modules, a 1.2 V LDO is used to generate the battery voltage for the built-in RTC.

<sup>16</sup>On modules revision 1 and 2 the VCC\_1V8 supply is rated 2 A and is using VCC\_3V3 as input.

<sup>17</sup>On revision 1 modules, the 2.5 V converter cannot be disabled via PWR\_EN signal.

<sup>18</sup>On modules revision 1 and 2 the VCC\_3V3 supply is rated 9 A.

### Power Converter Synchronization

Starting with revision 4.2 modules, the switching converters used on the Mercury+ XU1 SoC module are upgraded to a newer version due to end of life of the original parts. They do not support synchronization of the switching frequency with any clock signal anymore.

Table 15 presents the control signals that were used for the power converter synchronization in revisions 3 to 4.1, and how they should be connected starting from revision 4.2.

Signal	MPSoC Pin	Description
PWR_SYNC_EN#	MIO7 (package pin A18)	Reserved. This pin is equipped with a pull-up resistor to 1.8 V. Leave this pin floating or drive it high to use the default switching frequencies as specified in the schematics.
LED2#_PWR_SYNC	Package pin AE8	Multi-function FPGA pin. When PWR_SYNC_EN# is high (default configuration), this pin is connected to LED2#.

Table 15: Power Converter Synchronization

### 2.11.2 Power Enable/Power Good

The Mercury+ XU1 SoC module provides a power enable input on the module connector. This input may be used to shut down the DC/DC converters and LDOs for 0.72/0.85/0.9 V, 0.85/0.9 V, 0.9 V, 1.2 V, 1.8 V and 2.5 V. The list of regulators that can be disabled via PWR\_EN signal is provided in Section 2.11.1.

The PWR\_EN input is pulled to VCC\_3V3 on the Mercury+ XU1 SoC module with a 10 k $\Omega$  resistor. The PWR\_GOOD signal is pulled to VCC\_3V3 on the Mercury+ XU1 SoC module with a 10 k $\Omega$  resistor.

PWR\_GOOD is an open collector signal and must not be used to drive a load directly. This signal is pulled to GND if the on-board regulators fail or if the module is disabled via PWR\_EN. The list of regulators that influence the state of PWR\_GOOD signal is provided in Section 2.11.1.

Pin Name	Module Connector Pin	Remarks
PWR_EN	A-10	Floating/3.3 V: Module power enabled Driven low: Module power disabled
PWR_GOOD	A-12	0 V: Module supply not ok 3.3 V: Module supply ok

Table 16: Module Power Status and Control Pins



## Warning!

Do not apply any other voltages to the PWR\_EN pin than 3.3 V or GND, as this may damage the Mercury+ XU1 SoC module. PWR\_EN pin can be left unconnected.

Do not power the VCC\_IO pins (for example by connecting VCC\_3V3 to VCC\_IO directly) if PWR\_EN is used to disable the module. In this case, VCC\_IO needs to be switched off in the manner indicated in Figure 13.

### 2.11.3 Voltage Supply Inputs

Table 17 describes the power supply inputs on the Mercury+ XU1 SoC module. The VCC voltages used as supplies for the I/O banks are described in Section 2.9.5.

Pin Name	Module Connector Pins	Voltage	Description
VCC_MOD	A-1, 2, 3, 4, 5, 6, 7, 8, 9, 11	5 - 15 V $\pm$ 5%	Supply for 0.72/0.85/0.9 V, 0.85/0.9 V, 0.9 V, 1.2 V, 1.8 V, 3.3 V and 5.0 V voltage regulators. The 2.5 V supply is generated from the 3.3 V supply. The input current is rated at 3 A (0.3 A per connector pin).
VCC_BAT	A-168	2.7 - 3.6 V	Battery voltage for MPSoC battery-backed RAM and battery-backed RTC

Table 17: Voltage Supply Inputs

### 2.11.4 Voltage Supply Outputs

Table 18 presents the supply voltages generated on the Mercury+ XU1 SoC module, that are available on the module connector.

Pin Name	Module Connector Pins	Voltage	Maximum Current <sup>19</sup>	Comment
VCC_3V3	A-26, 29, 50, 86 B-55, 79, 115, 127, 152, 155 C-96, 103, 136, 143	3.3 V $\pm$ 5%	4 A (and max 0.3 A per pin)	Always active
VCC_2V5	A-53, 62, 65, 89	2.5 V $\pm$ 5%	0.25 A	Controlled by PWR_EN <sup>20</sup>
VCC_1V8	B-52, 76, 108, 128 C-83, 123, 165	1.8 V $\pm$ 5%	1 A	Controlled by PWR_EN

Table 18: Voltage Supply Outputs

<sup>19</sup>The maximum available output current depends on your design. See sections 2.11.1 and 2.11.5 for details.

<sup>20</sup>On revision 1 modules, the 2.5 V converter cannot be disabled via PWR\_EN signal.

### Warning!

*Do not connect any power supply to the voltage supply outputs nor short circuit them to GND, as this may damage the Mercury+ XU1 SoC module.*

## 2.11.5 Power Consumption

Please note that the power consumption of any MPSoC device strongly depends on the application (on the configured bitstream and I/O activity).

To estimate the power consumption of your design, please use the Xilinx Power Estimator available on the Xilinx website.

## 2.11.6 Heat Dissipation

High performance devices like the Xilinx Zynq UltraScale+ MPSoC need cooling in most applications; always make sure the MPSoC is adequately cooled.

For Mercury modules an Enclustra heat sink kit is available for purchase along with the product. It represents an optimal solution to cool the Mercury+ XU1 SoC module - the heat sink body is low profile and usually covers the whole module surface. The kit comes with a gap pad for the MPSoC device, a fan and required mounting material to attach the heat sink to the module PCB and baseboard PCB. With additional user configured gap pads, it is possible to cool other components on board as well.

Alternatively, if the Enclustra heat sink does not match the application requirements, a third-party heat sink body (ATS) and an additional gap pad (t-Global) may be used. Please note that the Enclustra heat sink kit already contains all necessary items for cooling the module (heat sink body, gap pad, fan, mounting material).

Table 19 lists the heat sink and thermal pad part numbers that are compatible with the Mercury+ XU1 SoC module. Details on the Mercury heatsink kit can be found in the Mercury Heatsink Application Note [21].

Product Name	Package Name	Enclustra Heat Sink	ATS Heat Sink	t-Global Thermal Pad
Mercury+ XU1	FFVC900 [27]	ACC-HS4-Set	ATS-52310G-C1-R0	TG-A6200-30-30-1

Table 19: Heat Sink Type

Please note that the adhesive heat sink part is recommended only for prototyping purposes. In cases where the module is used in environments subject to vibrations, additional mechanical fixation is recommended.

### Warning!

*Depending on the user application, the Mercury+ XU1 SoC module may consume more power than can be dissipated without additional cooling measures; always make sure the MPSoC is adequately cooled by installing a heat sink and/or providing air flow.*

### 2.11.7 Voltage Monitoring

Several pins on the module connector on the Mercury+ XU1 SoC module are marked as VMON. These are voltage monitoring outputs that are used in the production test for measuring some of the on-board voltages.

It is not allowed to draw power from the voltage monitoring outputs.

Table 20 presents the VMON pins on the Mercury+ XU1 SoC module.

Pin Name	Module Connector Pin	Connection	Description
VMON_INT	A-102	VCC_INT	PL core voltage
VMON_1V2_VBAT	B-8	VCC_1V2	1.2 V on-board voltage (default)/MP-SoC battery voltage (assembly option)
VMON_PSINT	C-8	VCC_PSINT	PS core voltage
VMON_0V9	B-167	VCC_0V9	0.9 V on-board voltage
VMON_1V8	B-168	VCC_1V8	1.8 V on-board voltage

Table 20: Voltage Monitoring Outputs

#### Warning!

*The voltage monitoring outputs are for Enclustra-use only. Pinout changes may be applied between revisions.*

### 2.12 Clock Generation

A 33.33 MHz oscillator is used for the Mercury+ XU1 SoC module clock generation; the 33.33 MHz clock is fed to the PS.

A 100 MHz LVDS oscillator and a 27 MHz CMOS oscillator provide reference clock inputs to the PS GTR bank 505. A 24 MHz clock and a 25 MHz clock are used for the USB PHYs and Ethernet PHYs respectively. The crystal pads for the MPSoC RTC are connected to a 32.768 kHz oscillator on the Mercury+ XU1 SoC module.

Table 21 describes the clock connections to the MPSoC device.

Signal Name	Frequency	Package Pin	MPSoC Pin Type
CLK33	33.33 MHz	P20	PS_REF_CLK
CLK27_GTR_P	27 MHz	H25	PS_MGTREFCLK3P_505
CLK27_GTR_N		H26	PS_MGTREFCLK3N_505
CLK100_GTR_P	100 MHz	K25	PS_MGTREFCLK2P_505
CLK100_GTR_N		K26	PS_MGTREFCLK2N_505
PS_PADI	32.768 kHz	R22	PS_PADI (crystal pad input for MPSoC built-in RTC)
PS_PADO		R23	PS_PADO (crystal pad output for MPSoC built-in RTC)

Table 21: Module Clock Resources

## 2.13 Reset

The power-on reset signal (POR) and the PS system reset signal (SRST) of the MPSoC device are available on the module connector.

Pulling PS\_POR# low resets the MPSoC device, the Ethernet and the USB PHYs, and the QSPI and eMMC flash devices. Please refer to the Enclustra Module Pin Connection Guidelines [11] for general rules regarding the connection of reset pins.

Pulling PS\_SRST# low resets the MPSoC device and enables the connection between QSPI flash and module connector, allowing the flash to be programmed from an external SPI master.

For details on the functions of the PS\_POR\_B and PS\_SRST\_B signals refer to the Zynq UltraScale+ MPSoC Technical Reference Manual [22].

Table 22 presents the available reset signals. Both signals, PS\_POR# and PS\_SRST#, have on-board 10 kΩ pull-up resistors to VCC\_CFG\_MIO. For on-board devices using 1.8 V signaling, a PS\_POR# low voltage variant is generated (PS\_POR#\_LV).

Signal Name	Connector Pin	Package Pin	FPGA Pin Type	Description
PS_POR#	A-132	U23	PS_POR_B	Power-on reset
PS_SRST#	A-124	P19	PS_SRST_B	System reset

Table 22: Reset Resources

Please note that PS\_POR# is automatically asserted if PWR\_GOOD is low.

## 2.14 LEDs

There are three active-low user LEDs on the Mercury+ XU1 SoC module - two of them are connected to the PS and one is connected to the PL. The PS LED signals are shared with the debug connector trace signals on modules revisions 1 and 2.

On revision 1 modules, LED1# is connected to both PS and PL, while LED2# is mapped to a different FPGA pin. Also, an additional LED signal, LED3#, is available on revision 1 modules on package pin Y7.

For details, please refer to the Mercury+ XU1 SoC Module Known Issues and Changes document [7] and to the Mercury+ XU1 SoC Module User Schematics [6].

PS Signal Name	PS Signal Location	PL Signal Name	PL Signal Location	Remarks
PS_LED0# <sup>21</sup>	J16 (MIO24)	-	-	User function/active-low
PS_LED1# <sup>21</sup>	G16 (MIO25)	_22	_22	User function/active-low
-	-	LED2#_PWR_SYNC <sup>23</sup>	AE8 <sup>24</sup>	User function/active-low

Table 23: User LEDs

In addition to the user LEDs, two status LEDs are equipped on the module, offering details on the configuration process for debugging purposes.

PS Signal Name	PS Signal Location	Remarks
PS_ERROR	P21 (PS_ERROR_OUT)	Refer to Zynq UltraScale+ MPSoC Technical Reference Manual [22]
PS_STATUS	P22 (PS_ERROR_STATUS)	Refer to Zynq UltraScale+ MPSoC Technical Reference Manual [22]

Table 24: Status LEDs

On revision 1 modules, the PS\_STATUS LED is active-low. Starting with revision 2, the polarity for the PS\_STATUS LED has been inverted, as the PS\_ERROR\_STATUS signal is active-high in the MPSoC device.

## 2.15 DDR4 SDRAM

There is a single DDR4 SDRAM channel on the Mercury+ XU1 SoC module attached directly to the PS side and is available only as a shared resource to the PL side.

The DDR4 SDRAM is connected to PS I/O bank 504. The memory configuration on the Mercury+ XU1 SoC module supports ECC error detection and correction; the correction code type used is single bit error correction and double bit error detection (SEC-DED).

Five 16-bit memory chips are used to build an 72-bit wide memory (8 bits are unused): 64 bits for data and 8 bits for ECC.

The maximum memory bandwidth on the Mercury+ XU1 SoC module is:  
 $2400 \text{ Mbit/sec} \times 64 \text{ bit} = 19200 \text{ MB/sec}$

### 2.15.1 DDR4 SDRAM Type

Table 25 describes the memory availability and configuration on the Mercury+ XU1 SoC module.

<sup>21</sup>Shared with debug UART interface on modules revision 1 and 2 (signals PS\_LED0#\_UA1TX and PS\_LED1#\_UA1RX)

<sup>22</sup>Shared with LED1# signal on revision 1 modules, mapped to package pin AE8.

<sup>23</sup>On revision 3 to 4.1 modules: May be used as LED signal or as clock for power converter synchronization. Refer to Section 2.11.1 for details.

<sup>24</sup>Mapped to package pin V3 on revision 1 modules.

Module	SDRAM Type	Density	Configuration	Manufact.
ME-XU1-D11E (extended)	MT40A256M16GE-083E	4 Gbit	256 M × 16 bit	Micron
ME-XU1-D11E (extended)	H5AN4G6NAFR-UHC	4 Gbit	256 M × 16 bit	SK Hynix
ME-XU1-D11E (industrial)	MT40A256M16GE-083E-IT-B	4 Gbit	256 M × 16 bit	Micron
ME-XU1-D11E (industrial)	K4A4G165WE-BIRC	4 Gbit	256 M × 16 bit	Samsung
ME-XU1-D12E (industrial)	K4A8G165WB-BIRC	8 Gbit	512 M × 16 bit	Samsung

Table 25: DDR4 SDRAM Types

### Warning!

*Other DDR4 memory devices may be equipped in future revisions of the Mercury+ XU1 SoC module. Please check the user manual regularly for updates. Any parts with different speed bins or temperature ranges that fulfill the requirements for the module variant may be used.*

In custom configurations up to 8 GB of SDRAM memory may be equipped on the module.

### 2.15.2 Signal Description

Please refer to the Mercury+ XU1 SoC Module FPGA Pinout Excel Sheet [4] for detailed information on the DDR4 SDRAM connections.

### 2.15.3 Termination

### Warning!

*No external termination is implemented for the data signals on the Mercury+ XU1 SoC module. Therefore, it is strongly recommended to enable the on-die termination (ODT) feature of the DDR4 SDRAM device.*

### 2.15.4 Parameters

Please refer to the Mercury+ XU1 SoC module reference design [2] for DDR4 settings guidelines.

The DDR4 SDRAM parameters to be set in the Vivado project are presented in Table 26.

The values given in Table 26 are for reference only. Depending on the equipped memory device on the Mercury+ XU1 SoC module and on the DDR4 SDRAM frequency, the configuration may be different to the one in the reference design. Please refer to the memory device datasheet for details.

Parameter	Value
Memory type	DDR4
DRAM bus width	64 bit
ECC	Enabled
DRAM chip bus width	16 bits
DRAM chip capacity	4096-8192 Mbits
Bank group address count	1
Rank address count	0
Bank address count	2
Row address count	15-16
Column address count	10
Speed bin	DDR4 2400T
Operating frequency	1200 MHz
CAS latency	17
CAS write latency	12
Additive latency	0
RAS to CAS delay	17
Precharge time	17
tRC	46.16 ns
tRASmin	32 ns
tFAW	30 ns

Table 26: DDR4 SDRAM Parameters

## 2.16 QSPI Flash

The QSPI flash can be used to boot the PS, and to store the FPGA bitstream, ARM application code and other user data.

### 2.16.1 QSPI Flash Type

Table 27 describes the memory availability and configuration on the Mercury+ XU1 SoC module.

As there is one QSPI flash chip equipped on the Mercury+ XU1 SoC module, type "single" must be selected when programming the flash from Vivado tools.

Flash Type	Size	Manufacturer
S25FL512S	512 Mbit	Cypress (Spansion)

Table 27: QSPI Flash Type

### Warning!

*Other flash memory devices may be equipped in future revisions of the Mercury+ XU1 SoC module. Please check the user manual regularly for updates. Any parts with different speeds and temperature ranges that fulfill the requirements for the module variant may be used.*

## 2.16.2 Signal Description

The QSPI flash is connected to the PS MIO pins 0-5. Some of these signals are available on the module connector, allowing the user to program the QSPI flash from an external source.

The reset of the QSPI flash is connected to the PS\_POR#\_LV power-on reset signal (note that modules revision 1 use PS\_POR# signal).

Please refer to Section 3 for details on programming the flash memory.

### Warning!

*Special care must be taken when connecting the QSPI flash signals on the base board. Long traces or high capacitance may disturb the data communication between the MPSoC and the flash device.*

## 2.16.3 Configuration

The QSPI flash supports up to 50 MHz operation for standard read. For fast, dual and quad read speed values, please refer to the flash device datasheet.

Note that the "Feedback Clk" option on pin MIO6 must be enabled in the Zynq configuration for clock rates higher than 40 MHz.

Please refer to Zynq UltraScale+ MPSoC Technical Reference Manual [22] for details on booting from the QSPI flash.

## 2.16.4 QSPI Flash Corruption Risk

There have been cases in which it was observed that the content of the flash device got corrupted. According to Cypress, this issue is caused by power loss during the Write Register (WRR) command. The most common reason to use the WRR command is to turn the QUAD bit ON or OFF - this operation takes place usually at the beginning of the boot process. If required, the bootloader code can be adjusted to set the QUAD bit to a fixed value, without invoking this command during boot.

For additional information on this issue, please refer to the Cypress documentation and forum discussions [28], [29].



## 2.17 eMMC Flash

The eMMC flash can be used to boot the PS, and to store the FPGA bitstream, ARM application code and other user data.

### 2.17.1 eMMC Flash Type

Table 28 describes the memory availability and configuration on the Mercury+ XU1 SoC module.

Module	Flash Type	Size	Manufacturer
ME-XU1 - R1	H26M41204HPR	8 GB	SK Hynix
ME-XU1 - R2 and newer	H26M52208FPRI	16 GB	SK Hynix
ME-XU1 - R2 and newer	EMMC16G-W525-X01U	16 GB	Kingston
ME-XU1 - R2 and newer	EMMC16G-IB29-PZ90	16 GB	Kingston

Table 28: eMMC Flash Type

#### Warning!

*Other flash memory devices may be equipped in future revisions of the Mercury+ XU1 SoC module. Please check the user manual regularly for updates. Any parts with different speeds and temperature ranges that fulfill the requirements for the module variant may be used.*

### 2.17.2 Signal Description

The eMMC flash signals are connected to the MIO pins 13-22 for 8-bit data transfer mode; some of these signals are shared with the PJTAG interface (Refer to Section 3.6.3 for details). The command signal has a 4.7 k $\Omega$  pull-up resistor to 1.8 V and the data lines have 47 k $\Omega$  pull-up resistors to 1.8 V.

## 2.18 SD Card

An SD card can be connected to the PS MIO pins 45-51. The corresponding MIO pins are available on the module connector. Information on SD card boot mode is available in Section 3.9.

Please note that external pull-ups are needed for SD card operation. Depending on the selected voltage for VCC\_CFG\_MIO, a level shifter to 3.3 V may be required (some level shifters also have built-in pull-ups).

For booting from an Ultra High Speed (UHS) SD card, an SD 3.0 compliant level shifter is required on the base board and VCC\_CFG\_MIO must be set to 1.8 V. Please note that this boot mode has not been tested, but it may be supported in the future.

## 2.19 Dual Gigabit Ethernet

Two 10/100/1000 Mbit Ethernet PHYs are available on the Mercury+ XU1 SoC module, both connected to the PS via RGMII interfaces.

## 2.19.1 Ethernet PHY Type

Table 29 describes the equipped Ethernet PHY devices type on the Mercury+ XU1 SoC module.

PHY Type	Manufacturer	Type
KSZ9031RNX	Microchip (Micrel)	10/100/1000 Mbit

Table 29: Gigabit Ethernet PHYs Type

## 2.19.2 Signal Description

PHY 0 is connected to ETH 0 controller from the PS I/O bank 501. One of the Ethernet TX data signals is shared with the PCIe reset signal (PERST#); if the application requires a hard PCIe block, the ETH 0 interface is not available. Refer to Section 2.9.2 for details on the PERST# connection.

### Warning!

*Gigabit Ethernet 0 interface is not available when the PCIe endpoint in the PS is used (because of the PERST# connection).*

PHY 1 is connected to ETH 3 controller from the PS bank 502. The corresponding MIO signals (64-75) are shared between Ethernet PHY 1 and USB PHY 1, therefore only one of them can be used. By default the Ethernet connection is enabled.

### Warning!

*Gigabit Ethernet 1 interface is not available when USB 1 interface is active.*

USB1\_RST#\_ETH1\_RST is pulled to GND via a 1 k $\Omega$  resistor; to release the USB PHY from reset, this signal must be driven high from MIO23. ETH1\_RST# is pulled to 1.8 V via a 10 k $\Omega$  resistor; if USB1\_RST#\_ETH1\_RST signal is driven high from the PS, the Ethernet reset is connected to GND.

Both reset signals (for Ethernet and USB) are pulled to GND if the PS\_POR# is active. Table 30 describes the behavior of the USB1/ETH1 selection circuit; the default selection is marked in bold.

Condition		Function	
PS_POR#	USB1_RST#_ETH1_RST (MIO23)	USB PHY 1	Ethernet PHY 1
0	-	In reset	In reset
<b>1</b>	<b>0</b>	<b>In reset</b>	<b>Active</b>
1	1	Active	In reset

Table 30: USB1/ETH1 Selection

The two Gigabit Ethernet PHYs have a shared MDIO interface and a shared interrupt line. The interrupt output of the Ethernet PHYs is connected to the I2C interrupt line, available on MIO pin 12.

### 2.19.3 External Connectivity

The Ethernet signal lines can be connected directly to the magnetics. Please refer to the Enclustra Module Pin Connection Guidelines [11] for details regarding the connection of Ethernet signals.

### 2.19.4 MDIO Address

The MDIO interface is shared between the two Gigabit Ethernet PHYs - these can be configured using the corresponding address. The MDIO address assigned to PHY 0 is 3 and to PHY 1 is 7.

The MDIO signals are mapped to MIO pins 76-77 and they are routed directly to PHY 1 and via a level shifter to PHY 0.

### 2.19.5 PHY Configuration

The configuration of the Ethernet PHYs is bootstrapped when the PHYs are released from reset. Make sure all I/Os on the RGMII interface are initialized and all pull-up or pull-down resistors are disabled at that moment.

The bootstrap options of the Ethernet PHYs are set as indicated in Table 31.

Pin	Signal Value	Description
MODE[3-0]	1110	RGMII mode: advertise all capabilities (10/100/1000, half/full duplex) except 1000Base-T half duplex.
PHYAD[2-0]	011	PHY0: MDIO address 3
	111	PHY1: MDIO address 7
Clk125_EN	0	125 MHz clock output disabled
LED_MODE	1	Single LED mode
LED1/LED2	1	Active-low LEDs

Table 31: Gigabit Ethernet PHYs Configuration - Bootstraps

For the Ethernet PHY configuration via the MDIO interface, the MDC clock frequency must not exceed 2 MHz.

### 2.19.6 RGMII Delays Configuration

The two Ethernet PHYs are connected directly to hard MAC controllers present in the MPSoC device. In order to achieve the best sampling eye for the RX and TX data, it is recommended to adjust the pad skew delays as specified in Table 32. These values have been successfully tested on Enclustra side.

The delays can be adjusted by programming the RGMII pad skew registers of the Ethernet PHY; please refer to the PHY datasheet for details.

PHY Register Name	Register Value [binary]	Delay Value
RXD0-RXD3	0111	0 ps
RX_DV	0111	0 ps
RX_CLK	01111	0 ps
TXD0-TXD3	0111	0 ps
TX_EN	0111	0 ps
GTX_CLK	11110	900 ps

Table 32: Gigabit Ethernet PHYs Configuration - RGMII Delays

## 2.20 USB 2.0

Two USB 2.0 PHYs are available on the Mercury+ XU1 SoC module, both connected to the PS to I/O bank 502. USB PHY 0 can be configured as host or device and USB PHY 1 can be used only as host.

### 2.20.1 USB PHY Type

Table 33 describes the equipped USB PHYs device type on the Mercury+ XU1 SoC module.

PHY Type	Manufacturer	Type
USB3320C	Microchip	USB 2.0 PHY

Table 33: USB 2.0 PHY Type

### 2.20.2 Signal Description

The ULPI interface for the PHY 0 is connected to MIO pins 52-63 for use with the integrated USB controller.

The ULPI interface for the PHY 1 is connected to MIO pins 64-75. The MIO signals are shared between Ethernet PHY 1 and USB PHY 1, therefore only one of them can be used. By default the Ethernet connection is enabled. Please refer to Section 2.19.2 for details on how to select Ethernet or USB mode.

#### Warning!

*USB 1 interface is not available when Gigabit Ethernet 1 interface is active.*

#### Warning!

*When generating the FSBL in certain SDK versions the power management of the USB interface is not properly implemented, causing the USB interface not to work as expected. A patch to psu\_init.c file fixing this issue (required for SDK 2017.4) is available from Enclustra upon request.*

## 2.21 USB 3.0

Xilinx Zynq UltraScale+ devices feature two built-in USB 3.0 controllers and PHYs, configurable as host or device. The PHY interface used by the USB 3.0 controller is PIPE3, supporting a 5 Gbit/sec data rate in host or device modes. The interface of each USB 3.0 controller uses one of the PS GTR lanes.

A 100 MHz differential clock is available on the module and connected to PS\_MGTREFCLK2 pins, to be used as a reference clock for the USB 3.0 interface. It is also possible to provide another reference clock from the base board to the MGTPS\_REFCLK\* pins.

Details on the built-in USB 2.0/3.0 controller and on the usage of the PS GTR lanes are available in the Zynq UltraScale+ MPSoC Technical Reference Manual [22] and in the Zynq UltraScale+ MPSoC Overview [26].

Figure 14 shows an example of a USB 3.0 implementation using the built-in Xilinx USB 3.0 interface and the USB 2.0 signals from the PHY, all routed to a USB 3.0 connector on the base board.

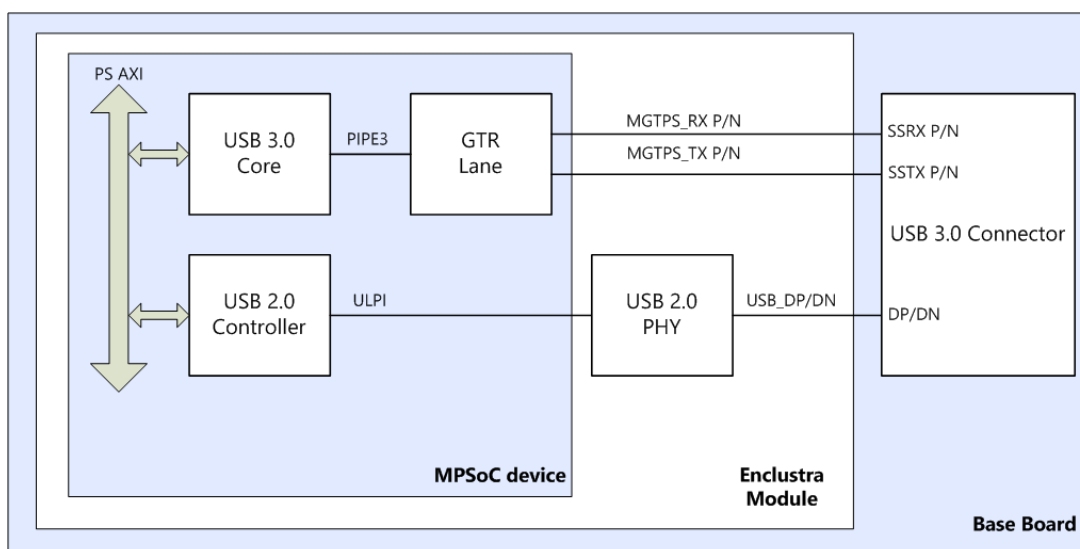


Figure 14: USB 3.0 Implementation Example

### Warning!

*The USB 3.0 interface on the Mercury+ XU1 SoC module uses the GTR lines (MGTPS signals on module connector B), and not the USB\_SSRX\_P/N and USB\_SSTX\_P/N connections on module connector A.*

## 2.22 Display Port

Xilinx Zynq UltraScale+ devices feature two built-in DisplayPort controllers and PHYs, supporting up to two lanes at a 5.4 Gbit/sec line rate. Each lane is represented by one of the PS GTR lines, available on the module connector.

A 27 MHz differential clock is available on the module and connected to PS\_MGTREFCLK3 pins, to be used as a reference clock for the DisplayPort interface. It is also possible to provide another reference clock from the base board to the MGTPS\_REFCLK\* pins.

Details on the built-in DisplayPort controller and on the usage of the PS GTR lanes is available in the Zynq UltraScale+ MPSoC Technical Reference Manual [22] and in the Zynq UltraScale+ MPSoC Overview [26].

## 2.23 Real-Time Clock (RTC)

Zynq UltraScale+ devices include an internal real-time clock. The internal RTC can be accessed by the platform management unit (PMU) - more information on the PMU is available in the Zynq UltraScale+ MPSoC Technical Reference Manual [22].

The RTC crystal pad input and crystal pad output are connected on the Mercury+ XU1 SoC module to a 32.768 kHz oscillator.

Starting with revision 2 modules, a 1.2 V LDO is used to generate the battery voltage for the built-in RTC (supplied to VCC\_PSBATT pin), based on the VCC\_BAT voltage mapped to the module connector. This pin can be connected directly to a 3 V battery on the base board. Please refer to the Enclustra Module Pin Connection Guidelines [11] for details.

On revision 1 modules, the battery voltage is generated using a voltage divider.

An external RTC (separate chip, not within the MPSoC) may be assembled optionally on the Mercury+ XU1 SoC module.

## 2.24 Secure EEPROM

The secure EEPROM is used to store the module type and serial number, as well as the Ethernet MAC address and other information. It is connected to the I2C bus.

The secure EEPROM must not be used to store user data.

Please refer to Section 4.4 for details on the content of the EEPROM.

### 2.24.1 EEPROM Type

Table 34 describes the equipped EEPROM device type on the Mercury+ XU1 SoC module.

Type	Manufacturer
ATSHA204A-MAHDA-T (default)	Atmel
DS28CN01 (assembly option)	Maxim

Table 34: EEPROM Type

An example demonstrating how to read data from the EEPROM is included in the Mercury+ XU1 SoC module reference design [2].

## 2.25 Debug Connector

The Mercury+ XU1 SoC module may optionally be equipped with a debug connector that allows the user to perform debug operations using JTAG or TRACE signals connected to the ARM DAP, to monitor and control FPGA configuration signals and to have access to the I2C bus and UART.

Note that starting with revision 3, the debug connector is not offered as an optional feature anymore. The related circuitry has been completely removed, including the MIO pin mappings for PJTAG, TRACE, and debug UART interfaces. PJTAG boot mode is also not supported any longer. The signals that were mapped to the debug connector have been renamed to reflect the changes.

Type	Manufacturer
DF40C-30DP-0.4V(51)	Hirose

Table 35: Debug Connector Type

**Warning!**

*The Hirose debug connector on the Mercury+ XU1 SoC module is not polarized. Special care must be taken when connecting the breakout board to the debug connector.*

*Connecting an external board the wrong way round on the debug connector may damage the equipped MPSoC device, as well as other devices on the Mercury+ XU1 SoC module.*

Table 36 describes the signals routed to the debug connector (valid only for modules revision 1 and 2).

Pin Number	Signal Name	Description
1	EMMC_IO2_PJTAG_TMS	PJTAG TMS
3	I2C_INT#_PJTAG_TCK	PJTAG TCK
7	EMMC_IO0_JTAG_TDI	PJTAG TDI
9	EMMC_IO1_PJTAG_TDO	PJTAG TDO
2	PJTAG_EN#	PJTAG enable (enable PJTAG boot mode)
5, 20, 31, 32, 33, 34	GND	Ground
10	VCC_3V3	
11	VCC_CFG_MIO	
21	VCC_1V8	
4	PS_SRST#	PS system reset
6	PS_PROG#	Configuration block reset (Refer to Zynq UltraScale+ MPSoC Technical Reference Manual [22])
8	PS_INIT#	Initialization completed (Refer to Zynq UltraScale+ MPSoC Technical Reference Manual [22])
12	PS_ERROR	PS_ERROR_OUT status signal (Refer to Zynq UltraScale+ MPSoC Technical Reference Manual [22])
14	PS_STATUS	PS_ERROR_STATUS (Refer to Zynq UltraScale+ MPSoC Technical Reference Manual [22])
13	I2C_SCL	I2C bus signals
15	I2C_SDA	
17	PS_LED1#_UA1RX	Debug UART signals, LED signals
19	PS_LED0#_UA1TX	

Continued on next page...

Pin Number	Signal Name	Description
16	TRACE_EN#	Trace interface enable signal
18	TRACE_CLK	Debug trace interface (Refer to Zynq UltraScale+ MPSoC Technical Reference Manual [22])
22	TRACE_CTL	
23	TRACE_DQ0	
24	TRACE_DQ4	
25	TRACE_DQ1	
26	TRACE_DQ5	
27	TRACE_DQ2	
28	TRACE_DQ6	
29	TRACE_DQ3	
30	TRACE_DQ7	

Table 36: Debug Connector Interface - Revision 1 and 2 Modules

The trace signals can be used to debug the processor running at full speed, allowing the user to collect information on the CPU instruction execution and data transfers.

In order to enable the trace interface, TRACE\_EN# signal must be pulled low from the debug connector, and MIO pins 0-9 must be assigned to TRACE controller in the PS settings of the Vivado project. Additionally, starting with revision 2 modules, the trace clock multiplexer must be equipped. Refer to the Mercury+ XU1 SoC Module User Schematics [6] for details.



# 3 Device Configuration

## 3.1 Configuration Signals

The PS of the MPSoC needs to be configured before the FPGA logic can be used. Xilinx Zynq devices need special boot images to boot from QSPI flash, eMMC flash or SD card. For more information, please refer to the Zynq UltraScale+ MPSoC Technical Reference Manual [22].

Table 37 describes the most important configuration pins and their location on the module connector. These signals allow the MPSoC to boot from QSPI flash, eMMC flash or SD card, and can be used to program the QSPI flash from an external master. Please refer to Section 3.12 for details.

Signal Name	MPSoC Pin Type	Mod. Conn. Pin	Description	Comments
FLASH_CLK	MIO0	A-118	SPI CLK	10 kΩ pull-up to VCC_CFG_MIO
FLASH_DO	MIO1	A-122	SPI MISO	-
FLASH_DI	MIO4	A-114	SPI MOSI	10 kΩ pull-up to VCC_CFG_MIO
FLASH_CS#	MIO5	A-116	SPI CS#	10 kΩ pull-up to VCC_CFG_MIO
PS_DONE	PS_DONE	A-130	MPSoC device configuration done	1 kΩ pull-up to VCC_CFG_MIO
PS_POR#	PS_POR_B	A-132	MPSoC power-on reset	10 kΩ pull-up to VCC_CFG_MIO
PS_SRST#	PS_SRST_B	A-124	MPSoC system reset	10 kΩ pull-up to VCC_CFG_MIO
BOOT_MODE0	-	A-126	Boot mode selection	10 kΩ pull-up to VCC_CFG_MIO
BOOT_MODE1	-	A-112	Boot mode selection	10 kΩ pull-up to VCC_CFG_MIO

Table 37: MPSoC Configuration Pins

## Warning!

All configuration signals except for *BOOT\_MODE* must be high impedance as soon as the device is released from reset. Violating this rule may damage the equipped MPSoC device, as well as other devices on the Mercury+ XU1 SoC module.

### 3.2 Module Connector C Detection

Signal *C\_PRSENT#* (pin C-167) must be connected to GND on the base board if the designed base board has three connectors. Depending on the value of this pin, the FPGA banks routed to module connector C are supplied with the voltages provided by the user (when *C\_PRSENT#* is low) or with a default voltage of 1.8 V (when *C\_PRSENT#* is unconnected).

*C\_PRSENT#* is equipped with a 4.7 k $\Omega$  pull-up resistor on the module.

### 3.3 Pull-Up During Configuration

The Pull-Up During Configuration signal (*PUDC*) is pulled to GND on the module; as *PUDC* is an active-low signal, all FPGA I/Os will have the internal pull-up resistors enabled during device configuration.

If the application requires the pull-up during configuration to be disabled, this can be achieved by removing *R201* component and by mounting *R228* - in this configuration the *PUDC* pin is connected to 1.8 V.

Figure 15 illustrates the configuration of the I/O signals during power-up. Figure 16 indicates the location of the pull-up/pull-down resistors on the module PCB - lower right part on the bottom view drawing.

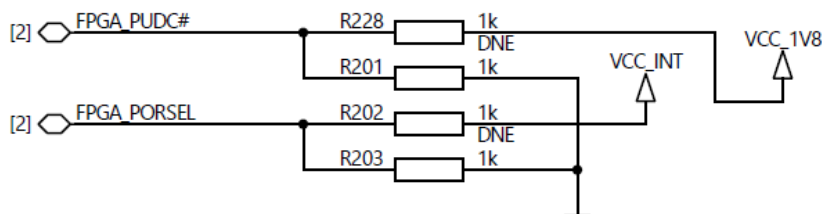


Figure 15: Pull-Up During Configuration (*PUDC*) and Power-on Reset Delay Override (*PORSEL*) - Revision 4 Modules

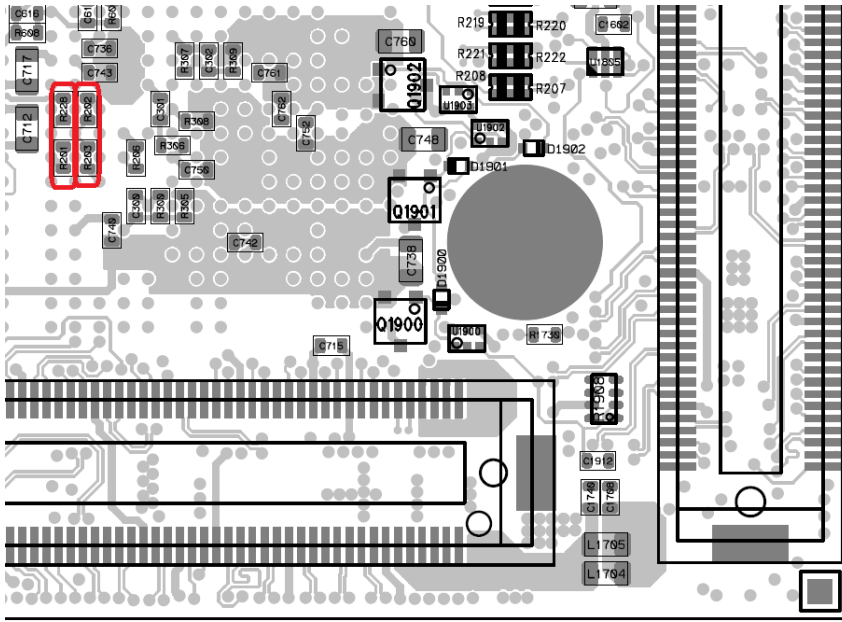


Figure 16: Pull-Up During Configuration (PUDC) and Power-on Reset Delay Override (PORSEL) Resistors - Assembly Drawing Bottom View (lower right part) for Revision 4 Modules

For details on the PUDC signal please refer to the Zynq UltraScale+ MPSoC Technical Reference Manual [22].

### 3.4 Power-on Reset Delay Override

The power-on reset delay override MPSoC signal (POR\_OVERRIDE) is pulled to GND on the module, setting the PL power-on delay time to the default standard time.

If the application requires faster PL power-on delay time, this can be achieved by removing R203 component and by mounting R202.

Figure 15 illustrates the configuration of the POR\_OVERRIDE signal. Figure 16 indicates the location of the pull-up/pull-down resistors on the module PCB - lower right part on the bottom view drawing.

For details on the POR\_OVERRIDE signal please refer to the Zynq UltraScale+ MPSoC Technical Reference Manual [22].

### 3.5 Boot Mode

The boot mode can be selected via two signals available on the module connector and a signal available on the debug connector.

Table 38 describes the available boot modes on the Mercury+ XU1 SoC module. PJTAG\_EN# signal is only available on the optional debug connector. It has a 10 k $\Omega$  pull-up resistor to VCC\_CFG\_MIO, therefore it may be left unconnected.

Note that starting with revision 3, the debug connector is not offered as an optional feature anymore. The related circuitry has been completely removed and the PJTAG boot mode is not supported any longer.

Starting with revision 4, JTAG boot mode has been introduced to increase the usability with Xilinx tools, which may report issues when programming the on-board QSPI flash or when loading the FPGA bitstream in a non-JTAG boot mode.

BOOT MODE1	BOOT MODE0	PJTAG_EN#	Mode Straps [3:0]	Description	Remarks
0	0	1	0110	Boot from eMMC flash	-
0	1	1	1110	Boot from SD card (with an external SD 3.0 compliant level shifter; only available when VCC_CFG_MIO is 1.8 V)	Not supported (may be supported in the future)
1	0	1	0010	Boot from QSPI flash	-
1	1	1	0101	Boot from SD card (default mode)	-
1	1	0	1001	PJTAG boot mode <sup>25</sup>	Not supported in the standard configuration <sup>25</sup>
1	0	-	0000	JTAG boot mode	Available only starting with revision 4 modules in certain conditions (refer to Section 3.6.4 for details).

Table 38: Boot Modes

## 3.6 JTAG

The Zynq UltraScale+ devices include two separate JTAG controllers: the Zynq UltraScale+ TAP and the ARM DAP. The first one uses the PS dedicated JTAG pins and has access to both PS and PL and the second one uses the PS PJTAG pins and is used for loading programs, system test, and PS debug.

Details on JTAG and on system test and debug are available in the Zynq UltraScale+ MPSoC Technical Reference Manual [22].

On modules equipped with ES1 (engineering samples 1) MPSoC devices, PJTAG boot mode is required in order to program the FPGA and download a program to one of the ARM processors via JTAG.

Certain Xilinx tool versions support QSPI flash programming via JTAG only when JTAG boot mode is used (unavailable in the standard configurations of the Mercury+ XU1 SoC module). Alternatively, the QSPI flash can be programmed in u-boot or Linux by the SPI controller in the PS or from an SPI external master.

### 3.6.1 JTAG on Module Connector

The PL and the PS JTAG interfaces are connected into one single chain available on the module connector. The PS\_JTAG pins are used by the Zynq UltraScale+ TAP controller - the controller has full functionality only after the PS boot is complete. In order to enable the ARM DAP controller, special commands must

<sup>25</sup>Starting with revision 3, PJTAG boot mode is not supported anymore on any configuration.

be sent to the Zynq UltraScale+ TAP.

The MPSoC device and the flash devices can be configured via JTAG from Xilinx SDK or Xilinx Vivado Hardware Manager - for this operation, the ARM DAP must be enabled.

Signal Name	Module Connector Pin	PS Dedicated Pin	Resistor
JTAG_TCK	A-123	PS_JTAG_TCK	10 k $\Omega$ pull-up to VCC_CFG_MIO
JTAG_TMS	A-119	PS_JTAG_TMS	10 k $\Omega$ pull-up to VCC_CFG_MIO
JTAG_TDI	A-117	PS_JTAG_TDI	10 k $\Omega$ pull-up to VCC_CFG_MIO
JTAG_TDO	A-121	PS_JTAG_TDO	10 k $\Omega$ pull-up to VCC_CFG_MIO

Table 39: JTAG Interface - PL and PS Access and Debug

### 3.6.2 External Connectivity

JTAG signals can be connected directly on the base board to a JTAG connector. No pull-up/pull-down resistors are necessary. The VREF pin of the programmer must be connected to VCC\_CFG\_MIO.

It is recommended to add 22  $\Omega$  series termination resistors between the module and the JTAG header, close to the source. Please refer to the Enclustra Module Pin Connection Guidelines for details on JTAG interface.

### 3.6.3 PJTAG on Debug Connector

The JTAG pins available on the debug connector are used by the ARM DAP for debugging the PS. These pins can be used when the ARM DAP is not on the JTAG chain.

Signal Name	Pin on Debug Connector	PS Pin	Resistor
I2C_INT#_PJTAG_TCK	3	MIO12	51.7 k $\Omega$ pull-up to VCC_3V3
EMMC_IO2_PJTAG_TMS	1	MIO15	47 k $\Omega$ pull-up to VCC_1V8
EMMC_IO0_PJTAG_TDI	7	MIO13	47 k $\Omega$ pull-up to VCC_1V8
EMMC_IO1_PJTAG_TDO	9	MIO14	47 k $\Omega$ pull-up to VCC_1V8

Table 40: JTAG Interface - ARM DAP Access via PJTAG Signals (valid only for modules revision 1 and 2)

In the standard configuration, PJTAG boot mode is not supported. In order to enable the PJTAG boot mode via MIO pins 12-15 (PJTAG1 pins), PJTAG\_EN# must be driven low from pin 2 of the optional debug connector.

Note that starting with revision 3, the debug connector is not offered as an optional feature anymore. The related circuitry has been completely removed, including the MIO pin mappings for PJTAG, TRACE, and debug UART interfaces. PJTAG boot mode is also not supported any longer. The signals that were mapped to the debug connector have been renamed to reflect these changes.

### 3.6.4 JTAG Boot Mode

Starting with revision 4, support for JTAG boot mode has been added to increase the usability of the module with Xilinx tools, for example for QSPI flash programming or FPGA bitstream loading.

The following steps are required in order to boot the module in JTAG mode:

- Set the boot mode selection signals for QSPI boot
- Short-circuit R235 (see Figure 17) while powering-up the module (in order to sample the MPSoC boot selection pins correctly for JTAG boot mode)

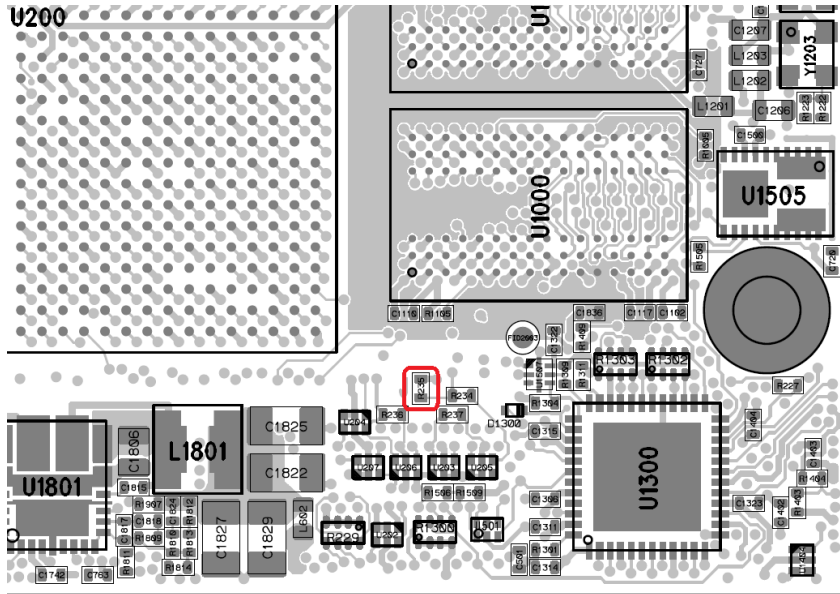


Figure 17: JTAG Boot Mode Resistor - Assembly Drawing Top View (lower right part) for Revision 4 Modules

### 3.7 eMMC Boot Mode

In the eMMC boot mode, the PS boots from the eMMC flash located on the module. The flash device is connected to the PS MIO pins 13-22 for 8-bit data transfer mode.

### 3.8 QSPI Boot Mode

In the QSPI boot mode, the PS boots from the QSPI flash located on the module. The flash device is connected to the PS MIO pins 0-5.

### 3.9 SD Card Boot Mode

In the SD card boot mode the PS boots from the SD card located on the base board. There are two SD card boot modes available on the Mercury+ XU1 SoC module. Please note that the SD boot mode with level shifter is currently not supported.

The SD boot mode with level shifter is used with Ultra High Speed (UHS) SD cards. The controller will start the communication at 3.3 V and afterwards it will command the card to drop from 3.3 V operation to 1.8 V operation. For this mode, an external SD 3.0 compliant level shifter is required. This boot mode may be supported in the future by Enclustra modules and base boards.

BOOT_MODE1	BOOT_MODE0	Description	VCC_CFG_MIO
0	1	Boot from SD card (with an external SD 3.0 compliant level shifter; currently not supported)	1.8 V
1	1	Boot from SD card (default mode)	Refer to Section 2.9.5

Table 41: SD Card Boot Modes

For the SD card boot mode, the following requirements must be met:

- The SD card must be connected to MIO pins 45-51
- A Zynq boot image must be generated from an MPSoC design having the SDIO controller enabled
- The boot image must be named "boot.bin" and then copied to the SD card
- The SDIO controller must be fed with a reasonable clock frequency. Please refer to the reference design for guidelines on SDIO settings.

For details on SD card boot, please refer to the Zynq UltraScale+ MPSoC Technical Reference Manual [22].

### 3.10 eMMC Flash Programming

The eMMC flash can be formatted and/or programmed in u-boot or Linux, like a regular SD card. The boot image or independent partition files can be transmitted via Ethernet or copied from another storage device.

Certain Xilinx tool versions support eMMC flash programming via JTAG.

### 3.11 QSPI Flash Programming via JTAG

The Xilinx Vivado and SDK software offer QSPI flash programming support via JTAG.

Certain Xilinx tools versions support QSPI flash programming via JTAG only when JTAG boot mode is used (unavailable in the standard configurations of the Mercury+ XU1 SoC module). For more information, please refer to the Xilinx documentation [22] and support. Alternatively, the QSPI flash can be programmed in u-boot or Linux by the SPI controller in the PS or from an SPI external master.

### 3.12 QSPI Flash Programming from an External SPI Master

The signals of the QSPI flash are directly connected to the module connector for flash access. As the flash signals are connected to the MPSoC device as well, the MPSoC device pins must be tri-stated while accessing the QSPI flash directly from an external device.

This is ensured by pulling the PS\_SRST# signal to GND followed by a pulse on PS\_POR#, which puts the MPSoC device into reset state and tri-states all I/O pins. PS\_SRST# must be low when PS\_POR# is released and kept low until the flash programming has finished. Afterwards, all SPI lines and PS\_SRST# must be tri-stated and another reset impulse must be applied to PS\_POR#.

Figure 18 shows the signal diagrams corresponding to flash programming from an external master.

In addition, a non-QSPI boot mode must be used during QSPI flash programming, otherwise the MPSoC device will attempt to boot from the flash and will disturb the clock.

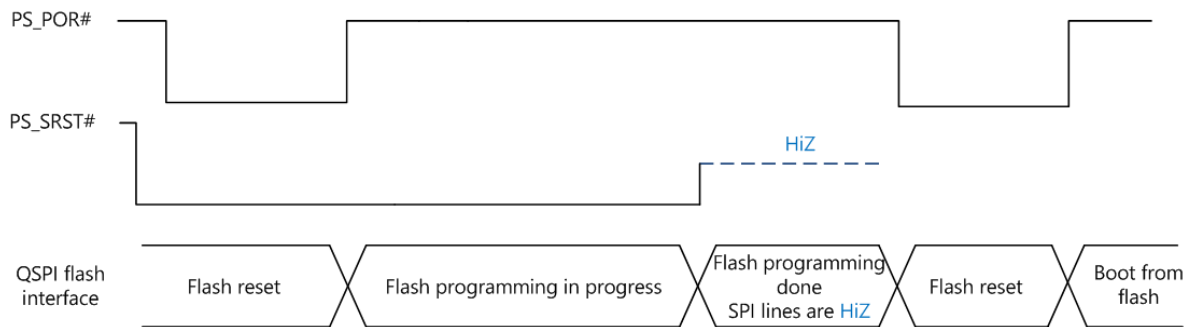


Figure 18: QSPI Flash Programming from an External SPI Master - Signal Diagrams

### Warning!

*Accessing the QSPI flash directly without putting the MPSoC device into reset may damage the equipped MPSoC device, as well as other devices on the Mercury+ XU1 SoC module.*

## 3.13 Enclustra Module Configuration Tool

In combination with an Enclustra base board, the QSPI flash can be programmed using Enclustra Module Configuration Tool (MCT) [20]. For this method, a non-QSPI boot mode must be used during QSPI flash programming. The entire procedure is described in the reference design documentation, and is only available starting with revision 2 modules.

Please note that the Xilinx Zynq devices do not support slave serial configuration, therefore only flash programming is supported by the Enclustra MCT for the Mercury+ XU1 SoC module.



# 4 I2C Communication

## 4.1 Overview

The I2C bus on the Mercury+ XU1 SoC module is connected to the MPSoC device and to the EEPROM, and is available on the module and debug connectors. This allows external devices to read the module type and to connect more devices to the I2C bus.

The I2C clock frequency should not exceed 400 kHz.

### Warning!

*Maximum I2C speed may be limited by the routing path and additional loads on the base board.*

### Warning!

*If the I2C traces on the base board are very long, 100  $\Omega$  series resistors should be added between module and I2C device on the base board.*

## 4.2 Signal Description

Table 42 describes the signals of the I2C interface - the pins are connected to the PS. All signals have on-board pull-up resistors to VCC\_3V3.

All signals must be connected to open collector outputs and must not be driven high from any source. I2C\_INT# is an input to the MPSoC and must not be driven from the MPSoC device.

Starting with revision 2 modules, the I2C bus is connected to both PS and PL sides (and not only to the PS), to offer extra flexibility and help on future development. I2C on PL side is functional only when the VCC\_IO\_B66 voltage is 1.8 V.

Level shifters are used between the I2C bus and MPSoC pins, as I/O banks 500 and 66 are supplied with 1.8 V. Please make sure that all pins are configured correctly and no pull-down resistors are enabled.

Signal Name	PS Pin	PL Package Pin	Connector Pin	Resistor
I2C_SDA	MIO11	Y7	A-113	2.2 k $\Omega$ pull-up
I2C_SCL	MIO10	V3	A-111	2.2 k $\Omega$ pull-up
I2C_INT#	MIO12	-	A-115	1.9 k $\Omega$ pull-up

Table 42: I2C Signal Description

## 4.3 I2C Address Map

Table 43 describes the addresses for several devices connected on I2C bus.

Address (7-bit)	Description
0x64	Secure EEPROM
0x5C	Secure EEPROM (assembly option, refer to Section 2.24)

Table 43: I2C Addresses

## 4.4 Secure EEPROM

The secure EEPROM is used to store the module serial number and configuration. In the future, the EEPROM will be used for copy protection and licensing features. Please contact us for further information.

An example demonstrating how to read the module information from the EEPROM memory is included in the Mercury+ XU1 SoC module reference design.

### Warning!

*The secure EEPROM is for Enclustra use only. Any attempt to write data to the secure EEPROM causes the warranty to be rendered void.*

### 4.4.1 Memory Map

Address	Length (bits)	Description
0x00	32	Module serial number
0x04	32	Module product information
0x08	40	Module configuration
0x0D	24	Reserved
0x10	48	Ethernet MAC address
0x16	48	Reserved
0x1C	32	Checksum (only for DS28CN01 EEPROM type)

Table 44: EEPROM Sector 0 Memory Map

#### Module Serial Number

The module serial number is a unique 32-bit number that identifies the module. It is stored using big-endian byte order (MSB on the lowest address).

#### Module Product Information

This field indicates the type of module and hardware revision.

Module	Product Family	Reserved	Revision	Product Information
Mercury+ XU1 SoC module	0x032F	0x[XX]	0x[YY]	0x032F [XX][YY]

Table 45: Product Information

### Module Configuration

Addr.	Bits	Comment	Min. Value	Max. Value	Comment
0x08	7-4	MPSoC type	0	4	See MPSoC type table (Table 47)
	3-0	MPSoC device speed grade	1	3	
0x09	7-6	Temperature range	0	2	See temperature range table (Table 48)
	5	Power grade	0 (Normal)	1 (Low power)	
	4-3	Gigabit Ethernet port count	0	2	
	2	RTC equipped	0	1	
	1	Extended MGT routing <sup>26</sup>	0 (No)	1 (Yes)	
	0	Reserved	-	-	
0x0A	7-2	Reserved	-	-	
	1-0	USB 2.0 port count	0	2	
0x0B	7-4	DDR4 ECC RAM size (GB)	0 (0 GB)	4 (8 GB)	Resolution = 1 GB
	3-0	QSPI flash memory size (MB)	0 (0 MB)	7 (64 MB)	Resolution = 1 MB
0x0C	7-4	eMMC flash size (GB)	0 (0 GB)	5 (16 GB)	Resolution = 1 GB
	3-0	Reserved	-	-	

Table 46: Module Configuration

The memory sizes are defined as  $\text{Resolution} \times 2^{(\text{Value}-1)}$  (e.g. DRAM=0: not equipped, DRAM=1: 1 GB, DRAM=2: 2 GB, DRAM=3: 4 GB, etc).

Table 47 shows the available MPSoC types.

<sup>26</sup>Property introduced starting with revision 3. For the "G1" module variants with 16 GTH transceivers on the module connector, a value of 1 (Yes) is programmed to the EEPROM. For the standard module variants, a value of 0 (No) is programmed to the EEPROM. The new EEPROM map definition is backwards compatible.

Value	MPSoC Device Type
0	XCZU9EG ES
1	XCZU6EG
2	XCZU9EG
3	XCZU15EG
4	XCZU6CG

Table 47: MPSoC Device Types

Table 48 shows the available temperature ranges.

Value	Module Temperature Range
0	Commercial
1	Extended
2	Industrial

Table 48: Module Temperature Range

### **Ethernet MAC Address**

The Ethernet MAC address is stored using big-endian byte order (MSB on the lowest address). Each module is assigned two sequential MAC addresses; only the lower one is stored in the EEPROM.

# 5 Operating Conditions

## 5.1 Absolute Maximum Ratings

Table 49 indicates the absolute maximum ratings for Mercury+ XU1 SoC module. The values given are for reference only; for details please refer to the Zynq UltraScale+ MPSoC, DC and AC Switching Characteristics Datasheet [24].

Symbol	Description	Rating	Unit
VCC_MOD	Supply voltage relative to GND	-0.5 to 16	V
VCC_BAT	Supply voltage for MPSoC battery-backed RAM and battery-backed RTC	0 to 3.6	V
VCC_IO_B47 VCC_IO_B48	Output drivers supply voltage relative to GND	-0.5 to 3.4	V
VCC_CFG_MIO	Output drivers supply voltage relative to GND	-0.5 to 3.63	V
VCC_IO_B64 VCC_IO_B65 VCC_IO_B66	Output drivers supply voltage relative to GND	-0.5 to 2.0	V
V_IO	I/O input voltage relative to GND	-0.5 to $V_{CC0}+0.5$	V
Temperature	Temperature range for extended temperature modules (E)*	0 to +85	°C
	Temperature range for industrial modules (I)*	-40 to +85	°C

Table 49: Absolute Maximum Ratings

## 5.2 Recommended Operating Conditions

Table 50 indicates the recommended operating conditions for Mercury+ XU1 SoC module. The values given are for reference only; for details please refer to the Zynq UltraScale+ MPSoC, DC and AC Switching Characteristics Datasheet [24].

Symbol	Description	Rating	Unit
VCC_MOD	Supply voltage relative to GND	4.75 to 15.75	V
VCC_BAT	Supply voltage for MPSoC battery-backed RAM and battery-backed RTC	2.7 to 3.6	V
VCC_IO_[x] VCC_CFG_[x]	Output drivers supply voltage relative to GND	Refer to Section 2.9.5	V
V_IO	I/O input voltage relative to GND	-0.2 to V <sub>CC0</sub> +0.2	V
Temperature	Temperature range for extended temperature modules (E)*	0 to +85	°C
	Temperature range for industrial modules (I)*	-40 to +85	°C

Table 50: Recommended Operating Conditions

### Warning!

\* The components used on the hardware are specified for the relevant temperature range. The user must provide adequate cooling in order to keep the temperature of the components within the specified range.

# 6 Ordering and Support

## 6.1 Ordering

Please use the Enclustra online request/order form for ordering or requesting information:  
<http://www.enclustra.com/en/order/>

## 6.2 Support

Please follow the instructions on the Enclustra online support site:  
<http://www.enclustra.com/en/support/>

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