# muRata Ps
## Murata Power Solutions

# D1U54P-W-450-12-HxxC Series
## 54mm 1U Front End AC-DC Power Supply Converter

## PRODUCT OVERVIEW

D1U54P-W-450-12-HAxC is a series of very high efficiency, 450 watt power factor corrected front end supplies, providing a 2Vdc main output and standby output. An active (digital) current share characteristic is provided to allow units to operate in parallel and share load current. The power supply may be hot plugged; recovers from overtemperature faults, and has status LEDs on the front panel in addition to hardware signal logic and PMBus™ status signals. The compact low profile 1U package and 14.8W/cubic inch power density make them ideal for delivering reliable, efficient power to networking equipment, workstations, storage systems and other 12Vdc distributed power architectures.

### ORDERING GUIDE

| Part Number | Power Output 90-264Vac | Main Output | Standby Output | Airflow |
|---|---|---|---|---|
| D1U54P-W-450-12- HA3C | 450W | 12Vdc | 5Vdc | Front to Back |
| D1U54P-W-450-12- HB3C | | | 12Vdc | |
| D1U54P-W-450-12- HA4C | | | 5Vdc | Back to front |
| D1U54P-W-450-12- HB4C | | | 12Vdc | |

### FEATURES

- 450W output power
- 12Vdc main output
- 5Vdc & 12Vdc standby output options
- <1U height:
  54.5mm x 228.6mm x 40mm
  (2.15" x 9.0" x 1.57")
- Card Edge DC Output and Signal I/O Connector
- IEC 60320-C14 AC Inlet
- 14.8 Watts per cubic inch density
- N+1 redundancy capable
- Active (digital) current sharing on 12Vdc main output; both outputs include ORING FET circuit
- Overvoltage, Overcurrent, Overtemperature protection
- Internal cooling fan (variable speed)
- PMBus™/I2C interface with status indicators
- RoHS compliant
- Two Year Warranty

### INPUT CHARACTERISTICS

| Parameter | Conditions | Min. | Nom. | Max. | Units |
|---|---|---|---|---|---|
| Input Source Voltage Operating Range | | 90 | 100/240 | 264 | Vac |
| Input Source Frequency | | 47 | 50/60 | 63 | Hz |
| Turn-on Input Voltage | Ramp up | 74 | | 84 | Vac |
| Turn-off Input Voltage | Ramp down | 70 | | 80 | |
| Maximum current at Vin = 100Vac | 450W; 100-240Vac | | | 6 | Arms |
| Inrush Current | Cold start between 0 to 200msec | | | 20 | Apk |
| Power Factor | At 230Vac, 100% load | 0.96 | | | W/VA |
| | At 230Vac, 50% load | 0.95 | | | |
| Efficiency | At 230Vac 20% load | | 90 | | % |
| | At 230Vac 50% load | | 94 | | |
| | At 230Vac 100% load | | 91 | | |

### OUTPUT VOLTAGE CHARACTERISTICS

| Nominal Output Voltage | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| 12V | Output Set Point Accuracy | 50% load; Tamb =25°C | 11.96 | 12.00 | 12.04 | Vdc |
| | Line and Load Regulation [2] | Setpoint; temperature; line and load | -1.0% | | +1.5 | % |
| | Ripple Voltage & Noise[1, 2] | 20MHz Bandwidth | | | 120 | mV p-p |
| | Output Current Range | | 0 | | 37.5 | A |
| | Load Capacitance | | 500 | | 4000 | µF |
| 5VSB | Nominal Output Voltage | | | 5.0 | | Vdc |
| | Line and Load Regulation [3] | | 4.76 | | 5.24 | |
| | Ripple Voltage & Noise[13] | 20MHz Bandwidth | | | 75 | mV p-p |
| | Output Current | | 0 | | 2 | A |
| | Load Capacitance | | 250 | | 1000 | µF |
| 12VSB | Nominal Output Voltage | | | 12.0 | | Vdc |
| | Line and Load Regulation [3] | | 11.7 | | 12.3 | |
| | Ripple Voltage & Noise[13] | 20MHz Bandwidth | | | 120 | mV p-p |
| | Output Current | | 0 | | 1 | A |
| | Load Capacitance | | 250 | | 1000 | µF |

[1] Ripple and noise are measured with 0.1 µF of ceramic capacitance and 10 µF of tantalum capacitance on each of the power supply outputs. A short coaxial cable to the measurement 'scope input, is used.
[2] Minimum Load of 1.75A
[3] Minimum load of 0.28A

RoHS COMPLIANT
For full details go to
www.murata-ps.com/rohs

PMBus   CB Test Certificate and Test Report   CSA   TÜVRheinland CERTIFIED   CE   CCC

## OUTPUT CHARACTERISTICS

| Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Startup Time | AC ramp up | | | 3 | s |
| Current sharing accuracy (main 12Vdc output) | > 10%  load (* % total Current) | -5 | | +5 | * % |
| Transient Response (Single transient, main 12Vdc output) | Load step of 50% max. load, > 2.5A load, 1A/µs  slew rate | -5 | | +5 | % |
| | Recovery Time to within 1% Vnom | | 2 | | ms |
| Transient Response (Single transient, Standby output) | Load step of 50% max. load, > 10% Max load, 1A/µs  slew rate | -5 | | +5 | % |
| | Recovery Time to within 1% Vnom | | 2 | | ms |
| Hot Swap Transients | | -5 | | +5 | % |
| Holdup Time (Total Effective Hold Up - See Timing Waveforms) | Full AC Input Source Range; 450W maximum total output power | 12 | | | ms |
| | Full AC Input Source Range; 270W maximum total output power | 20 | | | ms |

## ENVIRONMENTAL CHARACTERISTICS

| Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Storage Temperature Range | | -40 | | 70 | °C |
| Operating Temperature Range | 90V-264Vac, 450W | -5 | | 50 | |
| Operating Humidity | Noncondensing; +45°C | 5 | | 90 | |
| Storage Humidity | | 5 | | 95 | % |
| Altitude (without derating at 40°C) | | | | 3000 | m |
| Acoustic noise levels | 25°C, 50%load | | 45 | 50 | dB |
| Shock | 30G non-operating | | | | |
| Operational Vibration | Sine sweep; 5-200Hz, 2G; random vibration, 5-500Hz, 1.11G | | | | |
| MTBF (Target) | Per Telcordia SR-332 Issue 3 M1C3 at 40°C | | 520K | | hrs |
| Safety Approval Standards (Planned; Pending Submission) | CAN/CSA C22.2 No 60950-1: 2007, A2: 2014<br>UL 60950-1-2014<br>IEC60950-1:2005+A2:2013<br>EN 60950-1:2006+A2:2013<br>BSMI: CNS14336-1 (1999/09/30), CNS13438 (1995/06/01)<br>CCC: GB4943.1-2011; GB/T9254-2008; GB17625.1-2012<br>KCC: K60950-1 (2011-12)<br>BIS: IS 13252 (PART1): 2010 IEC 60950-1 : 2005 | | | | |
| Input Fuse | Power Supply has internal 8A/250V fast blow fuse on the AC line input | | | | |
| Weight | 1.51 lbs (0.685 kg) | | | | |

## PROTECTION CHARACTERISTICS

| Output | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| | Overtemperature (intake) | Auto-restart with 4°C hysteresis for recovery (warning issued at 70°C) | | 75 | | °C |
| 12V | Overvoltage | Latching | 13.0 | | 14.5 | Vdc |
| | Overcurrent (target) | The output shall shutdown when an overcurrent condition is detected.<br>It will auto restart after 1sec; however if the overcurrent condition is redetected the output will once again shutdown. The output will once again re-start, however if the overcurrent condition persists it will latch of after the fifth unsuccessful attempt.<br>To reset the latch it will be necessary to toggle the PS_ON_L signal or recycle the incoming DC source. | 40 | | 50 | Adc |
| 5VSB | Overvoltage | Latching | 5.4 | | 6.0 | Vdc |
| | Overcurrent | The output shall shutdown when an overcurrent is detected.<br>It will auto restart after 2sec; however if the overcurrent is re-detected the output will once again shutdown.<br>This cycle will occur indefinitely while the overcurrent condition persists. | 2.1 | | 3.0 | Adc |
| 12VSB | Over-Voltage | Latching;  toggle  PS_ON or recycle  DC input to reset | 13.0 | | 14.5 | Vdc |
| | Over-Current | The output shall shutdown when an overcurrent is detected.<br>It will auto restart after 2sec; however if the overcurrent is re-detected the output will once again shutdown.<br>This cycle will occur indefinitely while the overcurrent condition persists. | 1.2 | | 2 | Adc |

## ISOLATION CHARACTERISTICS

| Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Insulation Safety Rating | Input to Output - Reinforced | 3000 | | | Vrms |
| | Input to Chassis - Basic | 1500 | | | Vrms |
| Isolation | Output to Chassis | 500 | | | Vdc |

## EMISSIONS AND IMMUNITY

| Characteristic | Standard | Compliance |
|---|---|---|
| Input Current Harmonics | IEC/EN 61000-3-2 | Complies |
| Voltage Fluctuation and Flicker | IEC/EN 61000-3-3 | Complies |
| Conducted Emissions | FCC 47 CFR Part 15 CISPR 22/EN55022 | Class A with 6dB margin |
| ESD Immunity | IEC/EN 61000-4-2 | Level 4 criteria A |
| Radiated Field Immunity | IEC/EN 61000-4-3 | Level 3 criteria B |
| Electrical Fast Transients/Burst Immunity | IEC/EN 61000-4-4 | Level 3 criteria A |
| Surge Immunity | IEC/EN 61000-4-5 | 1. EN61000-4-5, Lev. 3 (Com. Mode: 2kV, 12Ω, Diff. Mode: 1kV, 2Ω), criteria A [1]<br>2. GR-1089-CORE (NEBS) Level 1 Table 4-30 (Com/Diff. Mode: 2kV, 2Ω) [1] |
| RF Conducted Immunity | IEC/EN 61000-4-6 | Level 3 criteria A |
| Magnetic Field Immunity | IEC/EN 61000-4-8 | 3 A/m criteria B |
| Voltage Dips, Interruptions | IEC/EN 61000-4-11 | 230Vin, 80% load, Phase 0°, Dip 100% Duration 10ms (A)<br>230Vin, 50% load, Phase 0°, Dip 100% Duration 20ms (VSB:A, V1:B)<br>230Vin, 100% load, Phase 0°, Dip 100% Duration > 20ms (VSB, V1:B) |

[1] tests are performed at 50% maximum load, and with minimum capacitance at both outputs

## STATUS INDICATORS AND CONTROL SIGNALS

**INPUT LED**

| Condition | LED Status |
|---|---|
| Input Voltage Present | Solid Green |
| Input Voltage fault or warning | Blinking Green |
| Input off | Off |

**POWER LED**

| Condition | LED Status |
|---|---|
| Fault concurrent indication via PMBus Status_x registers | Solid Amber |
| Warning, concurrent indication via PMBus Status_x registers | Blinking Amber |
| Standby, 12Vdc Main output off, Vstby On | Blinking Green |
| Power Good 12Vdc Main output on, Vstby On | Solid Green |
| Power Off 12Vdc Main output off, Vstby Off | Off |

## STATUS AND CONTROL SIGNALS

| Signal Name | I/O | Description | Interface Details |
|---|---|---|---|
| INPUT_OK (AC Source)<br>Link to connector pin | Output | The signal output is driven high when input source is available and within acceptable limits. The output is driven low to indicate loss of input power.<br>There is a minimum of 1ms pre-warning time before the signal is driven low prior to the PWR_OK signal going low. The power supply must ensure that this interface signal provides accurate status when AC power is lost. | Pulled up internally via 10K to VDD*.<br>A logic high >2.0Vdc<br>A logic low <0.8Vdc<br>Driven low by internal CMOS buffer (open drain output). |
| PW_OK (Output OK)<br>Link to connector pin | Output | The signal is asserted, driven high, by the power supply to indicate that the main output is valid. Should a main output or standby output fault occur, the PW_OK signal will de-assert + driven low. 5V & 3.3V Standby output products do not de-assert the PW_OK signal during OCP event on the standby output.<br>PW_OK output is driven low to indicate that the Main output is outside of lower limit of regulation. | Pulled up internally via 10K to VDD*.<br>A logic high >2.0Vdc<br>A logic low <0.8Vdc<br>Driven low by internal CMOS buffer (open drain output). |
| SMB_ALERT (FAULT/WARNING)<br>Link to connector pin | Output | The signal output is driven low to indicate that the power supply has detected a warning or fault and is intended to alert the system. This output must be driven high when the power is operating correctly (within specified limits).<br>The signal will revert to a high level when the warning/fault stimulus (that caused the alert) is removed. As reported by PMBus Status_x Registers, with exception of Status_CML. | Pulled up internally via 10K to VDD*.<br>A logic high >2.0Vdc<br>A logic low <0.8Vdc<br>Driven low by internal CMOS buffer (open drain output). |
| PRESENT_L (Power Supply Absent)<br>Link to connector pin | Output | The signal is used to detect the presence (installation) of a PSU by the host system. The signal is connected to PSU logic +VSB_Return within the power module. | Passive connection to +VSB_Return.<br>A logic low <0.8Vdc |
| PS_ON (Power Supply Enable/Disable<br>Link to connector pin | Input | This signal is pulled up internally to the internal housekeeping supply (within the power supply). The power supply main 12Vdc output will be enabled when this signal is pulled low to +VSB_Return.<br>In the low state the signal input shall not source more than 1mA of current. The 12Vdc output will be disabled when the input is driven higher than 2.4V, or open circuited. Cycling this signal shall clear latched fault conditions. | Pulled up internally via 10K to VDD*.<br>A logic high >2.0Vdc<br>A logic low <0.8Vdc<br>Input is via CMOS Schmitt trigger buffer. |
| PS_KILL<br>Link to connector pin | Input | This signal is used during hot swap to disable both outputs during hot swap extraction. The input is pulled up internally to VDD* (within the power supply).<br>The signal is provided on a short (lagging pin) and should be connected to +VSB_Return. | Pulled up internally via 10K to VDD*.<br>A logic high >2.0Vdc<br>A logic low <0.8Vdc<br>Input is via CMOS Schmitt trigger buffer. |
| ADDR (Address Select)<br>Link to connector pin | Input | An analog input that is used to set the address of the internal slave devices (EEPROM and microprocessor) used for digital communications.<br>Connection of a suitable resistor to +VSB_Return, in conjunction with an internal resistor divider chain, will configure the required address. See configuration table for details. | DC voltage between the limits of 0 and +3.3Vdc. |
| SCL (Serial Clock)<br>Link to connector pin | Both | A serial clock line compatible with PMBus™ Power Systems Management Protocol Part 1 – General Requirements Rev 1.1.<br>No additional internal capacitance is added that would affect the speed of the bus.<br>The signal is provided with a series isolator device to disconnect the internal power supply bus in the event that the power module is unpowered, | ** VIL is 0.8V maximum<br>VOL is 0.4V maximum when sinking 3mA<br>VIH is 2.1V minimum |
| SDA (Serial Data)<br>Link to connector pin | Both | A serial data line compatible with PMBus™ Power Systems Management Protocol Part 1 – General Requirements Rev 1.1.<br>The signal is provided with a series isolator device to disconnect the internal power supply bus in the event that the power module is unpowered, | ** VIL is 0.8V maximum<br>VOL is 0.4V maximum when sinking 3mA<br>VIH is 2.1V minimum |
| V1_SENSE<br>V1SENSE_RTN | Input | Remote sense connections intended to be connected at and sense the voltage at the point of load. The voltage sense will interact with the internal module regulation loop to compensate for voltage drops due to connection resistance between the output connector and the load.<br>If remote sense compensation is not required then the voltage can be configured for local sense by:<br>1. V1_SENSE directly connected to power gold fingers P1-P8 (inclusive)<br>2. V1_SENSE_RTN directly connected to gold fingers P9 to P16 (inclusive) | Compensation for a up to 0.12Vdc total connection drop (output and return connections). |
| ISHARE<br>Link to connector pin | Bi-Directional Digital Bus | The current sharing signal is connected between sharing units (forming an ISHARE bus). It is an input and/or an output (bi-directional analog bus) as the voltage on the line controls the current share between sharing units.<br>A power supply will respond to a change in this voltage but a power supply can also change the voltage depending on the load drawn from it.<br>On a single unit the voltage on the pin (and the common ISHARE bus would read 8VDC at 100% load (module capability). For two identical units sharing the same 100% load this would read 4VDC for perfect current sharing (i.e. 50% module load capability per unit). | Analogue voltage:<br>+8V maximum; 10K to +12V_RTN |

*VDD is an internal voltage rail derived from VSB and an internal housekeeping rail ("diode ORed") and is compatible with the voltage tolerances of VSB.

**For robust PMBus communications, it is recommended SDA and SCA lines be pulled up via external resistors to a voltage of 3.3V or greater.

## TIMING SPECIFICATIONS

### Turn-On Delay & Output Rise Time:
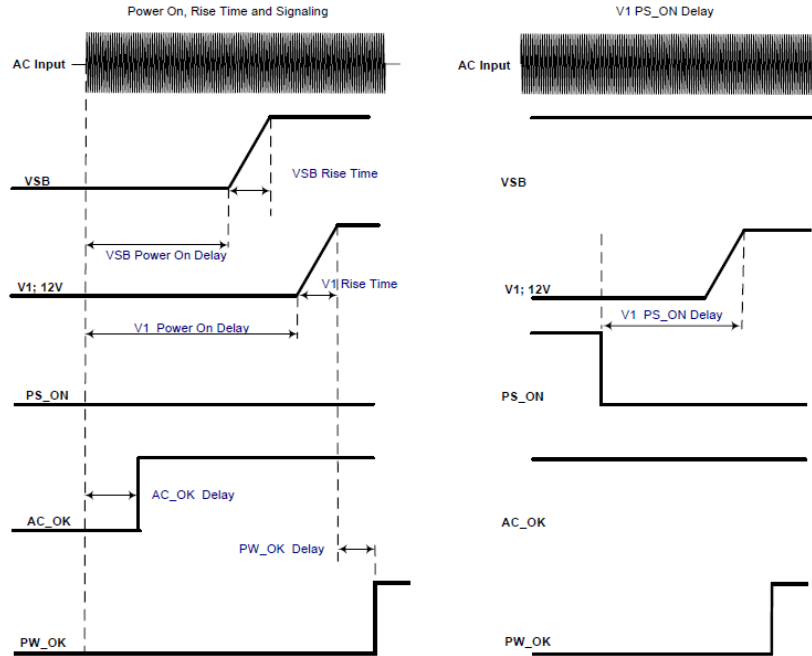


1. The turn-on delay after application of AC input within the operating range shall as defined in the following tables.
2. The output rise times shall be measured from 10% of the nominal output to the lower limit of the regulation band as defined in the following tables.

| Time | Min | Max |
|---|---|---|
| Vsb Rise time, from 10% to 90% Nominal output VDC | - | 60ms |
| V1 Rise time, form 10% to 90% Nominal output VDC | 6ms | 60ms |
| Vsb Power-on-delay | - | 2700ms |
| V1 Power-on-delay | - | 3000ms |
| V1 PS_ON delay | 100ms | 150ms |
| V1 PWOK delay | 100ms | 300ms |
| ACOK detect | 300ms | 1500ms |

## TIMING SPECIFICATIONS

### Turn-Off (Shutdown by PS_ON)
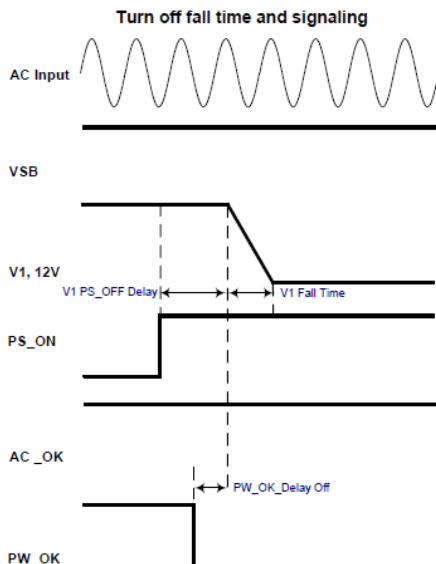


| Turn-Off Timing | Min | Max | Notes |
|---|---|---|---|
| V1 Fall time | - | - | Must be monotonic |
| V1 PS_OFF delay | - | 10ms | |
| PW_OK delay off | 1ms | - | |

1. Note this characteristic is applicable for the main 12Vdc output shutdown from PS_ON pulled high.

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## TIMING SPECIFICATIONS

### Power Removal Holdup



Power removed holdup, falltime and signaling
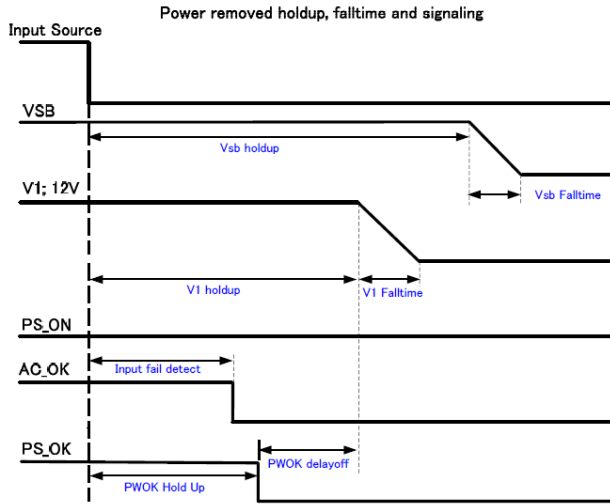
| Power Removal Timing | Min | Max | Notes |
|---|---|---|---|
| Vsb holdup | 40ms | 2S | 100% load |
| V1 holdup (Effective Total) | 12ms | - | 100% load |
| Input fail detect | 5ms | 11ms | 100% load |
| PWOK delay off | 1ms | - | 100% load |
| PWOK Hold Up | 11ms | - | 100% load |

## OUTPUT CONNECTOR & SIGNAL INTERFACE

### Gold Finger Layout & Pin Assignment

Mating Connector: FCI 10126933080820xALF; "Straddle" Connector



Representative View:
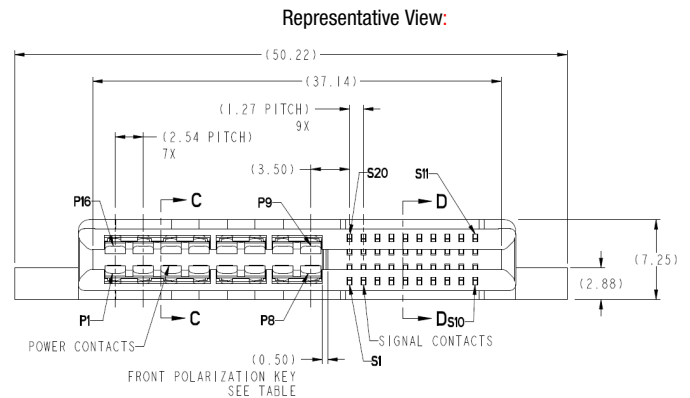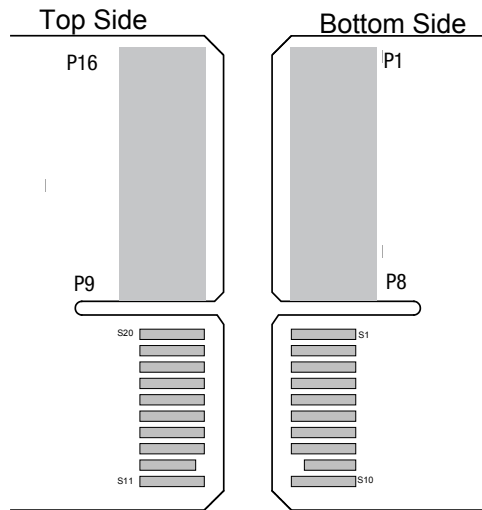
Notes: Gold Fingers S9 (PS_KILL) and S12 (PS PRESENT/L) are "last to make; fist to break" short pins.
For illustration purposes only, actual product may appear different. Dimensions as follows:
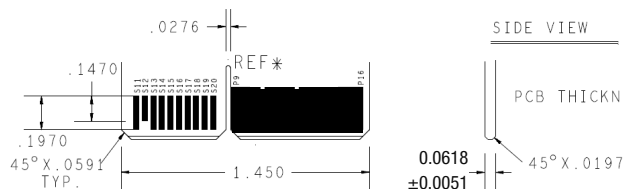


FINGER PLATING SHALL BE AS PER IPC 2221, SECTION 4.4.4, TABLE 4.3, CLASS 2.

## OUTPUT CONNECTOR PIN ASSIGNMENTS - D1U54P-W-450-12-HBxC

(Power Supply Gold Finger/Card

| Pin# | Signal Name | Description/Comment |
|---|---|---|
| P1-P8 inclusive | V1 (+12VOUT) | +12Vdc Main Output |
| P9-P16 inclusive | V1 (+12VOUT) RTN/PGND) | +12Vdc Main Output and Standby Output Return |
| S1 | +VSB | Standby Output |
| S2 | +VSB | Standby Output |
| S3 | Reserved | No User Connection |
| S4 | ISHARE | Active Current Share Bus; link back to signal definition |
| S5 | SDA | I²C Serial Data Line; link back to signal definition |
| S6 | SCL | I²C Serial Clock Line; link back to signal definition |
| S7 | SMB_ALERT | Alert signal to host system; link back to signal definition |
| S8 | PS_ON | Remote On/Off (Enable/Disable) ; link back to signal definition |
| S9 | PS_KILL | Power Supply "kill"; short pin ; link back to signal definition |
| S10 | INPUT_OK | AC Input Source Present & "OK" ; link back to signal definition |
| S11 | PW_OK | Output DC Power "OK"; link back to signal definition |
| S12 | PS PRESENT | Power Module Present; short pin; link back to signal definition |
| S13 | Reserved | No User Connection |
| S14 | Reserved | No User Connection |
| S15 | V1_SENSE_RTN | +12Vdc Main Output Remote Sense Return |
| S16 | V1_SENSE | +12Vdc Main Output Remote Sense |
| S17 | ADDR | Address Protocol Selection; (select address by use of the appropriate pull down resistor – see table below) ; link back to signal definition |
| S18 | Reserved | No User Connection |
| S19 | +VSB | Standby Output |
| S20 | +VSB | Standby Output |

## ADDR ADDRESS SELECTION

| ADDR pin (A3) resistor to GND (K-ohm)* | Power Supply Main Controller (Serial Communications Slave Address) | Power Supply External EEPROM (Serial Communications Slave Address) |
|---|---|---|
| 0.82 | 0xB0 | 0xA0 |
| 2.7 | 0xB2 | 0xA2 |
| 5.6 | 0xB4 | 0xA4 |
| 8.2 | 0xB6 | 0xA6 |
| 15 | 0xB8 | 0xA8 |
| 27 | 0xBA | 0xAA |
| 56 | 0xBC | 0xAC |
| 180 | 0xBE | 0xAE |

* The resistor shall be +/-5% tolerance

Link back to Address Definition
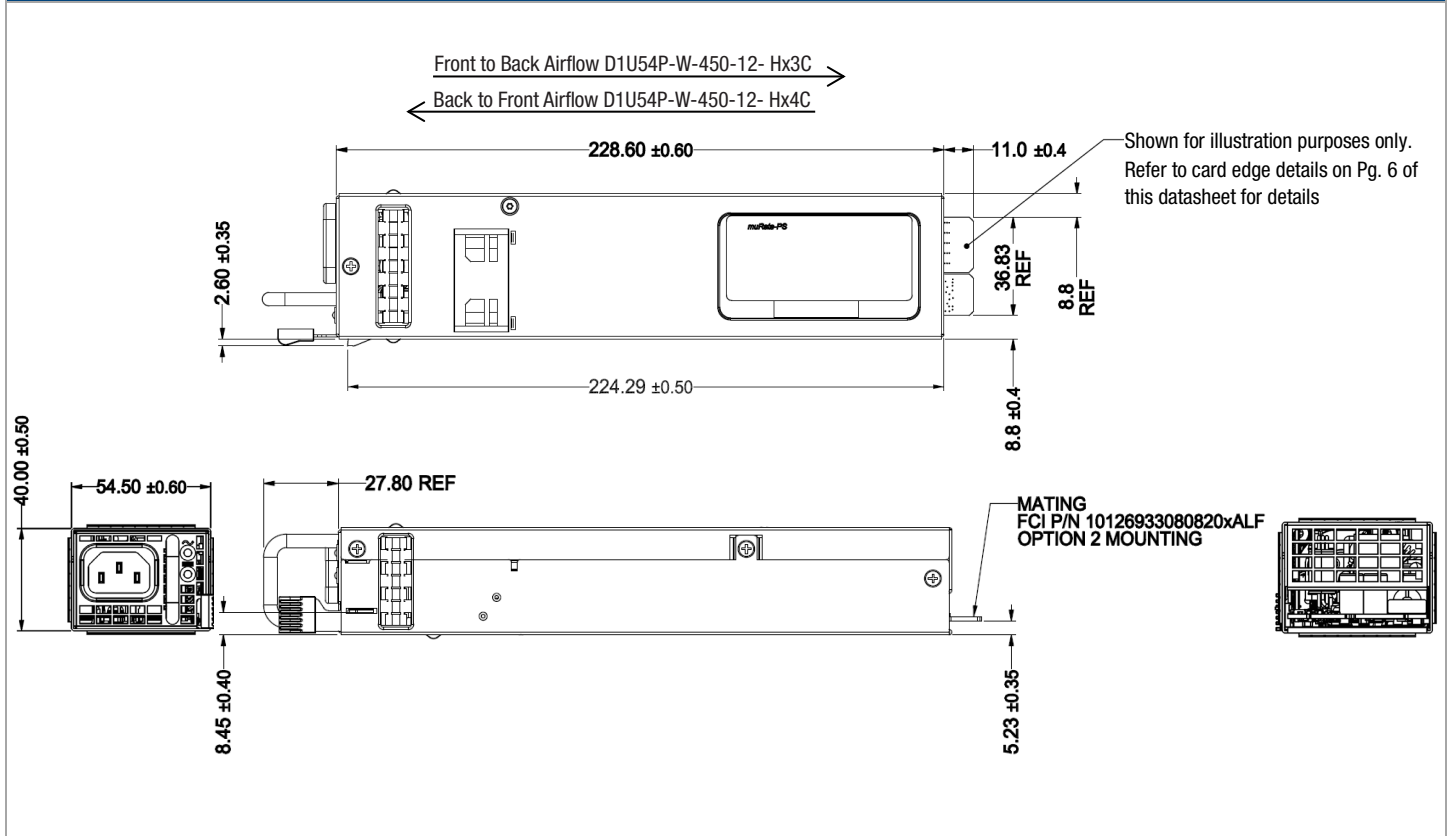
## WIRING DIAGRAM FOR OUTPUT



Dotted lines show optional remote sense connections.
Optional remote sense lines can be attached to a load that is a distance away from the power supply to improve regulation at the load.
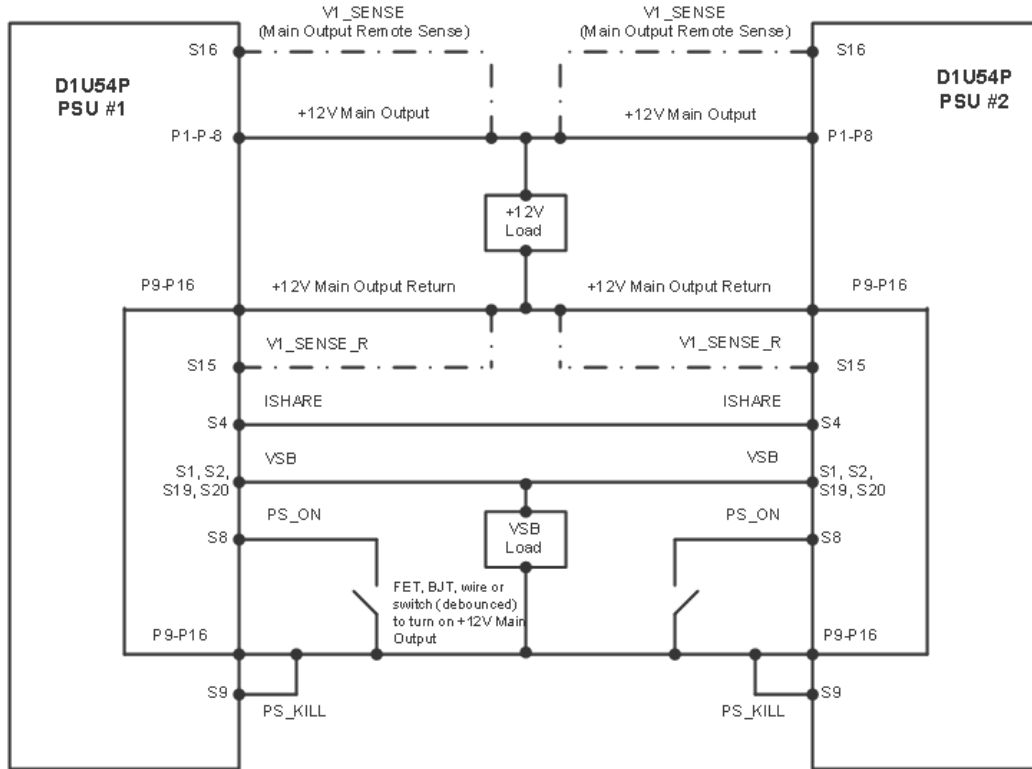
## CURRENT SHARE NOTES

1. Main Output: Current sharing is achieved using the active current share method details.)
2. Current sharing can be achieved with or without the remote (V_SENSE) connected to the common load.
3. +VSB Outputs can be tied together for redundancy but total combined output power must not exceed the rated standby power. The +VSB output has an internal ORing MOSFET for additional redundancy/internal short protection.
4. The current sharing pin B5 is connected between sharing units (forming an ISHARE bus). It is an input and/or an output (bi-directional analog bus) as the voltage on the line controls the current share between sharing units. A power supply will respond to a change in this voltage but a power supply can also change the voltage depending on the load drawn from it. On a single unit the voltage on the pin (and the common ISHARE bus would read 8VDC at 100% load. For two units sharing the same load this would read 4VDC for perfect current sharing (i.e. 50% load per unit).
5. The load for both the main 12Vdc and the VSB rails at initial startup shall not be allowed to exceed the capability of a single unit. The load can be increased after a delay of 3sec (minimum), to allow all sharing units to achieve steady state regulation.

**Mechanical Envelope**



Front to Back Airflow D1U54P-W-450-12- Hx3C

Back to Front Airflow D1U54P-W-450-12- Hx4C

228.60 ±0.60

11.0 ±0.4

Shown for illustration purposes only. Refer to card edge details on Pg. 6 of this datasheet for details

2.60 ±0.35

36.83 REF

8.8 REF

224.29 ±0.50

8.8 ±0.4

40.00 ±0.50

54.50 ±0.60

27.80 REF

MATING FCI P/N 10126933080820xALF OPTION 2 MOUNTING

8.45 ±0.40

5.23 ±0.35

1.  Reference file: I:\Eng_wip\UserPDDwg\1909\M1909_Drawing for Product Datasheet_20170407
2.  For illustration purposes of the envelope and main features only. Not all details visible on actual product are represented. 3D model is available upon request.
3.  Dimensions are in mm, Not to Scale

Link Back to Features

| OPTIONAL ACCESSORIES | |
|---|---|
| Description | Part Number |
| 12Vdc D1U54P 450W series Output Connector Card | D1U54P-12-EDGE |

| APPLICATION NOTES | | |
|---|---|---|
| Document Number | Description | Link |
| ACAN-72 | D1U54P-x Communication Protocol | http://power.murata.com/datasheet?/data/apnotes/acan-72.pdf |
| ACAN-73 | Output Connector Card with edge connector | http://power.murata.com/datasheet?/data/apnotes/acan-73.pdf |

**www.murata-ps.com/support**