

### FEATURES:

- 800W output power
- Anderson SAF-D-GRID® input connector rated for both AC (90-305VAC) or HVDC (260-400Vdc) input voltage from a single variant
- FCI 10122460-005LF combined DC output and signal interface connector
- 94% minimum efficiency at 230V, 50% load
- 12V Main output, up to 66.7ADC
- 12V Standby output, up to 2.0A
- Nominal Dimensions: 54.5mm [2.15"] (W) x 236.6mm [9.32"] (L) x 40.0mm [1.57"] (H)
- > 25 Watts per cubic inch density (W/in<sup>3</sup>)
- N+1 redundancy, hot swap capable
- Integral ORING isolation MOSFETS, both outputs
- Active (analogue DC I<sub>SHARE</sub> bus) current sharing on 12V main output, droop sharing on standby output
- Overvoltage, overcurrent, over temperature protection
- Internal cooling fan (variable speed)
- PMBus™ / I<sup>2</sup>C interface monitoring and control
- RoHS compliant
- Two Year Warranty



Available now at: [www.murata-ps.com/en/3d/acdc.html](http://www.murata-ps.com/en/3d/acdc.html)

### PRODUCT OVERVIEW

D1U54P-M-800-12-HBxC is a series of power factor corrected, AC/HVDC input, high efficiency front end power supplies each with both a 12V main and 12V Standby output. Standard features include active current sharing, hot plug capability, status LEDs, hardware signal logic and PMBus™ Communications. The low profile 1U package and 25.4W/cubic inch power density makes this series ideal for delivering reliable, efficient power to networking equipment, workstations, storage systems and other 12V distributed power architectures.

### ORDERING GUIDE

Part Number	Power Output (0-50°C) 90-305Vac or 260-400Vdc	Main Output	Standby Output	Airflow
D1U54P-M-800-12-HB3BC	800W	12Vdc	12Vdc	Front to Back
D1U54P-M-800-12-HB4BC				Back to front

### INPUT CHARACTERISTICS

Parameter	Conditions	Min.	Nom.	Max.	Units
Input Source Operating Range, AC Input		90	100/230/277	305	Vac
Input Frequency, AC Input		47	50/60	63	Hz
Turn-on Voltage, AC Input	Ramp up	80		90	Vac
Turn-off Voltage, AC Input	Ramp down	70		80	
Maximum current at Vin = 100Vac	800W output power			10	Arms
Input Source Voltage HVDC Operating Range		260 <sup>1</sup>	380	400	Vdc
Turn-on Voltage, HVDC Input	Ramp up	250	255	260	
Turn-off Voltage, HVDC Input	Ramp down	240	245	250	
Inrush Current, AC / HVDC	At 305VAC; 25°C; 0 to 200ms cold start			35	Apk
Power Factor	At 230Vac, 100% load	0.96			%
	At 230Vac, 50% load	0.95			
	At 230Vac, 20% load	90			
Efficiency (excluding fan load)	At 230Vac, 50% load	94			
	At 230Vac, 100% load	91			

<sup>1</sup> Min limit based on NTT TR No.176002 1.1.EDITION April 1st 2015 & ETSI EN300 132-3-1 V2.1.1 (2012-02)

NB: Line voltage type change-over time: 10s minimum time required between switch off of an incoming AC source and the switch on of an incoming DC source (or vice versa). Power supply damage will not result from faster change-over time, however the output may not operate.

### OUTPUT VOLTAGE CHARACTERISTICS

Nominal Output Voltage	Parameter	Conditions	Min.	Typ.	Max.	Units
12V	Output Set Point Accuracy	50% load; Tamb = 25°C	11.96	12.00	12.04	Vdc
	Line and Load Regulation <sup>2</sup>	Setpoint; temperature; line and load	-1.0%		+1.0	%
	Ripple Voltage & Noise <sup>1, 2</sup>	20MHz Bandwidth			150	mV p-p
	Output Current Range (800W)		0		66.7	A
	Load Capacitance		500		4000	µF
12VSB	Output Set Point Accuracy	50% load; Tamb = 25°C	11.96	12.00	12.04	Vdc
	Line and Load Regulation	Setpoint; temperature; line and load	11.7		12.3	
	Ripple Voltage & Noise <sup>1</sup>	20MHz Bandwidth			120	mV p-p
	Output Current Range (24W)		0		2	A

<sup>1</sup>Ripple and noise measured with a parallel combination of ceramic and tantalum capacitors on each of the power module outputs. A short coaxial cable connected directly to the input of a scope is required.

<sup>2</sup>Below 5% loading the overall voltage deviation shall be within ±500mV due to zero load "skip" cycle mode of operation. There will be a large LF ripple content when in "skip" mode. To meet the specified 150mV<sub>p-p</sub> ripple, a minimum 500µF load capacitance is required



Test Certificate  
and Test Report

### ENVIRONMENTAL CHARACTERISTICS

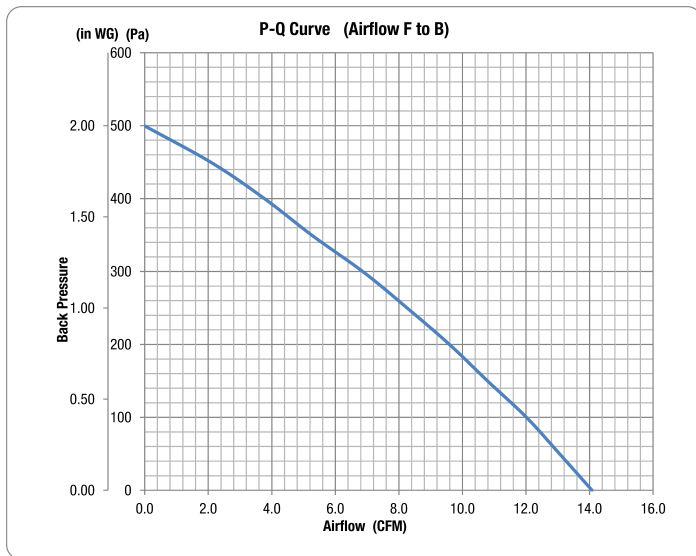
Parameter	Conditions	Min.	Typ.	Max.	Units
Storage Temperature Range		-40		70	°C
Operating Temperature Range	90V-305Vac; 800W	-5		50	
Operating Humidity	Noncondensing; +45°C	5		90	%
Storage Humidity		5		95	
Altitude (without derating at 40°C)				3000	m
Shock	30G non-operating				
Operational Vibration	Sine sweep; 5-200Hz, 2G; random vibration, 5-500Hz, 1.1G				
MTBF (Ground Benign, Controlled)	Per Telcordia SR-332 Issue 3 M1C3 @ 40°C		872K		hrs
Safety Approvals	CAN/CSA C22.2 No 60950-1-07, Am.1:2011, Am 2:2014 ANSI/UL 60950-1-2014 IEC60950-1:2005 (2nd Ed.), Am 1:2009 + Am 2:2013 EN 60950-1:2006+A11:2009 +A1:2010 +A12:2011 +A2:2013				
Input Fuse	Power Supply has dual internal (both incoming source lines) fast acting fuses; 16A/420Vac/420Vdc				
Weight	1.702 lbs (0.772 kg)				

### OUTPUT CHARACTERISTICS

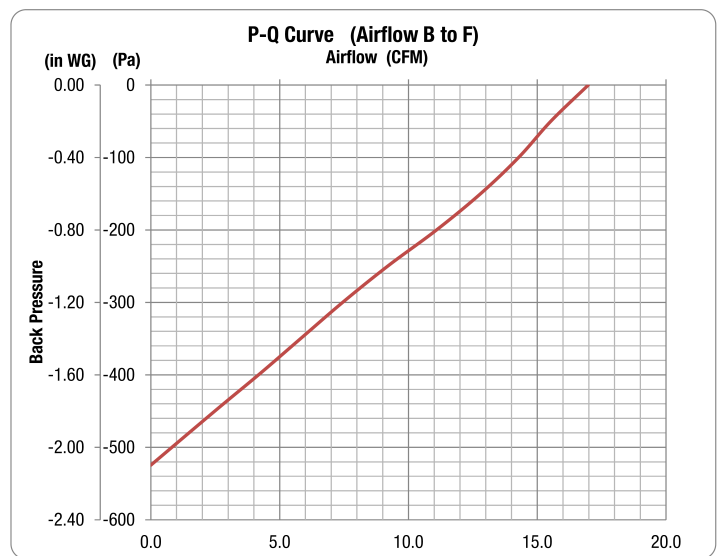
Parameter	Conditions	Min.	Typ.	Max.	Units
Startup Time	AC ramp up Note: Following a "turn off" of the 12V Main output (for any reason whatsoever) the output shall not be allowed to "turn on" again for 1sec (even if all necessary operating conditions are met).		1	3	s
Transient Response	Main 12V, 50% load step, 1A/μs di/dt			±5	%
	12VSB, 50% load step, 1A/μs di/dt			500	μs
Current sharing accuracy (Main 12V output)	>10% load; (* percentage of full load)			±5*	%
Hot Swap Transients				±5	%
Holdup Time (Total Effective Hold Up - See Timing Waveforms)	Full AC Input Source Range; full load (800W)	10			ms
	Full AC Input Source Range; (400W)	20			
Leakage/Touch Current	305VAC; 50/60Hz			1.5	mArms

### AIRFLOW; PRESSURE VS. FLOW (PQ) CURVES

D1U54P-M-800-12-HB3BC; Front to Back Airflow



D1U54P-M-800-12-HB4BC; Back to Front Airflow



**Notes:**

- The above curves represent performance based upon a the use of a Delta FFB0412EN (28mm) thickness fan.
- Curves recorded at room ambient (circa 25°C).
- Curves generated with internal fan running at 100% duty cycle

### PROTECTION CHARACTERISTICS

Output	Parameter	Conditions	Min.	Typ.	Max.	Units
	Overtemperature (intake)	Autorestart with 4°C hysteresis for recovery (warning issued at 70°C)		75		°C
12V	Overshoot	Latching	13.0		14.5	V
	Overcurrent (target; TBC)	The output shall shutdown when an overcurrent condition is detected. It will auto restart after 1sec; however if the overcurrent condition is re-detected the output will once again shutdown. The output will once again re-start, however if the overcurrent condition persists it will latch of after the fifth unsuccessful attempt. To reset the latch it will be necessary to toggle the PS_ON_L signal (pin B4) or recycle the incoming AC source.	70		90	A
12VSB	Overshoot	Latching	13.0		14.5	V
	Overcurrent	The output shall shutdown when an overcurrent is detected. It will auto restart after 2sec; however if the overcurrent is re-detected the output will once again shutdown. This cycle will occur indefinitely while the overcurrent condition persists.	2.5		3.5	A

### ISOLATION CHARACTERISTICS

Parameter	Conditions	Min.	Typ.	Max.	Units
Insulation Safety Rating	Input to Output - Reinforced	3000			Vrms
	Input to Chassis - Basic	1500			Vrms
Isolation	Output to Chassis	500			Vdc

### EMISSIONS AND IMMUNITY

Characteristic	Standard	Compliance	Notes
Input Current Harmonics	IEC/EN 61000-3-2	Complies with Class A limits	
Voltage Fluctuation and Flicker	IEC/EN 61000-3-3	Complies	
Conducted Emissions	FCC 47 CFR Part 15 CISPR 22/EN55032	Class A with 6dB margin	
ESD Immunity	IEC/EN 61000-4-2	±8KV Contact; ±15KV air discharge; Criteria A	
Radiated Field Immunity	IEC/EN 61000-4-3	10V/m, 1KHz, 80% AM, 80MHz to 1GHz Criteria A	
Electrical Fast Transients/Burst Immunity	IEC/EN 61000-4-4	Level 3 criteria A	
Surge Immunity	IEC/EN 61000-4-5	Level 3 criteria A	(1KV, 2ohm differential; 2KV, 12 ohm common mode)
RF Conducted Immunity	IEC/EN 61000-4-6	Level 3 criteria A	
Voltage Dips, Interruptions	IEC/EN 61000-4-11	230V <sub>in</sub> , 70% load, Phase 0°, Dip 100% Duration 10ms (A) 230V <sub>in</sub> , 50% load, Phase 0°, Dip 100% Duration 20ms (VSB:A, V1:B) 230V <sub>in</sub> , 100% load, Phase 0°, Dip 100% Duration >20ms (VSB, V1:B)	<ul style="list-style-type: none"> <li>Voltage dips, 230V or 100V V<sub>in</sub>, 70% load, phase 0, dip 100% duration 10ms (Criteria A)</li> <li>Voltage dips, 230V or 100V V<sub>in</sub>, 100% load, phase 0, dip 100% duration 5ms (Criteria A)</li> </ul>

### STATUS INDICATORS

LED NAME	LED MODE	LED STATE/OPERATION	DESCRIPTION
Input	OK	Solid Green	Input voltage operating within normal specified range
Input	OV/UV WARNING	Blinking Green	Input voltage operating in: 1) overvoltage warning, or 2) undervoltage warning range
Input	OFF OR FAULT	Off	Input voltage operating: 1) above overvoltage range, or 2) below undervoltage range, or 3) not present
Output	POWER GOOD	Solid Green	Main output and standby output enabled with no power supply warning or fault detected
Output	STANDBY	Blinking Green	Standby output enabled with no power supply warning or fault detected
Output	WARNING	Blinking Amber	Power supply warning detected as per PMBus™ STATUS_X reporting bytes*
Output	FAULT	Solid Amber	Power supply fault detected as per PMBus™ STATUS_X reporting bytes*

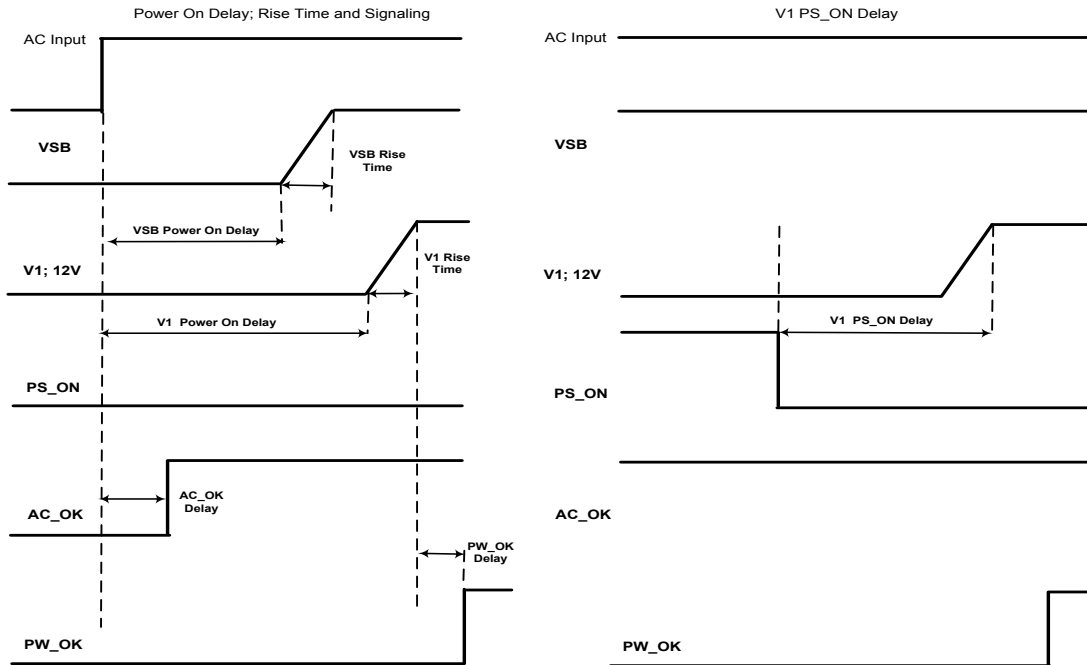
\* LED fault/warning operation follows PMBus™ fault/warning status flags reporting but will not be 'sticky';(i.e. if the fault stimulus is removed, even though the actual fault/warning status flag is still showing (still "sticky" and not cleared), the relevant LED will revert to normal (non-fault) operation.

**STATUS AND CONTROL SIGNALS**

Signal Name	I/O	Description	Interface Details
<a href="#">INPUT_OK</a> (AC & HVDC Source)	Output	The signal output is driven high when input source is available and within acceptable limits. The output is driven low to indicate loss of input power. There is a minimum of 1ms pre-warning time before the signal is driven low prior to the PWR_OK signal going low. The power supply must ensure that this interface signal provides accurate status when AC power is lost.	Pulled up internally via 10K to 3.3Vdc. A logic high >2.0Vdc A logic low <0.8Vdc Driven low by internal CMOS buffer (open drain output).
<a href="#">PW_OK</a> (Output OK)	Output	The signal is asserted, driven high, by the power supply to indicate that all outputs are valid. If any of the outputs fail then this output will be hi-impedance or driven low. The output is driven low to indicate that the Main output is outside of lower limit of regulation (11.4Vdc).	Pulled up internally via 10K to 3.3Vdc. A logic high >2.0Vdc A logic low <0.8Vdc Driven low by internal CMOS buffer (open drain output).
<a href="#">SMB_ALERT</a> (FAULT/WARNING)	Output	The signal output is driven low to indicate that the power supply has detected a warning or fault and is intended to alert the system. This output must be driven high when the power is operating correctly (within specified limits). The signal will revert to a high level when the warning/fault stimulus (that caused the alert) is removed.	Pulled up internally via 10K to 3.3Vdc. A logic high >2.0Vdc A logic low <0.8Vdc Driven low by internal CMOS buffer (open drain output).
<a href="#">PRESENT_L</a> (Power Supply Absent)	Output	The signal is used to detect the presence (installed) of a PSU by the host system. The signal is connected to PSU logic SGND within the power module.	Passive connection to +VSB_Return. A logic low <0.8Vdc
<a href="#">PS_ON</a> (Power Supply Enable/Disable)	Input	This signal is pulled up internally to the internal housekeeping supply (within the power supply). The power supply main 12Vdc output will be enabled when this signal is pulled low to +VSB_Return. In the low state the signal input shall not source more than 1mA of current. The 12Vdc output will be disabled when the input is driven higher than 2.4V, or open circuited. Cycling this signal shall clear latched fault conditions.	Pulled up internally via 10K to 3.3Vdc. A logic high >2.0Vdc A logic low <0.8Vdc Input is via CMOS Schmitt trigger buffer.
<a href="#">PS_KILL</a>	Input	This signal is used during hot swap to disable the main output during hot swap extraction. The input is pulled up internally to the internal housekeeping supply (within the power supply). The signal is provided on a short (lagging pin) and should be connected to +VSB_Return.	Pulled up internally via 10K to 3.3Vdc. A logic high >2.0Vdc A logic low <0.8Vdc Input is via CMOS Schmitt trigger buffer.
<a href="#">ADDR</a> (Address Select)	Input	An analogue input that is used to set the address of the internal slave devices (EEPROM and microprocessor) used for digital communications. Connection of a suitable resistor to +VSB_Return, in conjunction with an internal resistor divider chain, will <a href="#">configure the required address</a> .	DC voltage between the limits of 0 and +3.3Vdc.
<a href="#">SCL</a> (Serial Clock)	Both	A serial clock line compatible with PMBus™ Power Systems Management Protocol Part 1 – General Requirements Rev 1.2. No additional internal capacitance is added that would affect the speed of the bus. The signal is provided with a series isolator device to disconnect the internal power supply bus in the event that the power module is unpowered,	V <sub>IL</sub> is 0.8V maximum V <sub>OL</sub> is 0.4V maximum when sinking 3mA V <sub>IH</sub> is 2.1V minimum
<a href="#">SDA</a> (Serial Data)	Both	A serial data line compatible with PMBus™ Power Systems Management Protocol Part 1 – General Requirements Rev 1.2. The signal is provided with a series isolator device to disconnect the internal power supply bus in the event that the power module is unpowered,	V <sub>IL</sub> is 0.8V maximum V <sub>OL</sub> is 0.4V maximum when sinking 3mA V <sub>IH</sub> is 2.1V minimum
<a href="#">V1_SENSE</a> V1SENSE_RTN	Input	Remote sense connections intended to be connected at and sense the voltage at the point of load. The voltage sense will interact with the internal module regulation loop to compensate for voltage drops due to connection resistance between the output connector and the load. If remote sense compensation is not required then the voltage can be configured for local sense by: 1. V1_SENSE directly connected to power blades 6 to 10 (inclusive) 2. V1_SENSE_RTN directly connected to power blades 1 to 5 (inclusive)	Compensation for up to 0.12Vdc total connection drop (output and return connections).
<a href="#">ISHARE</a> See also <a href="#">Current_Share_Notes</a>	Bi-Directional Analogue Bus	The current sharing signal is connected between sharing units (forming an ISHARE bus). It is an input and/or an output (bi-directional analogue bus) as the voltage on the line controls the current share between sharing units. A power supply will respond to a change in this voltage but a power supply can also change (drive) the voltage depending on the load drawn from it. On a single unit the voltage on the pin (and the common ISHARE signal bus would read approximately 8VDC at 100% load (module capability). For two identical units sharing the same 100% load this would read approximately 4VDC for perfect current sharing (i.e. 50% module load capability per unit).	Analogue voltage: Approximately +8V maximum; 10K to +12V_RTN

### TIMING SPECIFICATIONS

#### Turn-On Delay & Output Rise Time:

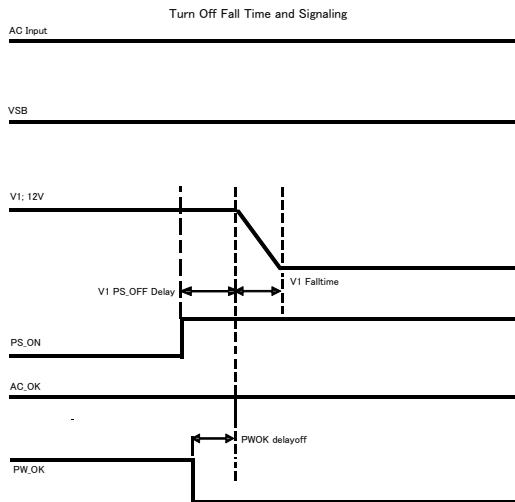


1. The turn-on delay after application of AC input within the operating range shall as defined in the following tables.
2. The output rise times shall be measured from 10% of the nominal output to the lower limit of the regulation band as defined in the following tables.

Time	Min	Max
Vsb Rise time	100ms	200ms
V1 Rise time	5ms	20ms
Vsb Power-on-delay		2700ms
V1 Power-on-delay		3000ms
V1 PS_ON delay	50ms	150ms
V1 PWOK delay	100ms	300ms
ACOK detect	300ms	2000ms

### TIMING SPECIFICATIONS

#### Turn-Off (Shutdown by PS\_ON)

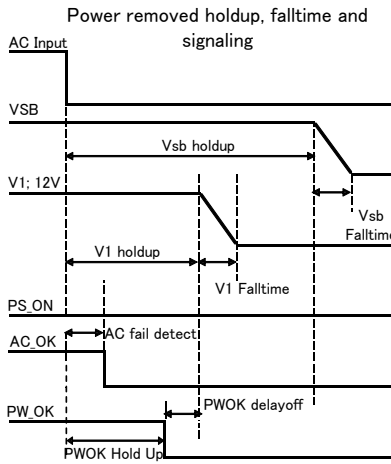


Turn-Off Timing	Min	Max	Notes
V1 Fall time	-	-	Must be monotonic
V1 PS_OFF delay	0ms	5ms	
PW_OK delay off	0.2ms		

1. Note this characteristic is applicable for the main 12Vdc output shutdown from PS\_ON pulled high.

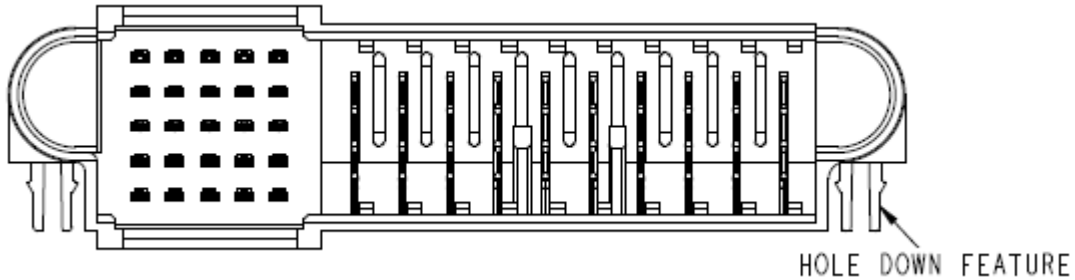
**TIMING SPECIFICATIONS**

**Power Removal Holdup**



Power Removal Timing	Min	Max	Notes
Vsb holdup	40ms	-	
V1 holdup (Effective Total)	10ms	-	800W (100% Load)
	20ms	-	400W
AC fail detect	4ms	8ms	
PWOK delay off	0.2ms	-	100% Load
PWOK Hold Up	9.0ms	-	100% Load

**OUTPUT CONNECTOR & SIGNAL INTERFACE; FCI PN 10122460-005LF**



PART NUMBER	ROWS	SIGNALS					POWERS												
		1	2	3	4	5	1	2	3	4	5	6	7	8	9	10			
10122460-005LF 25S + 10P	E																		
	D																		
	C		~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~
	B																		
	A	H																	H

NB: With respect to signals "3" in Columns 5, refers to the shortest level signal pin; the "shortest" pins are the "last to make, first to break" in the mating sequence.

### Murata Power Solutions

#### OUTPUT CONNECTOR PIN ASSIGNMENTS - D1U54P-M-800-12-HBxBC

(Power Supply)FCI PN 10122460-005LF

Pin	Signal Name	Comments
6, 7, 8, 9, 10	V1 (+12VOUT)	+12V Main Output
1, 2, 3, 4, 5	+12V RTN/PGND	+12V Main Output Return
A1	+VSB	Standby Output
B1	+VSB	Standby Output
C1	+VSB	Standby Output
D1	+VSB	Standby Output
E1	+VSB	Standby Output
A2	+VSB_Return	Standby Output Return
B2	+VSB_Return	Standby Output Return
C2	Unused	No End User Connection
D2	Unused	No End User Connection
E2	Unused	No End User Connection
A3	ADDR	<a href="#">I<sup>2</sup>C Address</a> Protocol Selection; (Select address by appropriate pull down resistor – See <a href="#">table below</a> )
B3	Unused	No End User Connection
C3	SDA	<a href="#">I<sup>2</sup>C Serial Data Line</a>
D3	V1_SENSE_R	<a href="#">-VE Remote Sense Return</a>
E3	V1_SENSE	<a href="#">+VE Remote Sense</a>
A4	SCL	<a href="#">I<sup>2</sup>C Serial Clock Line</a>
B4	PS_ON_L	<a href="#">Remote On/Off (Enable/Disable)</a>
C4	SMB_ALERT	<a href="#">Alert signal to host system</a>
D4	Unused	No End User Connection
E4	input_OK	<a href="#">Input Source Present &amp; "OK"</a>
A5	PS_KILL	<a href="#">Power Supply "kill"; short pin</a>
B5	ISHARE	<a href="#">Active Current Share Bus</a>
C5	PW_OK	<a href="#">Power "OK"; short pin</a>
D5	Unused	No End User Connection
E5	PRESENT_L	<a href="#">Power Module Present; short pin</a>

#### MATING CONNECTOR

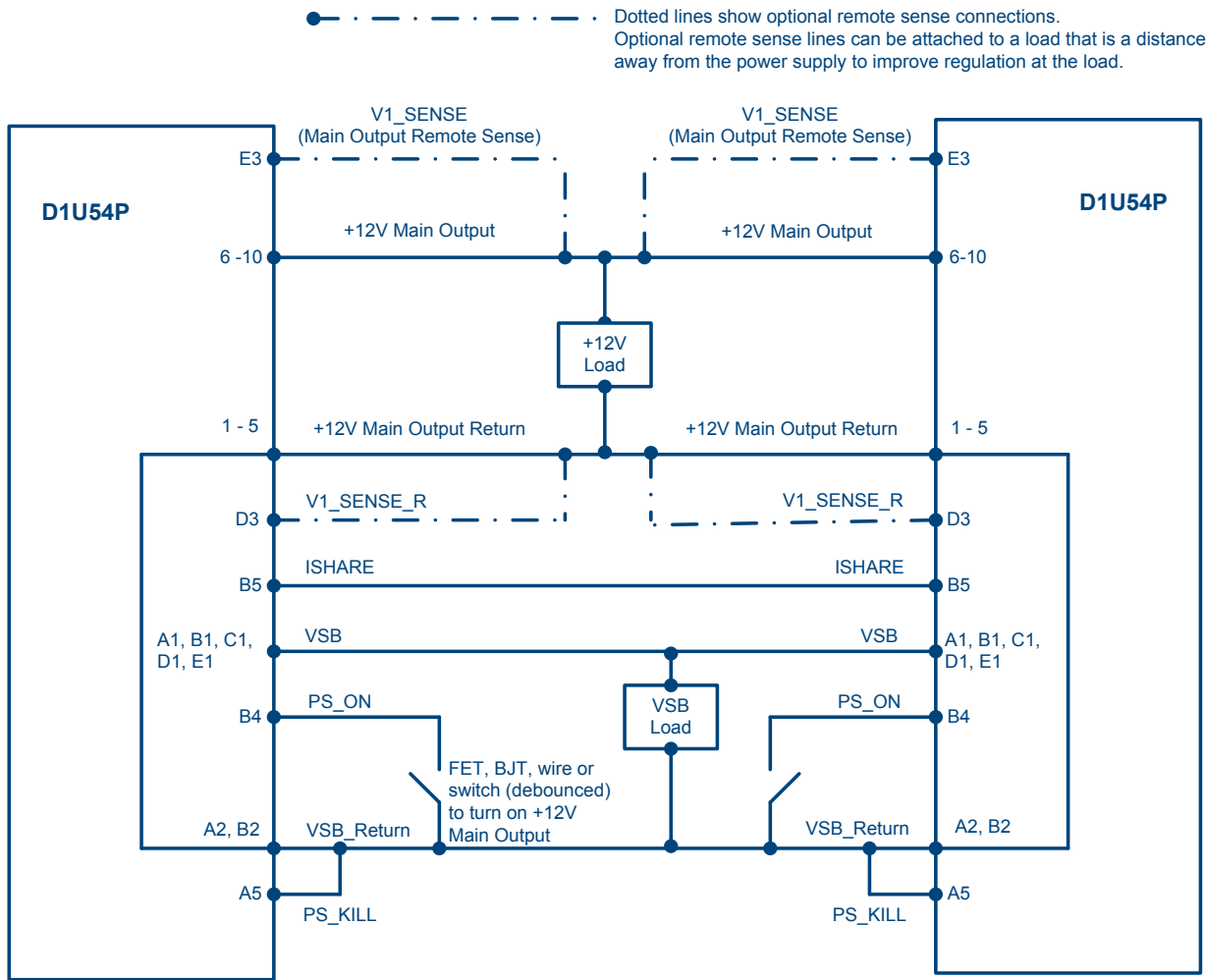
Part Number	Description
TE Connectivity 2-1926739-5	Right Angle
FCI 10108888-R10253SLF	Right Angle

#### ADDR ADDRESS SELECTION

ADDR pin (A3) resistor to GND (K-ohm)*	Power Supply Main Controller (Serial Communications Slave Address)	Power Supply External EEPROM (Serial Communications Slave Address)
0.82	0xB0	0xA0
2.7	0xB2	0xA2
5.6	0xB4	0xA4
8.2	0xB6	0xA6
15	0xB8	0xA8
27	0xBA	0xAA
56	0xBC	0xAC
180	0xBE	0xAE

\* The resistor shall be +/-5% tolerance; refer to [application note PMBus™](#) for additional details  
 Link Back to [signal definition](#)

### WIRING DIAGRAM FOR OUTPUT

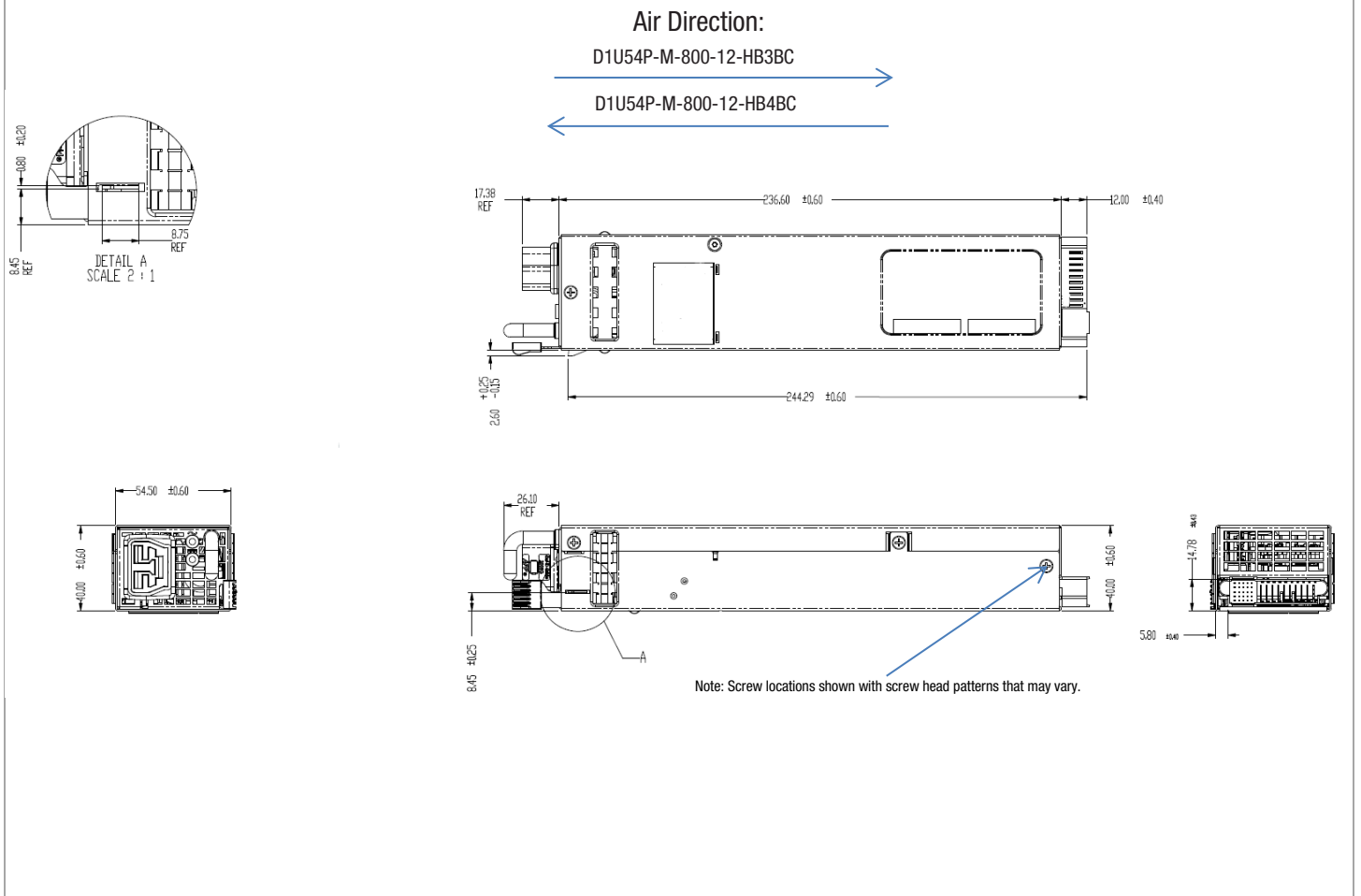


### CURRENT SHARE NOTES

1. Main Output: Current sharing is achieved using the active **ISHARE** signal bus method
2. Current sharing can be achieved with or without the remote (**V\_SENSE**) connected to the common load.
3. +VSB Outputs can be tied together for redundancy but total combined output power must not exceed the rated standby power. The +VSB output has an internal ORing MOSFET for additional redundancy/internal short protection.
4. The current sharing pin B5 is connected between sharing units (forming an ISHARE bus). It is an input and/or an output (bi-directional analogue bus) as the voltage on the line controls the current share between sharing units. A power supply will respond to a change in this voltage but a power supply can also change the voltage depending on the load drawn from it. On a single unit the voltage on the pin (and the common ISHARE bus would read approximately 8VDC at 100% load. For two units sharing the same load this would read approximately 4VDC for perfect current sharing (i.e. 50% load per unit).
5. The load for both the main 12V and the VSB rails at initial startup shall not be allowed to exceed the capability of a single unit. The load can be increased after a delay of 3sec (minimum), to allow all sharing units to achieve steady state regulation.



**MECHANICAL DIMENSIONS**



**Additional Notes**

1. The above drawing is a graphical representation of actual power supply; not all non-critical and fine details may be shown
2. AC input connector: Anderson SAF-D-GRID<sup>®</sup>; Type 2006G3; <http://www.andersonpower.com/us/en/products/saf-d-grid/index.aspx>
3. Mating connector for Anderson SAF-D-GRID<sup>®</sup>; Multiple Types Available; for Details visit: <http://www.andersonpower.com/global-assets/downloads/pdf/ds-sdg.pdf>
4. Dimensions: 2.15" x 9.32" x 1.57" [54.5mm x 236.6mm x 40.0mm]
5. Reference File: I:\Eng\_wip\UserPDDwg\2001\ D1U54P-M-800

**OPTIONAL ACCESSORIES**

Description	Part Number	MPS Internal Part Number
12V D1U54P Output Connector Card	D1U54P-12-CONC	8407001-1

**APPLICATION NOTES**

Document Number	Description	Link
ACAN-64	D1U54P Output Connector Card	<a href="http://power.murata.com/datasheet?/data/apnotes/acan-64.pdf">http://power.murata.com/datasheet?/data/apnotes/acan-64.pdf</a>
ACAN-86	D1U54P-x Communication Protocol	<a href="http://power.murata.com/datasheet?/data/apnotes/acan-86.pdf">http://power.murata.com/datasheet?/data/apnotes/acan-86.pdf</a>

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 ISO 9001 and 14001 REGISTERED



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