

1. General description

Planar passivated high commutation three quadrant triac in a SOT186A (TO-220F) "full pack" plastic package intended for use in circuits where high static and dynamic dV/dt and high dI/dt can occur. This "series BT" triac will commute the full RMS current at the maximum rated junction temperature ($T_{j(max)} = 150\text{ °C}$) without the aid of a snubber. It is used in applications where "high junction operating temperature capability" is required.

2. Features and benefits

- 3Q technology for improved noise immunity
- High commutation capability with maximum false trigger immunity
- High immunity to false turn-on by dV/dt
- High junction operating temperature capability
- High voltage capability
- Isolated mounting base package
- Least sensitive gate for highest noise immunity
- Planar passivated for voltage ruggedness and reliability
- Triggering in three quadrants only

3. Applications

- Applications subject to high temperature
- Heating controls
- High power motor control
- High power switching

4. Quick reference data

Table 1. Quick reference data

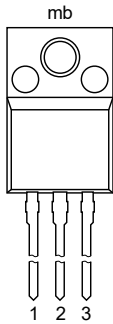
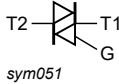
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_h \leq 63\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	-	25	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	-	250	A
		full sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 16.7\text{ ms}$	-	-	275	A
T_j	junction temperature		-	-	150	°C

Static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I _{GT}	gate trigger current	V _D = 12 V; I _T = 0.1 A; T2+ G+; T _j = 25 °C; Fig. 7	-	-	50	mA
		V _D = 12 V; I _T = 0.1 A; T2+ G-; T _j = 25 °C; Fig. 7	-	-	50	mA
		V _D = 12 V; I _T = 0.1 A; T2- G-; T _j = 25 °C; Fig. 7	-	-	50	mA
I _H	holding current	V _D = 12 V; T _j = 25 °C; Fig. 9	-	-	75	mA
V _T	on-state voltage	I _T = 35 A; T _j = 25 °C; Fig. 10	-	1.2	1.5	V
Dynamic characteristics						
dV _D /dt	rate of rise of off-state voltage	V _{DM} = 536 V; T _j = 150 °C; (V _{DM} = 67% of V _{DRM}); exponential waveform; gate open circuit	2000	-	-	V/μs
di _{com} /dt	rate of change of commutating current	V _D = 400 V; T _j = 150 °C; I _{T(RMS)} = 25 A; dV _{com} /dt = 20 V/μs; (snubberless condition); gate open circuit	15	-	-	A/ms

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1	 <p>TO-220F (SOT186A)</p>	 <p>sym051</p>
2	T2	main terminal 2		
3	G	gate		
mb	n.c.	mounting base; isolated		

6. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BTA425X-800BT	TO-220F	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack"	SOT186A

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_h \leq 63\text{ }^\circ\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	25	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	250	A
		full sine wave; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$; $t_p = 16.7\text{ ms}$	-	275	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; SIN	-	312.5	A^2s
di_T/dt	rate of rise of on-state current	$I_G = 0.2\text{ A}$	-	100	$\text{A}/\mu\text{s}$
I_{GM}	peak gate current		-	2	A
P_{GM}	peak gate power		-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.5	W
T_{stg}	storage temperature		-40	150	$^\circ\text{C}$
T_j	junction temperature		-	150	$^\circ\text{C}$

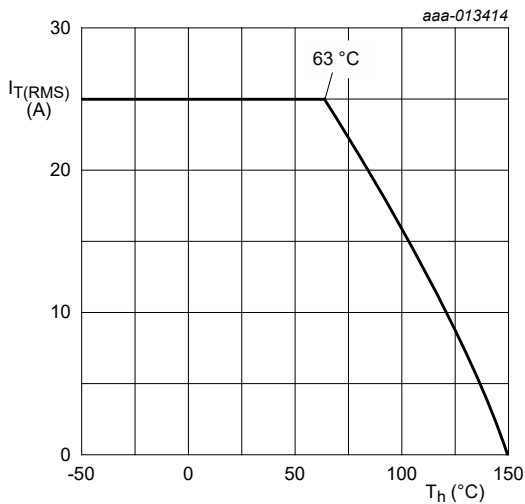


Fig. 1. RMS on-state current as a function of heatsink temperature; maximum values

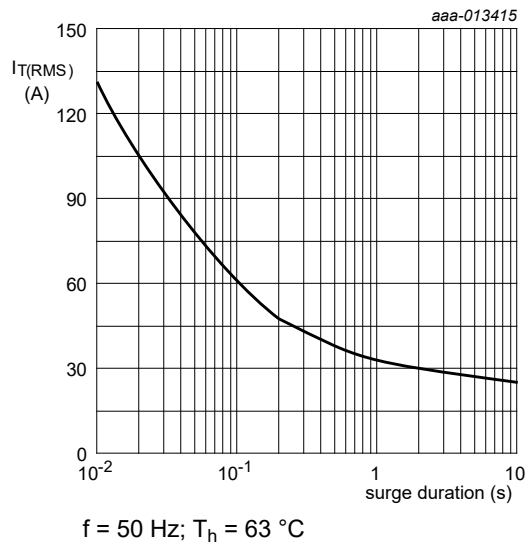


Fig. 2. RMS on-state current as a function of surge duration; maximum values

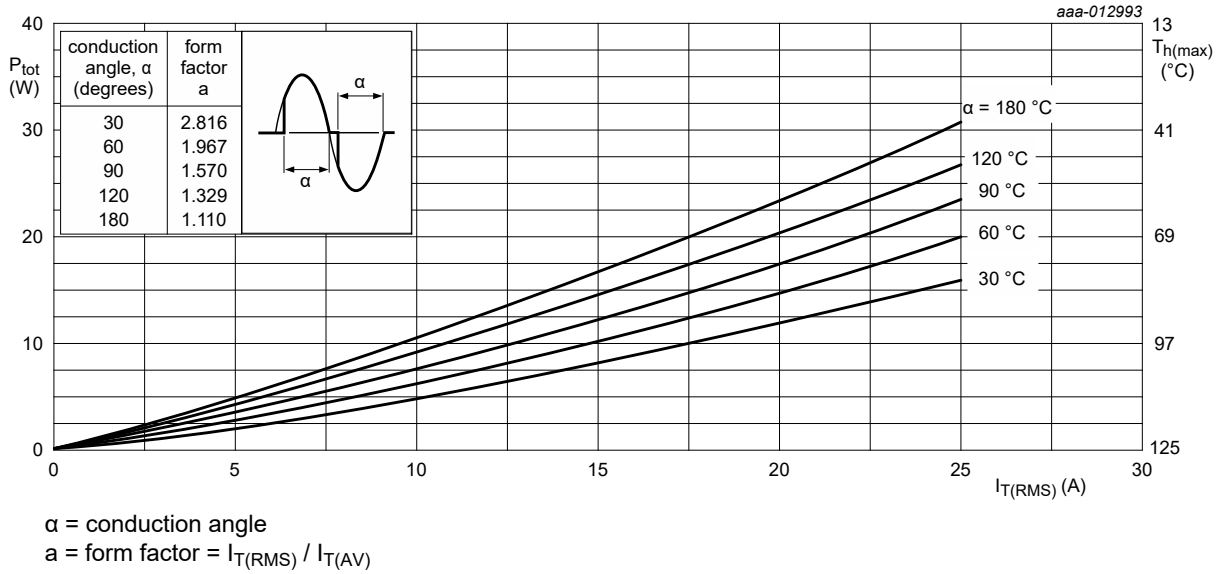


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

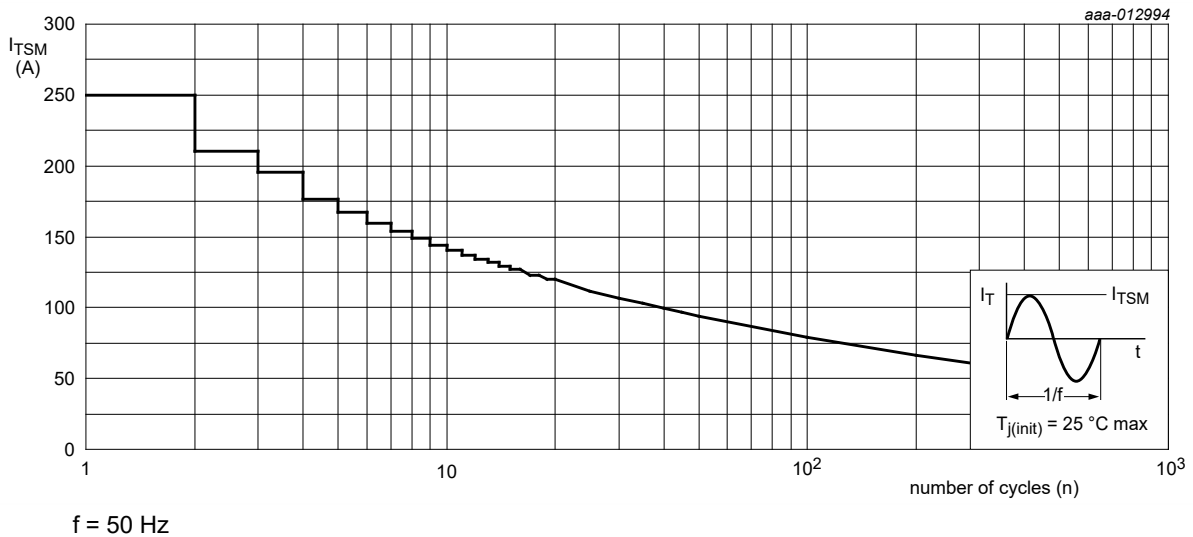
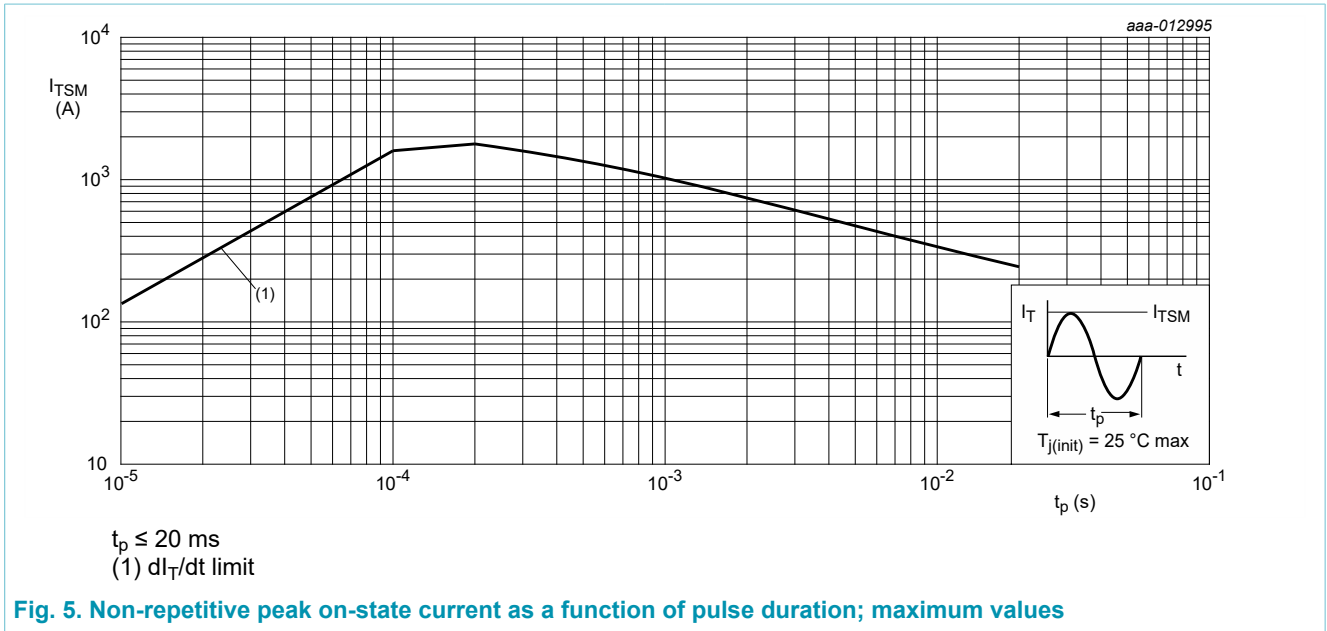


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-h)}$	thermal resistance from junction to heatsink	full cycle; with heatsink compound; Fig. 6	-	-	2.8	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	in free air	-	55	-	K/W

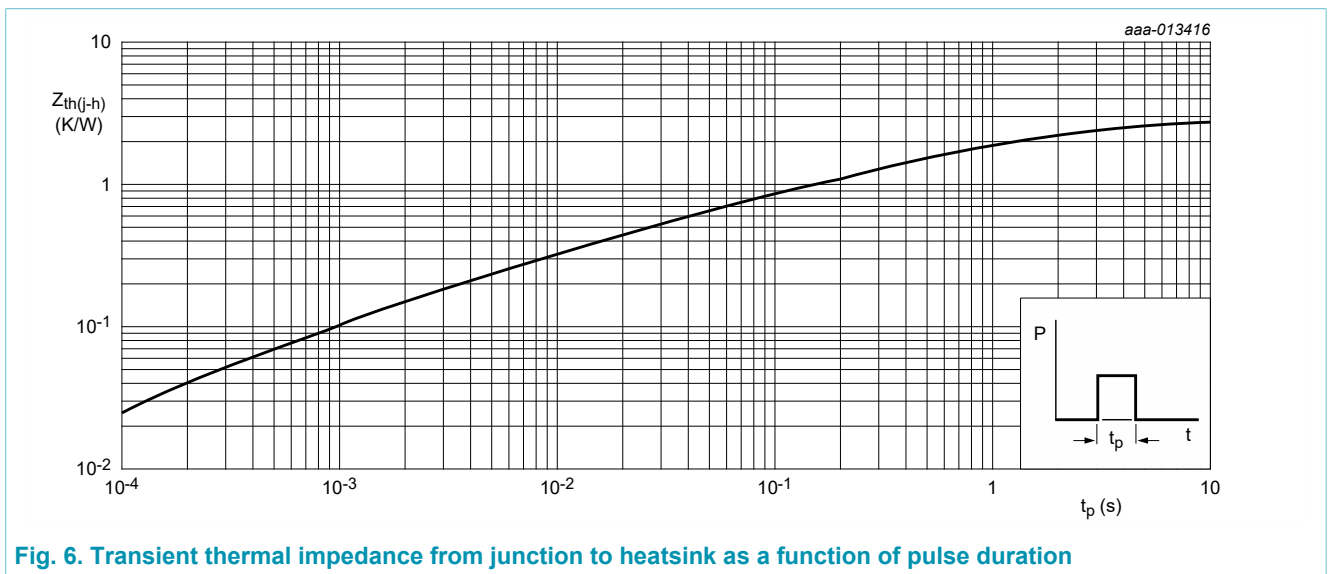


Fig. 6. Transient thermal impedance from junction to heatsink as a function of pulse duration

9. Isolation characteristics

Table 6. Isolation characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{isol(RMS)}$	RMS isolation voltage	from all terminals to external heatsink; sinusoidal waveform; clean and dust free; $50\text{ Hz} \leq f \leq 60\text{ Hz}$; $RH \leq 65\%$; $T_h = 25\text{ }^\circ\text{C}$	-	-	2500	V
C_{isol}	isolation capacitance	from main terminal 2 to external heatsink; $f = 1\text{ MHz}$; $T_h = 25\text{ }^\circ\text{C}$	-	10	-	pF

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T2+ G+;$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 7	-	-	50	mA
		$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T2+ G-;$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 7	-	-	50	mA
		$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T2- G-;$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 7	-	-	50	mA
I_L	latching current	$V_D = 12\text{ V}; I_G = 0.1\text{ A}; T2+ G+;$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 8	-	-	80	mA
		$V_D = 12\text{ V}; I_G = 0.1\text{ A}; T2+ G-;$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 8	-	-	100	mA
		$V_D = 12\text{ V}; I_G = 0.1\text{ A}; T2- G-;$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 8	-	-	80	mA
I_H	holding current	$V_D = 12\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 9	-	-	75	mA
V_T	on-state voltage	$I_T = 35\text{ A}; T_j = 25\text{ }^\circ\text{C};$ Fig. 10	-	1.2	1.5	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_j = 25\text{ }^\circ\text{C};$ Fig. 11	-	0.9	1.3	V
		$V_D = 400\text{ V}; I_T = 0.1\text{ A}; T_j = 150\text{ }^\circ\text{C};$ Fig. 11	0.2	0.45	-	V
I_D	off-state current	$V_D = 800\text{ V}; T_j = 150\text{ }^\circ\text{C}$	-	0.4	2	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}; T_j = 150\text{ }^\circ\text{C}; (V_{DM} = 67\%$ of $V_{DRM});$ exponential waveform; gate open circuit	2000	-	-	V/ μ s
dI_{com}/dt	rate of change of commutating current	$V_D = 400\text{ V}; T_j = 150\text{ }^\circ\text{C}; I_{T(RMS)} = 25\text{ A};$ $dV_{com}/dt = 20\text{ V}/\mu\text{s};$ (snubberless condition); gate open circuit	15	-	-	A/ms

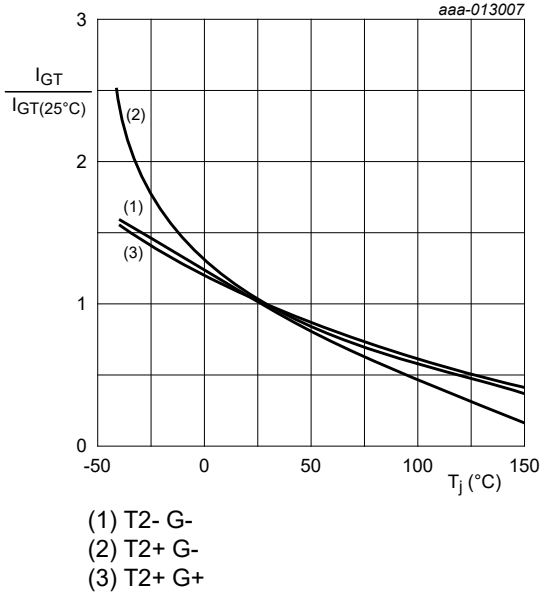


Fig. 7. Normalized gate trigger current as a function of junction temperature

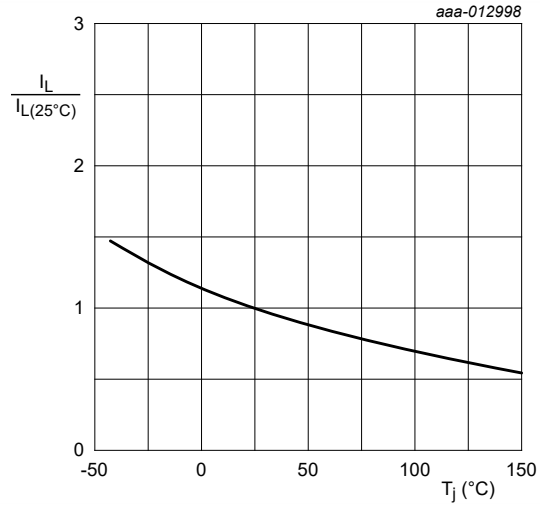


Fig. 8. Normalized latching current as a function of junction temperature

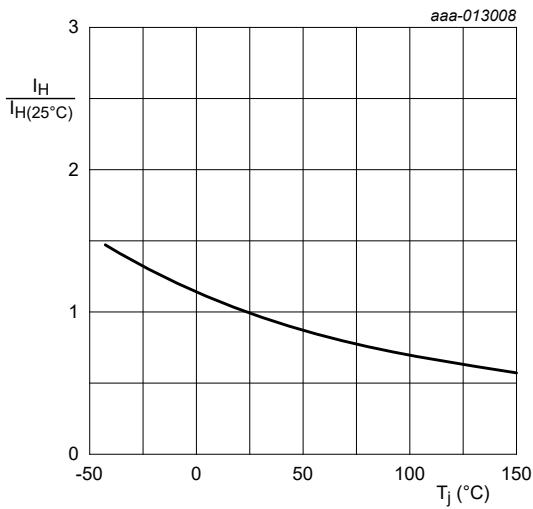
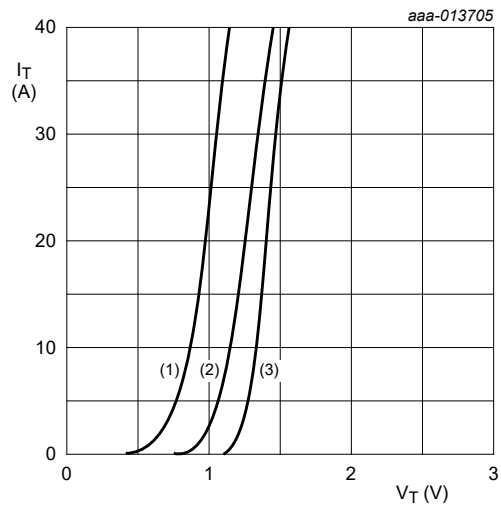


Fig. 9. Normalized holding current as a function of junction temperature



$V_o = 1.085 \text{ V}; R_s = 0.011 \ \Omega$
 (1) $T_j = 150 \text{ }^\circ\text{C}$; typical values
 (2) $T_j = 150 \text{ }^\circ\text{C}$; maximum values
 (3) $T_j = 25 \text{ }^\circ\text{C}$; maximum values

Fig. 10. On-state current as a function of on-state voltage

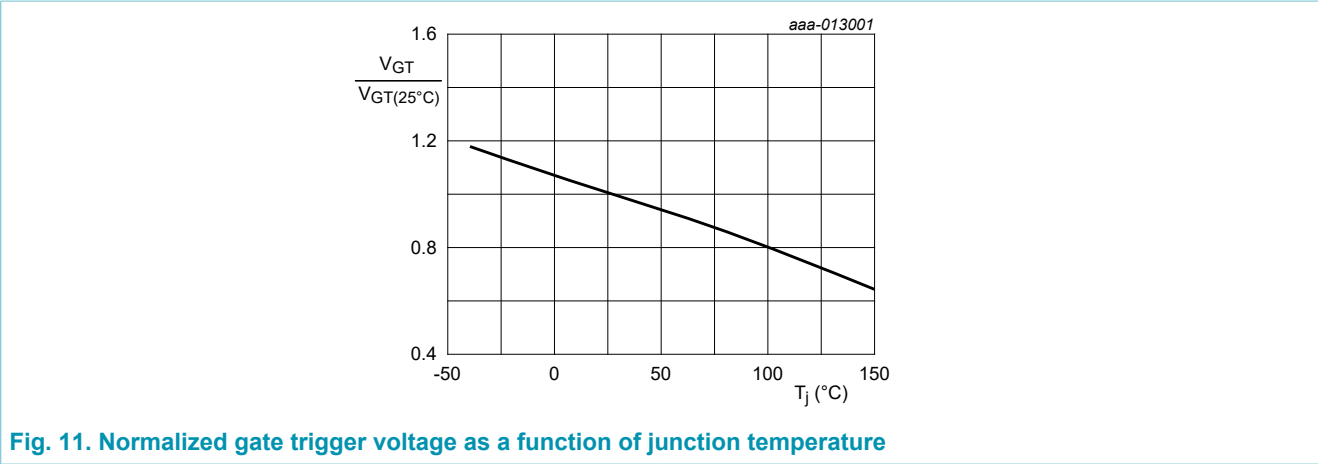


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

11. Package outline



Fig. 12. Package outline TO-220F (SOT186A)

12. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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- [2] The term 'short data sheet' is explained in section "Definitions".
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13. Contents

1. General description.....	1
2. Features and benefits.....	1
3. Applications.....	1
4. Quick reference data.....	1
5. Pinning information.....	2
6. Ordering information.....	2
7. Limiting values.....	3
8. Thermal characteristics.....	6
9. Isolation characteristics.....	6
10. Characteristics.....	7
11. Package outline.....	10
12. Legal information.....	11

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