

PNP Silicon Epitaxial Transistors

BCP53 Series

This PNP Silicon Epitaxial transistor is designed for use in audio amplifier applications. The device is housed in the SOT-223 package which is designed for medium power surface mount applications.

- High Current
- NPN Complement is BCP56
- The SOT-223 Package can be soldered using wave or reflow. The formed leads absorb thermal stress during soldering, eliminating the possibility of damage to the die
- Device Marking:
BCP53T1G = AH
BCP53-10T1G = AH-10
BCP53-16T1G = AH-16
- S and NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Ambient (Surface Mounted)	$R_{\theta JA}$	83.3	$^{\circ}C/W$
Lead Temperature for Soldering, 0.0625" from case	T_L	260	$^{\circ}C$
Time in Solder Bath		10	s

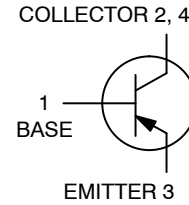
MAXIMUM RATINGS ($T_C = 25^{\circ}C$ unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	-80	V
Collector-Base Voltage	V_{CBO}	-100	V
Emitter-Base Voltage	V_{EBO}	-5.0	V
Collector Current	I_C	1.5	A
Collector Current - Peak, single pulse, $t_p \leq 1$ ms	I_{CM}	3.0	A
Base Current - Continuous	I_B	-0.3	A
Base Collector Current - Peak, single pulse, $t_p \leq 1$ ms	I_{BM}	-0.4	A
Total Power Dissipation @ $T_A = 25^{\circ}C$ (Note 1) Derate above $25^{\circ}C$	P_D	1.5 12	W mW/ $^{\circ}C$
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to +150	$^{\circ}C$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Device mounted on a glass epoxy printed circuit board 1.575 in. x 1.575 in. x 0.059 in.; mounting pad for the collector lead min. 0.93 sq. in.

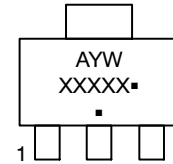
MEDIUM POWER HIGH CURRENT SURFACE MOUNT PNP TRANSISTORS



MARKING DIAGRAM



SOT-223
CASE 318E
STYLE 1



- A = Assembly Location
- Y = Year
- W = Work Week
- XXXXX = Specific Device Code
- = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping [†]
BCP53T1G	SOT-223 (Pb-Free)	1000/Tape & Reel
SBCP53-10T1G	SOT-223 (Pb-Free)	1000/Tape & Reel
BCP53-10T1G	SOT-223 (Pb-Free)	1000/Tape & Reel
SBCP53-10T1G	SOT-223 (Pb-Free)	1000/Tape & Reel
BCP53-16T1G	SOT-223 (Pb-Free)	1000/Tape & Reel
SBCP53-16T1G	SOT-223 (Pb-Free)	1000/Tape & Reel
BCP53-16T3G	SOT-223 (Pb-Free)	4000/Tape & Reel
NSVBCP53-16T3G	SOT-223 (Pb-Free)	4000/Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

BCP53 Series

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Collector-Base Breakdown Voltage ($I_C = -100\ \mu\text{Adc}$, $I_E = 0$)	$V_{(BR)CBO}$	-100	-	-	Vdc
Collector-Emitter Breakdown Voltage ($I_C = -1.0\ \text{mAdc}$, $I_B = 0$)	$V_{(BR)CEO}$	-80	-	-	Vdc
Collector-Emitter Breakdown Voltage ($I_C = -100\ \mu\text{Adc}$, $R_{BE} = 1.0\ \text{k}\Omega$)	$V_{(BR)CER}$	-100	-	-	Vdc
Emitter-Base Breakdown Voltage ($I_E = -10\ \mu\text{Adc}$, $I_C = 0$)	$V_{(BR)EBO}$	-5.0	-	-	Vdc
Collector-Base Cutoff Current ($V_{CB} = -30\ \text{Vdc}$, $I_E = 0$)	I_{CBO}	-	-	-100	nAdc
Emitter-Base Cutoff Current ($V_{EB} = -5.0\ \text{Vdc}$, $I_C = 0$)	I_{EBO}	-	-	-100	nAdc

ON CHARACTERISTICS

DC Current Gain ($I_C = -5.0\ \text{mAdc}$, $V_{CE} = -2.0\ \text{Vdc}$) All Part Types	h_{FE}	25	-	-	-
($I_C = -150\ \text{mAdc}$, $V_{CE} = -2.0\ \text{Vdc}$) BCP53, SBCP53		40	-	250	
BCP53-10, SBCP53-10		63	-	160	
BCP53-16, SBCP53-16, NSVBCP53-16		100	-	250	
($I_C = -500\ \text{mAdc}$, $V_{CE} = -2.0\ \text{Vdc}$) All Part Types		25	-	-	
Collector-Emitter Saturation Voltage ($I_C = -500\ \text{mAdc}$, $I_B = -50\ \text{mAdc}$)	$V_{CE(sat)}$	-	-	-0.5	Vdc
Base-Emitter On Voltage ($I_C = -500\ \text{mAdc}$, $V_{CE} = -2.0\ \text{Vdc}$)	$V_{BE(on)}$	-	-	-1.0	Vdc

DYNAMIC CHARACTERISTICS

Current-Gain - Bandwidth Product ($I_C = -10\ \text{mAdc}$, $V_{CE} = -5.0\ \text{Vdc}$, $f = 35\ \text{MHz}$)	f_T	-	50	-	MHz
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Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

BCP53 Series

TYPICAL CHARACTERISTICS

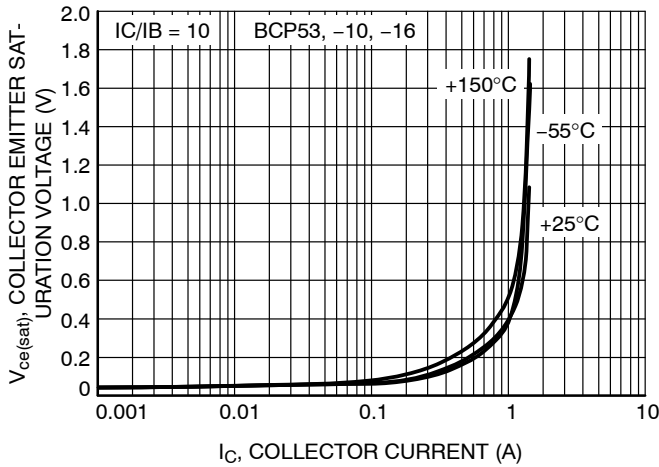


Figure 1. Collector Emitter Saturation Voltage vs. Collector Current

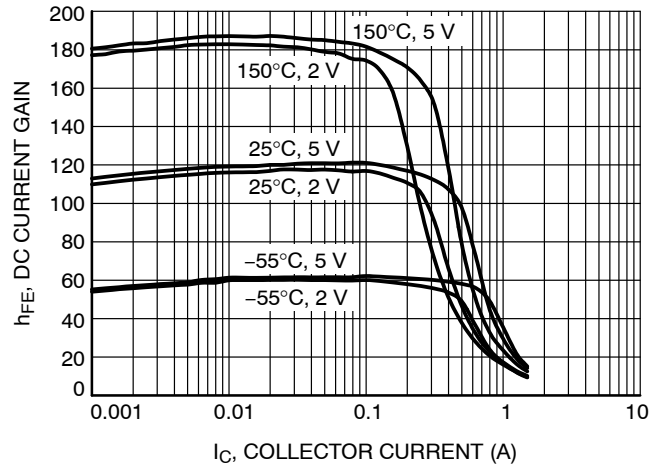


Figure 2. DC Current Gain vs. Collector Current (BCP53)

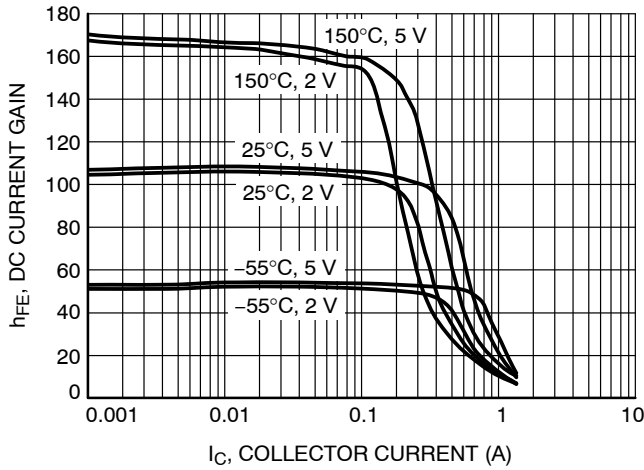


Figure 3. DC Current Gain vs. Collector Current (BCP53-10)

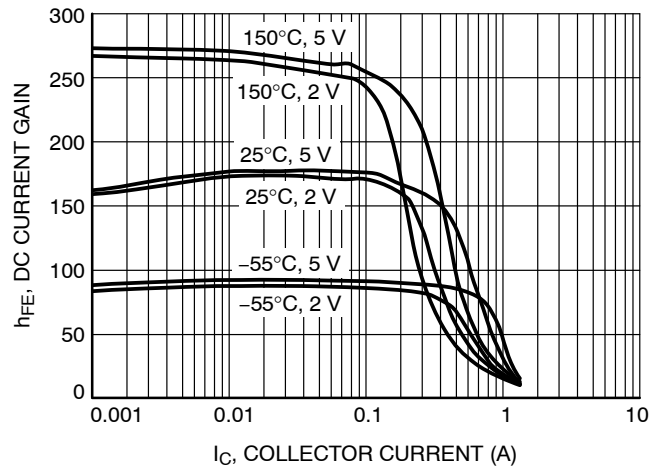


Figure 4. DC Current Gain vs. Collector Current (BCP53-16)

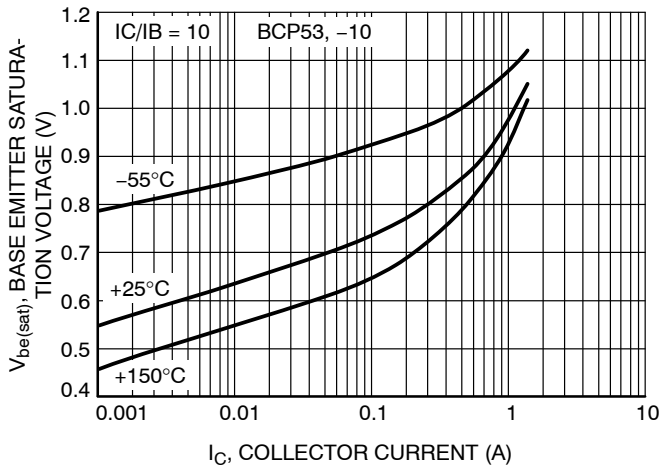


Figure 5. BCP53, -10 Base Emitter Saturation Voltage vs. Collector Current

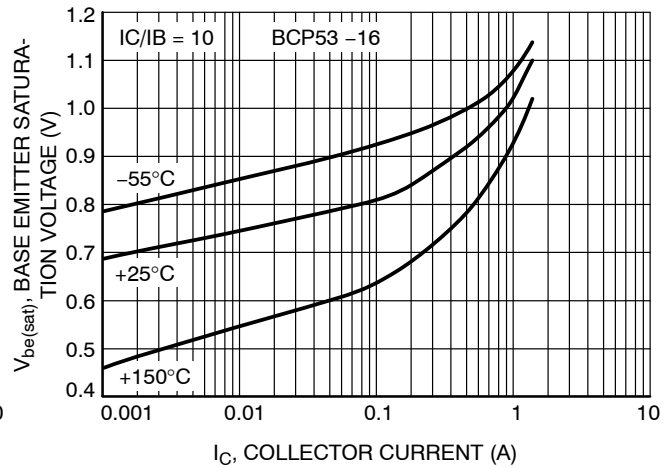


Figure 6. BCP53-16 Base Emitter Saturation Voltage vs. Collector Current

BCP53 Series

TYPICAL CHARACTERISTICS

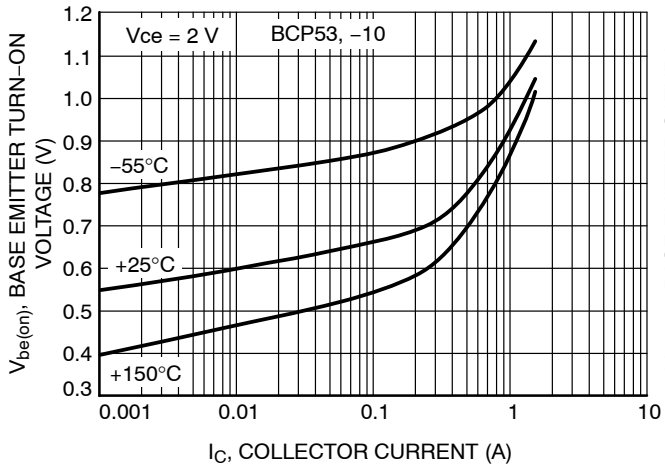


Figure 7. BCP53, -10 Base Emitter Turn-On Voltage vs. Collector Current $V_{BE(on)}$

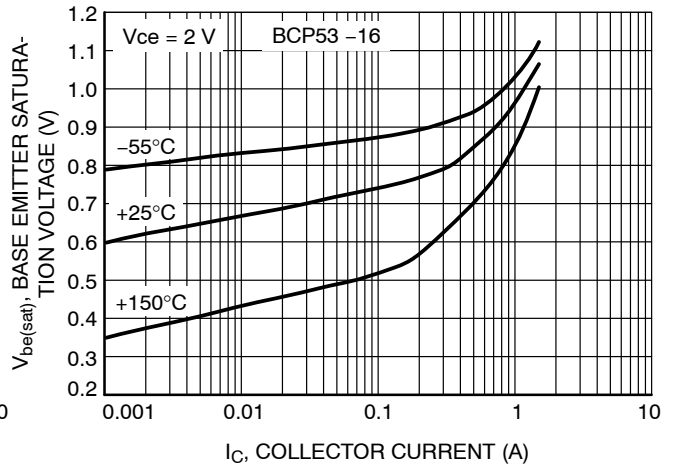


Figure 8. BCP53-16 Base Emitter Turn-On Voltage vs. Collector Current

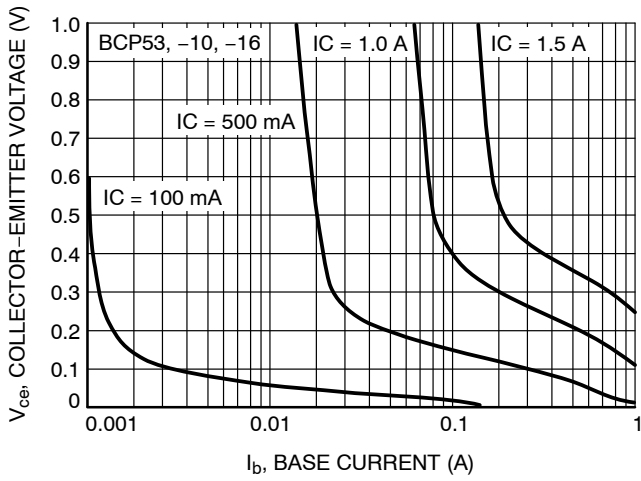


Figure 9. BCP53, -10, -16 Saturation Region

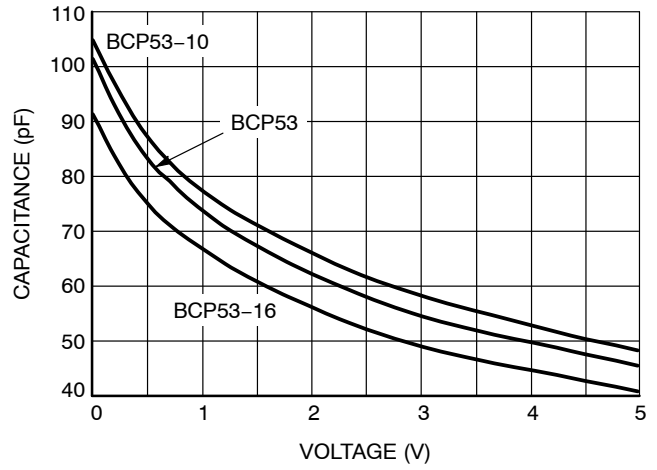


Figure 10. Input Capacitance

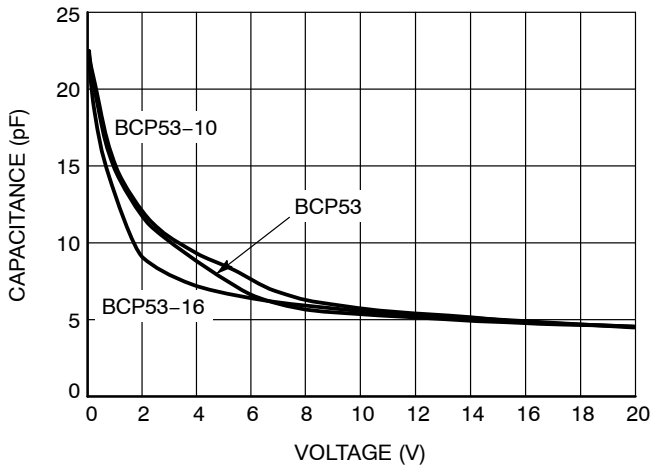


Figure 11. Output Capacitance

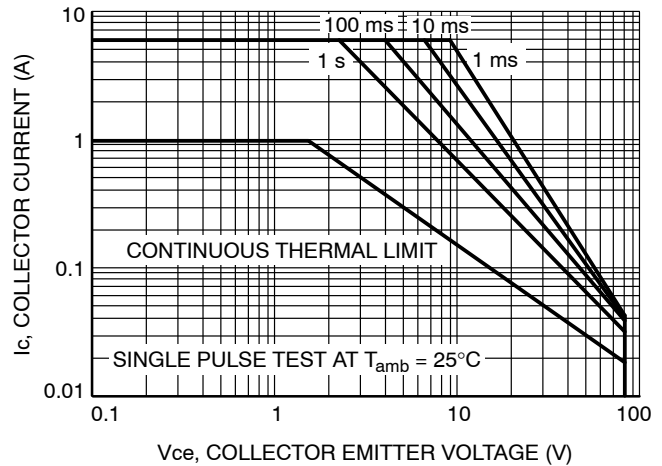


Figure 12. Standard Operating Area

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

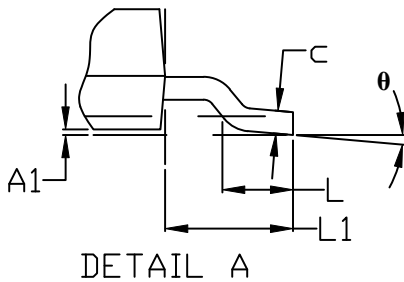
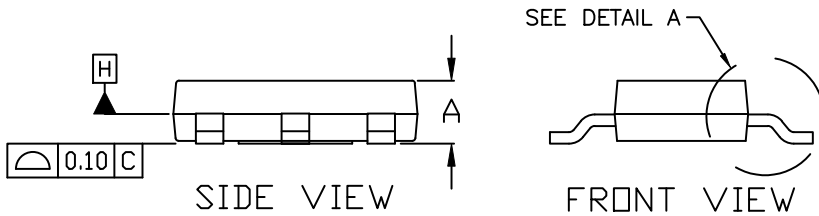
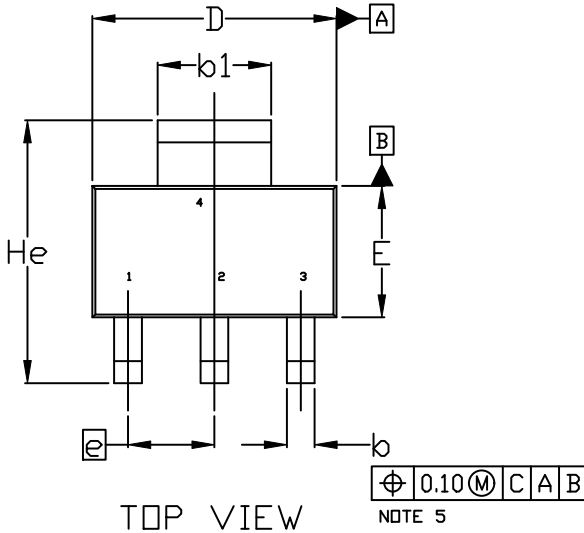
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SCALE 1:1

SOT-223 (TO-261)
CASE 318E-04
ISSUE R

DATE 02 OCT 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

MILLIMETERS			
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°



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SOT-223 (TO-261)
CASE 318E-04
ISSUE R

DATE 02 OCT 2018

- | | | | | |
|--|---|---|---|---|
| STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR | STYLE 2:
PIN 1. ANODE
2. CATHODE
3. NC
4. CATHODE | STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN | STYLE 4:
PIN 1. SOURCE
2. DRAIN
3. GATE
4. DRAIN | STYLE 5:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. GATE |
| STYLE 6:
PIN 1. RETURN
2. INPUT
3. OUTPUT
4. INPUT | STYLE 7:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2
4. CATHODE | STYLE 8:
CANCELLED | STYLE 9:
PIN 1. INPUT
2. GROUND
3. LOGIC
4. GROUND | STYLE 10:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE |
| STYLE 11:
PIN 1. MT 1
2. MT 2
3. GATE
4. MT 2 | STYLE 12:
PIN 1. INPUT
2. OUTPUT
3. NC
4. OUTPUT | STYLE 13:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR | | |

**GENERIC
 MARKING DIAGRAM***



- A = Assembly Location
- Y = Year
- W = Work Week
- XXXXX = Specific Device Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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