# AP1018

## 18V Dual H-Bridge Motor Driver IC

## 1. General Description

The AP1018 is a Dual H-Bridge small motor driver corresponding to the motor drive voltage 18V.
Since the AP1018 has two output channels, it is capable of driving two DC motors or one stepper motor.
It can be used up to peak current of 4.5A, so it can be used safely even with a motor that requires a large current at the start of driving.
Also it has under voltage detection and thermal shut down circuits as a protection circuit.
The AP1018 is housed in a high heat dissipation 24-pin QFN package (4mm x 4mm) with an exposed pad. It is a motor driver IC that realizes reduction of mounting area.

## 2. Features

- Control Supply Voltage 2.7 to 5.5V
- Logic Input Power Supply 1.62V to Control Supply Voltage (VC)
- Motor Drive Voltage 2 to 18V
- Maximum Output Current (DC) 1.3A (max)
- Maximum Output Current (Peak) 3.0A (Ta = 25°C, within 10ms in every 200ms)
  4.5A (Ta = 25°C, within 5ms in every 200ms)
- H-Bridge On Resistance RON (TOP+BOT) = 0.36Ω (typ) (Ta = 25°C)
- Power Saving Function VM Power Consumption is less than 2μA (Ta = 25°C)
- Under Voltage Lockout Circuit (UVLO)
- Thermal Shutdown Circuit (TSD)
- Package 24-pin QFN (4.0mm × 4.0mm)

## 3. Table of Contents

## 4. Block Diagram

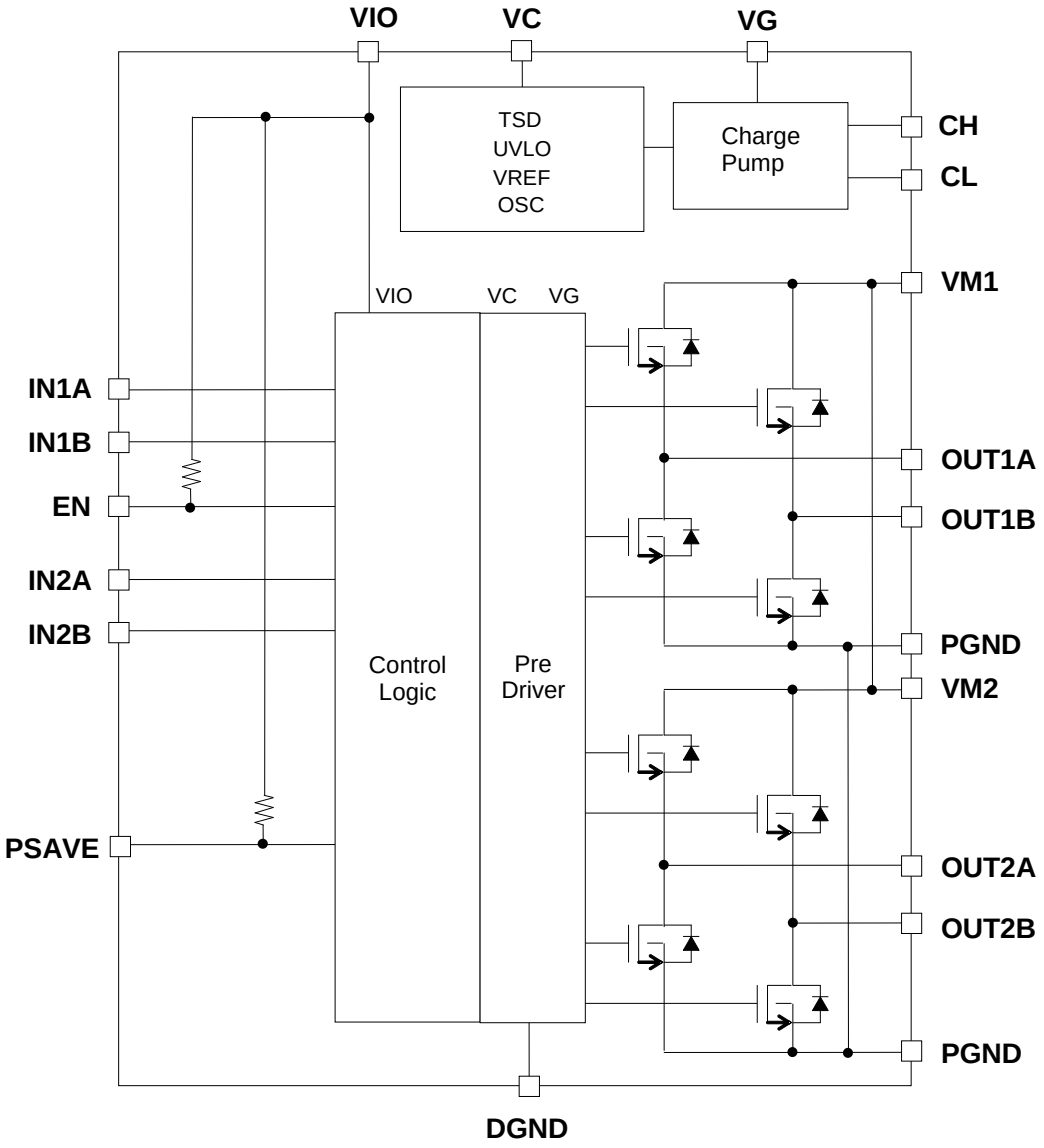
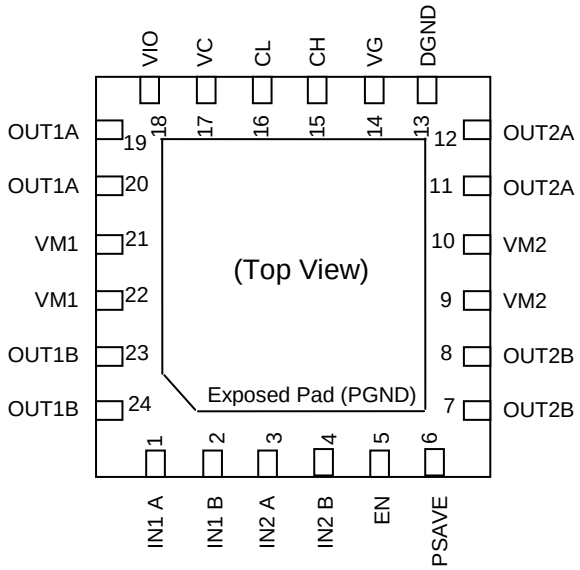



Figure 1. Block Diagram

## 5. Pin Configurations and Functions

### ■ Pin Configurations

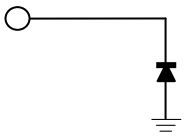
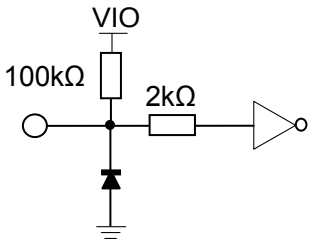
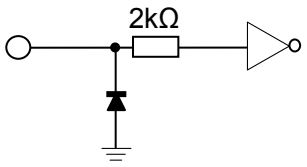
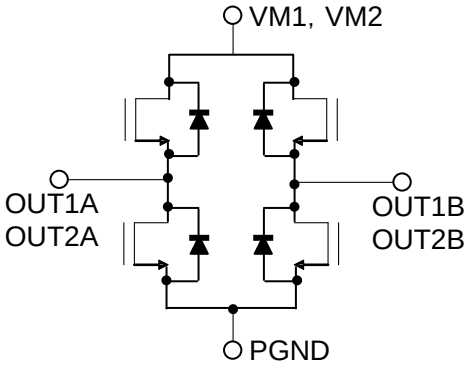
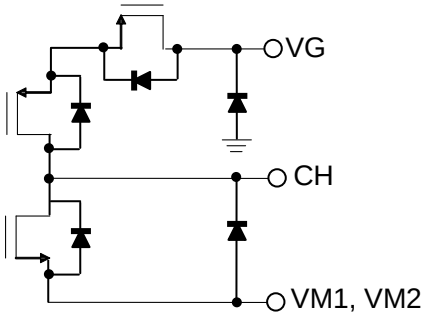
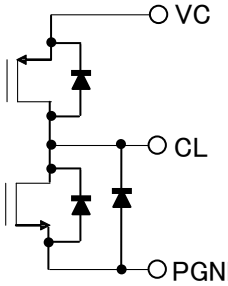
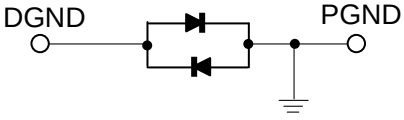



### ■ Functions

| Pin Number | Name | I/O (Note 1) | Function | Note |
|---|---|---|---|---|
| 14 | VG | O | Connection Terminal for Stabilizing Capacitor | |
| 15 | CH | I/O | Connection Terminal for Charge Pump Capacitor | |
| 16 | CL | I/O | Connection Terminal for Charge Pump Capacitor | |
| 21, 22 | VM1 | P | Motor Driver Power Supply 1 | (Note 3) |
| 19, 20 | OUT1A | O | Motor Driver Output Terminal 1A | |
| 23, 24 | OUT1B | O | Motor Driver Output Terminal 1B | |
| Exposed Pad | PGND | P | Ground Terminal | (Note 2) |
| 11, 12 | OUT2A | O | Motor Driver Output Terminal 2A | |
| 7, 8 | OUT2B | O | Motor Driver Output Terminal 2B | |
| 9, 10 | VM2 | P | Motor Driver Power Supply 2 | (Note 3) |
| 4 | IN2B | I | Control Signal Input Terminal 2B | |
| 3 | IN2A | I | Control Signal Input Terminal 2A | |
| 2 | IN1B | I | Control Signal Input Terminal 1B | |
| 1 | IN1A | I | Control Signal Input Terminal 1A | |
| 13 | DGND | P | Ground Terminal | |
| 5 | EN | I | Output Enable Terminal | Built-in 100kΩ pull-up |
| 6 | PSAVE | I | Power Save Terminal | Built-in 100kΩ pull-up |
| 18 | VIO | P | Logic Input Power Supply Terminal | |
| 17 | VC | P | Control System Power Supply Terminal | |

Note 1. I (Input pin), O (Output pin), P (Power pin)
Note 2. The exposed pad should be connected to the DGND pin for heat dissipation.
Note 3. VM1 (pin No.21 and 22) and VM2 (pin No.9 and 10) should be connected to the same power supply voltage.

■ **Terminal Equivalent Circuits**

| Pin No. | Name | Function | Equivalent Circuits |
|---|---|---|---|
| 18 | VIO | Logic Input Power Supply |  |
| 17 | VC | Control System Power Supply | |
| 5<br>6 | EN<br>PSAVE | Logic Input<br>(Built-in 100kΩ pull-up) |  |
| 1<br>2<br>3<br>4 | IN1A<br>IN1B<br>IN2A<br>IN2B | Control Signal Input |  |
| 21,22<br>9,10 | VM1<br>VM2 | Motor Driver Power Supply<br>(VM1 (pin No. 21, 22), VM2 (pin No. 9, 10) to connect the same power supply voltage) |  |
| 19, 20<br>23, 24<br>11, 12<br>7, 8 | OUT1A<br>OUT1B<br>OUT2A<br>OUT2B | Motor Driver Output | |
| 14<br>15 | VG<br>CH | Connection Terminal for Stabilizing Capacitor<br><br>Connection Terminal for Charge Pump Capacitor |  |
| 16 | CL | Connection Terminal for Charge Pump Capacitor |  |
| 13<br>Exposed Pad | DGND<br>PGND | Digital Ground<br>Power system ground |  |

## 6. Absolute Maximum Ratings

| Parameter | Symbol | Min. | Max. | Unit | Remarks |
|---|---|---|---|---|---|
| Control Supply Voltage | VC | -0.5 | 6.0 | V | |
| Logic Input Voltage | VIO | -0.5 | 6.0 | V | VIO ≤ VC (Note 6) |
| Motor Driver Operating Voltage | VM | -0.5 | 19 | V | |
| VIO Level Terminal Voltage (PSAVE,EN,IN1A,IN1B,IN2A,IN2B) | Vterminal1 | -0.5 | 5.5 | V | |
| VM Level Terminal Voltage (OUT1A,OUT1B,OUT2A,OUT2B) | Vterminal2 | -0.5 | 19 | V | |
| VG, CH Terminal Voltage | Vterminal3 | -0.5 | 25 | V | |
| CL Terminal Voltage | Vterminal4 | -0.5 | 6.0 | V | |
| Maximum DC Output Current | IloaddcMD | - | 1.3 | A | OUTnA and OUTnB terminal |
| Maximum Peak Output Current | IloadpeakMD | - | 3<br>4.5 | A | OUTnA and OUTnB terminal<br>within 10ms in 200ms<br>within 5ms in 200ms |
| Power Dissipation | PD | - | 1625 | mW | Ta = 85°C (Note 5) |
| Operating Temperature Range | Ta | -30 | 85 | °C | |
| Maximum Junction Temperature | Tj | - | 150 | °C | |
| Storage Temperature Range | Tstg | -65 | 150 | °C | |

Note 4. All above voltages are with respect to GND.

Note 5. This is calculated as θJA=40°C/W using a 4-layer board. The exposed pad must be connected to GND. SEMI JEDEC JESD51-6 and JESD51-7 compliant boards are used.

Note 6. Logic Input Power Supply (VIO) needs to be turned on at the same time or earlier than Control System Power Supply (VC).

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

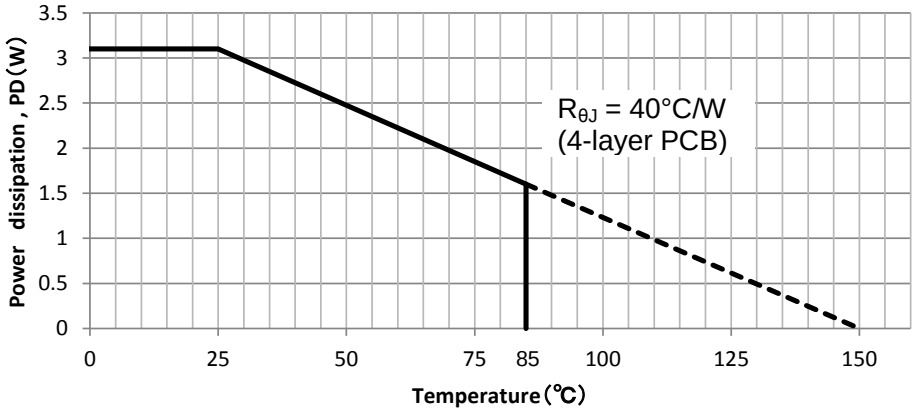



Figure 2. Maximum Power Dissipation

## 7. Recommended Operating Conditions

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Control Supply Voltage | VC | 2.7 | 3.3 | 5.5 | V |
| Logic Input Voltage | VIO | 1.62 | 1.8/3.3 | VC | V |
| Motor Power Supply Voltage | VM | 2.0 | - | 18 | V |
| Input Frequency Range (50% duty) | Fin | - | - | 200 | kHz |

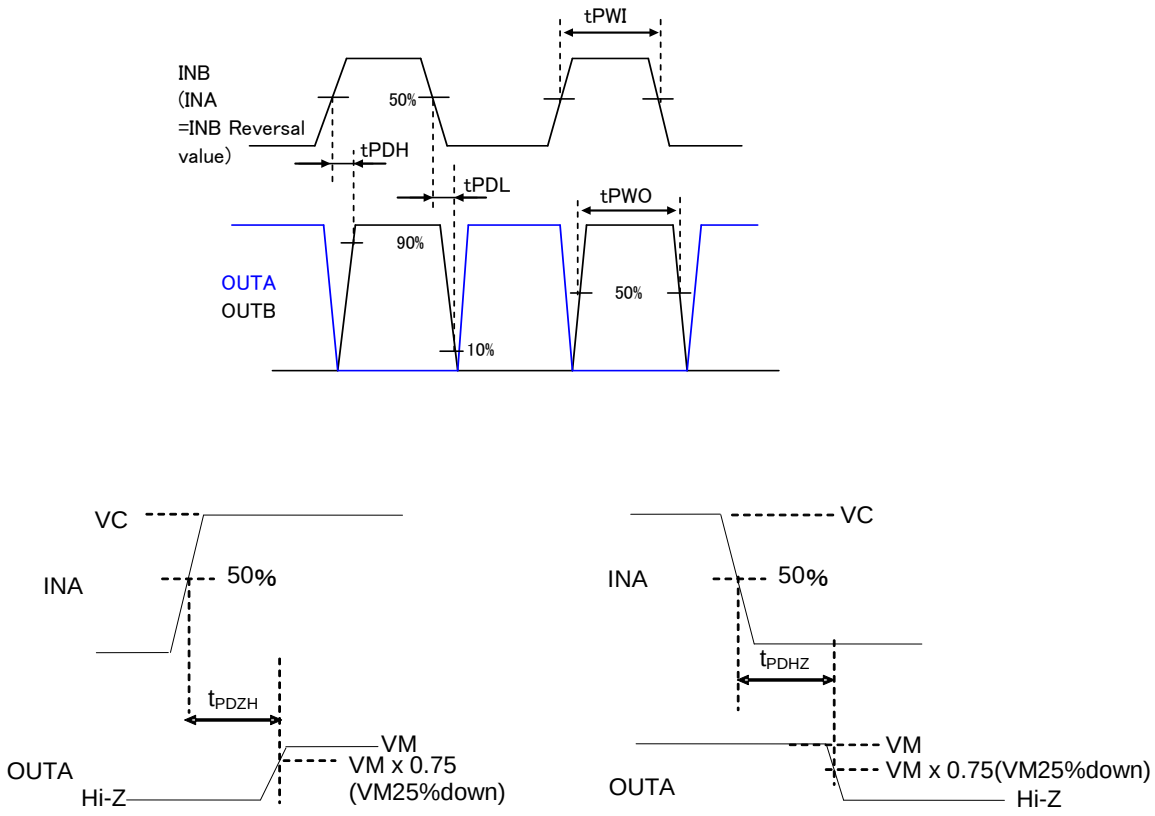
## 8. Electrical Characteristics

(Ta = 25°C, VM = 15V, VC = 3.3V, unless otherwise specified.)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Charge Pump | | | | | | |
| Charge Pump Voltage | VG | VG = VC + VM<br>INnA = "L", INnB = "L" | 18.0 | 18.2 | 18.3 | V |
| Charge Pump wake up time | $t_{VG}$ | VG = VC + VM – 0.3V<br>CVG = 0.1uF | 0.1 | 1 | 3 | ms |
| UVLO | | | | | | |
| VC under voltage lock out voltage | $VC_{UV}$ | | 1.9 | 2.2 | 2.5 | V |
| TSD | | | | | | |
| Thermal shutdown temperature (Note 7) | $T_{DET}$ | | 150 | 175 | 200 | °C |
| Temperature hysteresis (Note 7) | $T_{DETHYS}$ | | 20 | 30 | 40 | °C |
| Quiescent Current | | | | | | |
| VM quiescent current at no power | $I_{VMNOPOW+}$ | VIO = VC = 0V | - | - | 2 | µA |
| VM quiescent current at Standby | $I_{VMSTBY}$ | PSAVE = "L", EN = "H"<br>INnA = "L", INnB = "L" | - | 15 | 70 | µA |
| VC quiescent current at Standby | $I_{VCSTBY}$ | PSAVE = "L", EN = "H"<br>INnA = "L", INnB = "L" | - | 150 | 300 | µA |
| VC quiescent current at power save | $I_{VCPSAVE}$ | PSAVE = "H", EN = "H" | - | - | 1 | µA |
| VC quiescent current at PWM operation | $I_{VCPWM}$ | INnA= 200kHz,<br>INnB = "H" | - | 1 | 2 | mA |
| Motor Driver | | | | | | |
| On-resistance 1<br>(High side or Low side) | $R_{ON1}$ | VC = 3.3V, Iload =100mA<br>Ta = 25°C | - | 0.18 | 0.25 | Ω |
| On-resistance 2<br>(High side or Low side) (Note 7) | $R_{ON2}$ | VC = 3.3V, Iload = 1.2A<br>Ta = 25°C<br>(Equivalent Tj = 85°C) | - | 0.22 | 0.27 | Ω |
| On-resistance 3<br>(High side or Low side) (Note 7) | $R_{ON3}$ | VC = 3.3V, Iload = 1.2A<br>Ta = 85°C<br>(Equivalent Tj = 150°C) | - | 0.27 | 0.32 | Ω |
| Body diode forward voltage | $V_{FMD}$ | $I_F$ = 100 mA | - | 0.8 | 1.2 | V |
| Output delay time<br>(INn:"H"→"L" to OUTn:"H"→"L")<br>(Note 8) | $t_{PDL}$ | tr = tf = 10ns | - | - | 0.5 | µs |
| Output delay time<br>(INn:"L"→"H" to OUTn:"L"→"H")<br>(Note 8) | $t_{PDH}$ | tr = tf = 10ns | - | - | 1.0 | µs |
| Output delay time<br>(INn:"L"→"H" to OUTn:Hi-Z→"H")<br>(Note 8) | $t_{PDZH}$ | tr = tf = 10ns | - | - | 0.5 | µs |
| Output delay time<br>(INn:"H"→"L" to OUTn:"H"→Hi-Z)<br>(Note 8) | $t_{PDHZ}$ | tr = tf= 10ns | - | - | 2.0 | µs |
| H-bridge output pulse width<br>(Note 8) | $t_{PWO}$ | $t_{PWI}$ = 1.0µs,<br>tr = tf = 10ns | 0.6 | - | - | µs |
| Control logic | | | | | | |
| Input High level voltage<br>(INnA, INnB, EN, PSAVE) | $V_{IH}$ | VIO = 1.62V~5.5V | 0.7×VIO | - | - | V |
| Input Low level voltage<br>(INnA, INnB, EN, PSAVE) | $V_{IL}$ | | - | - | 0.3×VIO | V |

Note 7. Not tested in production.

Note 8. Refer to Figure 3.




Hi-Z →"H" Output Delay Time
(INB pin = "L")

"H" →Hi-Z Output Delay Time
(INB pin = "L")

Figure 3. Timing Chart of Output Propagation Delay Time and Pulse Width

# 9. Functional Descriptions

## 9.1 Control Logic

Input and Output statuses of each operation mode are shown below. (X: don't care)

| PSAVE | EN | Input | | Output | | Operation Mode |
|---|---|---|---|---|---|---|
| | | INnA | INnB | OUTnA | OUTnB | |
| L | H | L | L | Hi-Z | Hi-Z | Standby |
| L | H | L | H | L | H | Reverse (CCW) |
| L | H | H | L | H | L | Forward (CW) |
| L | H | H | H | L | L | Brake |
| L | L | X | X | L | L | Brake |
| H | X | X | X | Hi-Z | Hi-Z | Power Save (Note 9) |

Note 9. TSD, UVLO, Internal charge pump and VREF circuits stop operation.

## 9.2 The Basic Configuration of The Motor Driver Unit

The AP1018 has the N-channel LDM CMOS FETs for both high and low sides of the output stage, so that small package can be adopted. The high-side FET is driven by VG voltage. VG = VM + VC is generated by the charge pump. VG voltage reaches the target value within 1ms (typ.) after the charge pump starts operation. The charge pump operates at 360kHz (typ). The low-side FET is driven by the VC voltage.

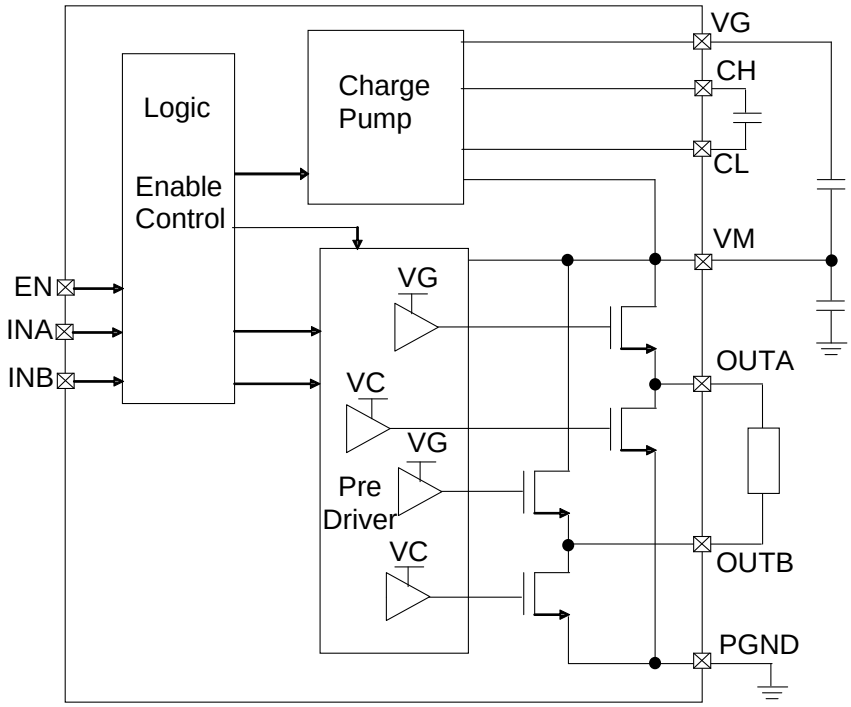



Figure 4. Equivalent Circuit of Motor Driver Block

The OSC block supplies a drive pulse to the charge pump. Logic input buffer is operated by the power supply from the VIO pin. Logic input power supply (VIO) should be turned on at the same time or earlier than the Control system power supply (VC). Logic Input Power Supply (VIO) is Control System Power Supply (VC) and turned on at the same time or earlier. (With applications such as the VIO is turned on later than the VC, it is recommend to connect a pull-up resistor about 500kΩ between the VIO and the VC pins to avoid an indefinite state of the circuit)

### 9.3 Protection Functions

The AP1018 has penetration current prevention, thermal shutdown and under voltage detection circuits.

• Penetration Current Prevention Circuit

MOSFETs are turned off for both high side and low side during the dead time period that is when the penetration current prevention circuit is in operation. The dead time is included in the H-Bridge output delay time of the electrical characteristics. Figure 5 shows the signal timing images.

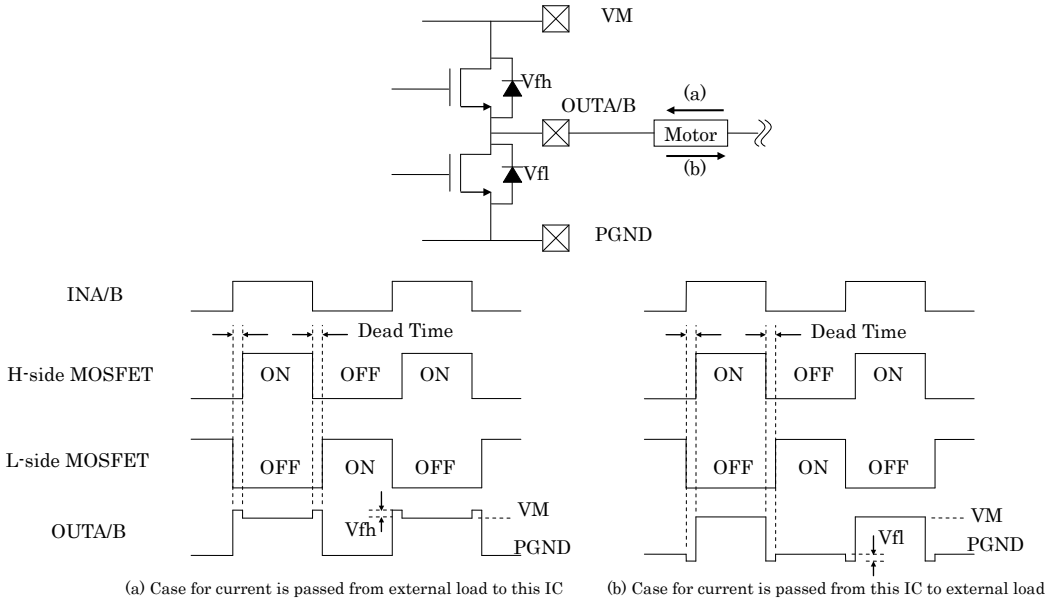



Figure 5. Difference In Output Terminal By Load Current Direction

• Thermal Shut Down (TSD)

The AP1018 prevents damages from self-heating by setting OUTA and OUTB outputs Hi-Z when abnormal high temperature is detected. The AP1018 is able to return to normal operation as soon as the temperature drops to the level lower than the bottom detection threshold.

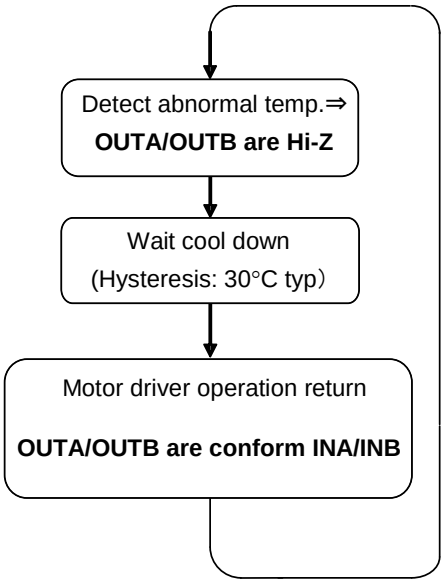



Figure 6. Detection of Abnormal Heat and Returning Normal Operation

• Under Voltage Detection Circuits
The H-bridge driver outputs become high-impedance by the under-voltage detection circuit (UVD) when the control power supply voltage (VC) is lower than the specified value.
After the low-voltage detection, the H-bridge driver will be operational when the control power supply voltage (VC) exceeds the value of specified voltage $VC_{UV}$ + hysteresis voltage $VC_{UVHYS}$ (0.08Vtyp).

□ Timing Chart

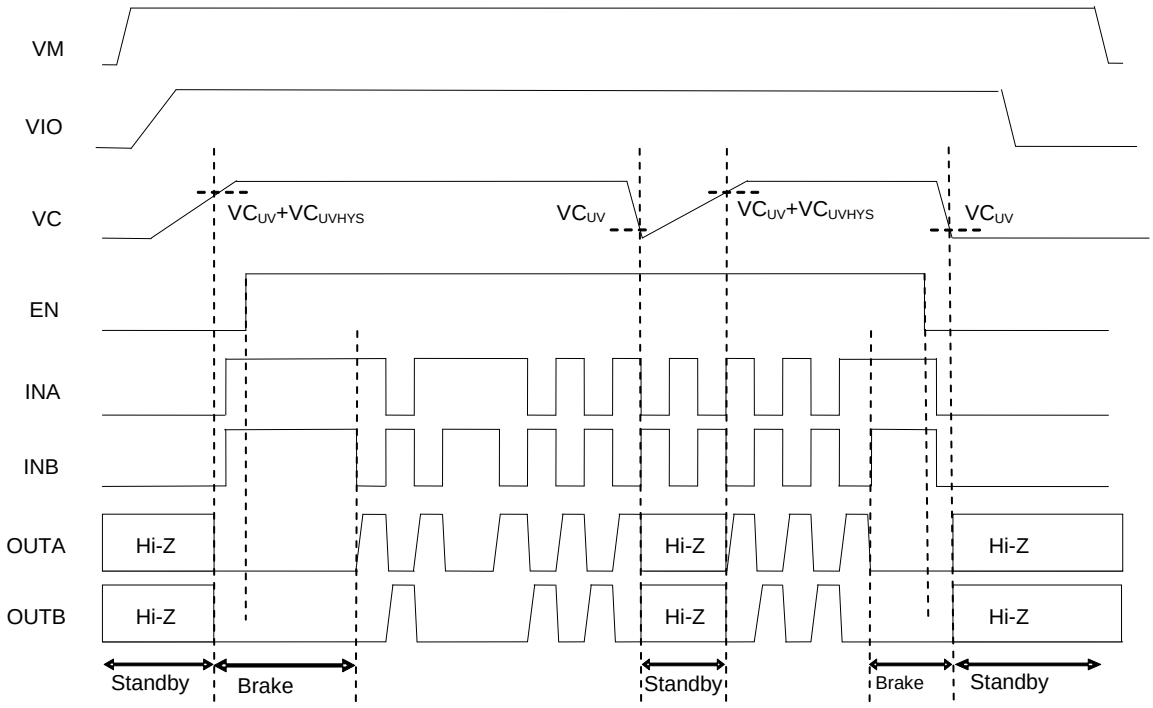



Figure 7. Timing Chart of Input and Output (In Cace of Under Voltage Detection)

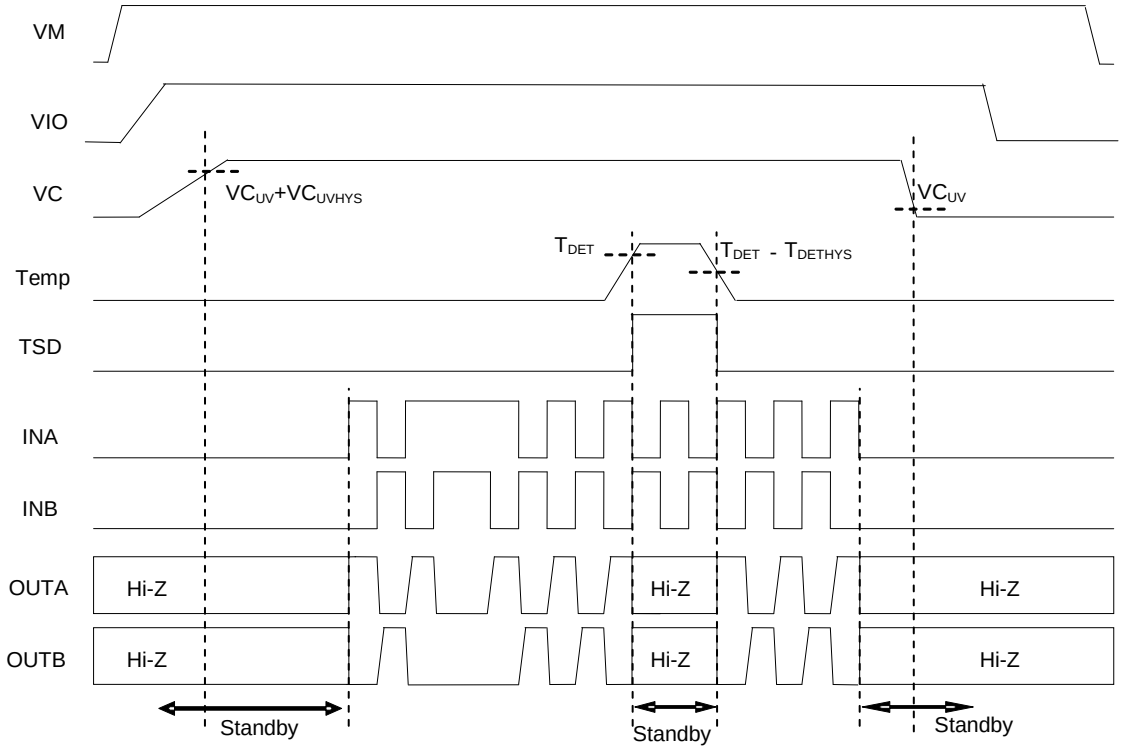



Figure 8. Timing Chart of Input and Output (In Cace of TSD Detection)

## 10. Recommended External Circuit

### ■ Recommended External Circuit

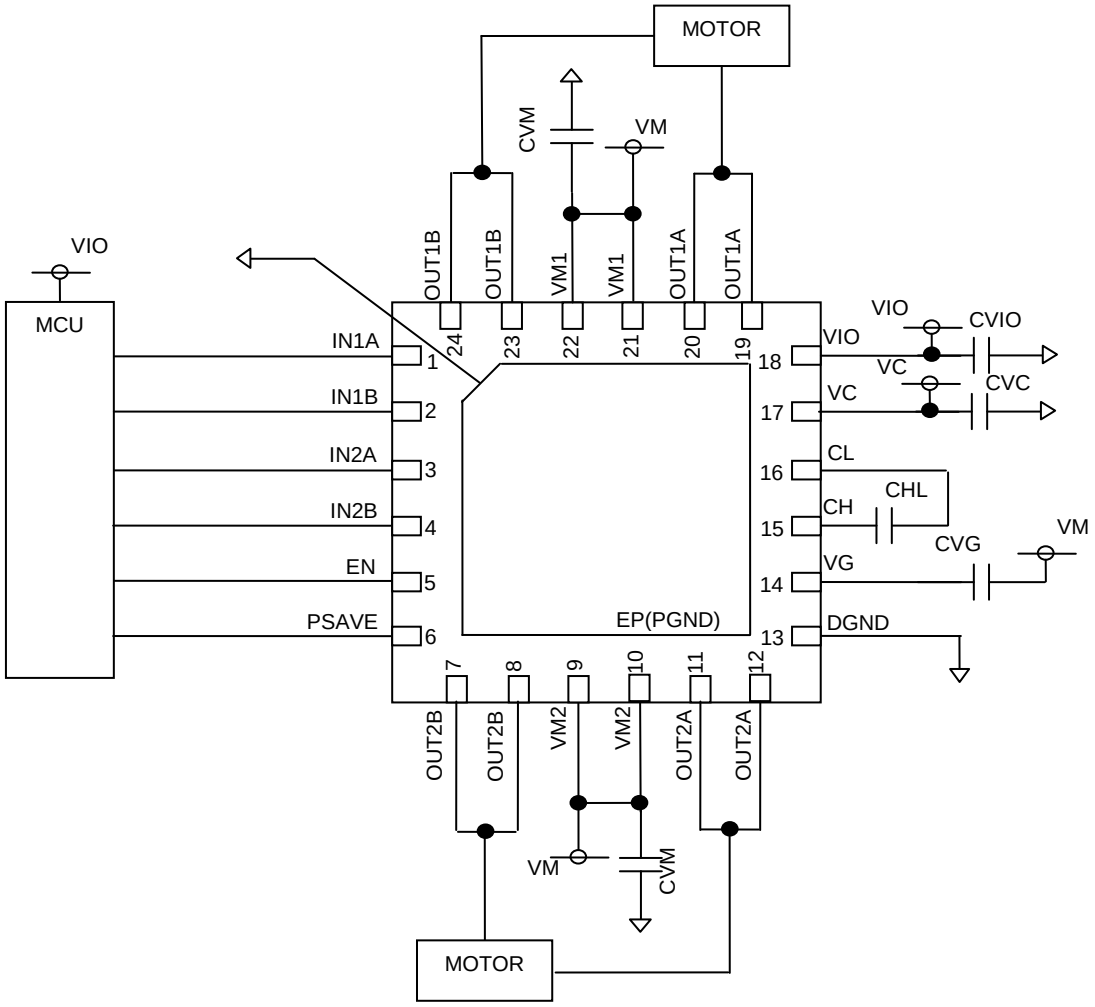



Figure 9. Recommended External Circuit

### ■ Recommended External Components

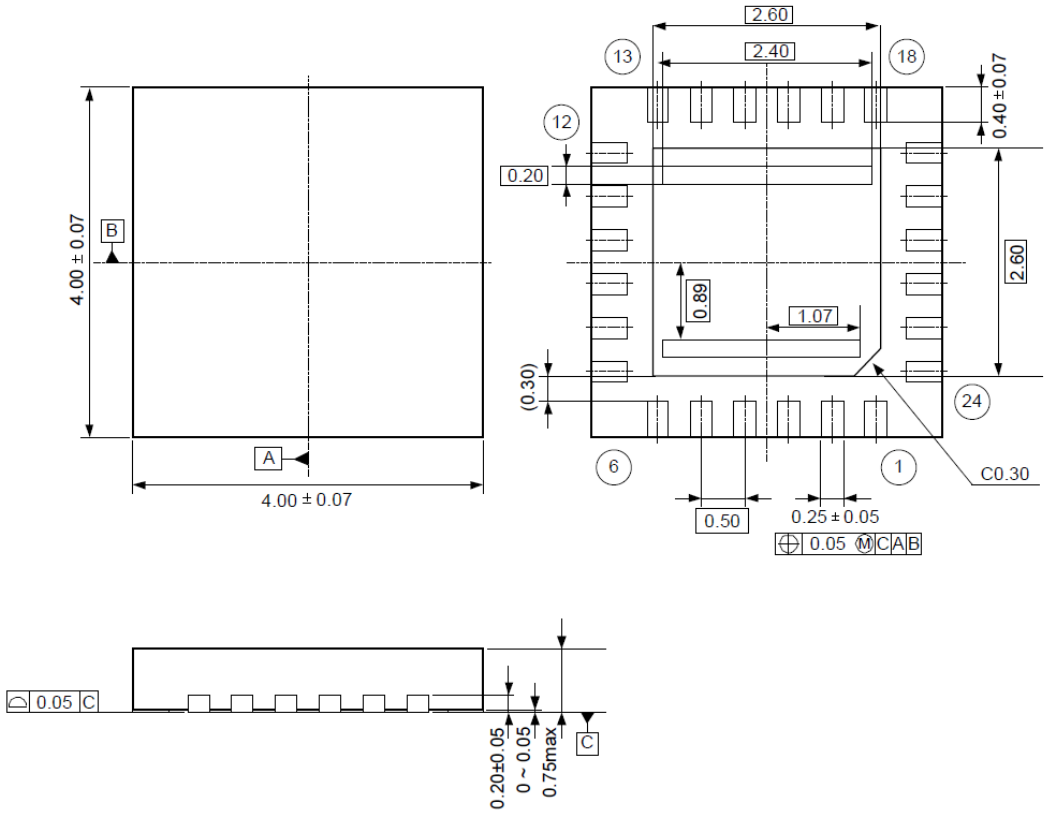
| Items | Symbol | min | typ | max | Unit | Remark |
|---|---|---|---|---|---|---|
| Motor Driver Power Supply (decoupling capacitor) | CVM | 1.0 | - | - | µF | Ceramic Capacitor (Note 10) |
| VC Control Power Supply (decoupling capacitor) | CVC | 0.1 | 1.0 | - | µF | |
| VIO Control Power Supply (decoupling capacitor) | CVIO | 0.1 | 1.0 | - | µF | |
| Charge Pump Capacitor 1 | CVG | 0.047 | 0.1 | 0.22 | µF | Ceramic Capacitor |
| Charge Pump Capacitor 2 | CHL | 0.047 | 0.1 | 0.22 | µF | Ceramic Capacitor |

Note 10. Above values are examples. Please choose appropriate external components for your system board.
Note 11. VM1 (pin No. 21 and 22) and VM2 (pin No. 9 and 10) should be connected to the same power supply voltage.
Note 12. The exposed pad should be connected to the DGND pin for heat dissipation.

## 11. Package

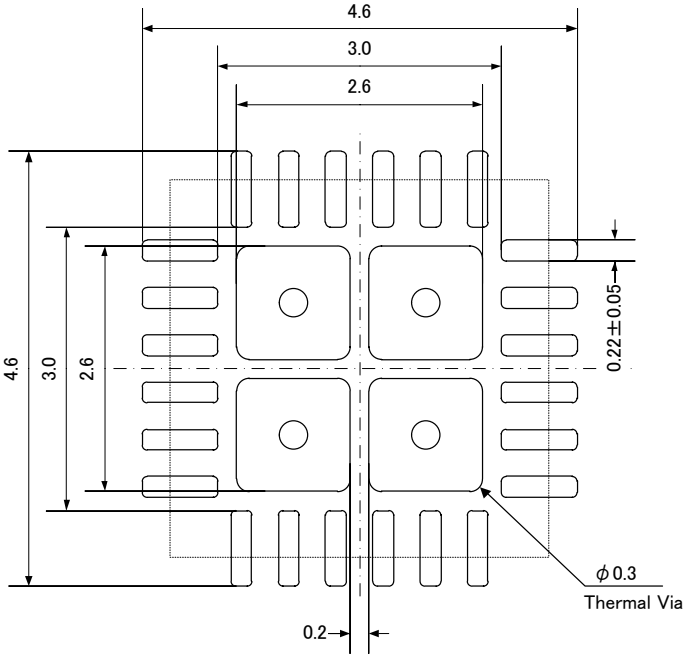
### ■ Outline Dimensions

24-pin QFN (Unit mm)




### ■ Recommended Land Pattern

AP1018AEN: 24-pin QFN Package

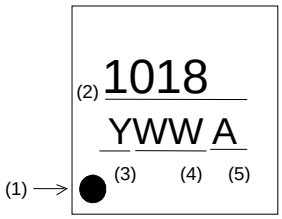



[unit: mm]



Detailed diagram of
^

■ **Marking**




(1) No.1 pin Indication
(2) Market No
(3) Year Code (last digit of the year)
(4) Week Code
(5) Management Code

## 12. Ordering Guide

| | | |
|---|---|---|
| AP1018AEN | -30 ~ 85°C | 24-pin QFN |

## 13. Revision History

| Date (YY/MM/DD) | Revision | Page | Contents |
|---|---|---|---|
| 17/05/29 | 00 | - | First Edition |

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