AMT49106

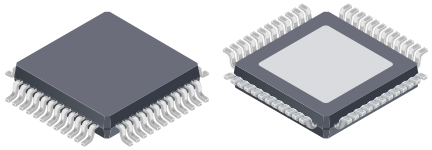
Automotive Three-Phase MOSFET Driver

FEATURES AND BENEFITS

- 3-phase bridge MOSFET driver
- Bootstrap gate drive for N-channel MOSFET bridge
- Cross-conduction protection with adjustable dead time
- Charge pump for low supply voltage operation
- Operation at any PWM duty cycle up to and including 100%
- 4.5 to 50 V supply voltage operating range
- Supply for external isolator
- Three programmable current sense amplifiers
- SPI-compatible serial interface
- Bridge control by direct logic inputs or serial interface
- Q&A watchdog
- Extensive programmable diagnostics
- Diagnostic verification
- Safety-assist features
- Automotive AEC-Q100 qualified
- A²-SIL™ product—device features for safety-critical systems*

PACKAGE:

48-pin LQFP with exposed thermal pad (suffix JP)



Not to scale

*The AMT49106 was developed in accordance with ISO 26262 as a hardware safety element out of context with ASIL D capability for use in automotive safety-related systems when integrated and used in the manner prescribed in the applicable safety application note and datasheet.

DESCRIPTION

The AMT49106 is an N-channel power MOSFET driver capable of controlling MOSFETs connected in a 3-phase bridge arrangement and is specifically designed for automotive applications with high-power inductive loads, such as BLDC motors.

A unique charge pump regulator provides the supply for the MOSFET gate drive for battery voltages down to 5.5 V and allows the AMT49106 to operate with a reduced gate drive down to 4.5 V. Gate drive voltage and strength are programmable to help reduce EMC issues. A bootstrap capacitor is used to provide the above-battery supply voltage required for N-channel MOSFETs with a VCP charge pump facilitating high side gate drive switching at any PWM duty cycle up to and including 100%.

Full control is provided over all six power MOSFETs in the 3-phase bridge, allowing motors to be driven with block commutation or sinusoidal excitation. The power MOSFETs are protected from shoot-through by integrated crossover control and optional programmable dead time.

Integrated diagnostics provide indication of multiple internal faults, system faults, and power bridge faults, and can be configured to protect the power MOSFETs under most short-circuit conditions. For safety-critical systems, the integrated diagnostic operation can be verified under control of the serial interface.

The serial interface is provided to alter programmable settings and read back detailed diagnostic information.

The AMT49106 is supplied in a 48-pin QFP package (suffix JP) with exposed thermal pad. The package is lead (Pb) free with 100% matte-tin leadframe plating.

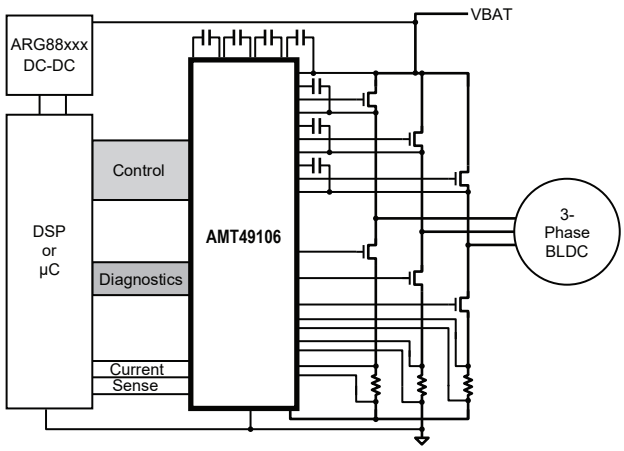


Figure 1: Typical Application

SELECTION GUIDE

Part Number	Packing	Package
AMT49106KJPTR	1500 pieces per 13-inch reel	48-terminal LQFP with exposed thermal pad

Table of Contents

ALLEGRO microsystems
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ABSOLUTE MAXIMUM RATINGS [1][2]

Characteristic	Symbol	Notes	Rating	Unit
Load Supply Voltage	V_{BB}	VBB	–0.3 to 50	V
VREG Charge Pump Terminal	V_{REG}	VREG	–0.3 to 16	V
VREG Charge Pump Capacitor Terminal	V_{CP}	CP1, CP3	–0.3 to 16	V
VREG Charge Pump Capacitor Terminal	V_{CP2}	CP2	V_{CP1} – 0.3 to V_{REG} + 0.3	V
VREG Charge Pump Capacitor Terminal	V_{CP4}	CP4	V_{CP3} – 0.3 to V_{REG} + 0.3	V
VCP Charge Pump Capacitor Terminal	V_{CP5}	CP5	–0.3 to V_{BB} + 0.3	V
VCP Charge Pump Capacitor Terminal [4]	V_{CP6}	CP6	V_{REG} – 0.3 to V_{VCP} + 0.3, V_{CP5} – 0.3 to V_{CP5} + 16	V
VCP Charge Pump Terminal	V_{VCP}	VCP	V_{BB} – 0.3 to V_{BB} + 16	V
Battery-Compliant Logic Inputs	V_{IB}	HA, HB, HC, LA, LB, LC, ENABLE	–0.3 to 50	V
Logic Supply Input	V_{IO}	VIO	–0.3 to 6	V
Logic Inputs	V_I	STRn, SCK, SDI	–0.3 to 6	V
Logic Outputs	V_O	SDO	–0.3 to V_{IO} + 0.3	V
Diagnostic Output Terminal	V_{DIAG}	DIAG	–0.3 to 50	V
Sense Amplifier Inputs	V_{CSI}	CSxP, CSxM	–10 to 10	V
Sense Amplifier Outputs	V_{CSO}	CSxO	–0.3 to V_{OOR} + 0.3	V
Sense Amplifier Output Offset Input	V_{OOR}	OOR	–0.3 to 6	V
Bootstrap Supply Terminals	V_{Cx}	CA, CB, CC	–0.3 to V_{VCP} + 0.3	V
		CA, CB, CC (transient) [3]	–0.3 to V_{VCP} + 5	V
High-Side Gate Drive Outputs	V_{GHx}	GHA, GHB, GHC	V_{Cx} – 16 to V_{Cx} + 0.3	V
		GHA, GHB, GHC (transient) [3]	–18 to V_{Cx} + 0.3	V
Motor Phase Terminals	V_{Sx}	SA, SB, SC	V_{Cx} – 16 to V_{Cx} + 0.3	V
		SA, SB, SC (transient) [3]	–18 to V_{Cx} + 0.3	V
Low-Side Gate Drive Outputs	V_{GLx}	GLA, GLB, GLC	V_{REG} – 16 to 18	V
		GLA, GLB, GLC (transient) [3]	–8 to 18	V
Bridge Low-Side Source Terminals	V_{LSS}	LSSA, LSSB, LSSC	V_{REG} – 16 to 18	V
		LSSA, LSSB, LSSC (transient) [3]	–10 to 18	V
NVM Maximum Programming Junction Temperature	T_{NVM}	Guaranteed by design characterization	85	°C
Ambient Operating Temperature Range	T_A	Limited by power dissipation	–40 to 150	°C
Maximum Continuous Junction Temperature	$T_{J(max)}$		165	°C
Transient Junction Temperature	T_{Jt}	Over temperature event not exceeding 10 seconds, lifetime duration not exceeding 10 hours, guaranteed by design characterization.	180	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C

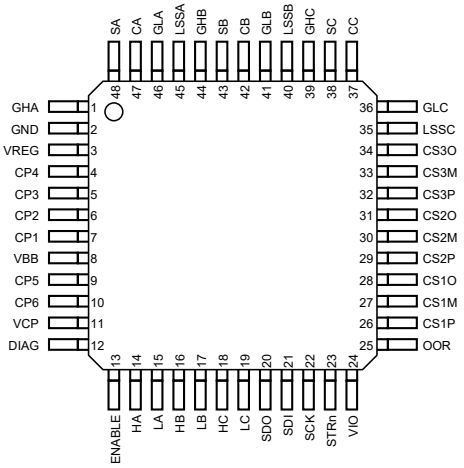
[1] With respect to GND. Ratings apply when no other circuit operating constraints are present.
[2] Lowercase “x” in terminal names and symbols indicates a variable sequence character.
[3] Not tested in production. Confirmed by design and characterization. Duration less than 1 µs.
[4] Both stated Rating limits apply.

THERMAL CHARACTERISTICS: May require derating at maximum conditions

Characteristic	Symbol	Test Conditions [4]	Value	Unit
JP Package Thermal Resistance	$R_{\theta JA}$	4-layer PCB based on JEDEC standard	24	°C/W
		2-layer PCB with 3.8 in.^{2} of copper area each side	44	°C/W
	$R_{\theta JP}$		2	°C/W

[4] Additional thermal information available on the Allegro website.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com



QFP-48 (JP) Package Pinout Diagram

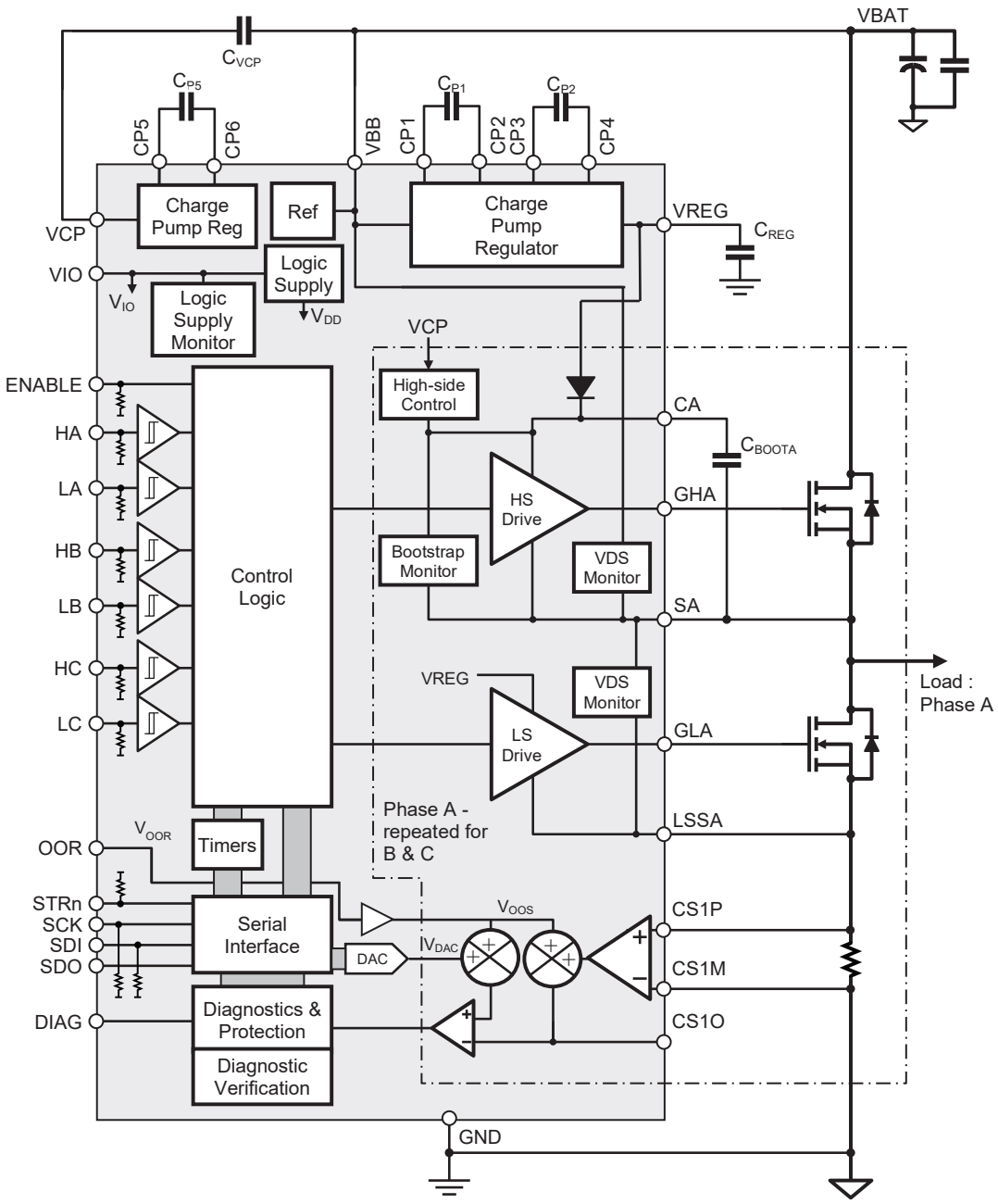
Terminal List Table

Name	Number	Function
CA	47	Bootstrap Capacitor Phase A
CB	42	Bootstrap Capacitor Phase B
CC	37	Bootstrap Capacitor Phase C
CP1	7	Pump Capacitor
CP2	6	Pump Capacitor
CP3	5	Pump Capacitor
CP4	4	Pump Capacitor
CP5	9	VCP Charge Pump Capacitor
CP6	10	VCP Charge Pump Capacitor
CS1M	27	Current Sense Amp 1 -Input
CS1O	28	Current Sense Amp 1 Output
CS1P	26	Current Sense Amp 1 +Input
CS2M	30	Current Sense Amp 2 -Input
CS2O	31	Current Sense Amp 2 Output
CS2P	29	Current Sense Amp 2 +Input
CS3M	33	Current Sense Amp 3 -Input
CS3O	34	Current Sense Amp 3 Output
CS3P	32	Current Sense Amp 3 +Input
DIAG	12	Programmable diagnostic output
ENABLE	13	Direct Output Activity Control
GHA	1	High-side Gate Drive Phase A
GHB	44	High-side Gate Drive Phase B
GHC	39	High-side Gate Drive Phase C
GLA	46	Low-side Gate Drive Phase A
PAD	Pad	Connect To Ground

Name	Number	Function
GND	2	Ground
GLB	41	Low-side Gate Drive Phase B
GLC	36	Low-side Gate Drive Phase C
HA	14	Control Input A High Side
HB	16	Control Input B High Side
HC	18	Control Input C High Side
LA	15	Control Input A Low Side
LB	17	Control Input B Low Side
LC	19	Control Input C Low Side
LSSA	45	Low-side Source Phase A
LSSB	40	Low-side Source Phase B
LSSC	35	Low-side Source Phase C
SA	48	Load Connection Phase A
SB	43	Load Connection Phase B
SC	38	Load Connection Phase C
SCK	22	Serial Clock Input
SDI	21	Serial Data Input
SDO	20	Serial Data output
STRn	23	Serial Strobe (chip select) Input
VBB	8	Main Power Supply
VCP	11	VCP charge pump terminal
VIO	24	Digital I/O Supply Input
OOR	25	Current Sense Amplifier’s Bias Voltage Input
VREG	3	VREG charge pump terminal

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

FUNCTIONAL BLOCK DIAGRAM



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS: Valid at T_J = –40°C to 150°C, V_{BB} = 4.5 to 50 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY AND REFERENCE						
VBB Functional Operating Range	V_{BB}	Operating; outputs active	4.5	–	50	V
		Operating[1]; outputs disabled	3.4	–	50	V
		No unsafe states	0	–	50	V
VBB Quiescent Current	I_{BBQ}	ENABLE = high, V_{BB} = 12 V, all gate drive outputs low	–	10	17	mA
	I_{BBS}	ENABLE = low, sleep mode, V_{BB} < 35 V	–	–	18	µA
VIO Functional Operating Range	V_{IO}	Device logic operational	3	–	5.5	V
VIO Quiescent Current	I_{IOQ}	Active State	–	–	20	mA
	I_{IOS}	Sleep State, ENABLE ≤ 300 mV, SDI ≤ 300 mV, SCK ≤ 300 mV, STRn = V_{IO}	–	–	10	µA
Core Logic Supply Voltage [10]	V_{DD}		2.5	–	3.5	V
VREG Output Voltage	V_{REG}	5.5 V < V_{BB} ≤ 7.5 V, I_{VREG} = 0 to 32 mA	11	13	14.5	V
		V_{BB} > 7.5 V, I_{VREG} = 40 mA	11	13	14.5	V
VCP Voltage [8]	V_{CP}	V_{CP} = V_{VCP} – V_{BB}, I_{CP} = 15 mA, V_{REG} ≥ 11 V	9.5	–	15.2	V
Bootstrap Diode Forward Voltage	V_{fBOOT}	I_D = 10 mA	0.4	0.7	1.0	V
		I_D = 100 mA	1.5	2.2	2.8	V
Bootstrap Diode Resistance	r_D	$r_{D(100\ mA)}$ = ($V_{fBOOT(150\ mA)}$ – $V_{fBOOT(50mA)}$)/ 100 mA	5	11	24	Ω
Bootstrap Diode Current Limit	I_{DBOOT}		230	500	750	mA
High-Side Gate Drive Static Load Resistance	R_{GSH}		50	–	–	kΩ
High-Side Control Voltage Drop [8]	V_{HIGH}	V_{HIGH} = V_{VCP} – V_{CX}, I_{HIGH} = 5 mA	–	–	300	mV
System Clock Period	t_{OSC}		42.5	50	57.5	ns

Continued on the next page…

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS (continued): Valid at T_J = –40°C to 150°C, V_{BB} = 4.5 to 50 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GATE OUTPUT DRIVE						
Turn-On Time, High-Side	$t_{r(HS)}$	C_{LOAD} = 30 nF, 2 V to 8 V, $V_{Cx} – V_{Sx}$ = 11 V	110	–	454	ns
Turn-On Time, Low-Side	$t_{r(LS)}$	C_{LOAD} = 30 nF, 2 V to 8 V, $V_{REG} – V_{LSSx}$ = 11 V	110	–	454	ns
Turn-Off Time, High-Side	$t_{f(HS)}$	C_{LOAD} = 30 nF, 8 V to 2 V, $V_{Cx} – V_{Sx}$ = 11 V	47	–	250	ns
Turn-Off Time, Low-Side	$t_{f(LS)}$	C_{LOAD} = 30 nF, 8 V to 2 V, $V_{REG} – V_{LSSx}$ = 11 V	47	–	250	ns
Pull-Up On-Resistance	$R_{DS(on)UP}$	T_J = 25°C, I_{GH} = –150 mA [2]	2.5	–	7.7	Ω
		T_J = 150°C, I_{GH} = –150 mA [2]	4	–	11.9	Ω
Pull-Up Peak Source Current (High-Side)	$I_{PUPK(HS)}$	$V_{Cx} – V_{Sx}$ = 11 V	–2200	–	–600	mA
Pull-Up Peak Source Current (Low-Side)	$I_{PUPK(LS)}$	$V_{REG} – V_{LSSx}$ = 11 V	–2200	–	–600	mA
Pull-Down On-Resistance	$R_{DS(on)DN}$	T_J = 25°C, I_{GL} = 150 mA [2]	0.6	–	1.9	Ω
		T_J = 150°C, I_{GL} = 150 mA [2]	0.9	–	2.7	Ω
Pull-Down Peak Sink Current (High-Side)	$I_{PDPK(HS)}$	$V_{Cx} – V_{Sx}$ = 11 V	1100	–	4100	mA
Pull-Down Peak Sink Current (Low-Wide)	$I_{PDPK(LS)}$	$V_{REG} – V_{LSSx}$ = 11 V	1100	–	4100	mA
High-Side Minimum Turn-On Time	t_{HRM}	THR = 0	42	55	65	ns
High-Side Turn-On Time Mean Step Size	t_{HRS}	THR > 0	12	16	20	ns
High-Side Turn-On Current 1	I_{HR1}	V_{GS} = 0 V, IHR1 = 15	–1050	–240	–160	mA
		Programmable setpoint range	–240	–	–16	mA
High-Side Turn-On Current 2	I_{HR2}	V_{GS} = 0 V, IHR2 = 15	–1050	–240	–160	mA
		Programmable setpoint range	–240	–	–16	mA
High-Side Minimum Turn-Off Time	t_{HFM}	THF = 0	42	55	65	ns
High-Side Turn-Off Time Mean Step Size	t_{HFS}	THF > 0	12	16	20	ns
High-Side Turn-Off Current 1	I_{HF1}	V_{GS} = 9 V, IHF1 = 15	160	240	320	mA
		Programmable setpoint range	16	–	240	mA
High-Side Turn-Off Current 2	I_{HF2}	V_{GS} = 9 V, IHF2 = 15	160	240	320	mA
		Programmable setpoint range	16	–	240	mA
Low-Side Minimum Turn-On Time	t_{LRM}	TLR = 0	42	55	65	ns
Low-Side Turn-On Time Mean Step Size	t_{LRS}	TLR > 0	12	16	20	ns
Low-Side Turn-On Current 1	I_{LR1}	V_{GS} = 0 V, ILR1 = 15	–1050	–240	–160	mA
		Programmable setpoint range	–240	–	–16	mA
Low-Side Turn-On Current 2	I_{LR2}	V_{GS} = 0 V, ILR2 = 15	–1050	–240	–160	mA
		Programmable setpoint range	–240	–	–16	mA
Low-Side Minimum Turn-Off Time	t_{LFM}	TLF = 0	42	55	65	ns
Low-Side Turn-Off Time Mean Step Size	t_{LFS}	TLF > 0	12	16	20	ns
Low-Side Turn-Off Current 1	I_{LF1}	V_{GS} = 9 V, ILF1 = 15	160	240	320	mA
		Programmable setpoint range	16	–	240	mA
Low-Side Turn-Off Current 2	I_{LF2}	V_{GS} = 9 V, ILF2 = 15	160	240	320	mA
		Programmable setpoint range	16	–	240	mA

Continued on the next page…

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS (continued): Valid at T_J = –40°C to 150°C, V_{BB} = 4.5 to 50 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GATE OUTPUT DRIVE (continued)						
GHx Output Voltage High	V_{GHH}	Bootstrap capacitor fully charged	V_{Cx} – 0.02	–	–	V
GHx Output Voltage Low	V_{GHL}	–10 µA < I_{GH} < 10 µA	–	–	V_{Sx} + 0.02	V
GLx Output Voltage High	V_{GLH}		V_{REG} – 0.02	–	–	V
GLx Output Voltage Low	V_{GLL}	–10 µA < I_{GL} < 10 µA	–	–	V_{LSSx} + 0.02	V
Gate-Source Voltage, MOSFET On	V_{GSon}	No faults present	V_{ROFF}	–	V_{REG}	V
GHx Passive Pull-Down	R_{GHPD}	V_{BB} = 0 V, V_{GHx} – V_{Sx} = 0.1 V	0.25	–	2	MΩ
		V_{BB} = 0 V, I_{GHx} = 500 µA	0.5	–	10	kΩ
GLx Passive Pull-Down	R_{GLPD}	V_{BB} = 0 V, V_{GLx} – V_{LSSx} = 0.1 V	0.25	–	2	MΩ
		V_{BB} = 0 V, I_{GLx} = 500 µA	0.5	–	10	kΩ
GHx Active Pull-Down	R_{GHPA}	V(Cx-Sx) > 4 V	0.3	–	20	Ω
GLx Active Pull-Down	R_{GLPA}	V(VREG-LSSx) > 4 V	0.3	–	20	Ω
Turn-Off Propagation Delay	$t_{P(off)}$	Phase input change to unloaded gate output change (see Figure 5); DT[5:0] = 0	–	–	73	ns
		Phase input change to unloaded gate output change, excluding jitter[4] (see Figure 5); DT[5:0] > 0	–	–	148	ns
Turn-On Propagation Delay	$t_{P(on)}$	Phase input change to unloaded gate output change (see Figure 5); DT[5:0] = 0	–	–	58	ns
		Phase input change to unloaded gate output change, excluding jitter[4] (see Figure 5); DT[5:0] > 0	–	–	133	ns
Propagation Delay Matching (Phase-to-Phase)	Δt_{PP}	Same state change, DT[5:0] = 0	–	–	15	ns
Propagation Delay Matching (On-to-Off)	Δt_{OO}	Single phase, DT[5:0] = 0	–	–	22	ns
Propagation Delay Matching (GHx-to-GLx)	Δt_{HL}	Same state change, DT[5:0] = 0	–	–	17	ns
Dead Time (Turn-Off to Turn-On Delay)	t_{DEAD}	DT[5:0] = 100000 (see Figure 5)	1.35	1.6	1.85	µs
		Programmable range	0.1	–	6.35	µs
Phase Output Leakage Current	I_{Sx}	CPM1 = 1, CPM0 = 1	–500	–	500	µA

Continued on the next page…

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS (continued): Valid at T_J = –40°C to 150°C, V_{BB} = 4.5 to 50 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
LOGIC INPUTS & OUTPUTS						
Input Low Voltage	V_{IL}		–	–	0.3 × V_{IO}	V
Input High Voltage	V_{IH}		0.7 × V_{IO}	–	–	V
Input Hysteresis	V_{Ihys}		250	550	1000	mV
Input Pull-Down ENABLE	R_{PD}	0 V < V_{IN} < V_{IO} [7]	30	50	77	kΩ
	I_{PD}	V_{IO} <V_{IN} < 50 V [7]	40	100	170	µA
Input Pull-Down LA, LB, LC, HA, HB, HC	R_{PD}	0 V < V_{IN} < V_{IO} [7]	30	50	77	kΩ
	I_{PD}	V_{IO} < V_{IN} < 50 V [7]	40	100	170	µA
Input Pull-Down SDI, SCK	R_{PDS}	0 V < V_{IN} < V_{IO} [7]	30	50	77	kΩ
Input Pull-Up STRn (to V_{IO})	R_{PUS}		30	50	77	kΩ
Output Low Voltage	V_{OL}	I_{OL} = 1 mA [2]	–	0.2	0.4	V
Output High Voltage	V_{OH}	I_{OL} = –1mA [2]	V_{IO} – 0.4	V_{IO} – 0.2	–	V
Output Leakage SDO [2]	I_{OSD}	0 V < V_{SDO} < V_{IO}, STRn = 1	–1	–	1	µA
Output Leakage DIAG [2]	I_{ODI}	0 V < V_{DIAG} < 5.5 V, DG[1:0] = 0	–	–	1	µA
Output Short Circuit Current SDO High [2][9]	I_{OSC}	SDO pulled to ground	–30	–	–	mA
LOGIC I/O – DYNAMIC PARAMETERS						
ENABLE Reset Pulse Width	t_{RST}	GTS = 1	1	–	4.5	µs
Reset Shutdown Time	t_{RSD}	GTS = 1 and ENABLE = low to gate drives disabled and DIAG output high impedance	–	–	40	µs
Clock High Time	t_{SCKH}	A in Figure 4	50	–	–	ns
Clock Low Time	t_{SCKL}	B in Figure 4	50	–	–	ns
Strobe Lead Time	t_{STLD}	C in Figure 4	100	–	–	ns
Strobe Lag Time	t_{STLG}	D in Figure 4	30	–	–	ns
Strobe High Time [12]	t_{STRH}	E in Figure 4 (Serial Registers 0-15, 18-21)	350	–	–	ns
		E in Figure 4 (Serial Registers 16, 17)	2100	–	–	ns
Data Out Enable Time	t_{SDOE}	F in Figure 4; C_{LOAD} = 10 pF	–	–	40	ns
Data Out Disable Time	t_{SDOD}	G in Figure 4	–	–	30	ns
Data Out Valid Time From Clock Falling	t_{SDOV}	H in Figure 4; C_{LOAD} = 10 pF	–	–	40	ns
Data Out Hold Time From Clock Falling	t_{SDOH}	I in Figure 4	5	–	–	ns
Data In Setup Time To Clock Rising	t_{SDIS}	J in Figure 4	15	–	–	ns
Data In Hold Time From Clock Rising	t_{SDIH}	K in Figure 4	10	–	–	ns
Wake Up From Sleep	t_{EN}	C_{REG} = 22 µF	–	–	10	ms

Continued on the next page…

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS (continued): Valid at T_J = –40°C to 150°C, V_{BB} = 4.5 to 50 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
CURRENT SENSE AMPLIFIERS						
Input Offset Voltage	V_{IOS}	After V_{IOS} calibration	–1	–	+1	mV
Input Offset Voltage Drift Over Temperature	ΔV_{IOS}		–2	–	+2	µV/°C
Input Bias Current [2]	I_{BIAS}	V_{ID} = 0 V, V_{CM} in range	–100	–	–5	µA
Input Offset Current [2]	I_{OS}	V_{ID} = 0 V, V_{CM} in range	–1.5	–	+1.5	µA
Input Common-Mode Range (DC)	V_{CM}	V_{ID} = 0 V	–1.5	–	2	V
Gain	A_V	Default power-up value	–	12.5	–	V/V
Gain Error	E_A	V_{CM} in range	–1.6	–	1.6	%
Gain Drift Over Temperature	E_{AD}	V_{CM} in range	–50	–	+50	ppm/°C
Output Offset Reference	V_{OOR}		3	–	5.5	V
Output Offset Reference Input Current	I_{OOR}	All CSxO outputs unloaded	–	–	3	mA
Output Offset Ratio	A_{OO}		1.985	2	2.015	V_{OOR} / V_{OOS}
Small Signal –3 dB Bandwidth [11]	BW	V_{IN} = 10 mVpp [7]	1	–	–	MHz
Output Settling Time (to within 40 mV)	t_{SET}	V_{CSO} = 1 Vpp square wave, Gain = 20 V/V, C_{OUT} = 50 pF	0.2	–	1	µs
Output Dynamic Range	V_{CSOUT}	–100 µA < I_{CSO} < 100 µA	0.3	–	V_{OOR} – 0.3	V
Output Current Sink [2]	I_{CSsink}	V_{ID} = 0 V, V_{CSO} = 1.5 V, Gain = 20 V/V	230	–	470	µA
Output Current Sink (Boosted) [2][5]	$I_{CSsinkb}$	V_{OOS} = 1.5 V, V_{ID} = –50 mV, Gain = 20 V/V, V_{CSO} = 1.5 V	1.9	–	4.4	mA
Output Current Source [2]	$I_{CSsource}$	V_{OOR} = 5V, V_{ID} = 75 mV, Gain = 20 V/V, V_{CSO} = 1.5 V	–15.1	–	–1.6	mA
VBB Supply Ripple Rejection	PSRR	V_{ID} = 0 V, 100 kHz, Gain = 20 V/V	–	75	–	dB
		V_{CSP} = V_{CSM} = 0 V, DC, Gain = 20 V/V	75	–	–	dB
DC Common-Mode Rejection	CMRR	V_{CM} step from 0 to 200 mV, Gain = 20 V/V	52	100	–	dB
AC Common-Mode Rejection	CMRR	V_{CM} = 200 mVpp, 100 kHz, Gain = 20 V/V	–	62	–	dB
		V_{CM} = 200 mVpp, 1 MHz, Gain = 20 V/V	–	43	–	dB
		V_{CM} = 200 mVpp, 10 MHz, Gain = 20 V/V	–	25	–	dB
Common-Mode Recovery Time (to within 100 mV)	t_{CMrec}	V_{CM} step from –4 V to +1 V, Gain = 20 V/V, C_{OUT} = 50 pF	–	–	2.1	µs
Output Slew Rate 10% to 90%	SR	V_{OOR} = 5 V, V_{ID} step from –75 mV to 100 mV, Gain = 20 V/V, C_{OUT} = 50 pF	1.8	–	–	V/µs
Input Overload Recovery (to within 40 mV)	t_{IDrec}	V_{ID} step from 250 mV to 0 V, Gain = 20 V/V, C_{OUT} = 50 pF	–	–	2.1	µs
Offset Calibration Time	t_{Cal}	From STRn rising edge	–	–	100	µs
NVM – PROGRAMMING PARAMETERS						
Programming Voltage	V_{PP}	Applied to V_{BB} when programming	24	–	–	V
Programming Supply Setup Time	t_{PRS}	V_{PP} > V_{PPMIN} to start of NVM write	10	–	–	ms
Number of Write Cycles [11]	N_{WC}	T_J ≤ 85ºC	–	–	400	–

Continued on the next page…

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS (continued): Valid at T_J = –40°C to 150°C, V_{BB} = 4.5 to 50 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
DIAGNOSTICS AND PROTECTION						
VREG Undervoltage	V_{RON}	V_{REG} rising	9.4	9.8	10.2	V
	V_{ROFF}	V_{REG} falling	9.2	9.5	10	V
VREG Overvoltage Warning	V_{ROV}	V_{REG} rising	16.2	16.8	17.3	V
VREG Overvoltage Hysteresis	V_{ROVHys}		900	1200	1700	mV
VBB Overvoltage Warning	V_{BBOV}	V_{BB} rising	32	34	36	V
VBB Overvoltage Hysteresis	$V_{BBOVHys}$		2.5	2.8	3.1	V
VBB Undervoltage	V_{BBUV}	V_{BB} falling	3.5	3.8	4.3	V
VBB Undervoltage Hysteresis	$V_{BBUVHys}$		300	500	700	mV
VPP Undervoltage	V_{PPUV}		20	–	22	V
VIO POR Voltage (rising)	V_{PORON}		2.5	2.8	2.97	V
VIO POR Voltage (falling)	V_{POROFF}		2.4	2.6	2.8	V
Logic Undervoltage when VLM = 0	V_{IOULON}		–	2.9	3.0	V
	$V_{IOULOFF}$		–	2.8	2.9	V
Logic Undervoltage when VLM = 1	V_{IOULON}		4.2	4.3	4.5	V
	$V_{IOULOFF}$		4.1	4.2	4.4	V
Logic Overvoltage when VLM = 0	V_{IOOLON}		3.7	3.8	4.0	V
	$V_{IOOLOFF}$		3.5	3.7	3.9	V
Logic Overvoltage when VLM = 1	V_{IOOLON}		5.55	5.8	5.95	V
	$V_{IOOLOFF}$		5.45	5.7	5.85	V
VOOR Undervoltage when VLR = 0	V_{ORULON}		2.8	2.9	3.0	V
	$V_{ORULOFF}$		2.7	2.8	2.9	V
VOOR Undervoltage when VLR = 1	V_{ORULON}		4.1	4.3	4.5	V
	$V_{ORULOFF}$		4.0	4.2	4.4	V
VOOR Overvoltage when VLR = 0	V_{OROLON}		3.65	3.8	4.0	V
	$V_{OROLOFF}$		3.5	3.7	3.9	V
VOOR Overvoltage when VLR = 1	V_{OROLON}		5.55	5.8	5.95	V
	$V_{OROLOFF}$		5.4	5.7	5.85	V
Bootstrap Undervoltage	V_{BCUV}	V_{BOOT} falling, $V_{BOOT} = V_{Cx} – V_{Sx}$	6.85	8.0	8.85	V
Bootstrap Undervoltage Hysteresis	$V_{BCUVHys}$		150	–	650	mV
VCP Undervoltage [8]	V_{CPUV}	V_{CP} falling, $V_{CP} = V_{VCP} – V_{BB}$	7.3	8.4	9.5	V
VCP Undervoltage Hysteresis	$V_{CPUVhys}$		100	–	350	mV
Gate Drive Undervoltage Warning HS	V_{GSHUV}		$V_{BOOT} – 1.15$	$V_{BOOT} – 1$	$V_{BOOT} – 0.85$	V
Gate Drive Undervoltage Warning LS	V_{GSLUV}		$V_{REG} – 1.15$	$V_{REG} – 1$	$V_{REG} – 0.85$	V
Logic Terminal Overvoltage Warning	V_{LOV}	Voltage rising on HA, LA, HB, LB, HC, LC, or DIAG	6.3	–	9.5	V
Q&A Watchdog Timeout (Minimum) [9]	t_{QMI}	QAT[3:0]=0	85	100	115	µs
Q&A Watchdog Timeout (Maximum) [9]	t_{QMA}	QAT[3:0]=0	170	200	230	µs

Continued on the next page…

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS (continued): Valid at T_J = –40°C to 150°C, V_{BB} = 4.5 to 50 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
DIAGNOSTICS AND PROTECTION (continued)						
VDS Threshold, High-Side	V_{DSTH}	Default power-up value	–	1.2	–	V
		V_{BB} ≥ 5.5 V [6]	–	–	3.15	V
		4.5 V ≤ V_{BB} < 5.5 V [6]	–	–	1.75	V
VDS Threshold Offset, High-Side [3]	V_{DSTHO}	High side on, V_{DSTH} ≥ 1 V	–200	±100	+200	mV
		High side on, V_{DSTH} <1 V	–150	±50	+150	mV
VDS Threshold, Low-Side	V_{DSTL}	Default power-up value	–	1.2	–	V
		V_{BB} ≥ 4.5 V [6]	–	–	3.15	V
VDS Threshold Offset, Low-Side [3]	V_{DSTLO}	Low side on, V_{DSTL} ≥ 1 V	–200	±100	+200	mV
		Low side on, V_{DSTL} < 1 V	–150	±50	+150	mV
VDS and VGS Qualify Time	t_{VDQ}	Default power-up value	1.5	1.7	2.0	µs
		Programmable range	0.6	–	6.3	µs
Phase Comparator Threshold	V_{PT}	Phase voltage rising; default power-up value	48	50	52	%V_{BB}
Overcurrent Threshold Voltage	V_{OCT}	Default power-up value	0.8	0.9	1.08	V
Overcurrent Qualify Time	t_{OCQ}	Default power-up value	6.37	7.5	8.63	µs
On-State Open-Load Threshold Voltage	V_{OLTH}	Default power-up value	90	200	260	mV
		Programmable range	0	–	375	mV
LSS Disconnect Threshold (Rising)	V_{LSD}		4.5	5	5.5	V
LSS Disconnect Threshold Hysteresis	V_{LSDHys}		330	520	630	mV
LSS Verification Current	I_{LU}		–150	–70	–43	µA
DIAG Output: Fault Pulse Period	t_{FP}	DG = 1	85	100	115	ms
DIAG Output: Fault Pulse Duty Cycle	D_{FP}	DG = 1: No Fault present		80		%
		DG = 1: Fault present		20		%
DIAG Output: Temperature Range [13]	V_{TJD}	DG = 2, T_J = 0°C	–	1440	–	mV
DIAG Output: Temperature Slope [13]	A_{TJD}	DG = 2	–	–3.92	–	mV/°C
DIAG Output: Clock Division Ratio	N_D	DG = 3		256000		–
DIAG Output: Temperature Sink Current	I_{TJSI}	DG = 2, V_{DIAG} = 2 V	–	70	–	µA
DIAG Output: Temperature Source Current	I_{TJSO}	DG = 2, V_{DIAG} = 0 V	–	1.1	–	mA
Temperature Warning Threshold [13]	T_{JW}	Temperature increasing	125	135	145	°C
Temperature Warning Hysteresis [13]	T_{JWhys}		11	15	19	°C
Overtemperature Threshold [13]	T_{JF}	Temperature increasing	165	175	185	°C
Overtemperature Hysteresis [13]	T_{JFhys}	Recovery = T_{JF} – T_{JFhys}	11	15	19	°C
Open-Load Timeout	t_{OLTO}		85	100	115	ms

Continued on the next page…

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS (continued): Valid at T_J = –40°C to 150°C, V_{BB} = 4.5 to 50 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Off-State Test Sink Current	I_{SD}	YPS = 3, V(Sx) = 3 V	1.25	2.5	3.77	mA
Off-State Test Source Current	I_{SU}	YSC = 0, V(Sx) = 1 V	–120	–90	–50	µA
		YSC = 1, V(Sx) = 1 V	–460	–410	–300	µA

[1] No internal reset.
[2] For input and output current specifications, negative current is defined as coming out of (being sourced by) the specified device terminal.
[3] VDS offset is the difference between the programmed threshold, V_{DSTH} or V_{DSTL} and the actual trip voltage.
[4] For DT[5:0] > 0, jitter of ±25 ns must be added to the limits shown.
[5] If the amplifier output voltage (V_{CSO}) is more positive than the value demanded by the applied differential input (V_{ID}) and output offset (V_{OOS}) conditions, output current sink capability is boosted to enhance negative going transient response.
[6] Maximum value of VDS threshold that should be set in the configuration registers for correct operation when V_{BB} is within the stated range.
[7] V_{IN} is voltage from relevant terminal with respect to GND.
[8] V_{CP} refers to the voltage on the VCP terminal with respect to the voltage on the VBB terminal. V_{VCP} refers to the voltage on the VCP terminal with respect to the device GND pin.
[9] Confirmed by design.
[10] V_{DD} derived from V_{IO} for internal use only. Not accessible on any device terminal.
[11] Confirmed by characterization. Not production tested.
[12] Strobe high time values apply after serial interface frames addressing the registers listed in the test conditions column.
[13] Stated values confirmed by design and characterization (not production-tested) Associated function production-tested.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

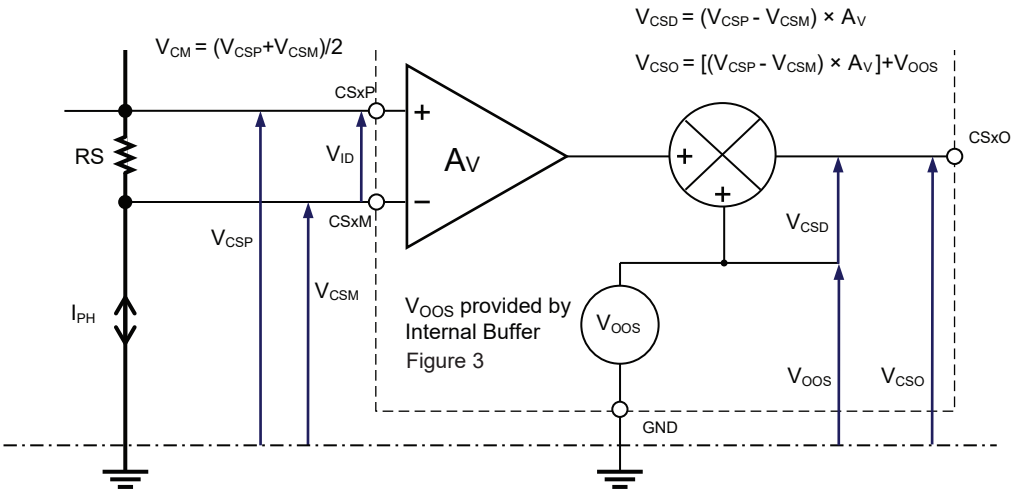


Figure 2: Sense Amplifier Voltage Definitions

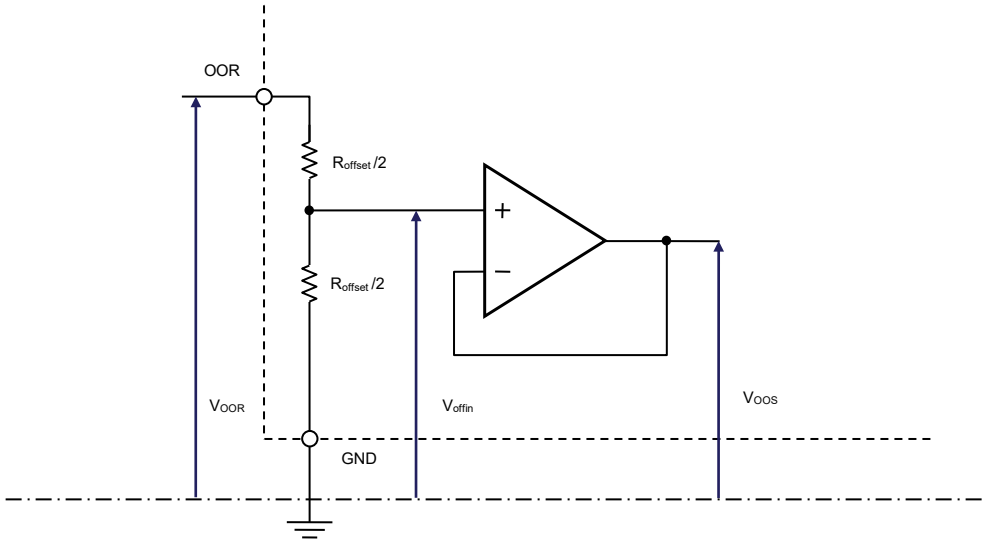
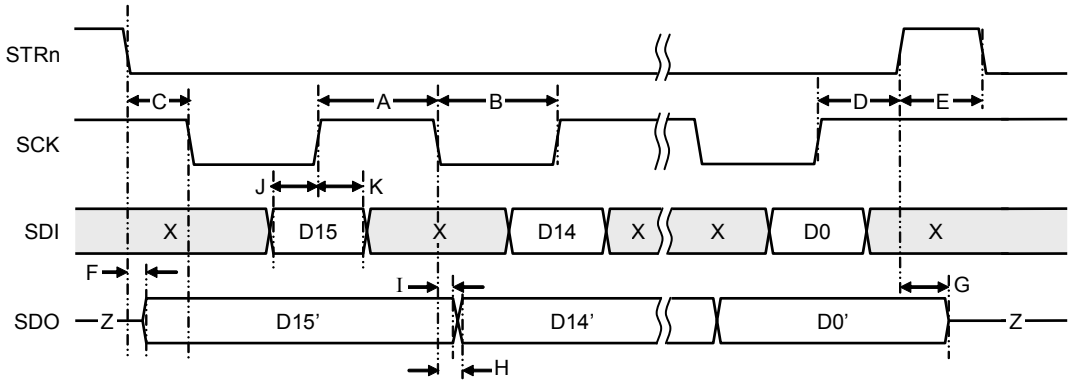


Figure 3: Sense Amplifier Output Offset Voltage Definition

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com



X=don't care, Z=high impedance (tri-state)

Figure 4: Serial Interface Timing

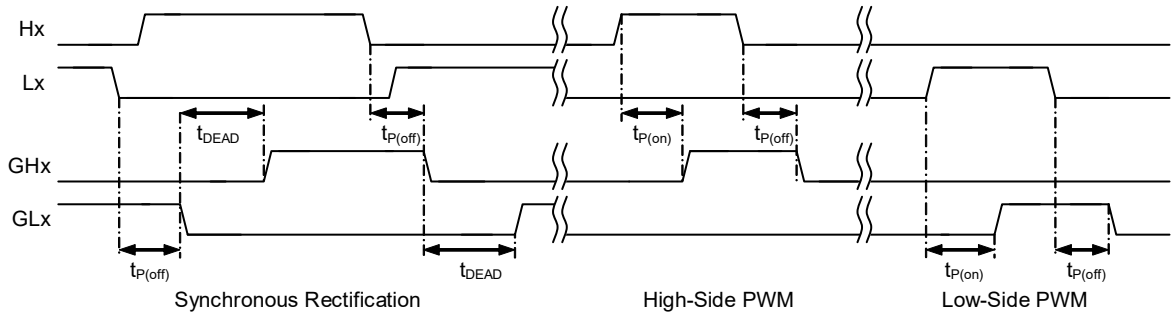


Figure 5: Gate Drive Timing, Phase Logic Inputs

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

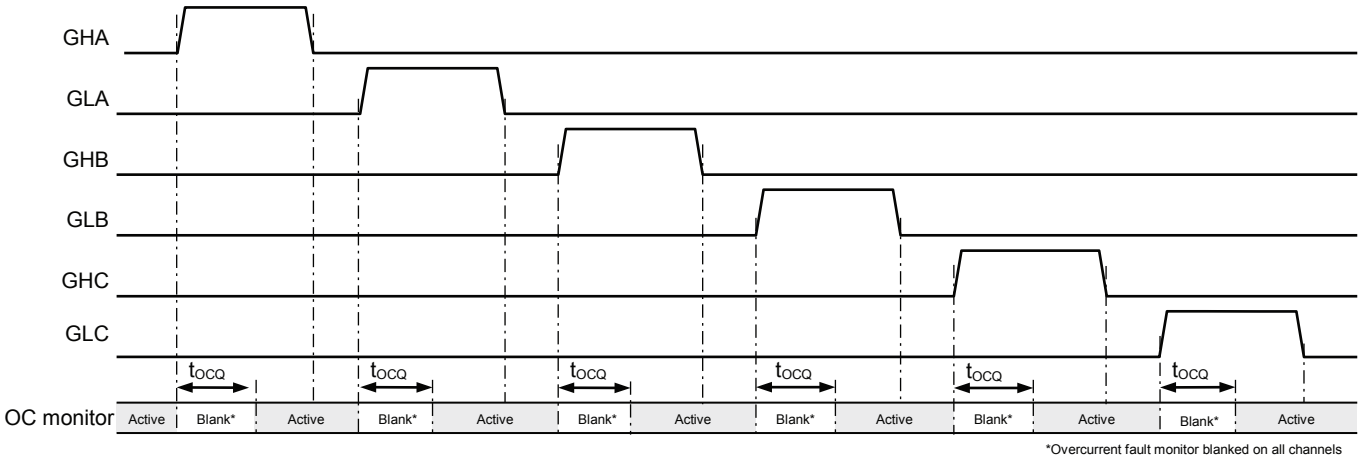


Figure 6: Overcurrent Fault Monitor – Blank Mode Timing (OCQ = 1)

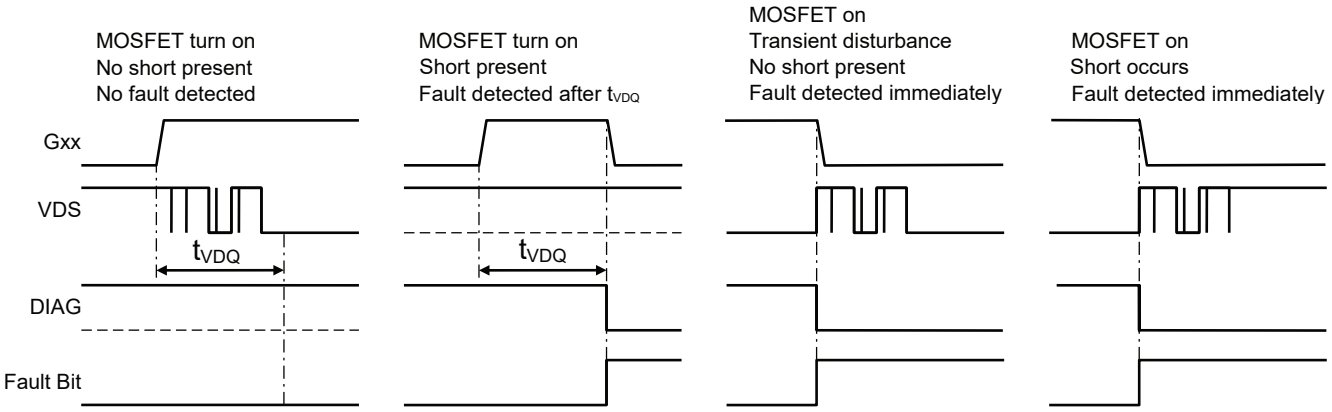


Figure 7: VDS Fault Monitor – Blank Mode Timing (VDQ = 1)

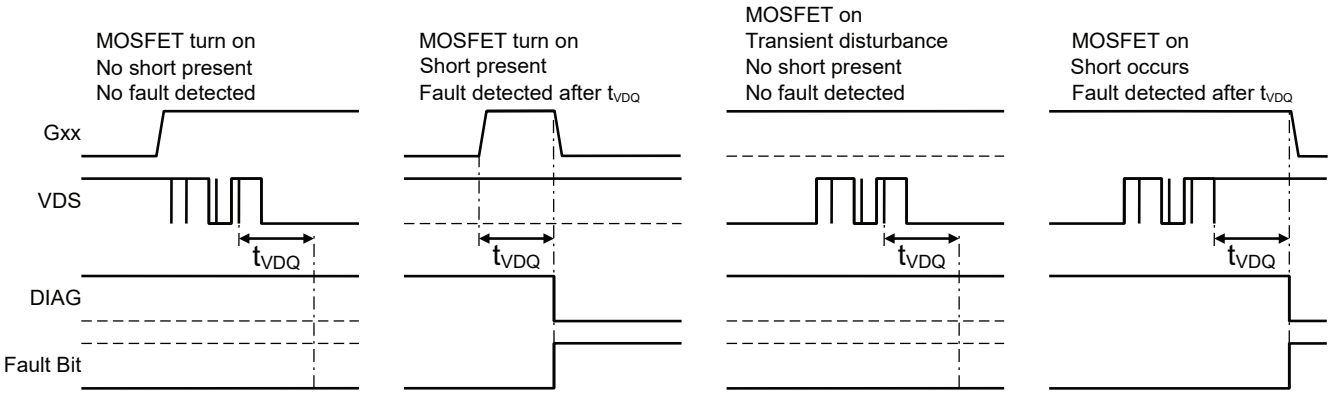


Figure 8: VDS Fault Monitor – Debounce Mode Timing (VDQ = 0)

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

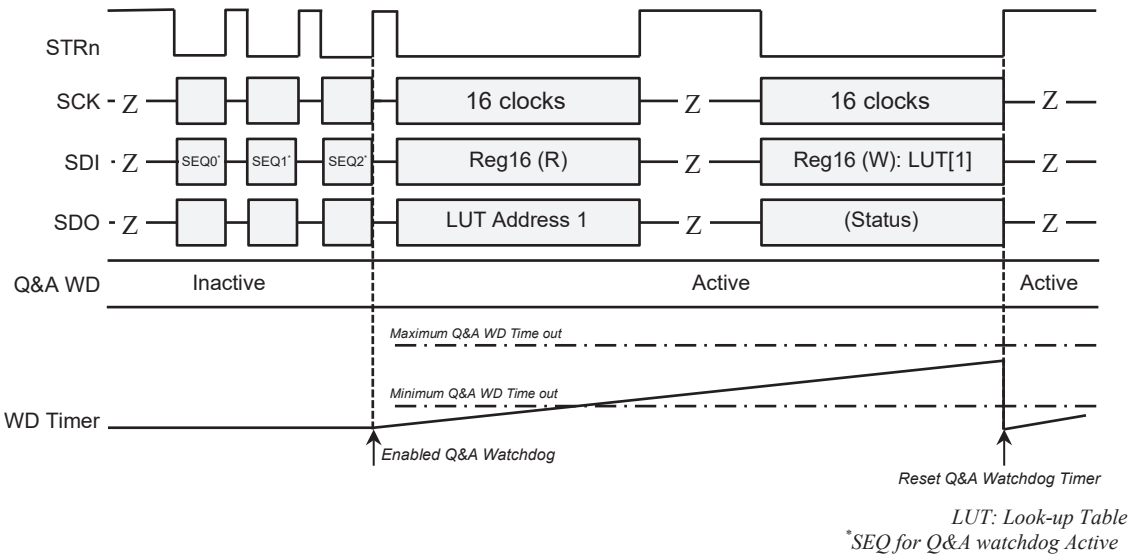


Figure 9: Q&A Watchdog Activation and Correct Reset

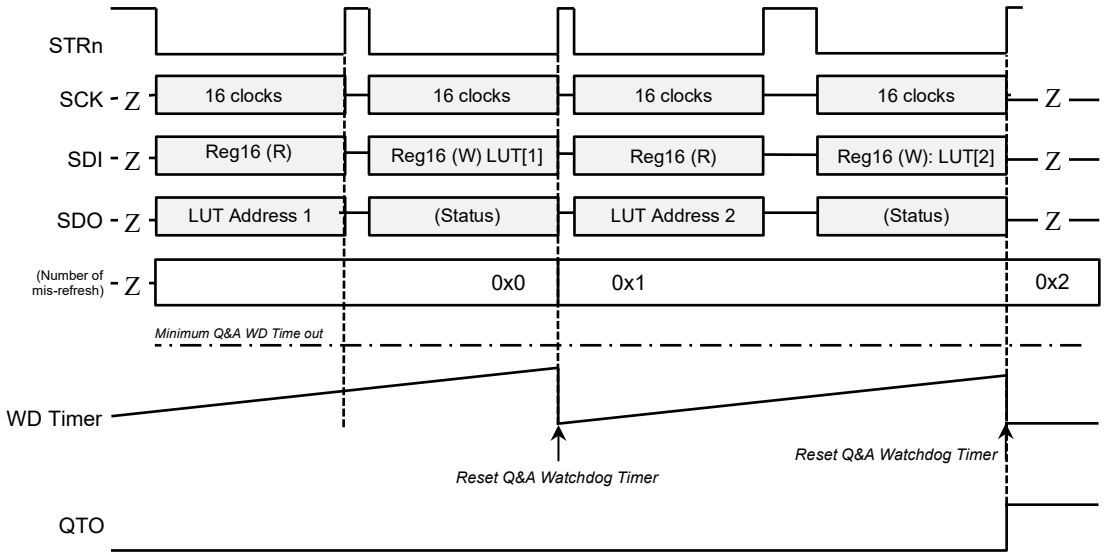


Figure 10: Q&A Watchdog Incorrect Timing Reset (Early Reset)

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

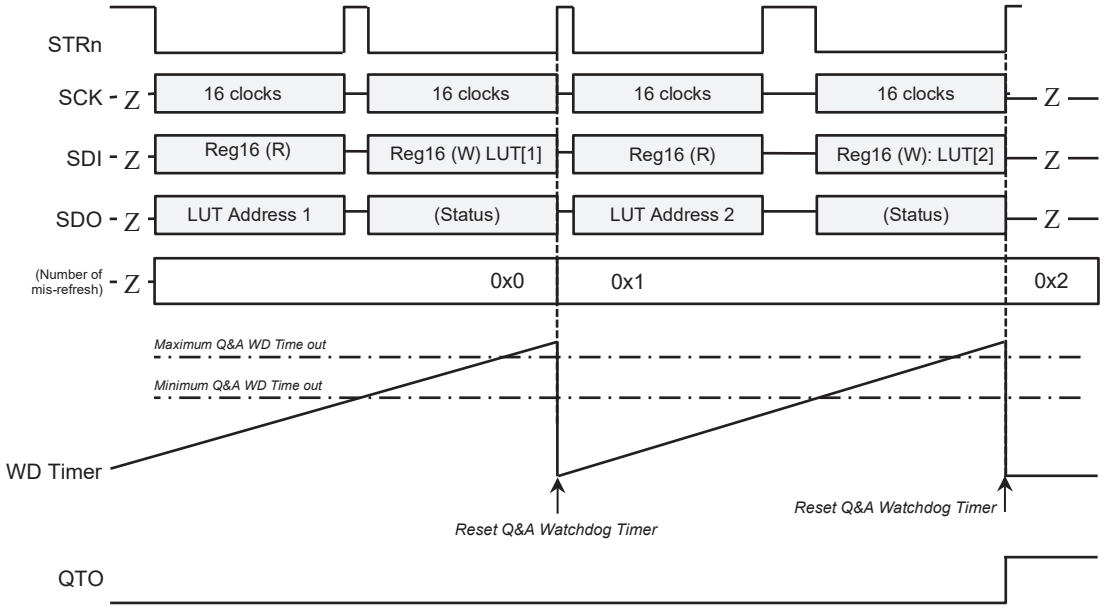


Figure 11: Q&A Watchdog Incorrect Timing Reset (Late Reset)

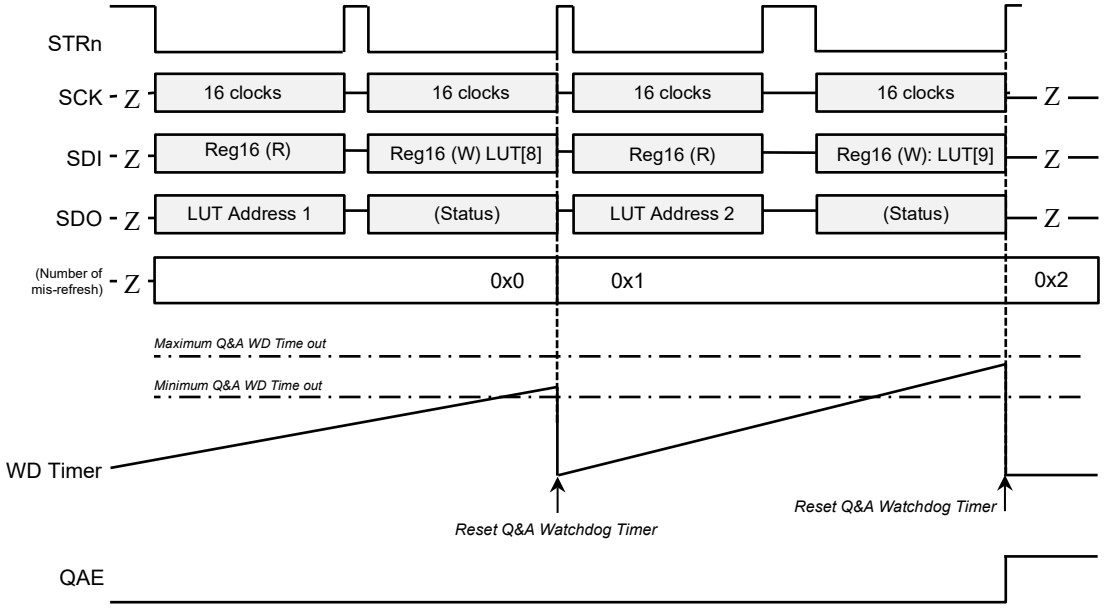


Figure 12: Q&A Watchdog Reset with Wrong Answer

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

LOGIC TRUTH TABLES

Table 1: Control Logic – Logic Inputs

Phase A					Phase B					Phase C				
HA	LA	GHA	GLA	SA	HB	LB	GHB	GLB	SB	HC	LC	GHC	GLC	SC
0	0	LO	LO	Z	0	0	LO	LO	Z	0	0	LO	LO	Z
0	1	LO	HI	LO	0	1	LO	HI	LO	0	1	LO	HI	LO
1	0	HI	LO	HI	1	0	HI	LO	HI	1	0	HI	LO	HI
1	1	LO	LO	Z	1	1	LO	LO	Z	1	1	LO	LO	Z

HI = high-side FET [1] active, LO = low-side FET [1] active
Z = high impedance, both FETs [1] off
All control register bits set to 0; ENABLE = 1

Table 2: Control Logic – Serial Register

Phase A					Phase B					Phase C				
AH	AL	GHA	GLA	SA	BH	BL	GHB	GLB	SB	CH	CL	GHC	GLC	SC
0	0	LO	LO	Z	0	0	LO	LO	Z	0	0	LO	LO	Z
0	1	LO	HI	LO	0	1	LO	HI	LO	0	1	LO	HI	LO
1	0	HI	LO	HI	1	0	HI	LO	HI	1	0	HI	LO	HI
1	1	LO	LO	Z	1	1	LO	LO	Z	1	1	LO	LO	Z

HI = high-side FET [1] active, LO = low-side FET [1] active
Z = high impedance, both FETs [1] off
Logic 0 input on HA, LA, HB, LB, HC, and LC. ENABLE = 1

Table 3: Control Combination Logic – Logic Inputs and Serial Register

Terminal	Register	Internal
Hx	xH	HIx
0	0	0
0	1	1
1	0	1
1	1	1

Terminal	Register	Internal
Lx	xL	LOx
0	0	0
0	1	1
1	0	1
1	1	1

The three phases are controlled independently.

Internal control signals (HIx, LOx) are derived by combining the logic states applied to the control input terminals (Hx, Lx) with the bit patterns held in the Control register (xH, xL).

Normally the input terminals or the Control register method is used for control with the other being held inactive (all terminals or bits at logic 0).

ENABLE	HIx	LOx	GHx	GLx	Sx	Comment
1	0	0	L	L	Z	Phase disabled
1	0	1	L	H	LO	Phase sinking
1	1	0	H	L	HI	Phase sourcing
1	1	1	L	L	Z	Phase disabled
0	X	X	L	L	Z	Phase disabled

X = don't care

[1] In the case of GLx and GHx table columns, "FET" refers to devices internal to the gate driver output stage. In the case of Sx table columns, "FET" refers to discrete devices in the external bridge.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Table 4: Open-Load Detect Mode

						OL detect	
HIA	LOA	HIB	LOB	HIC	LOC	Off-State	On-State
0	0	0	0	0	0	Yes	
0	0	0	0	0	1		
0	0	0	0	1	0		
0	0	0	0	1	1	Yes	
0	0	0	1	0	0		
0	0	0	1	0	1		
0	0	0	1	1	0		Yes
0	0	0	1	1	1		
0	0	1	0	0	0		
0	0	1	0	0	1		Yes
0	0	1	0	1	0		
0	0	1	0	1	1		
0	0	1	1	0	0	Yes	
0	0	1	1	0	1		
0	0	1	1	1	0		
0	0	1	1	1	1	Yes	
0	1	0	0	0	0		
0	1	0	0	0	1		
0	1	0	0	1	0		Yes
0	1	0	0	1	1		
0	1	0	1	0	0		
0	1	0	1	0	1		
0	1	0	1	1	0		Yes
0	1	0	1	1	1		
0	1	1	0	0	0		Yes
0	1	1	0	0	1		Yes
0	1	1	0	1	0		Yes
0	1	1	0	1	1		Yes
0	1	1	1	0	0		
0	1	1	1	0	1		
0	1	1	1	1	0		
0	1	1	1	1	1		
1	0	0	0	0	0		
1	0	0	0	0	1		Yes
1	0	0	0	1	0		
1	0	0	0	1	1		
1	0	0	1	0	0		Yes
1	0	0	1	0	1		Yes
1	0	0	1	1	0		Yes
1	0	0	1	1	1		Yes
1	0	1	0	0	0		
1	0	1	0	0	1		Yes
1	0	1	0	1	0		
1	0	1	0	1	1		
1	0	1	1	0	0		
1	0	1	1	0	1		Yes
1	0	1	1	1	0		
1	0	1	1	1	1		
1	1	0	0	0	0	Yes	
1	1	0	0	0	1		
1	1	0	0	1	0		
1	1	0	0	1	1	Yes	
1	1	0	1	0	0		
1	1	0	1	0	1		
1	1	0	1	1	0		Yes
1	1	0	1	1	1		
1	1	1	0	0	0		
1	1	1	0	0	1		Yes
1	1	1	0	1	0		
1	1	1	0	1	1		
1	1	1	1	0	0	Yes	
1	1	1	1	0	1		
1	1	1	1	1	0		
1	1	1	1	1	1	Yes	

HIx, LOx derived from Table 3.
ENABLE = 1, AOL = 1.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

FUNCTIONAL DESCRIPTION

The AMT49106 provides six high current gate drives capable of driving a wide range of N-channel power MOSFETs. The gate drives are configured as three half bridges, each with a high-side drive and a low-side drive. The three half bridges can be operated independently or together as a three-phase bridge driver for BLDC or PMSM motors.

Gate drives have programmable drive strength and can be controlled individually with logic inputs or through the SPI-compatible serial interface. Independent control over each MOSFET allows each driver to be driven with an independent PWM signal for full sinusoidal excitation.

The AMT49106 requires two power supplies: an analog supply of 4.5 to 50 V connected to VBB and a 3 to 5.5 V logic supply connected to VIO.

The analog supply powers two internal charge pumps. The first charge pump generates a regulated supply (V_{REG}) to provide all the current necessary to drive the low-side gate drive outputs plus most of the charge necessary to drive the high-side gate drives via the bootstrap capacitors. The second charge pump generates an above-battery regulated supply (V_{CP}) to ensure the bootstrap capacitors remain adequately charged during high duty cycle operation. This architecture ensures that all external MOSFETs are fully enhanced at unregulated supply voltages down to 4.5 V and PWM duty cycles over the full range of 0 to 100% without exceptions.

The logic supply directly powers all logic input/output circuitry (V_{IO}) and is linearly regulated to also power the device core logic (V_{DD}).

All logic inputs and outputs have standard CMOS threshold levels derived from the applied V_{IO}. All gate drive control logic inputs are battery voltage compliant, meaning they can be shorted to ground or supply without damage, up to the maximum battery voltage of 50 V.

The AMT49106 will not reset any internal states and the SPI interface will remain active at VIO voltages down to the VIO POR voltage (falling) threshold, V_{POROFF}. If VIO drops below VIO POR voltage (falling) threshold, V_{POROFF}, the part may reset—all internal states will be lost, the SPI interface will cease to operate, and all gate drive outputs will be disabled. If the applied VIO remains above VIO POR voltage (falling) threshold, V_{POROFF}, and the VBB voltage drops below 4.5 V, it is possible that the gate drive outputs may fall below a safe level and be disabled. However, the device logic and SPI interface will remain functional.

A low power sleep mode allows the AMT49106, the power bridge, and the load to remain connected to a vehicle battery supply without the need for an additional supply switch.

The AMT49106 includes many diagnostic features to provide indication of and/or protection against undervoltage, overvoltage, overtemperature, and power bridge faults. Detailed diagnostic information is available through the serial interface.

For systems requiring a higher level of safety integrity, the AMT49106 includes additional overvoltage monitors on the supplies and the control inputs. In addition, the integrated diagnostics include self-test and verification circuits to ensure verifiable diagnostic operation. When used in conjunction with appropriate system level control, these features can assist power drive systems using the AMT49106 to meet stringent ASIL D safety requirements.

The serial interface also provides access to programmable dead time, fault blanking time, programmable V_{DS} threshold for short detection, and programmable thresholds and currents for open-load detection.

The AMT49106 includes three amplifiers designed for low-side current sensing in the presence of high current and voltage transients. These can be used independently to provide three current sense readouts or in combination to provide redundant sensing of a single current. All sense amplifier signal input pins are monitored to ensure they remain connected to the external current sense resistor(s). The gain of each amplifier can be set independently and a common pedestal (offset reference voltage) can be applied to the OOR input pin to allow sensing of bidirectional sense resistor current flow.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Input and Output Terminal Functions

VBB: Power supply for VREG charge pump regulator. Should be connected to VBB through a reverse voltage protection circuit and should be decoupled with ceramic capacitors connected close to the supply and ground terminals.

CP1, CP2, CP3, CP4: Pump capacitor connections for VREG charge pump. Connect capacitors with a recommended nominal value of 2.2 µF between CP1 and CP2 and between CP3 and CP4. These devices should have a rated working voltage of at least 50 V and a tolerance of ±20% or better.

CP5, CP6: Pump capacitor connection for external VCP charge pump. Connect a capacitor with a recommend nominal value of 2.2 µF between CP5 and CP6. This device should have a rated working voltage of at least 25 V and a tolerance of ±20% or better.

VREG: Regulated output voltage, used to supply the low-side gate drivers and to charge the bootstrap capacitors. A sufficiently large storage capacitor must be connected between this terminal and the GND terminal to provide the transient charging current.

GND: Ground. See Layout Recommendations section for further information.

CA, CB, CC: High-side connections for the bootstrap capacitors and positive supply for high-side gate drivers.

GHA, GHB, GHC: High-side gate drive outputs for external N-channel MOSFETs.

SA, SB, SC: Load phase connections. These terminals are the negative supply connections for the floating high-side drivers and are also connected to the negative side of the bootstrap capacitors.

GLA, GLB, GLC: Low-side gate drive outputs for external N-channel MOSFETs.

LSSA, LSSB, LSSC: Low-side return path for discharge of the capacitance on the MOSFET gates, connected to the common sources of the low-side external MOSFETs independently through a low impedance track.

HA, HB, HC: Logic inputs to control the high-side gate drive outputs. Battery voltage compliant terminal.

LA, LB, LC: Logic inputs to control the low-side gate drive outputs. Battery voltage compliant terminal.

SDI: Serial data logic input with pull-down. 16-bit serial word input MSB first.

SDO: Serial data output. High impedance when STRn is high. Outputs bit 15 of the Status register, the fault flag, as soon as STRn goes low.

SCK: Serial clock logic input with pull-down. Data is latched in from SDI on the rising edge of SCK. There must be 16-rising edges per write and SCK must be held high when STRn changes.

STRn: Serial data strobe and serial access enable logic input with pull-up. When STRn is high, any activity on SCK or SDI is ignored and SDO is high impedance, allowing multiple SDI slaves to have common SDI, SCK, and SDO connections.

CS1P, CS1M, CS2P, CS2M, CS3P, CS3M: Current sense amplifier inputs.

CS1O, CS2O, CS3O: Current sense amplifier outputs.

DIAG: Diagnostic output. Programmable output to provide one of four functions: fault flag, pulsed fault flag, temperature, or internal timer. Default is fault flag.

OOR: Power supply for current sense amplifier output stages. Voltage applied to this pin, V_{OOR}, internally divided by a factor of two to generate the current sense amplifier output offset voltage, V_{OOS}.

ENABLE: Disables all gate drive outputs when pulled low. Provides an independent output disable, directly to the gate drive outputs, to allow a fast disconnect on the power bridge. Battery voltage compliant terminal.

VCP: Pumped gate drive voltage referenced to the VBB terminal. Can be used to bias external circuitry in accordance with the VCP voltage specification in the Electrical Characteristics table. Connect a ceramic capacitor, C_{VCP}, of nominal value 2.2 µF between VCP and VBB. This device should have a rated working voltage of at least 25 V and a tolerance of ±20% or better.

VIO: Logic I/O and core logic supply input. Sets logic input thresholds and powers all digital functions including the SPI interface.

ALLEGRO microsystems
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Power Supplies

Two power supplies are required: a digital supply to power all logic circuitry, and an analog supply to power other device functions including the gate drive outputs.

The digital supply, V_{IO}, should be connected to the VIO terminal. This provides the supply voltage for the logic output terminals, the reference for the logic input thresholds, and the input voltage to the linear regulator that generates the supply for the core logic, V_{DD}.

All internal logic is guaranteed to operate correctly to below the regulator undervoltage levels, ensuring that the AMT49106 will continue to operate safely until all logic is reset when a power-on-reset state is present.

A 470 nF decoupling capacitor must be connected close to the VIO and ground terminals. Additional external filtering should be incorporated on these pins as required to mitigate noise propagation back into the system.

The analogue power supply, V_{BB}, should be connected to the VBB terminal through a reverse voltage protection circuit. A 100 nF ceramic decoupling capacitor must be connected close to the VBB and ground terminals.

The output stage of each current sense amplifier is biased from the voltage applied to the OOR terminal, V_{OOR}. A capacitor may be connected between the OOR terminal and ground to provide filtering as required. V_{BB} must be present to allow the current sense amplifiers to operate. If V_{OOR} is present and V_{BB} drops below the VBB undervoltage threshold, V_{BBUV}, all amplifier outputs are disabled and pulled to ground.

The VIO, VBB, and OOR terminals are each monitored by internal diagnostics to detect if the applied voltage is outside acceptable limits. In the case of VIO and VOOR, these limits are set to values appropriate for 5 V or 3.3 V operation according to the state of the VLM and VLR bits in the Config 6 register.

Low Supply Voltage Operation

The AMT49106 will operate within specified parameters with V_{BB} from 4.5 to 50 V. For V_{BB} less than 4.5 V, the outputs may be disabled. As all logic circuitry is powered from the applied VIO supply, the serial interface and core logic will operate even if a VBB supply is not connected. In all cases, the AMT49106 will operate safely between 0 and 50 V on the V_{BB} supply, under all supply switching conditions. This provides a very rugged solution for use in the harsh automotive environment.

VREG Charge Pump Regulator

The gate drivers are powered by an internal voltage regulator which generates a voltage, V_{REG}, at the VREG terminal. It limits the supply voltage to the drivers and therefore the maximum gate voltage. At low supply voltage, the regulated supply is maintained by a charge pump boost converter.

This regulator uses a charge pump scheme with a switching frequency of 62.5 kHz. It operates as a regulated doubler/tripler or a step-down regulator depending on the input voltage on the VBB terminal. Three external capacitors are required for the regulator to operate: two pump capacitors and one storage capacitor. The pump capacitors, C_{P1} and C_{P2} should have a nominal value of 2.2 µF and be connected between the CP1 and CP2 terminals and between the CP3 and CP4 terminals respectively. These devices should have a rated working voltage of at least 50 V and a tolerance of ±20% or better. The storage capacitor, C_{REG}, is connected between the VREG and GND terminals. The storage capacitor value will depend on the size of the bootstrap capacitors and the total gate charge of the external power MOSFETs. Further details on selecting the value of C_{REG} are provided in the Applications Notes section.

VCP Charge Pump Regulator

This regulator generates a voltage above the bridge supply, VBB. It provides some of the switching current for the high-side drives, the charge current for the bootstrap capacitors at high PWM duty cycles, the bias current, and the gate drive current to hold the high-side MOSFET in the on-state.

This regulator also uses a charge pump scheme with a switching frequency of 62.5 kHz. The voltage at the VREG terminal is pumped to produce the required output. Two external capacitors are required for the regulator to operate: one pump capacitor and one storage capacitor. The pump capacitor, C_{P5}, should have a nominal value of 2.2 µF and be connected between the CP5 and CP6 terminals. The storage capacitor, C_{VCP}, should have a nominal value of 2.2 µF and be connected between the VCP and VBB terminals. Both the pump and storage capacitors should have a rated working voltage of at least 25 V and a tolerance of ±20% or better.

One of four modes of operation may be selected according the value of the CPM[1:0] bits in the Configuration 5 register. If CPM[1:0] is set to 00b the regulator runs in auto mode. Average regulator current is greater than 5 mA per phase until internal device logic detects that no high-side gate drive has been commanded on for more than 200 µs and then it drops back to a value of just over 200 µA per phase to reduce device dissipation. Alternatively, if CPM[1:0] is set to 01b or 10b the regulator will drive a fixed current of 200 µA or 5 mA respectively. If CPM[1:0] is set to 11b, the regulator is turned off.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Gate Drives

The AMT49106 is designed to drive external, low on-resistance, power N-channel MOSFETs. It will supply the large transient currents necessary to quickly charge and discharge the external MOSFET gate capacitance in order to reduce dissipation in the external MOSFET during switching. The charge current for the low-side drives and the main recharge current for the bootstrap capacitors are provided by the capacitor on the VREG terminal. The charge current for the high-side drives is provided by the bootstrap capacitors connected between the Cx and Sx terminals, one for each phase. MOSFET gate charge and discharge rates may be controlled by setting a group of parameters via the serial interface.

Bootstrap Supply

When the high-side drivers are active, the reference voltage for the driver will rise close to the bridge supply voltage. The supply to the driver will then have to be above the bridge supply voltage to ensure that the driver remains active. This temporary high-side supply is provided by bootstrap capacitors, one for each high-side driver. These three bootstrap capacitors are connected between the bootstrap supply terminals, CA, CB, CC, and the corresponding high-side reference terminal, SA, SB, SC.

The bootstrap capacitors are independently charged to approximately V_{REG} when the associated reference Sx terminal is low. When the output swings high, the voltage on the bootstrap supply terminal rises with the output to provide the boosted gate voltage needed for the high-side N-channel power MOSFETs.

When the Sx terminal remains high for extended periods of time, the gate drive voltage is maintained by the above-V_{BB} regulated voltage at the VCP terminal. This supply also provides the charging current when the output PWM duty cycle is too high to permit the bootstrap capacitor to be recharged between high-side turn-on events. This combination of bootstrap drive and boosted regulator provides the most efficient gate drive system for a PWM system able to operate between 0 and 100% without restriction.

High-Side Gate Drive

High-side, gate-drive outputs for external N-channel MOSFETs are provided on terminals GHA, GHB, and GHC. GHx = 1 (or “high”) means that the upper half of the driver is turned on and its drain will source current to the gate of the high-side MOSFET in the external motor-driving bridge, turning it on. GHx = 0 (or “low”) means that the lower half of the driver is turned on and its drain will sink current from the external MOSFET’s gate circuit to the respective Sx terminal, turning it off.

The reference points for the high-side drives are the load phase connections, SA, SB and SC. These terminals sense the voltages at the load connections. These terminals are also connected to the negative side of the bootstrap capacitors and are the negative supply reference connections for the floating high-side drivers. The discharge current from the high-side MOSFET gate capacitance flows through these connections, which should have low impedance traces, to the MOSFET bridge.

MOSFET gate charge and discharge rates may be controlled via the serial interface as detailed in the Gate Drive Control section below.

Low-Side Gate Drive

The low-side gate-drive outputs on GLA, GLB, and GLC are referenced to the corresponding LSSx terminal. These outputs are designed to drive external N-channel power MOSFETs. GLx = 1 (or “high”) means that the upper half of the driver is turned on and its drain will source current to the gate of the low-side MOSFET in the external power bridge, turning it on. GLx = 0 (or “low”) means that the lower half of the driver is turned on and its drain will sink current from the external MOSFET’s gate circuit to the LSSx terminal, turning it off.

The LSSx terminals provide the return paths for discharge of the capacitance on the low-side MOSFET gates. These terminals are connected independently to the common sources of the low-side external MOSFETs through a low-impedance tracks.

MOSFET gate charge and discharge rates may be controlled via the serial interface as detailed in the Gate Drive Control section below.

Gate Drive Passive Pull-Down

Each gate drive output includes a discharge circuit to ensure that any external MOSFET connected to the gate drive output is held off when V_{BB} is removed. This discharge circuit appears as a variable pull-down resistance which rapidly falls in value with increasing gate drive voltage. If any MOSFET gate becomes charged by external means, the passive pull-down rapidly discharges it to below the device turn on threshold. In some applications, this can eliminate the requirement for a permanent external gate source resistor. If V_{BB} is applied to the AMT49106, the passive pull-down circuit becomes inactive and does not affect gate drive operation.

Dead Time

To prevent cross-conduction (shoot-through) in any phase of the power MOSFET bridge, it is necessary to have a dead-time delay between a high- or low-side turn off and the next complementary

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

turn-on event. The potential for cross-conduction occurs when any complementary high-side and low-side pair of MOSFETs are switched at the same time, for example, at the PWM switch point. In the AMT49106, the dead time for all phases is set by the contents of the DT[5:0] bits in Configuration 0 register. These six bits contain a positive integer that determines the dead time by division from the system clock.

The dead time is defined as:

$$t_{DEAD} = n \times 50\ ns$$

where n is a positive integer defined by DT[5:0] and t_{DEAD} has a minimum active value of 100 ns.

For example, when DT[5:0] contains [11 0000] (= 48 in decimal), then t_{DEAD} = 2.4 µs, typically.

The accuracy of t_{DEAD} is determined by the accuracy of the system clock as defined in the Electrical Characteristics table. The range of t_{DEAD} is 100 ns to 3.15 µs. A value of 1 or 2 in DT[5:0] sets the minimum active dead time of 100 ns.

If DT[5:0] is set to zero, the dead timer is disabled and no minimum dead time is generated by the AMT49106. The logic that prevents permanent cross-conduction is, however, still active. Adequate dead time must be generated externally by, for example, the microcontroller producing the drive signals applied to the AMT49106 logic inputs or control register.

If using gate drive control, the extended MOSFET switching times that result must be accounted for when setting dead time, as described in the Gate Drive Control section below.

The internally generated dead time is only present if the on command for one MOSFET occurs within one dead time after the off command for its complementary partner. In the case where one side of a phase drive is permanently off, for example when using diode rectification with slow decay, then the dead time does not occur. In this case, the gate drive turns on within the specified propagation delay after the corresponding phase input goes high. (See Figure 5).

Gate Drive Control

MOSFET gate drives are controlled according to the values set in registers 7 through 12.

High-side off-to-on transitions are controlled as detailed in Figure 13a. When a gate drive is commanded to turn on a current, I_1 (as defined by IHR1[3:0]), is sourced on the relevant GHx terminal for a duration, t_1 (defined by THR[3:0]). These parameters should typically be set to quickly charge the MOSFET input capacitance to the start of the Miller region, as drain-source voltage does not change during this period. Thereafter, the current

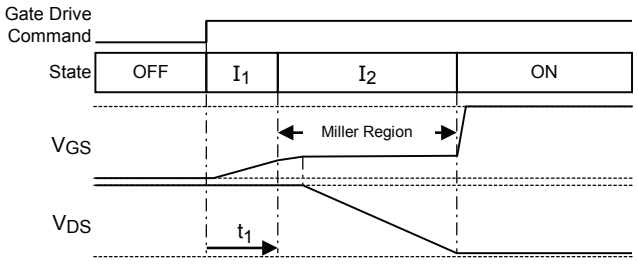


Figure 13a: Off-to-On Transition (Gate Drive Control)

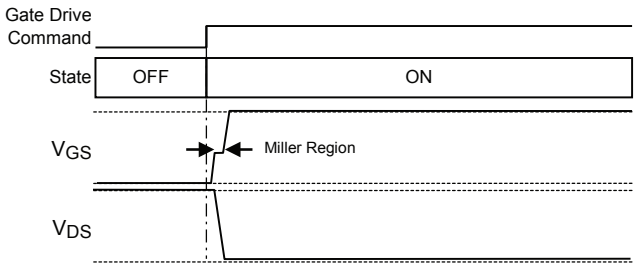


Figure 13b: Off-to-On Transition (Switched)

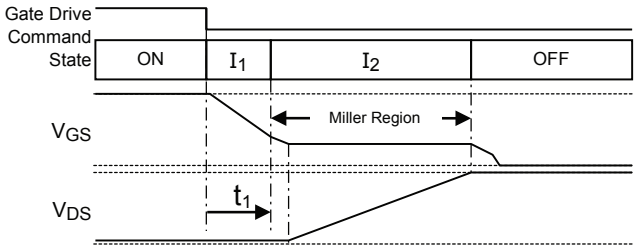


Figure 13c: On-to-Off Transition (Gate Drive Control)

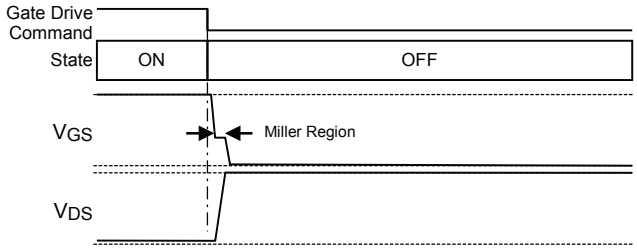


Figure 13d: On-to-Off Transition (Switched)

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

sourced on GHx is set to a value of I_2 (as defined by IHR2[3:0]) and remains at this value while the MOSFET transitions through the Miller region and reaches the fully on-state. For high-side gate drives, the MOSFET fully on-state is defined as the voltage on the GHx gate drive output rising to a value within 1 V(typ) of the Cx terminal. I_2 should be set to achieve the required rising time on the motor phase connection. Once in the fully on-state, the GHx output switches from current to voltage drive to hold the MOSFET in the on-state.

If the values of IHR1 and IHR2 are set to 0, GHx produces maximum drive to turn on the MOSFET as quickly as possible without attempting to control the input capacitance charge time (Figure 13b). The value of THR has no effect on switching speed.

Low-side off-to-on transitions are controlled in a similar manner by setting TLR[3:0], ILR1[3:0], and ILR2[3:0] to control GLx. For low-side gate drives, the MOSFET fully on-state is defined as the voltage on the GLx gate drive output rising to a value within 1 V(typ) of VREG. I_2 should be set to achieve the required falling slew time on the motor phase connection.

High-side on-to-off transitions are controlled as detailed in Figure 13c. When a gate drive is commanded to turn off, a current, I_1 (as defined by IHF1[3:0]), is sunk by the relevant GHx terminal for a duration, t_1 (defined by THF[3:0]). These parameters should typically be set to quickly discharge the MOSFET input capacitance to the start of the Miller region as drain-source voltage does not change during this period. Thereafter, the current sunk by GHx is set to a value of I_2 (as defined by IHF2[3:0]) and remains at this value while the MOSFET transitions through the Miller region and reaches the fully off-state. For high-side gate drives, the MOSFET fully off-state is defined as the voltage on the GHx gate drive output falling to a value within 1 V(typ) of the Sx terminal. I_2 should be set to achieve the required falling slew time on the motor phase connection. Once in the fully off condition, the GHx output switches from current to voltage drive to hold the MOSFET in the off-state.

If the values of IHF1 and IHF2 are set to 0, GHx produces maximum drive to turn off the MOSFET as quickly as possible without attempting to control the input capacitance discharge time (Figure 13d). The value of THF has no effect on switching speed.

Low-side on-to-off transitions are controlled in a similar manner by setting TLF[3:0], ILF1[3:0] and ILF2[3:0] to control GLx. For low-side gate drives the MOSFET fully off-state is defined as the voltage on the GLx gate drive output falling to a value within 1 V(typ) of LSSx. I_2 should be set to achieve the required rising slew time on the motor phase connection.

If non-zero values of I_1 and I_2 are selected a long enough value of dead time must be set to ensure that any MOSFET turning off, fully transitions to the off-state before the complementary MOSFET in the same phase is allowed to start turning on. Gate drive control is active regardless of the set value of dead time.

Logic Control Inputs

Six logic level digital inputs, HA, LA, HB, LB, HC, LC, provide direct control for the gate drives, one for each drive. The Hx inputs correspond to the high-side drives, and the Lx inputs correspond to the low-side drives. All logic inputs are standard CMOS levels referenced to the voltage of the logic I/O supply, V_{IO}. Logic inputs have a typical hysteresis of 500 mV to improve noise performance. Each of the six gate control inputs can be shorted to the VBB supply, up to the absolute maximum supply voltage, without damage to the input.

The operation of the inputs is shown in Table 1: Control Logic Table. A pull-down resistor is connected to each input to ensure a safe state if the control becomes disconnected.

The gate drive outputs can also be controlled through the serial interface by setting the appropriate bit in the control register. In the control register, all bits are active high. The logical relationship between the register bit setting and the gate drive outputs is defined in Table 2.

The logic inputs are combined, using logical OR, with the corresponding bits in the serial interface control register, to determine the state of the gate drive. The logical relationship between the combination of logic input and register bit setting and the gate drive outputs is defined in Table 3. In most applications, either the logic inputs or the serial control will be used. When using only the logic inputs to control the bridge, the serial register should be left in the reset condition with all control bits set to 0. When using only the serial interface to control the bridge, the inputs should be connected to GND. The internal pull-down resistors on these inputs then ensure that they go to the inactive state should they become disconnected from the control signal level.

Internal lockout logic ensures that the high-side gate drive output and low-side gate drive output on the same phase cannot be active (high) simultaneously If the control inputs request both the high-side and the low-side gate drives to be active at the same time, then both high-side and low-side gate drives are switched into the inactive (low) state.

Output Enable / Disable

The ENABLE input is connected directly to the gate drive output command signal, bypassing the main synchronous logic block on the chip (including all phase control logic). This input can be used to provide a fast output disable (emergency cut-off) or to

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

provide non-synchronous fast decay PWM.

Pulsing ENABLE low for a duration equal to the reset pulse width, t_{RST} with the GTS bit in the Config 0 register is set to 1 clears any faults, sets the general fault flag on DIAG high, and re-enables any gate drives that have been disabled as a result of fault conditions (Table 6). All device registers retain their values during and after ENABLE pulses of duration t_{RST}.

Sleep Mode

The AMT49106 provides a low-power sleep state where the consumption from the supply is reduced to a minimum by disabling all normal functions including the two charge pump regulators and all internal logic circuitry.

The AMT49106 is put into sleep mode by setting the GTS bit in the Config 0 register to 1 and pulling the ENABLE terminal low. If the GTS bit is set to 0, sleep mode will be inactive regardless of the ENABLE terminal state. To minimize quiescent supply current consumption in sleep mode, the ENABLE, SDI, and SCK terminals must be held within 300 mV of ground.

Sleep mode can be initiated by first setting ENABLE low and then setting the GTS bit to 1 or by first setting the GTS bit to 1 and then taking ENABLE low. All gate drive outputs are disabled, and quiescent current begins to decay toward the specified sleep mode limits within a Reset Shutdown Time, t_{RSD}, of both conditions being satisfied.

The AMT49106 wakes from sleep when a low-to-high transition is applied to the ENABLE terminal. When exiting sleep mode, all configuration and control registers are reset to the default values programmed into the device non-volatile memory. All fault states are cleared and all fault bits in the diagnostic and status registers are set to 0 with the following exceptions. First, the POR and FF bits are set in the Status register to indicate that the part has been in sleep mode. Second, the VRU, VCPU, and VR bits may be set as the voltages on the VREG and VCP terminals rise relatively slowly and may not exceed their associated undervoltage thresholds prior to the fault detection mechanisms within the part becoming active. V_{REG} and V_{CP} will rise to their respective regulation levels within a Wake From Sleep period, t_{EN}, with C_{REG} as defined in the Electrical Characteristics table (22 µF).

At initial power up (V_{IO} applied to the device), the AMT49106 will be in sleep mode if ENABLE is low or in active mode if ENABLE is high.

Logic Outputs

Any current sourced from the SDO output into an external load must be provided by the supply connected to the VIO pin in addition to the VIO quiescent current specified in the Electrical Characteristics table. The SDO pin may be shorted to ground without interfering with the operation of other device functions. In this condition, the maximum current that may be sourced is defined by the Output Short Circuit Current SDO parameter, I_{OSC}, in the Electrical Characteristics table. The DIAG output has an open drain configuration and does not internally draw current from VIO.

Current Sense Amplifiers

Three programmable-gain differential sense amplifiers are provided to allow the use of a low value sense resistor or current shunt as a current sensing element in the low-side connection of each phase. The input common mode range of the CSxP and CSxM inputs allows below ground current sensing typically required for low-side current sense in PWM control of motors, or other inductive loads, during switching transients. The output of the sense amplifier is available at the CSxO outputs and can be used in peak or average current control systems.

The internal supply for the output stage of each amplifier is provided by the external supply connected to the OOR terminal. The output can drive up to V_{OOR} – 0.3 V to achieve good dynamic range with higher input voltage A-to-D converters.

The output signal from each amplifier is driven with respect to the output offset voltage, V_{OOS}, as defined in Figure 2. V_{OOS} is nominally half of V_{OOR}, the external voltage applied to the OOR terminal as detailed in Figure 3. The accuracy with which V_{OOS} is related to V_{OOR} is defined by the Output Offset Ratio parameter, A_{OO}, in the Electrical Characteristics table.

The supply connected to the OOR pin must provide the bias currents for the three amplifier output stages plus any currents that the amplifiers might source into external loads. The maximum combined bias current for all three amplifiers is defined by the Output Offset Reference Input Current parameter, I_{OOR}, in the Electrical Characteristics table. The operational load current sourced by each amplifier is defined by the amplifier output voltage and external load impedance. The current that each amplifier may source under abnormal load conditions is defined by the Output Current Source parameter in the Electrical Characteristics table.

V_{BB} must be present for the sense amplifiers to be operational. If V_{BB} drops below the VBB undervoltage threshold, V_{BBUV}, each amplifier output will be disabled and pulled to ground by a resistance of no more than 500 Ω. The amplifier outputs will be re-enabled when V_{BB} rises above the VBB undervoltage threshold plus hysteresis, $V_{BBUV} + V_{BBUVHys}$.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

The gain, A_V, of each sense amplifier is independently programmable and defined by the contents of the S1G[2:0], S2G[2:0] and S3G[2:0] variables as:

SxG	Gain
0	7.5
1	10
2	12.5
3	15

SxG	Gain
4	17.5
5	20
6	22.5
7	25

Current sense amplifier calibration minimizes Input Offset Voltage, V_{IOS}, and is initiated via the serial interface. Unless calibrated, input offset voltage may exceed the limits detailed in the Electrical Characteristics table. Calibration is not required to achieve the specified Input Offset Voltage Drift Over Temperature, ΔV_{IOS}, and leaves this parameter unaltered.

Amplifiers are calibrated by writing a 1 to the appropriate SxC bit. If an SxC bit is already set to 1, it must first be cleared to 0 before writing 1, otherwise a calibration cycle will not take place. Before initiating a calibration, the relevant positive and negative amplifier input terminals (CSxP and CSxM) must be held at the same potential by ensuring that no current is flowing in the associated sense resistor and this condition must be maintained until the calibration operation is complete. Calibration starts on the STRn rising edge associated with writing 1 to the SxC bit and is completed within an Offset Calibration Time, t_{Cal}, from this point. After a calibration, the amplifier automatically reverts to normal operating mode. More than one amplifier may be calibrated simultanously by setting multiple SxC bits on a given serial interface write cycle. The calibration of one amplifier should not be initiated if the calibration of any other is in progress as the accuracy of both operations may be reduced. During calibration transient voltage variations may be observed on the CSxO terminals.

For higher accuracy it is possible to output the sense amplifier output offset on each sense amp output by setting the YOL bit (on-state open-load verification function) to 1. This internally shorts the sense amplifier input to the offset adder to zero resulting in only the output offset at each sense amplifier. If the offset is then sampled, it can be used to mathematically remove the offset from the current sense signal.

Diagnostic Monitors

Multiple diagnostic features provide three levels of fault monitoring. These include critical protection for the AMT49106, monitors for operational voltages and states, and detection of power bridge and load fault conditions. All diagnostics, except for POR, serial transfer error, EEPROM fault, and overtemperature can be masked by setting the appropriate bits in the configuration or mask registers.

Except for the three phase state monitors, the fault status is available from two sources: the DIAG output terminal, and the Diagnostic and Status registers accessed through the serial interface.

Table 5: Diagnostic Functions

Name	Diagnostic	Level
POR	Internal logic supply undervoltage causing power-on reset	Chip
OT	Chip junction overtemperature	Chip
SE	Serial transmission error or system error	Chip
EE	EEPROM error	Chip
TW	High chip junction temperature warning	Monitor
VSO	VBB supply overvoltage (load dump detection)	Monitor
VSU	VBB supply undervoltage	Monitor
VLO	Logic terminal overvoltage	Monitor
QTO	Q&A watchdog timeout	Monitor
QAE	Q&A watchdog answer error	Monitor
VRO	VREG output overvoltage	Monitor
VRU	VREG output undervoltage	Monitor
VCPU	VCP undervoltage	Monitor
VDU	VIO or VOOR undervoltage	Monitor
VDO	VIO or VOOR overvoltage	Monitor
AHU	A high-side V_{GS} undervoltage	Monitor
ALU	A low-side V_{GS} undervoltage	Monitor
BHU	B high-side V_{GS} undervoltage	Monitor
BLU	B Low-side V_{GS} undervoltage	Monitor
CHU	C high-side V_{GS} undervoltage	Monitor
CLU	C Low-side V_{GS} undervoltage	Monitor
LAD	LSSA disconnect	Monitor
LBD	LSSB disconnect	Monitor
LCD	LSSC disconnect	Monitor
OC1	Overcurrent on sense amp 1	Bridge
OC2	Overcurrent on sense amp 2	Bridge
OC3	Overcurrent on sense amp 3	Bridge
OL	Open-load	Bridge
VA	Bootstrap undervoltage phase A	Bridge
VB	Bootstrap undervoltage phase B	Bridge
VC	Bootstrap undervoltage phase C	Bridge
AHO	Phase A high-side V_{DS} overvoltage	Bridge
ALO	Phase A low-side V_{DS} overvoltage	Bridge
BHO	Phase B high-side V_{DS} overvoltage	Bridge
BLO	Phase B low-side V_{DS} overvoltage	Bridge
CHO	Phase C high-side V_{DS} overvoltage	Bridge
CLO	Phase C low-side V_{DS} overvoltage	Bridge

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

DIAG Diagnostic Output

The DIAG terminal is a single diagnostic output signal that can be programmed by setting the contents of the DG[1:0] variable through the serial interface to provide one of four dedicated diagnostic signals:

DG = 0 – a general fault flag

DG = 1 – a pulsed fault flag

DG = 2 – a voltage representing the temperature of the internal silicon

DG = 3 – a clock signal derived from the internal chip clock

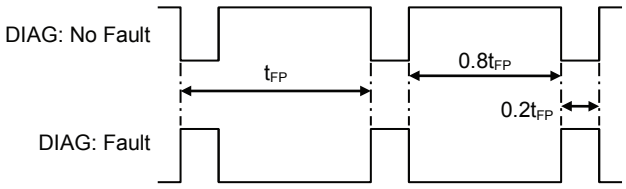


Figure 14: DIAG – Pulsed Output Mode

At power-up, or after a power-on-reset, the DIAG terminal outputs a general logic-level fault flag which will be active-low if a fault is present. This fault flag remains low while the fault is present or if one of the latched faults has been detected and the outputs disabled. When the general fault flag is reset, the DIAG output will be high.

The pulsed fault output option provides a continuous, low frequency, low-duty cycle pulsed output when a fault is present or if one of the latched faults has been detected and the outputs disabled. When the general fault flag is reset and no fault is present, the signal output on the DIAG terminal is a continuous low frequency, high-duty cycle pulse train. The period of the DIAG signal in pulsed mode is defined by t_{FP} and is typically 100 ms. The two duty cycles are defined by D_{FP} and are typically 20% when a fault is present and 80% when no fault is present.

The temperature output option provides access to the internal voltage representing the surface temperature of the silicon. Temperature may be approximated from this voltage as:

$$T_J \approx (V_{DIAG} - V_{TJD}) / A_{TJD}$$

where T_J is the approximate silicon temperature in ºC, V_{DIAG} is the analog voltage on the DIAG terminal in mV, and V_{TJD} and A_{TJD} are the typical range and slope values presented in the Electrical Characteristics table.

The circuit that generates the temperature output is powered from the V_{IO} supply. Any load current drawn from the DIAG terminal when DG = 2 must be provided by the supply connected to the VIO pin. The maximum drive capability of the temperature output, I_{TJSO}, is specified in the Electrical Characteristics table.

The clock output option provides a logic-level square wave output at a ratio of the internal clock frequency to allow more precise calibration of the timing settings if required.

All digital outputs available on DIAG (DG set to 0, 1, or 3) are open drain. On-state drive capability and off-state leakage current limits are defined in the Electrical Characteristics table by the V_{OL} and I_{ODI} parameters respectively and may be used to calculate a suitable pull-up resistance. In most applications, a resistor in the range 10 to 20 kΩ is acceptable.

Diagnostic Registers

The serial interface allows detailed diagnostic information to be read from the diagnostic registers on the SDO output terminal at any time.

A system status register provides a summary of all faults in a single read transaction. The status register is always output on SDO when any register is written.

The first bit (bit 15) of the status register contains a fault flag, FF, which will be high if any of the fault bits in the Status register have been set. This allows fault condition to be detected using the serial interface by simply taking STRn low. As soon as STRn goes low, the first bit in the status register can be read on SDO to determine if a fault has been detected at any time since the last fault register reset. In all cases, the fault bits in the diagnostic registers are latched and only cleared after a diagnostic register reset when DSR = 0.

Note that FF (bit 15) does not provide the same function as the general fault flag output on the DIAG terminal when STRn is high and the DIAG output is in its default mode. The fault output on the DIAG terminal provides an indication that either a fault is present or the outputs have been disabled due to a latched fault state. FF provides an indication that a fault has occurred since the last fault reset and one or more fault bits have been set.

Chip-Level Protection

Chip-wide parameters critical for correct operation of the AMT49106 are monitored. These include maximum chip temperature, minimum internal logic supply voltage, and serial interface transmission. These three monitors are necessary to ensure that the AMT49106 can respond as specified.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Chip Fault State: Internal Logic Undervoltage (POR)

The AMT49106 has an independent integrated low dropout regulator to supply the core logic from the applied 3.3 V or 5 V VIO logic supply. This allows digital functions within the part including the serial interface to operate even if the V_{BB} supply drops to a very low value due to a severe cold crank event or fault condition.

Correct logic operation is guaranteed by a power-on-reset (POR) circuit which shuts down the part if the logic supply voltage, V_{IO}, drops too low. This lockout mechanism is essential in all circumstances and cannot be masked.

When V_{IO} is applied to the AMT49106, the internal logic is prevented from operating until the VIO POR voltage (rising) threshold, V_{PORON}, is exceeded. At this point, all serial control registers are set to their power-on state and all fault states are clear, except for the FF and POR bits in the Status register, which are set to indicate that a power-on-reset has taken place. Other Diagnostic and Status register bits including V_{IO}, V_{OOR}, V_{REG}, V_{CP}, and V_{BB} undervoltages, may immediately then be set as a result of startup conditions within the part. It is recommended that the Diagnostic and Status registers are read after V_{IO}, V_{OOR}, V_{REG}, V_{CP}, and V_{BB} have settled within their respective operational ranges to clear any fault indications of this type. In addition, the gate drive outputs are held in the off-state for 10 ms immediately after coming out of POR.

Once the AMT49106 is operational, the applied logic supply voltage, V_{IO}, continues to be monitored. If it drops below the VIO POR voltage (falling) threshold, V_{POROFF}, the logical function of the AMT49106 cannot be guaranteed and the part will enter a power-down state. If the logic supply undervoltage is a transient event, then the AMT49106 will follow the power-up sequence above as the voltage rises.

If an internal logic undervoltage (POR) condition is present, all gate drive outputs will be disabled.

Chip Fault State: Overtemperature

If the chip temperature rises above the overtemperature threshold, T_{JF}, the overtemperature bit, OT, will be set in the Status register, the general fault flag will be set, and if FOT = 1, all gate drive outputs will be disabled. When the temperature drops below T_{JF} by more than the hysteresis value, T_{JFhys}, the fault will be reset and the gate drive outputs will be enabled, but the overtemperature bit remains in the Status register until reset. If FOT = 0, fault reporting will be the same, but the gate drive outputs are not disabled and action must be taken by the user to limit the power dissipation in some way to prevent overtemperature damage to the chip and unpredictable device operation. When the temperature drops below T_{JF} by more than the hysteresis value, T_{JFhys}, the general fault flag will be reset but the overtemperature bit remains in the Status register until reset.

Chip Fault State: Serial Error

The data transfer into the AMT49106 through the serial interface is monitored for two fault conditions: transfer length and parity. A transfer length fault is detected if there are more than 16 rising edges on SCK or if STRn goes high and there have been fewer than 16 rising edges on SCK. A parity fault is detected if the total number of logic 1 states in the 16-bit transfer is an even number. In both cases, the write will be cancelled without writing data to the registers. In addition, the status register will not be reset, and the FF bit and SE bit will be set to indicate a data transfer error. If the transfer is a diagnostic or verification result read, then the addressed register will not be reset.

If a serial error is detected and FSE = 1, then all gate drive outputs will be driven low (disabled). If FSE = 0, no further action will be taken.

Chip Fault State: EEPROM

Configuration and calibration information is stored within internal EEPROM and loaded into working registers to configure the device at power up. As part of this process, a data integrity check is carried out. If the check returns a single bit error, automatic error correction is applied, and the part starts up. If the check returns a multiple bit error, all gate drives are disabled, the general fault flag is set low, and the EEPROM error bit, EE, is set in the Status register. EEPROM faults can only be cleared by a power-on-reset (POR).

Operational Monitors

Parameters related to the safe operation of the AMT49106 in a system are monitored. These include parameters associated with external active and passive components, power supplies, and interaction with external controllers. In addition, the Q&A watchdog timer is available to verify continued operation of the external controller.

Voltages relating to driving the external power MOSFETs are monitored, specifically V_{REG}, V_{VCP}, each bootstrap capacitor voltage, and the V_{GS} of each gate drive output. The main supply voltage, V_{BB}, is monitored for overvoltage and undervoltage events.

The battery-compliant logic inputs are capable of being shorted to

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

the main supply voltage without damage, but any high voltage on these terminals (excluding ENABLE) will be detected.

Monitor: VREG Undervoltage and Overvoltage

The internal VREG charge-pump regulator supplies the low-side gate driver and the bootstrap charge current. It is critical to ensure that the regulated voltage, V_{REG}, at the VREG terminal is sufficiently high before enabling any of the gate drive outputs.

If VREG goes below the corresponding undervoltage threshold, V_{ROFF}, the VREG undervoltage bit, VRU, in the Diagnostic 1 register and the associated VR bit, in the Status register, will be set to 1. The general fault flag on the DIAG terminal will go low.

If a VREG undervoltage state is present and FVRU = 1, all gate drive outputs go low. When VREG rises above the rising threshold, V_{RON}, the fault is cleared, and if FVRU = 1, the gate drive outputs are re-enabled. The fault bit remains in the Diagnostic register until cleared. If FVRU = 0, fault reporting will be the same, but the gate drive outputs are not disabled, and appropriate action must be taken by the external controller to avoid potential misoperation or damage to the AMT49106 and/or bridge MOSFETs.

The VREG undervoltage monitor circuit is active during power up. If FVRU = 1, all gate drives will be low until V_{REG} is greater than V_{RON}. If FVRU = 0, the gate drive outputs will be active as soon as there is sufficient voltage on VREG to activate the gate drive outputs.

Note that this is sufficient to turn on standard threshold external power MOSFETs at a battery voltage as low as 4.5 V, but the on-resistance of the MOSFET may be higher than its specified maximum.

The VREG undervoltage monitor can be disabled by setting the VRU bit in the Mask 1 register. Although not recommended, setting VRU to 1 or setting FVRU to 0 can allow the AMT49106 to operate below its minimum specified supply voltage level with a severely impaired gate drive. The specified electrical parameters will not be valid in this condition.

The output of the VREG regulator is also monitored to detect any overvoltage applied to the VREG terminal.

If V_{REG} goes above the corresponding overvoltage threshold, V_{ROV}, the VREG overvoltage bit VRO in the Diagnostic 1 register and the associated VR bit in the Status register will be set to 1. The general fault flag on the DIAG terminal will go low. If FVRO = 1, all gate drive outputs go low, the motor drive is disabled, and the motor coasts. If FVRO = 0, no action is taken, and the gate drive outputs are protected from overvoltage by independent Zener clamps. When V_{REG} falls below V_{ROV} by more than the hysteresis voltage, V_{ROVHys}, the fault is cleared but the VRO bit remains in the Diagnostic 1 register until reset. If the outputs have been disabled, because FVRO = 1 they are re-enabled.

Monitor: VCP Undervoltage

The external voltage on the VCP terminal with respect to VBB, identified as V_{CP}, is monitored.

When V_{CP} goes below the VCP undervoltage threshold, V_{CPUV}, then the VCP undervoltage bit, VCPU, is set in the Diagnostic 0 register. The DIAG terminal immediately indicates a fault when the VCP undervoltage is detected and will stop indicating a fault as soon as the voltage rises above $V_{CPUV} + V_{CPUVHys}$. The VCPU bit will remain until cleared.

In addition, if FCPU = 1, the gate outputs will be disabled when the fault is detected. If FCPU = 0, then AMT49106 will not take any action except setting VCPU and indicating the fault on the DIAG terminal.

Monitor: Temperature Warning

If the chip temperature rises above the temperature warning threshold, T_{JW}, the hot warning bit, TW, will be set in the Status register, and if FTW = 1, all gate drives will be low. If FTW = 0, gate drives will remain active. When the temperature drops below T_{JW} by more than the hysteresis value, T_{JWHys}, the fault is reset and if FTW = 1, the outputs are re-enabled. The TW bit remains in the Status register until reset.

Monitor: VBB Supply Overvoltage and Undervoltage

The analog supply to the AMT49106 on the VBB terminal, V_{BB}, is monitored to indicate if the supply voltage has exceeded its normal operating range (for example, during a load dump event). If V_{BB} rises above the VBB overvoltage warning threshold, V_{BBOV}, then the VSO bit will be set in the Diagnostic 2 register, the VS bit (which indicates the logical OR of VSO and VSU) will be set in the Status register, and if FVSO = 1, all gate drive outputs will be driven low (disabled). When V_{BB} drops below the falling VBB overvoltage warning threshold, $V_{BBOV} - V_{BBOVHys}$, the fault will be cleared and the gate drive outputs will be re enabled, but the VSO and VS bits will remain set until the Diagnostic 2 register is read with DSR = 0. If FVSO = 0, fault reporting will be the same, but the gate drive outputs will not be disabled.

If V_{BB} falls below the VBB undervoltage warning threshold, V_{BBUV}, the VSU bit will be set in the Diagnostic 2 register, the VS bit (which indicates the logical OR of VSO and VSU) will be

ALLEGRO microsystems
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

set in the Status register, and if FVSU = 1, all gate drive outputs will be driven low (disabled). When V_{BB} rises above the rising VBB undervoltage threshold, $V_{BBUV} + V_{BBUVHys}$, the fault will be cleared and the gate drive outputs will be re-enabled, but the VSU and VS bits will remain set until the Diagnostic 2 register is read with DSR = 0. If FVSU = 0, fault reporting will be the same, but the gate drive outputs will not be disabled.

Monitor: VIO Undervoltage and Overvoltage

The logic voltage input, V_{IO}, is monitored to ensure that the logic interface voltage is within the appropriate range to permit correct operation of the logic input/output buffers.

If V_{IO} drops below the logic undervoltage falling threshold, $V_{IOULOFF}$, the DIAG terminal indicates a fault and the VIO and VOOR undervoltage bit, VDU, is set in the Diagnostic 0 register. In addition, if FVDD = 1, all gate drive outputs will go low.

If V_{IO} rises above the logic overvoltage rising threshold, $V_{IOOLOFF}$, the DIAG terminal indicates a fault and the VIO and VOOR overvoltage bit, VDO, is set in the Diagnostic 0 register. In addition, if FVDD = 1, all gate drive outputs will go low.

If FVDD = 0 when VIO drops below the undervoltage falling threshold or rises above the overvoltage rising threshold, fault reporting will be the same, but the gate drive outputs will not be disabled.

If FVDD = 1 (the power-up default state) when V_{IO} rises above the logic undervoltage rising threshold, V_{IOULON}, the gate drive output will remain low for 10 ms. After this timeout, the gate drive outputs will revert to the commanded state.

The logic undervoltage and overvoltage thresholds are set to values appropriate for 3.3 V or 5 V logic supplies by setting the VLM bit in the Config 6 register to 0 or 1 respectively. The relevant thresholds are listed in the Electrical Characteristics table.

If operating with the VLM bit set to 0 (3.3 V compatible thresholds), the AMT49106 may or may not indicate a logic terminal undervoltage fault (VDU bit set) after coming out of the VIO POR state. If it does, this should be cleared by reading the Diagnostic 0 register as part of device initialization. Similarly, if VLM is set to 0 and V_{IO} falls from its normal operating range to a value below the VIO POR voltage (falling) threshold, a logic terminal undervoltage may or may not be indicated (VDU bit set) prior to the part entering the POR (power down) state. These behaviors arise because the VIO POR voltage and logic undervoltage threshold ranges overlap if the VLM bit is set to 0. If operating with the VLM bit set to 1, the VIO POR voltage and logic undervoltage thresholds are distinct. Logic terminal undervoltage faults will always be indicated after exiting VIO POR (power up) and prior to entering VIO POR (power down).

Monitor: VOOR Undervoltage and Overvoltage

The output offset reference voltage, V_{OOR}, is monitored to ensure that it is within an appropriate range for amplifier operation.

If V_{OOR} drops below the VOOR undervoltage falling threshold, $V_{ORULOFF}$, the DIAG terminal indicates a fault and the VIO and VOOR undervoltage bit, VDU, is set in the Diagnostic 0 register. In addition, if FVDD = 1, all gate drive outputs will go low.

If V_{OOR} rises above the VOOR overvoltage rising threshold, $V_{OROLOFF}$, the DIAG terminal indicates a fault and the VIO and VOOR overvoltage bit, VDO, is set in the Diagnostic 0 register. In addition, if FVDD = 1, all gate drive outputs will go low.

If FVDD = 0 when V_{OOR} drops below the undervoltage falling threshold or rises above the overvoltage rising threshold, fault reporting will be the same, but the gate drive outputs will not be disabled.

If FVDD = 1 (the power up default state) when V_{OOR} rises above the VOOR undervoltage rising threshold, V_{ORULON}, the gate drive output will remain low for 10 ms. After this timeout, the gate drive outputs will revert to the commanded state.

The VOOR undervoltage and overvoltage thresholds are set to values appropriate for 3.3 V or 5 V logic supplies by setting the VLR bit in the Config 6 register to 0 or 1 respectively. The relevant thresholds are listed in the Electrical Characteristics table.

Monitor: VGS Undervoltage

To ensure that the gate drive output is operating correctly, each gate drive output voltage is independently monitored, when active, to ensure the gate-source drive voltage, V_{GS}, is sufficient to fully enhance the power MOSFET in the external bridge.

If the V_{GS} on any active gate drive output is lower than the corresponding undervoltage warning threshold, V_{GSHUV} for the high-side and V_{GSLUV} for the low-side, the relevant VGS undervoltage bit, AHU, ALU, BHU, BLU, CHU, or CLU, in the Diagnostic 0 register and the associated GSU bit in the Status register, will be set to 1. The general fault flag on the DIAG terminal will go low.

If FGSU = 1, all gate drive outputs will be inactive (low). The gate drive outputs will remain inactive (low) until the fault state and the general fault flag are reset by a serial read of the Diagnostic 0 register when DSR = 0, or by a power-on reset. The gate

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

drive undervoltage bits, AHU, ALU, BHU, BLU, CHU, or CLU will be reset by a serial read of the Diagnostic 0 register when DSR = 0, or by a power-on reset. Clearing the gate drive undervoltage bits in the Diagnostic 0 register, also clears the GSU bit in the Status register. If FGSU = 0, fault reporting will be the same, but the gate drive outputs will not be disabled.

For high-side VGS comparators, the V_{GSHUV} thresholds are set 1 V(typ) below the voltage on the corresponding CX terminal, and for low-side gate comparators, the V_{GSLUV} thresholds are set 1 V(typ) below V_{REG}.

The output from each VGS undervoltage comparator is filtered by a VGS fault qualifier circuit. This circuit uses a timer to verify that the output from the comparator is indicating a valid VGS fault. The duration of the VGS fault qualifying timer, t_{VDQ}, is determined by the contents of the TVD[5:0] variable. t_{VDQ} is approximately defined as:

$$t_{VDQ} = n \times 100\ ns$$

where n is a positive integer defined by TVD[5:0].

The qualifier can operate in one of two ways: debounce mode or blanking mode, selected by the VDQ bit.

In debounce mode (the default setting), a timer is started each time the comparator output indicates a VGS fault detection when the corresponding MOSFET is active. This timer is reset when the comparator changes back to indicate V_{GS} is within 1 V of the voltage on the Cx terminal (high-side gate drives) or V_{REG} (low-side gate drives). If the debounce timer reaches the end of the timeout period, set by t_{VDQ}, then the VGS fault is considered valid and the AMT49106 follows the fault action described above.

In blanking mode (optional), a timer is started when any gate drive is turned on or turned off. The outputs from the VGS undervoltage comparators for all MOSFETs are ignored (blanked) for the duration of the timer's active period, set by t_{VDQ}. If any gate drive changes state while a blanking period is in progress, the timer is re-triggered, resulting in an extended overall blanking time. If any comparator output indicates a VGS fault and the blanking timer is not active, then the VGS fault is considered valid and the AMT49106 follows the fault action described above.

The VDQ and TVD[5:0] qualifier parameters apply to both the VGS undervoltage and VDS overvoltage monitors.

Monitor: LSS Disconnect

Each LSS terminal includes a continuous current source, I_{LU}, biased from V_{REG}, that will pull the LSS terminal up if there is no low impedance path from LSS to ground.

If FLSS = 1 and the voltage with respect to ground at any LSS terminal rises above the LSS disconnect threshold, V_{LSD}, then the general fault flag will become active and the relevant LxD bit will be set in the Verify Result 0 register. Additionally, the corresponding low-side VDS fault bit, xLO, will be set in the Diagnostic 1 register, the DSO bit will be set in the Status register and all gate drive outputs will be disabled. When the voltage on the LSS terminal falls below the falling LSS disconnect threshold voltage, $V_{LSD} - V_{LSDHys}$, no action is taken. If the Verify Result 0 register is subsequently read, the LxD bit is cleared. The xLO and DSO bits and the general fault flag may then be cleared by reading the Diagnostic 1 register. If the Diagnostic 1 register is read before the Verify Result 0 register, the xLO and DSO bits are cleared and then immediately set again.

If FLSS = 0 and the voltage with respect to ground at any LSS terminal rises above the LSS disconnect threshold, V_{LSD}, then the relevant LxD bit will be set in the Verify Result 0 register. The general fault flag and VDS fault bits will not be set. When the voltage at the LSS terminal falls below the falling LSS disconnect threshold voltage, $V_{LSD} - V_{LSDHys}$, no action is taken. If the Verify Result 0 register is subsequently read, the LxD bit is cleared.

Monitor: Logic Terminal Overvoltage

Eight of the logic terminals are capable of being shorted to the main supply voltage, up to 50 V, without damage: HA, LA, HB, LB, HC, LC, ENABLE, and DIAG.

The voltages on the HA, LA, HB, LB, HC, and LC terminals are monitored to provide an indication of an input short-to-battery fault. If the voltage on any of the terminals rises above the logic input overvoltage warning threshold, V_{LOV}, then the general fault flag is set to active, the VLO bit is set in the Status register, and if FVLO = 1, all gate drive outputs are disabled. When the voltage on all terminals falls below the logic input overvoltage warning threshold, V_{LOV}, the general fault flag is reset and the outputs are re-activated. The VLO bit remains in the Status register until reset. If FVLO = 0, fault reporting will be the same, but the gate drive outputs will not be disabled.

If the voltage on the ENABLE terminal exceeds the overvoltage warning threshold, V_{LOV}, then the general fault flag remains inactive, the VLO bit is not set in the Status register, and all gate drive outputs remain enabled. This allows this terminal to be

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

permanently tied to VBB if required.

If the voltage on the DIAG terminal exceeds the overvoltage warning threshold, V_{LOV}, then the general fault flag remains inactive but the VLO bit is set in the Status register. All gate drive outputs remain enabled. Maintaining the general fault flag in the inactive state avoids the voltage contention that would otherwise arise on the DIAG pin (the high fault voltage working against the DIAG output attempting to drive to logic low).

Monitor: Q&A Watchdog Timeout

A Q&A watchdog using the serial interface is available to provide a monitor function for the external controller activity.

There are three modes of operation: Bridge Disable, Q&A Watchdog active, and Q&A Watchdog inactive. When the mode is set to Bridge Disable, the gate drive outputs are permanently driven low and do not respond to any commands to switch high. When the mode is set to Q&A Watchdog inactive, the gate drive outputs are active and respond to gate drive commands. In this mode, the Q&A Watchdog is not operating and does not cause any faults.

Following a power-on-reset, the AMT49106 is held in the Bridge Disable mode. The gate drive outputs are held low to avoid incorrect driving of any load attached to the bridge. To enable the bridge, the watchdog mode must be set to Q&A Watchdog active or Q&A Watchdog inactive. When set to Q&A Watchdog inactive mode, no further action is required to fully enable and command the gate drive outputs.

The Q&A Watchdog mode is changed by entering a sequence of three words into the WDM[7:0] variable in serial register 17 as described below. The present mode state can be determined by reading WDM.

Q&A Watchdog Active Mode

To enter Q&A Watchdog active mode, an uninterrupted sequence of three specific words must be written to WDM through the serial interface. The three words to change the mode are identified as SEQ0 (=0xA1), SEQ1 (=0x78) and SEQ2 (=0x98) in the Serial Register Reference section under Register 17.

To enter Q&A Watchdog active mode, SEQ0, SEQ1, and SEQ2 must be written in that sequence to register 17. When the last word is transferred, the Q&A watchdog timer is immediately active. If the three-word sequence is incorrect or interrupted by another serial communication frame, then the mode change command is ignored. The full mode change command sequence needs to be resent from the start. The presently configured watchdog mode can be determined by reading WDM. If the Q&A Watchdog

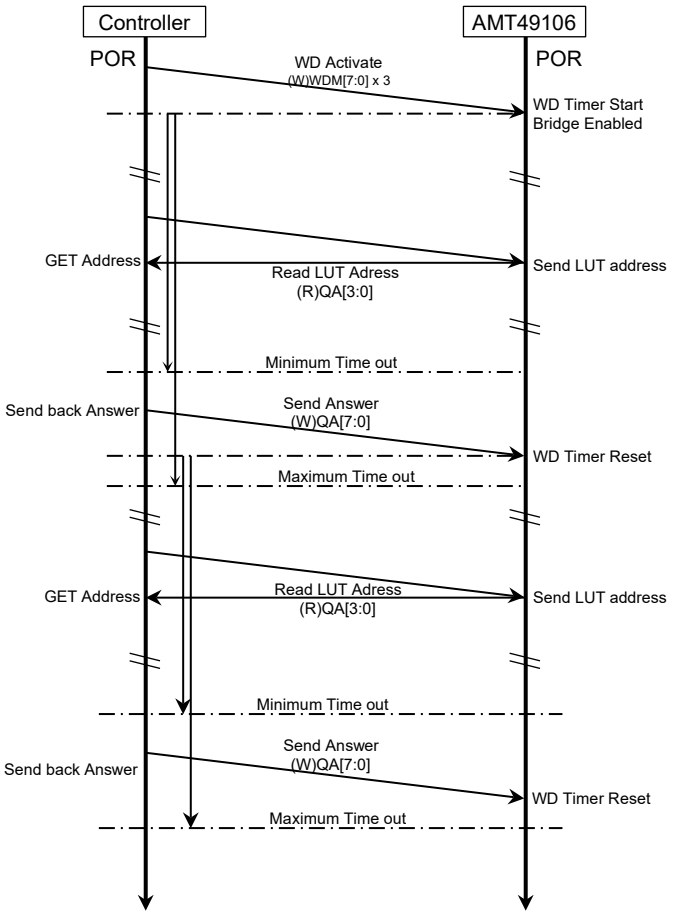


Figure 15: Q&A Communication Sequence

active mode is the presently configured mode, the value in WDM will be 0x55. The read value of WDM for each mode is described in Serial Register Reference Section under register 17.

The Q&A sequence starts with the external controller reading a Q&A look-up table (LUT) address, QA[7:0] from the Q&A Watchdog register, register 16. The LUT address is generated by the AMT49106. The controller must use this address to select the required response. This response must then be written back to the Q&A Watchdog register within a defined time window to pass the Q&A watchdog check. This sequence then continues until the AMT49106 is powered down, put to sleep, a watchdog fault occurs, or the microcontroller sets the Q&A watchdog mode to Bridge Disable or Q&A Watchdog inactive. The external controller can change the Q&A watchdog mode at any time.

The Q&A watchdog becomes active on the rising edge of the STRn input following a correct Q&A watchdog enable sequence

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

written to WDM. On this rising edge, the Q&A watchdog minimum and maximum timers are started and the LUT address is available by reading QA from register 16.

Once the Q&A watchdog timer is started, the external controller must first read the LUT address in QA from register 16, then wait until the end of the minimum timeout before writing the correct response back to QA. Writing the correct response must also be completed before the end of the maximum timeout. This sequence is shown in Figure 15.

The minimum and maximum timeouts, t_{QMI} and t_{QMA} respectively, are defined by the value in QAT[3:0] in register 13. Sixteen min/max timeout pairs are available from 0.1 ms / 0.2 ms to 20 ms / 40 ms. The maximum timeout is twice the minimum timeout.

Once the AMT49106 receives an answer from the external controller, the watchdog timers are restarted. If a response is not received before the end of the maximum timeout period, the watchdog timers are restarted at the end of that timeout.

The external controller can write to and read from all registers during Q&A watchdog active mode, with the exception of WDC[1:0] and QAT[3:0] in Register 13. The desired values of the Watchdog counter and timings must be set prior to entering Q&A watchdog active mode. Any commands to change these parameters will be ignored while in Q&A watchdog active mode. Adjusting the watchdog counter and timings is only possible in Q&A watchdog inactive or Bridge disable mode.

Every time a Q&A watchdog answer is received, the new Q&A watchdog LUT address is available to read from QA in register 16. Once the external controller reaches the last LUT address, the next available address will be the first in the sequence. The full look up table addresses along with the appropriate answers can be found in Serial Register Reference Section under Register 16.

If an incorrect response is written to QA, or a correct response is written to QA before the end of the minimum time or after the end of the maximum time, then the Q&A watchdog sequence will fail. A watchdog counter is provided to permit a number of Q&A watchdog sequence failures before reporting any fault or taking any action. Each time a Q&A watchdog sequence failure is detected, the watchdog counter is incremented. Each time a successful Q&A watchdog sequence takes place, the counter is decremented. This continues until the count exceeds the threshold set by the value in WDC[1:0] in register 13. If an incorrect answer is sent outside the permitted time window, the AMT49106 will recognise this as two separate failure events and the counter will be incremented by two. If a Q&A watchdog sequence failure is detected and the count is less than the threshold, then the watchdog timer is reset, and the watchdog sequence continues. If the watchdog failure count is greater than WDC, then a watchdog failure will be reported, and appropriate action will be taken. When a Q&A watchdog fault is reported, the watchdog timers are stopped until the fault is cleared. After that, the timers will reset immediately.

The AMT49106 will report a Q&A watchdog failure by setting one or both Q&A watchdog fault bits, QTO and QAE. The AMT49106 will report all faults that have occurred, not just the one that caused the counter to exceed the value set by WDC[1:0]. QTO indicates that a Q&A watchdog timeout has occurred and will be set when the Q&A response is received too early or too late. QAE indicates that an incorrect Q&A watchdog response has been received. Q&A watchdog faults will not be reported until the watchdog failure count is greater than WDC. If QTO or QAE is set, then the WD bit in the Status register will also be set and the DIAG terminal will indicate a fault. The QTO and QAE fault bits will remain set until cleared by reading the Verify Result 0 register. The WD bit will only be cleared when both QTO and QAE are cleared. The DIAG terminal will indicate a fault until WD is cleared.

The action taken when a Q&A watchdog failure is detected is determined by the FWD bit. When FWD is set to 1, the gate outputs will be driven low when the fault is detected. The outputs will become active when the fault is cleared. When FWD is set to 0, the gate outputs will remain active, the fault is still reported in the fault bits and on the DIAG terminal, but no action is taken.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Power Bridge and Load Faults

Bridge: Overcurrent Detect

Current sense amplifiers 1, 2, and 3 are fully independent and may be allocated to any phase (A, B, or C).

The output from each of the three sense amplifiers is fed into a comparator referenced to the overcurrent threshold voltage, V_{OCT}, to provide indication of overcurrent events. V_{OCT} is generated by a 4-bit DAC with a resolution of 150 mV and defined by the contents of the OCT[3:0] variable. V_{OCT} is approximately defined as:

$$V_{OCT} = (n + 1) \times 150\ mV$$

where n is a positive integer defined by OCT[3:0].

Any V_{OOS} offset programmed via the OOR terminal is applied to both the current sense amplifier output and the V_{OCT} threshold and has no effect on the overcurrent threshold, I_{OCT}. In effect, V_{CSD} is compared with V_{OCT} and the relationship between the threshold voltage and threshold current is given by:

$$I_{OCT} = V_{OCT} / (R_S \times A_V)$$

where V_{OCT} is the overcurrent threshold voltage programmed by OCT[3:0], I_{OCT} is the corresponding current value, R_S is the sense resistor value in Ω, and A_V is the sense amplifier gain defined by S1G, S2G, or S3G.

The output from each overcurrent comparator is filtered by an overcurrent qualifier circuit. This circuit uses a timer to verify that the output from comparator is indicating a valid overcurrent event. The qualifier can operate in one of two ways: debounce or blanking, selected by the OCQ bit.

In the default debounce mode, a timer is started each time a comparator output indicates an overcurrent detection. This timer is reset when the comparator changes back to indicate normal operation. If the debounce timer reaches the end of the timeout period, set by t_{OCQ}, then the overcurrent event is considered valid and the corresponding overcurrent bit (OC1, OC2, or OC3) will be set in the Diagnostic 2 register.

In the optional blanking mode, a timer is started when any gate drive is turned on. The output from all comparators is ignored (blanked) for the duration of the timeout period, set by t_{OCQ}. If a comparator output indicates an overcurrent event when the blanking timer is not active, then the overcurrent event is considered valid and the corresponding overcurrent bit (OC1, OC2, or OC3) will be set in the Diagnostic 2 register. If a gate drive is turned on while a timeout period is in progress, the timeout is extended to run for a period of t_{OCQ} from the new turn on event. If all gate drives are turned off during a timeout period, the timeout period is terminated.

The duration of the overcurrent qualifying timer, t_{OCQ}, is determined by the contents of the TOC[4:0] variable. t_{OCQ} is approximately defined as:

$$t_{OCQ} = n \times 500\ ns$$

where n is a positive integer defined by TOC[4:0].

When a valid overcurrent is detected with FOC = 1, the general fault flag is set, all gate drive outputs are driven inactive (low), and the corresponding OC1, OC2, and OC3 bits are set. The gate drive outputs will remain inactive (low) until the fault state and the general fault flag are reset by a serial read of the Diagnostic 2 register when DSR = 0, or by a power-on reset. The OC1, OC2, and OC3 bits will only be reset by a serial read of the Diagnostic 2 register when DSR = 0 or by a power-on reset.

If FOC = 0 and an overcurrent is detected, the general fault flag is not affected, the outputs remain active, and only the corresponding OC1, OC2, and OC3 bit is set.

Bridge: Open-Load Detect

Two open-load fault detection methods are provided: an on-state current monitor and an off-state open-load detector. An on-state is defined by the state of the gate drive outputs as one or two high-side MOSFETs switched on and one or two low-side MOSFETs switched on. The resulting combinations are the only ones where current can be passed through the low-side sense resistor. An off-state is defined by the state of the gate drive outputs as all MOSFETs switched off. In this state, the load connections are high impedance and can be used to detect the presence or otherwise of a load. Table 4 provides a listing of input combinations for each open-load detection mode.

On-State Open-Load Detection

On-state open-load detection is only active when AOL = 1, one or two high-side MOSFETs are switched on and one or two low-side MOSFETs are switched on. This excludes the cases where a high-side MOSFET and a low side MOSFET in the same phase are commanded to be on at the same time. Table 4 shows the open-load detection mode for each combination of output demand.

During the on-state, the AMT49106 compares the output from each sense amplifier against the open-load threshold voltage, V_{OLTH}. V_{OLTH} is generated by an internal DAC and is defined by the value in the OLT[3:0] variable. These bits provide the input to a 4-bit DAC with a least significant bit value of typically 25 mV.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

The output of the DAC produces V_{OLTH} approximately defined as:

$$V_{OLTH} = (n + 1) \times 25\ mV$$

where n is a positive integer defined by OLT[3:0].

Any V_{OOS} offset programmed via the OOR terminal is applied to both the current sense amplifier output and the V_{OLTH} threshold and has no effect on the open-load detect threshold current, I_{OLT}. In effect, V_{CSD} is compared with V_{OLTH}, and the relationship between the threshold voltage and threshold current is given by:

$$I_{OLT} = V_{OLTH} / (R_S \times A_V)$$

where V_{OLTH} is the open-load threshold voltage programmed by OLT[3:0], I_{OLT} is the corresponding current value, R_S is the sense resistor value in Ω, and A_V is the sense amplifier gain defined by S1G, S2G, or S3G.

If the output of all sense amplifiers is less than V_{OLTH} during the on-state, then a timer is allowed to increment. If the output of either amplifier is higher than V_{OLTH} during the on-state, then the timer is reset. If the timer reaches the open-load timeout value, t_{OLTO}, typically 100 ms, the open-load fault bit, OL, will be set in the Diagnostic 2 register and the LDF and FF bits will be set in the Status register indicating a valid open-load condition.

As soon as the output of any amplifier is higher than V_{OLTH} during the on-state, then the fault will be reset, but the open-load fault bit remains in the Diagnostic 2 register until reset.

If the sense amplifiers are not used in an application, then the on-state open-load detection can be completely disabled by setting AOL to 0.

Off-State Open-Load Detection

Prior to initiating an off-state open-load test, the bootstrap charge pump must be turned off by setting the charge pump mode variable, CPM[1:0], to 3 and all gate drive outputs must be commanded off. Open-load detection is then initiated by setting YPS = 3. While YPS = 3, a current sink, I_{SD}, is applied to the SB terminal and a current source, I_{SU}, is applied to the SA and SC terminals.

I_{SD} is typically 2.5 mA which is low enough to allow the AMT49106 to survive a short to VBB on the SB terminal during the off-state without damage, and high enough to discharge any output capacitance in an acceptable time.

The value of I_{SU} is selected by the YSC bit. When YSC = 0, I_{SU} = –90 µA; when YSC = 1, I_{SU} = –410 µA.

Off-state open-load detection relies on there being no residual current in the load or the bridge and no large capacitors connected to the load or the bridge phase connections. If either of these are not the case, then sufficient time must elapse before the state of the load connection is correctly indicated. This timeout is not provided by the AMT49106 and must be managed by the external controller.

Once any residual energy has dissipated, the sink current, I_{SD}, pulls the SB terminal to ground. The source current, I_{SU}, applies a test current to the load. As the sink current is much larger than the source current, the current through the load will be the source current. The voltage at the SB terminal, V_{SB}, should be close to zero and the voltages at the SA and SC terminals, V_{SA} and V_{SC}, will allow the load resistance to be measured. V_{SA} and V_{SC} are compared to the low-side VDS threshold, V_{DSTL}. If V_{SA} or V_{SC} is greater than V_{DSTL}, then the open load fault bit, OL, will be set in the Diagnostic 2 register. The LDF and FF bits will not be set in the Status register. If there are external capacitors connected to the bridge phase nodes or there is residual current in the load then it may take some time for these nodes to discharge to the final value and OL may indicate a fault during this time. On reaching the final steady-state value, if V_{SA} and V_{SC} are both less than V_{DSTL}, then OL will be 0 and a load is assumed to be present.

To allow the external controller to read the present state of the open-load test result, OL is not latched. The point at which the open-load result is read is therefore controlled by the external controller and should be determined by characterization of the system settling time during the open-load test.

The threshold for load resistance is determined by the current source, I_{SU}, and the low-side VDS threshold, V_{DSTL}.

For example, if V_{DSTL} is 1.2 V and I_{SU} = –410 µA, the equivalent threshold resistance is approximately 3 kΩ, so any load resistance greater than this value is detected as an open-load.

On completion of the open-load test, the variables YSC, YPS, and CPM should all be set to 0 to resume normal operation.

Motor Winding Considerations

If driving a star-connected motor, the on-state and off-state methods described above allow the detection of open-load faults in the bridge-to-motor interconnects and within the motor itself. If driving a delta-connected motor, only faults in the bridge-to-motor interconnects may be detected as motor inter-terminal impedance will remain relatively low in the event of a single-point failure internal to the motor (this type of motor having two internal current paths between each terminal).

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Bridge: Bootstrap Capacitor Undervoltage Fault

The AMT49106 monitors the individual bootstrap capacitor charge voltages to ensure enough high-side drive. If the voltage on a bootstrap capacitor drops below the bootstrap undervoltage falling threshold, V_{BCUV}, a bootstrap undervoltage fault is flagged.

If FVBU = 1, the general fault flag will be active and all gate drive outputs will be disabled (low). The associated bootstrap undervoltage fault bit (VA, VB, VC) will be set in the Diagnostic 2 register as will the BSU bit in the Status register. When the voltage on the bootstrap capacitor rises above the rising bootstrap undervoltage threshold, $V_{BCUV} + V_{BCUVHys}$, the general fault flag will be cleared, and all gate drive outputs will be re-enabled. The associated bootstrap undervoltage fault bit (VA, VB, VC) and the BSU bit will remain set until the Diagnostic 2 register is read with DSR = 0.

If FVBU = 0, fault reporting will be the same, but the gate drive outputs will not be disabled.

Each bootstrap undervoltage monitor is always active, regardless of whether the associated high-side gate drive is commanded on or off.

The bootstrap undervoltage monitor can be disabled for all phases by setting the BSU bit in the Mask 2 register. Although not recommended, this can allow the AMT49106 to operate below its minimum specified supply voltage level with a severely impaired gate drive. The specified electrical parameters may not be valid in this condition.

Bridge: MOSFET VDS Overvoltage Fault

Faults on any external MOSFETs are determined by monitoring the drain-source voltage of the MOSFET and comparing it to a drain-source overvoltage threshold. There are two thresholds, V_{DSTH}, for the high-side MOSFETs, and V_{DSTL} for the low-side. V_{DSTH} and V_{DSTL} are generated by internal DACs and are defined by the values in the VTH[5:0] and VTL[5:0] variables respectively. These variables provide the input to two 6-bit DACs with a least significant bit value of typically 50 mV. The output of the DAC produces the threshold voltage approximately defined as:

$$V_{DSTH} = n \times 50\,mV$$

where n is a positive integer defined by VTH[5:0],

or

$$V_{DSTL} = n \times 50\,mV$$

where n is a positive integer defined by VTL[5:0].

The low-side drain-source voltage for any MOSFET is measured between the adjacent Sx terminal and the adjacent LSSx terminal. Using the LSSx terminal rather than the ground connection avoids adding any low-side current sense voltage to the real low-side drain-source voltage and avoids false VDS fault detection.

The high-side drain-source voltage for any MOSFET is measured between the adjacent Sx terminal and the VBB terminal.

Separate track from the VBB terminal should be connected independently and directly to the common connection point for the drains of the power bridge MOSFETs at the positive supply connection point in the bridge.

The output from each VDS overvoltage comparator is filtered by a VDS fault qualifier circuit. This circuit uses a timer to verify that the output from the comparator is indicating a valid VDS fault. The duration of the VDS fault qualifying timer, t_{VDQ}, is determined by the contents of the TVD[5:0] variable. t_{VDQ} is approximately defined as:

$$t_{VDQ} = n \times 100\,ns$$

where n is a positive integer defined by TVD[5:0].

The qualifier can operate in one of two ways: debounce mode or blanking mode, selected by the VDQ bit.

In debounce mode (the default setting), a timer is started each time the comparator output indicates a VDS fault detection when the corresponding MOSFET is active. This timer is reset when the comparator changes back to indicate normal operation. If the debounce timer reaches the end of the timeout period, set by t_{VDQ}, then the VDS fault is considered valid and the corresponding VDS fault bit, ALO, AHO, BLO, BHO, CLO, or CHO will be set in the Diagnostic 1 register.

In blanking mode (optional), a timer is started when any gate drive is turned on or turned off. The outputs from the VDS overvoltage comparators for all MOSFETs are ignored (blanked) for the duration of the timer's active period, set by t_{VDQ}. If any gate drive changes state while a blanking period is in progress, the timer will be retriggered, resulting in an extended overall blanking time. If any comparator output indicates a VDS fault and the blanking timer is not active, then the VDS fault is considered valid and the corresponding VDS fault bit, ALO, AHO, BLO, BHO, CLO, or CHO is set in the Diagnostic 1 register.

The VDQ and TVD[5:0] qualifier parameters set in the Config 2 register apply to both the VGS undervoltage and VDS overvoltage monitors.

The action taken when a valid VDS fault is detected and the

ALLEGRO microsystems
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

action then required to clear the fault state depend upon the FDSO bit value.

If FDSO = 0, the fault state will be latched, the general fault flag will be active, the associated VDS fault bit will be set and the gate drive for the associated MOSFET will be inactive (low). The gate drive output will remain inactive (low) until the fault state and the general fault flag are reset the next time the MOSFET, on which the fault was detected, is commanded to switch on. The associated VDS fault bit remains set in the Diagnostic 1 register until reset. If the MOSFET is being driven with a PWM signal then this will usually mean that the MOSFET will be turned on again each PWM cycle. If this is the case, and the fault condition remains, then a valid fault will again be detected after the timeout period and the sequence will repeat. The general fault flag will only be reset for the duration of the validation timer. The VDS fault bits will only be reset by a serial read of the Diagnostic 1 register with DSR = 0 or by a power-on reset.

If FDSO = 1, the fault will be latched, the general fault flag will be active, the associated VDS fault bit will be set and all gate drive outputs will be inactive (low). The gate drive outputs will remain inactive (low) until the fault state and the general fault flag are reset by a serial read of the Diagnostic 1 register with DSR = 0, or by a power-on reset. The VDS fault bit will only be reset by a serial read of the Diagnostic 1 register with DSR = 0 or by a power-on reset.

If FDSO = 0, care must be taken to avoid damage to the MOSFET where the VDS fault is detected. Although the MOSFET will be switched off as soon as the fault is detected at the end of the fault validation timeout, it is possible that it could still be damaged by excessive power dissipation and heating. To limit any damage to the external MOSFETs or the motor, the gate drive outputs should be fully disabled by logic inputs from the external controller.

Fault Action

The action taken when one of the diagnostic functions indicates a fault is listed in Table 6.

When a fault is detected, a corresponding fault state is considered to exist. In some cases, the fault state only exists during the time the fault is detected. In other cases, when the fault is only detected for a short time, the fault state is latched (held in the fault state) until reset. The faults that are latched are indicated in Table 6. Latched fault states are always reset when a power-on-reset state is present or when the associated fault bit is read through the serial interface with DSR = 0. Any fault bits that have been set in the diagnostic registers are only reset when a power-on-reset state is present or when the associated fault bit is read through the serial interface with DSR = 0.

For most of the diagnostic functions, the action taken when a fault state is detected can be programmed to force the gate drive outputs into the inactive (low) state or to leave them active. The action is selected by setting a 1 or 0 in specific stop on fault (SoF) bit associated with the diagnostic. The specific SoF bits for each diagnostic and the actions taken for each setting are listed in Table 6.

Table 6: Fault Actions

Fault Description	SoF Bit Name	Disable Outputs		Fault State Latched
		SoF Bit = 0	SoF Bit = 1	
No Fault	–	No	No	–
Power-on-Reset	–	Yes [1]	Yes [1]	No
VREG Undervoltage	FVRU	No [3]	Yes [1]	No
VCP Undervoltage	FCPU	No	Yes	No
VIO or VOOR Out of Range	FVDD	No	Yes [1]	No
Bootstrap Undervoltage	FVBU	No	Yes [1]	No
Logic Terminal Overvoltage	FVLO	No	Yes [1][4]	No
WD Timeout	FWD	No	Yes [1]	Yes
Overtemperature	FOT	No [3]	Yes [1]	No
LSS Disconnect	FLSS	No	Yes [5]	Yes
VDS Fault	FDSO	Yes [2]	Yes [1]	Yes
Serial Transmission Error	FSE	No	Yes [1]	No
VREG Overvoltage	FVRO	No	Yes [1]	No
VBB Undervoltage	FVSU	No [3]	Yes [1]	No
VBB Overvoltage	FVSO	No	Yes [1]	No
VGS Undervoltage	FGSU	No [3]	Yes [1]	Yes
Temperature Warning	FTW	No	Yes [1]	No
Overcurrent	FOC	No	Yes [1]	Yes
Open Load	–	No	No	No
EEPROM	–	Yes [1]	Yes [1]	Yes

[1] All gate drives low, all MOSFETs off.
[2] Gate drive for the affected MOSFET low, only the affected MOSFET off.
[3] Stated fault condition may damage the AMT49106 and/or bridge MOSFETs unless appropriate action taken by the external controller.
[4] Outputs disabled on Hx, Lx, overvoltage but not on DIAG, ENABLE overvoltage.
[5] Creates VDS fault.

If a Power-on-Reset state is detected, then all gate drive outputs are driven low and all MOSFETs in the bridge are held in the off-state. This persists until the Power-on-Reset state is cleared.

Setting any of the FVRU, FCPU, FVDD, FVBU, FVLO, FWD, FDSO, FSE, FVRO, FVSU, FVSO, FOT, FTW, FOC, FLSS, or FGSU bits in the Stop-on-Fault registers to 0 such that the gate

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

drive outputs are not disabled in the event of the corresponding fault being detected means that the AMT49106 will not take any action to protect itself or the external bridge MOSFETs and damage may occur. Appropriate action must be taken by the external controller.

Fault Masks

Individual diagnostics except power-on reset, EEPROM error, serial transmission error, overtemperature, open-load, and overcurrent can be disabled by setting the corresponding bit in the mask registers. Power-on-reset cannot be disabled because the diagnostics and the output control depend on the logic regulator for the internal logic to operate correctly. If a bit is set to one in the mask registers, then the corresponding diagnostic will be completely disabled. No fault states for the disabled diagnostic will be generated, no fault flags or diagnostic bits will be set, and no action will be taken. See Mask Register definition for bit allocation.

Care must be taken when diagnostics are disabled to avoid potentially damaging conditions.

Diagnostic and System Verification

To comply with various aspects of safe system design, it is necessary for higher-level safety systems to verify that any diagnostics or functions used to guarantee safe operation are operating within specified tolerances.

There are four basic aspects to verification of diagnostic functions:

- Verify connections
- Verify comparators
- Verify thresholds
- Verify fault propagation

These must be completed for each diagnostic. In addition, the operation of system functions not directly covered by diagnostics should also be verified.

The AMT49106 includes additional verification functions to help the system design comply with any safety requirements. Many of these functions can only be completed when the diagnostics are not required and must be commanded to run by the main system controller. These functions are referred to “off-line” verification.

A few of the functions can be continuously active but the results must be checked by the main system controller on a regular basis. These functions are referred to “on-line” verification.

The frequency with which these off-line verification functions are run, or on-line verifications results are checked, will depend on the safety requirements of the system using the AMT49106.

Table 7: Verification Functions

Verification Type	Function Verified	Operation	
		Offline	Online
Connection	Phase Connection	Y	
Connection	Sense Amplifier Connection		Y
Monitor	Q&A Watchdog	Y	
Monitor	Overcurrent Detectors	Y	
Monitor	Phase State Monitor		Y
Diagnostic	LSS Connection	Y	
Diagnostic	Overtemperature	Y	
Diagnostic	Temperature Warning	Y	
Diagnostic	VBB Undervoltage	Y	
Diagnostic	VBB Overvoltage	Y	
Diagnostic	VREG Diagnostics	Y	
Diagnostic	Bootstrap Capacitor	Y	
Diagnostic	VCP Undervoltage	Y	
Diagnostic	VIO Undervoltage	Y	
Diagnostic	VIO Overvoltage	Y	
Diagnostic	VOOR Undervoltage	Y	
Diagnostic	VOOR Overvoltage	Y	
Diagnostic	VGS Undervoltage	Y	
Diagnostic	Logic Terminal Diagnostic	Y	
Diagnostic	Open Load Detector	Y	
Diagnostic	VDS Overvoltage Diagnostic	Y	
Diagnostic	All Gate Drives Off	Y	

On-Line Verification

The following functions are permanently active and will set the appropriate bit in the verification result registers to indicate that the verification has failed. No other action will be taken by the AMT49106 unless described below. These verification functions verify that certain of the AMT49106 terminals are correctly connected to the power bridge circuit.

Bridge: Phase State Monitor

The bridge phase connections at the SA, SB, and SC terminals are connected to programmable threshold comparators. The outputs of the comparators set the states of SAS, SBS, and SCS bits of the Verify Result 1 register, to provide a logic level representation of the power bridge output states (logic 1 indicating voltage

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

on SA, SB, SC more positive than the threshold, logic 0 more negative). The SAS, SBS, and SCS bit states follow the bridge output states in real time and are not latched.

The threshold for the three comparators, V_{PT}, is generated, as a ratio of the V_{BB}, by a 6-bit DAC and determined by the contents of the VPT[5:0] variable. VPT is approximately defined as:

$$V_{PT} = (n / 64) \times V_{BB}$$

where n is a positive integer defined by VPT[5:0].

V_{PT} can be programmed between 0 and 98.4%V_{BB}.

Sense Amplifier Disconnect

Each sense amplifier includes continuous current sources, I_{SAD}, that will allow detection of an input open-circuit condition. If an input open circuit occurs, the voltage rises above the sense amplifier open-load detect threshold, V_{SAD} and the S1D, S2D, or S3D bit is set in the Verify Result 1 register depending upon the sense amplifier affected.

Off-Line Verification

The following functions are only active when commanded by setting the appropriate bit in the verification command registers in addition to any required gate drive commands. If the function only verifies a connection, then a fail will set the appropriate bit in the verification result register. No other action will be taken by the AMT49106. If the function is to verify one of the diagnostic circuits in the AMT49106, then the verification is completed by checking that the associated fault bit is set in the diagnostic registers.

Bridge: Phase Disconnected

The connections from each Sx terminal to the corresponding common node of the high-side MOSFET source and low-side MOSFET drain are verified individually by a combination of MOSFET commands and test currents. The connection to all MOSFETs must be checked to fully verify the connection for each phase.

Connection to each high-side MOSFET is tested by first turning it on using the logic inputs or the serial interface. Other high-side MOSFETs and all low-side MOSFETs must be turned off to avoid corrupting the test result.

The phase to be tested is selected by the value in the verify phase select variable, YPS: 0 for phase B, 1 for phase A, and 2 for phase C. The value of 3 is reserved for open-load testing.

In addition, the bootstrap charge pump must be switched to

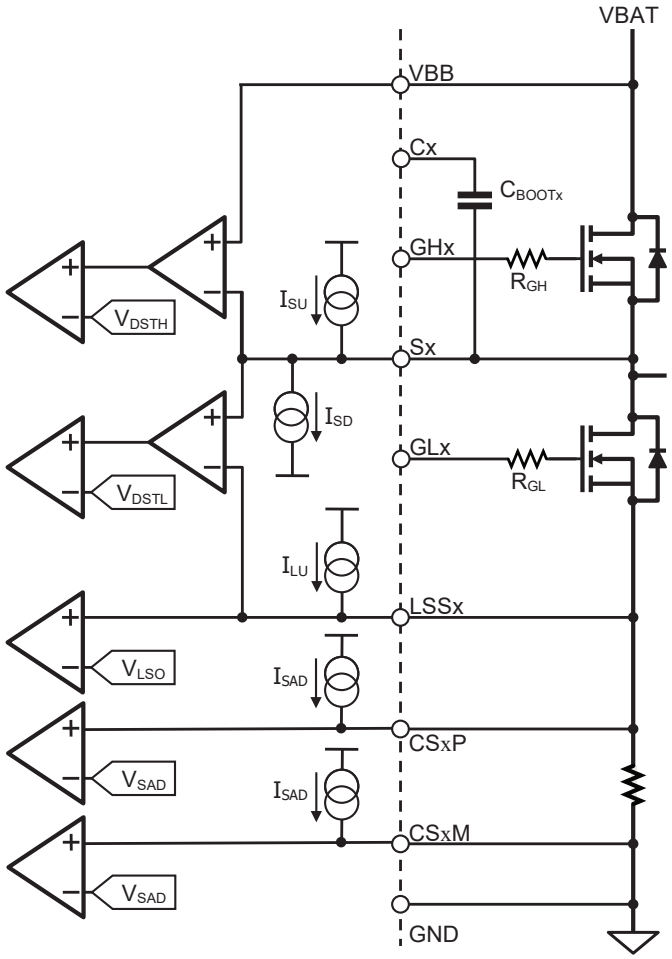


Figure 16: Bridge Terminal Connection Verification

low current mode by setting the CPM variable in the Config 5 register to 1. This is to avoid any unnecessary dissipation in the pump regulator during testing. A pull-down current, I_{SD}, is then switched on by setting YSK to 1 in order to pull the phase low if the high-side MOSFET is either disconnected or not switched on. I_{SD} is typically 2.5 mA, which is low enough to allow the AMT49106 to survive a short to VBB on the SB terminal without damage, and high enough to discharge any output capacitance in an acceptable time.

The high-side VDS monitors are used to determine the state of the phase connection by comparing the VDS voltage of the high-side MOSFET, measured between VBB and Sx with the programmed high-side VDS threshold, V_{DSTH}.

Test timing is not controlled by the AMT49106 and must be man-

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

aged by the external controller using the phase disconnect verify command bit, YPH.

Phase disconnect detect relies upon there being no residual current in the load or the bridge and time must be allowed for Sx terminal voltages to stabilize prior to completion of the test.

YPH is taken high to initiate the test and should be held in this state until it is known that any residual energy has dissipated, giving the sink current, I_{SD}, time to pull the Sx terminal to ground in the case of a phase disconnect. At the end of this period, YPH should be set to 0. The PxD bit will then be 1 if the phase is connected and the MOSFET is on and 0 if the phase is disconnected or the MOSFET is off. The PxD bit is reset when the state of the PxD bit is determined by reading the Verify Result 0 register. The value of the PxD bit is not valid when YPH is high.

The low-side disconnect test is complementary to the high-side test. Connection to each low-side MOSFET is tested by first turning it on using the logic inputs or the serial interface. Other low-side MOSFETs and all high-side MOSFETs must be turned off to avoid corrupting the test result.

The phase to be tested is selected by the value in the verify phase select variable, YPS: 0 for phase B, 1 for phase A, and 2 for phase C. The value of 3 is reserved for open-load testing.

In addition, the bootstrap charge pump must be set to normal operation by setting the charge pump mode variable, CPM, to 0.

A pull-up current, I_{SU}, is provided in order to pull the phase high if the low-side MOSFET is either disconnected or not switched on. It is recommended that the value of I_{SU} is switched to –410 µA by setting the YSC bit to 1 when performing phase disconnect tests. This allows I_{SU} to charge any output capacitances in an acceptable time. YSK must be set to 0 during low-side disconnect tests.

The low-side VDS monitors are used to determine the state of the phase connection by comparing the VDS voltage of the low-side MOSFET, measured between Sx and LSSx with the programmed low-side VDS threshold, V_{DSTL}.

Test timing is not controlled by the AMT49106 and must be managed by the external controller using the phase disconnect verify command bit, YPL.

Phase disconnect detect relies upon there being no residual current in the load or the bridge and time must be allowed for Sx terminal voltages to stabilize prior to completion of the test.

YPL is taken high to initiate the test and should be held in this state until it is known that any residual energy has dissipated, giving the source current, I_{SU}, time to pull the Sx terminal to VBB in the case of a phase disconnect. At the end of this period, YPL should be set to 0. The PxD bit will then be 1 if the phase is connected and the MOSFET is on and 0 if the phase is disconnected or the MOSFET is off. The PxD bit is reset when the state of the PxD bit is determined by reading the Verify Result 0 register. The value of the PxD bit is not valid when YPL is high

Verify: VREG Undervoltage

The VREG undervoltage detector is verified by setting the YRU bit in the Verify Command 0 register to 1. This applies a voltage to the comparator that is lower than the undervoltage threshold and should cause the VREG undervoltage fault bit, VRU, to be latched in the Diagnostic 1 register. When YRU is reset to 0, the VRU bit will remain set in the Diagnostic 1 register until reset. If the VRU bit is not set, then the verification has failed.

Verify: VREG Overvoltage

The VREG overvoltage detector is verified by setting the YRO bit in the Verify Command 0 register to 1. This applies a voltage to the comparator that is higher than the overvoltage threshold and should cause the VREG overvoltage fault bit, VRO, to be latched in the Diagnostic 1 register. When YRO is reset to 0, the VRO bit will remain set in the Diagnostic 1 register until reset. If the VRO bit is not set, then the verification has failed.

Verify: Temperature Warning

The temperature warning detector is verified by setting the YTW bit in the Verify Command 2 register to 1. This applies a voltage to the comparator that is lower than the temperature warning threshold and should cause the temperature warning fault bit, TW, to be latched in the Status register. When YTW is reset to 0, the TW bit will remain set in the Status register until reset. If the TW bit is not set, then the verification has failed.

Verify: Overtemperature

The overtemperature detector is verified by setting the YOT bit in the Verify Command 2 register to 1. This applies a voltage to the comparator that is lower than the overtemperature threshold and should cause the overtemperature fault bit, OT, to be latched in the Status register. When YOT is reset to 0, the overtemperature fault will remain in the Status register until reset. If the OT bit is not set, then the verification has failed.

Verify: VBB Supply Overvoltage

The VBB overvoltage detector is verified by setting the YSO bit in the Verify Command 0 register to 1. This applies a voltage to

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

the comparator that is higher than the VBB overvoltage threshold and should cause the VBB overvoltage fault bit, VSO, to be latched in the Diagnostic 2 register. When YSO is reset to 0, the VSO bit will remain set in the Diagnostic 2 register until reset. If the VSO bit is not set, then the verification has failed.

Verify: VBB Supply Undervoltage

The VBB undervoltage detector is verified by setting the YSU bit in the Verify Command 0 register to 1. This applies a voltage to the comparator that is lower than the VBB undervoltage threshold and should cause the VBB undervoltage fault bit, VSU, to be latched in the Diagnostic 2 register. When YSU is reset to 0, the VSU bit will remain set in the Diagnostic 2 register until reset. If the VSU bit is not set, then the verification has failed. During the period when YSU is set to 1, the VREG and VCP charge pump regulators are disabled and both VREG and VCP may decay. Consequently VRU, VCPU, Vx, and OCx fault bits may be set in the Diagnostic registers after carrying out a VBB supply undervoltage verification. It is therefore recommended that all three Diagnostic registers are read to clear any such faults immediately after each VBB supply undervoltage verification.

Verify: VGS Undervoltage

The VGS undervoltage detectors can be verified individually or in two groups, high-side and low-side. The detectors are verified by switching on the required MOSFET using the serial Control register bits or the logic input terminals and then setting the YGU bit in the Verify Command 0 register to 1. This applies a voltage that is lower than the VGS undervoltage threshold to the active comparator and should cause a VGS undervoltage fault to be latched in the corresponding VGS undervoltage fault bit in the Diagnostic 0 register. (For example, the CHU bit should be set after the CH bit is set in the Control register or the HC input is driven high, etc.) After a period exceeding the programmed VGS qualification time plus a dead time, $t_{VDQ} + t_{DEAD}$, YGU must be returned to 0 and all gate drives must be commanded off. The general fault flag and the VGS undervoltage fault bits will remain set until the Diagnostic 0 register is read. This must be repeated until all MOSFETs have been switched to verify all VGS undervoltage comparators. If any VGS fault bit is not set after all MOSFETs have been switched, then the verification has failed for the corresponding comparator.

Verify: Bootstrap Capacitor Undervoltage Fault

The bootstrap capacitor undervoltage detectors are verified by setting the YBU bit in the Verify Command 0 register to 1. This applies a voltage that is lower than the bootstrap undervoltage threshold to each of the three bootstrap circuit detectors and should cause the general fault flag to be active and bootstrap undervoltage faults to be indicated in the corresponding bootstrap undervoltage fault bits (VA, VB, and VC) in the Diagnostic 2 register.

When YBU is reset to 0, the states of the bootstrap fault bits are latched into the Diagnostic 2 register. If any of the bootstrap fault bits is not set, then the verification of the corresponding detector has failed. All bootstrap fault bits and the general fault flag are cleared when the Diagnostic 2 register is read.

Verify: MOSFET VDS Overvoltage Fault

The VDS overvoltage detectors can be verified individually or in two groups, high-side and low-side. The detectors are verified by commanding the intended MOSFETs to turn on using the serial command register bits or the logic input terminals and then setting the YDO bit in the Verify Command 0 register to 1. This applies a voltage that is higher than the VDS overvoltage threshold set for any active detector by turning on the complementary MOSFET in the same phase (rather than the commanded MOSFET) to pull the Sx node toward VBB (low-side verification) or LSSx (high-side verification). In response, a VDS overvoltage fault should be latched in the corresponding VDS overvoltage fault bit in the Diagnostic 1 register. (For example, the CHO bit should be set after the CH bit is set in the Control register or the HC input set to turn on the GHC output, etc.). After a period exceeding the programmed VDS qualification time plus a dead time, $t_{VDQ} + t_{DEAD}$, the YDO bit must be returned to 0 to exit the verification mode. Diag 1 should then be read to inspect and clear the xLO, xHO bits. This must be repeated until all MOSFETs have been switched to verify all VDS overvoltage comparators. If any VDS overvoltage fault bit has not been set after all MOSFETs have been commanded on, then the verification has failed for the corresponding comparator.

Verify: LSS Disconnect

The LSS disconnect detectors are verified by setting the YLS bit in the Verify Command 2 register to 1. This applies a voltage to each LSS disconnect comparator that is greater than the LSS disconnect threshold and should cause the LSS disconnect fault bits, LAD, LBD, and LCD, to be latched in the Verify Result 0 register. When YLS is reset to 0, the disconnect fault bits will remain set in the Verify Result 0 register until reset. If any of the LSS disconnect fault bits, LAD, LBD, and LCD, is not set, then the verification has failed.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Verify: VIO Input Out of Range

The VIO input overvoltage detector is verified by setting the YIO bit in the Verify Command 2 register to 1. This applies a voltage to the comparator associated with the VIO input that is higher than the VIO input overvoltage threshold, V_{IOOLON}. Consequently, the input overvoltage fault bit, VDO, in Diagnostic 0 register, should be set, along with the VD bit in the Status register. When YIO is reset to 0, the VDO and VD bits will remain set in the corresponding registers indicating a successful verification. During the period when YIO is set to 1, the general fault flag on the DIAG output may indicate a fault and the gate drive outputs may be disabled, but this condition does not indicate a successful logic input voltage verification.

The VIO undervoltage detector is verified by setting the YIU bit in the Verify Command 2 register to 1. This applies a voltage to the comparator associated with the VIO input that is lower than the corresponding undervoltage threshold. Consequently, the input undervoltage bit, VDU, in the Diagnostic 0 register, should be set along with the VD bit in the Status register. When YIU is reset to 0, the VDU and VD bits will remain set in the corresponding registers, indicating a successful verification.

Verify: VOOR Input Out of Range

The VOOR input overvoltage detector is verified by setting the YMO bit in the Verify Command 2 register to 1. This applies a voltage to the comparator associated with the VOOR input that is higher than the corresponding overvoltage threshold and should cause the VDO fault bit and the associated Status register bit VD to be set and latched. When YMO is reset to 0, the VDO and VD bits will remain set, indicating a successful verification. If the VDO and VD bits are not set, then the verification has failed.

The VOOR undervoltage detector is verified by setting the YMU bit in the Verify Command 2 register to 1. This applies a voltage to the comparator associated with the VOOR input that is lower than the corresponding undervoltage threshold and should cause the VDU fault bit and the associated Status register bit, VD, to be set and latched. When YMU is reset to 0, the VDU and VD bits will remain set in the corresponding registers, indicating a successful verification. If the VDU or VD bits are not set then the verification has failed.

Verify: VCP Undervoltage

The VCP input undervoltage detector is verified by setting the YCP in the Verify Command 2 register to 1. This applies a voltage to the VCP undervoltage comparator that is lower than the corresponding undervoltage threshold and should cause the VCPU fault bit to be set in the Diagnostic 0 register. When YCP is reset to 0, the VCPU bit will remain set, indicating a successful verification. If the VCPU bit is not set, the verification has failed.

Verify: Logic Terminal Overvoltage

The logic terminal overvoltage detector is verified by setting the YLO bit in the Verify Command 1 register to 1. This applies a voltage to the comparator associated with each relevant logic terminal that is higher than the logic terminal overvoltage warning, V_{LOV}. Consequently, the input overvoltage fault bit, VLO, in the Status register should be set. To complete the verification, the YLO bit should be set to 0 and the state of the VLO bit should be read by writing to the Verify Command 1 register. If the VLO bit is set to 1, the verification has passed, and if set to 0, it has failed. During the period when YLO is set to 1, the general fault flag on the DIAG pin may be set to logic low and the gate drive outputs may be disabled, but neither of these conditions indicates a successful logic terminal voltage verification.

Verify: Overcurrent Detect and Sense Amplifier

The overcurrent detector is verified by setting the YOC bit in the Verify Command 1 register to 1. This forces the output of each sense amplifier to positive full-scale, which can then be measured. The sense amplifier outputs remain connected to the overcurrent comparators and the full-scale output applies a voltage to the comparator that is higher than the overcurrent threshold, VOCT. Consequently, the overcurrent fault bits, OC1, OC2, and OC3 in Diagnostic 2 register should be set, along with the LDF, bit in the Status register. When YOC is reset to 0, the sense amplifier outputs will return to normal operation and the OC1, OC2, OC3, and LDF bits will remain latched until reset. Unless the OC1, OC2, OC3, and LDF bits are all set, the verification has failed.

During verification of the overcurrent detector, the overcurrent threshold voltage, V_{OCT}, set by OCT[3:0] plus any offset, V_{OOS}, set by OOR terminal must not exceed the positive extreme of the sense amplifier output dynamic range of 4.8 V. If it does, then the OC1, OC2, and OC3 bits may not be set and the verification may fail.

Verify: Q&A Watchdog Timeout

The Q&A watchdog is verified in six stages:

1. The required values of failure count threshold and watchdog timeout are written to WDC[1:0] and QAT[3:0] in the Config 13 register by the system controller. The watchdog is then set to active mode by writing SEQ0 = 0xA1, SEQ1 = 0x78, and SEQ2 = 0x98 to the Q&A Mode register.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

2. LUT address-request/answer-write cycles are initiated by the system controller (each answer having the incorrect value but delayed from the address request by a period longer than the set QAT([min] and shorter than the set QAT[max]) until the set WDC count threshold is exceeded. The QAE bit state is then inspected by reading the Verify Result 0 register and the verification is passed if a value of 1 is returned. Reading the verify Result 0 register resets the QAE bit to 0.
3. LUT address-request/answer-write cycles are made by the system controller (each answer having the correct value but delayed from the address request by a period shorter than the set QAT[min] time) until the set WDC count threshold is exceeded. The QTO bit state is then inspected by reading the Verify Result 0 register and the verification is passed if a value of 1 is returned. Reading the verify Result 0 register resets the QTO bit to 0.
4. LUT address-request/answer-write cycles are made by the system controller (each answer having the correct value but delayed from the address request by a period longer than the set QAT[max] time) until the set WDC count threshold is exceeded. The QTO bit state is then inspected by reading the Verify Result 0 register and the second phase of verification is passed if a value of 1 is returned. Reading the verify Result 0 register resets the QTO bit to 0.
5. LUT address-request/answer-write cycles are made by the system controller (each answer having the incorrect value and delayed from the address request by a period shorter than the set QAT[min] time) until the set WDC count threshold is exceeded. The QAE bit and the QTO bit are then inspected by reading the Verify Result 0 register and verification is passed if a value of 1 is returned for both bits. Reading the Verify Result 0 register resets the QAE and QTO bits to 0.
6. LUT address-request/answer-write cycles are made by the system controller (each answer having the incorrect value and delayed from the address request by a period longer than the set QAT[max] time) until the set WDC count threshold is exceeded. The QAE bit and the QTO bit are then inspected by reading the Verify Result 0 register and verification is passed if a value of 1 is returned for both bits. Reading the Verify Result 0 register resets the QAE and QTO bits to 0.

If the FWD bit it set to 1, all gate drive outputs will be driven low each time a fault condition is generated during the verification process. If FWD is set to 0, they will not.

Verify: All Gate Drives Off

The successful propagation of control inputs demanding all-gate-drives-off to the gate drive outputs is verified by setting up an appropriate input condition and inspecting the GDO bit in the Verify Result 1 register. If the input condition has successfully turned off all six gate drives, the GDO bit is set. The control input conditions (i.e. the combinational states of Hx, Lx, xH, xL, and ENABLE) that demand all outputs off (GHx = L, GLx = L) and hence set the GDO bit as a result of a successful verification test, can be determined by inspection of Tables 1 through 3.

Verification of propagation from an appropriate combination of phase logic inputs (Hx, Lx) and serial register bits (xH, xL) to the gate drive outputs does not verify propagation from the ENABLE input to the gate drive outputs and vice versa. Gate drive off events are not latched in the Verify Result 1 register and the GDO bit returns to 0 as soon as any gate drive is detected to be in the on state.

Verify: On-State Open-Load Detection and Sense Amplifier

The on-state open load detector is verified by turning on a low-side gate drive (to select a sense amplifier for test) and at least one high-side (on a different phase), setting the AOL bit to 1 and then setting the YOL bit in the Verify Command 1 register to 1. For this verification operation, sense amplifier 1 is verified by turning on phase A low-side, sense amplifier 2 by turning on phase B low-side and sense amplifier 3 by turning on phase C low side. Turning on the low-side forces the output of the associated sense amplifier to its zero current output condition (equivalent to zero differential input) which then drives the open-load comparator with a voltage that is lower than the comparator's threshold and produces an on-state open-load fault after the open-load timeout.

When YOL is first set to 1, any open-load faults are cleared, and the open-load timer is reset. At the end of a 100 ms timeout period, if an open-load state has successfully been detected, the YOL bit is reset by the AMT49106 to indicate that the timeout is complete and the OL (Diagnostic 2 register) and LDF (Status register) bits should be inspected. If both bits are set, the verification has been successful. The OL bit in the Diagnostic 2 register and the LDF bit is the Status register remain latched until reset. After a period of 102 ms from YOL being set to 1, if an open-load state has not been successfully detected, the YOL bit is reset by the AMT49106. If YOL is reset to 0 before the timeout has completed, then the verification is terminated without setting any fault bits. All three phases must be tested separately to complete the verification.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

SERIAL INTERFACE

Table 8: Serial Register Definition*

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0:Config 0	0	0	0	0	0	WR	GTS	OCQ		DT5	DT4	DT3	DT2	DT1	DT0	P
							0	0	0	1	1	1	1	1	1	
1:Config 1	0	0	0	0	1	WR	OCT3	OCT2	OCT1	OCT0	TOC4	TOC3	TOC2	TOC1	TOC0	P
							0	1	0	1	0	1	1	1	1	
2:Config 2	0	0	0	1	0	WR	VDQ			TVD5	TVD4	TVD3	TVD2	TVD1	TVD0	P
							0	0	0	0	1	0	0	0	0	
3:Config 3	0	0	0	1	1	WR				VTL5	VTL4	VTL3	VTL2	VTL1	VTL0	P
							0	0	0	0	1	1	0	0	0	
4:Config 4	0	0	1	0	0	WR				VTH5	VTH4	VTH3	VTH2	VTH1	VTH0	P
							0	0	0	0	1	1	0	0	0	
5:Config 5	0	0	1	0	1	WR	AOL	CPM1	CPM0			OLT3	OLT2	OLT1	OLT0	P
							0	0	0	0	0	1	0	0	0	
6:Config 6	0	0	1	1	0	WR	VLR	VLM		VPT5	VPT4	VPT3	VPT2	VPT1	VPT0	P
							0	0	0	1	0	0	0	0	0	
7:Config 7	0	0	1	1	1	WR		THR3	THR2	THR1	THR0	THF3	THF2	THF1	THF0	P
							0	0	0	0	0	0	0	0	0	
8:Config 8	0	1	0	0	0	WR		IHR13	IHR12	IHR11	IHR10	IHF13	IHF12	IHF11	IHF10	P
							0	0	0	0	0	0	0	0	0	
9:Config 9	0	1	0	0	1	WR		IHR23	IHR22	IHR21	IHR20	IHF23	IHF22	IHF21	IHF20	P
							0	0	0	0	0	0	0	0	0	
10:Config 10	0	1	0	1	0	WR		TLR3	TLR2	TLR1	TLR0	TLF3	TLF2	TLF1	TLF0	P
							0	0	0	0	0	0	0	0	0	
11:Config 11	0	1	0	1	1	WR		ILR13	ILR12	ILR11	ILR10	ILF13	ILF12	ILF11	ILF10	P
							0	0	0	0	0	0	0	0	0	
12:Config 12	0	1	1	0	0	WR		ILR23	ILR22	ILR21	ILR20	ILF23	ILF22	ILF21	ILF20	P
							0	0	0	0	0	0	0	0	0	
13:Config 13	0	1	1	0	1	WR	S3C	S2C	S1C	WDC1	WDC0	QAT3	QAT2	QAT1	QAT0	P
							0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Continued on the next page...

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Table 8: Serial Register Definition*

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
14:Config 14	0	1	1	1	0	WR	S3G2	S3G1	S3G0	S2G2	S2G1	S2G0	S1G2	S1G1	S1G0	P
							0	1	0	0	1	0	0	1	0	
15:NVM Write	0	1	1	1	1	WR	SAV1	SAV0								P
							0	0	0	0	0	0	0	0	0	
16: Q&A Watchdog	1	0	0	0	0	WR		QA7	QA6	QA5	QA4	QA3	QA2	QA1	QA0	P
							0	0	0	0	0	0	0	0	0	
17: WD Mode	1	0	0	0	1	WR		WDM7	WDM6	WDM5	WDM4	WDM3	WDM2	WDM1	WDM0	P
							0	1	0	1	0	1	0	1	0	
18: Stop on Fault 0	1	0	0	1	0	WR	FOT	FTW		FLSS	FCPU	FSE	FVDD	FVLO	FWD	P
							1	1	0	0	0	1	1	1	1	
19: Stop on Fault 1	1	0	0	1	1	WR	FOC		FDSO	FGSU	FVBU	FVRO	FVRU	FVSO	FVSU	P
							1	0	1	1	1	1	1	1	1	
20: Verify Command 0	1	0	1	0	0	WR			YDO	YRO	YRU	YBU	YSO	YSU	YGU	P
							0	0	0	0	0	0	0	0	0	
21: Verify Command 1	1	0	1	0	1	WR	YPH	YPL	YOC	YLO	YOL	YPS1	YPS0	YSK	YSC	P
							0	0	0	0	0	0	0	0	0	
22: Verify Command 2	1	0	1	1	0	WR	YTW	YOT		YLS	YCP	YIO	YIU	YMO	YMU	P
							0	0	0	0	0	0	0	0	0	
23: Verify Result 0	1	0	1	1	1	WR	PCD	PBD	PAD	QAE	QTO		LCD	LBD	LAD	P
							0	0	0	0	0	0	0	0	0	
24: Verify Result 1	1	1	0	0	0	WR			GDO	SCS	SBS	SAS	S3D	S2D	S1D	P
							0	0	1	0	0	0	0	0	0	
25: Mask 0	1	1	0	0	1	WR	VCPU	VDU	VDO	CHU	CLU	BHU	BLU	AHU	ALU	P
							0	0	0	0	0	0	0	0	0	
26: Mask 1	1	1	0	1	0	WR	VRO	VRU		CHO	CLO	BHO	BLO	AHO	ALO	P
							0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Continued on the next page...

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Table 8: Serial Register Definition*

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
27: Mask 2	1	1	0	1	1	WR	VS	VLO	BSU	TW			LCD	LBD	LAD	P
							0	0	0	0	0	0	0	0	0	
28: Diag 0	1	1	1	0	0	WR	VCPU	VDU	VDO	CHU	CLU	BHU	BLU	AHU	ALU	P
							0	0	0	0	0	0	0	0	0	
29: Diag 1	1	1	1	0	1	WR	VRO	VRU		CHO	CLO	BHO	BLO	AHO	ALO	P
							0	0	0	0	0	0	0	0	0	
30: Diag 2	1	1	1	1	0	WR	VC	VB	VA	VSO	VSU	OC3	OC2	OC1	OL	P
							0	0	0	0	0	0	0	0	0	
31: Control	1	1	1	1	1	WR	DG1	DG0	DSR	CH	CL	BH	BL	AH	AL	P
							0	0	0	0	0	0	0	0	0	
Status	FF	POR	SE	EE	OT	TW	VS	VLO	WD	VR	VD	LDF	BSU	GSU	DSO	P
	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

A three-wire synchronous serial interface, compatible with SPI, is used to control the features of the AMT49106. In addition, the SDO terminal can be used, during a serial transfer, to provide diagnostic feedback and readback of the register contents.

The AMT49106 can operate without the serial interface using the default settings and the logic control inputs. However, application-specific configurations and several verification functions are only possible by setting the appropriate register bits through the serial interface. If the serial interface is not used, then some diagnostics cannot be cleared without a power off-on cycle. The serial interface can also be used to control the bridge MOSFETs directly.

The serial interface timing requirements are specified in the Electrical Characteristics table and illustrated in Figure 4. Data is received on the SDI terminal and clocked through a shift register on the rising edge of the clock signal input on the SCK terminal. STRn is normally held high and is only brought low to initiate a serial transfer. No data is clocked through the shift register when STRn is high, allowing multiple slave units to use common SDI and SCK connections. Each slave then requires an independent STRn connection. The SDO output assumes a high-impedance state when STRn is high allowing a common data readback connection.

After 16 data bits have been clocked into the shift register, STRn must be taken high to latch the data into the selected register. When this occurs, the internal control circuits act on the new data and the registers are reset depending on the type of transfer and the state of the DSR bit.

If there are more than 16 rising edges on SCK or if STRn goes high and there are fewer than 16 rising edges on SCK (either being described as a framing error), the write will be cancelled without latching data to the register. The read-only registers, Status, Diagnostic, or Verification Result will not be reset.

The first five bits, D[15:11], in a serial word are the register address bits, giving the possibility of 32 register addresses. The sixth bit, WR (D[10]), is the write/read bit. Except for the read-only registers, when WR is 1, the following 9 bits, D[9:1], clocked in from the SDI terminal are written to the addressed register. When WR is 0, the following 9 bits, D[9:1], clocked in from the SDI terminal are ignored, no data is written to the serial registers, and the contents of the addressed register are clocked out on the SDO terminal.

The last bit in any serial transfer, D[0], is a parity bit that is set to ensure odd parity in the complete 16-bit word. Odd parity means that the total number of 1s in any transfer should always be an odd number. This ensures that there is always at least one bit set to 1 and one bit set to 0 and allows detection of stuck-at faults on the serial input and output data connections. The parity bit is not stored but generated on each transfer.

In addition to the addressable registers, a read-only status register is output on SDO for all register addresses when WR is set to 1. For all serial transfers, the first six bits output on SDO will always be the first six bits from the status register. Register data is output on the SDO terminal msb first while STRn is low and changes to the next bit on each falling edge of SCK. The first bit, which is always the FF bit from the status register, is output as soon as STRn goes low.

Registers 23-24 and 28-30 contain verification results and diagnostic fault indicators and are read only. If the WR bit for these registers is set to 1 then the data input through SDI is ignored and the contents of the status register is clocked out on the SDO terminal then reset as for a normal write. No other action is taken. If the WR bit for these registers is set to 0, then the data input through SDI is ignored and the contents of the addressed register are clocked out on the SDO terminal and the addressed register is reset when DSR = 0.

If a framing error is detected and/or the parity of any received transfer is even rather than odd, the SE bit is set in the Status register to indicate a data transfer error. Any data write will be cancelled without latching data to the register and read-only registers will not be reset. This fault condition can be cleared by a subsequent valid serial write or by a power-on-reset.

In some systems, it is preferable to be able to read the status or diagnostic registers without causing a reset and allowing the AMT49106 to re-enable the outputs. The DSR (Disable Serial Reset) bit provides this functionality. When DSR is set to one, any valid read of any of the read-only registers will not result in that register being reset. When DSR = 0, any valid read of any of the read-only registers will reset the content of that register. This provides a way for the external controller to access the diagnostic information without automatically re-enabling any outputs but retains a way to reset the faults under control of the controller.

If V_{IO} is above the VIO POR threshold, the serial interface is operational, and it is possible to write to and read from registers as described, even if V_{BB} is below the VBB undervoltage threshold. However, most of the bits in the Verification Result, Diagnostic and Status registers will not report valid fault states when read.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Configuration Registers

Eighteen registers are used to configure the operating parameters of the AMT49106.

Config 0: Bridge timing settings:

- GTS, sets sleep mode if ENABLE input low.
- OCQ, selects the over current time qualifier mode, blank or debounce.
- DT[5:0], a 6-bit integer to set the dead time, t_{DEAD}, in 50 ns increments.

Config 1: Bridge monitor setting:

- OCT[3:0], a 4-bit integer to set the overcurrent threshold voltage, V_{OCT}, in 150 mV increments.
- TOC[4:0], a 5-bit integer to set the overcurrent verification time, t_{OCQ}, in 500 ns increments.

Config 2: Bridge monitor setting:

- VDQ, selects the VDS and VGS qualifier mode, blank or debounce.
- TVD[5:0], a 6-bit integer to set the VDS and VGS fault qualification time, t_{VDQ}, in 100 ns increments.

Config 3: Bridge monitor setting:

- VTL[5:0], a 6-bit integer to set the low-side drain-source threshold voltage, V_{DSTL}, in 50 mV increments.

Config 4: Bridge monitor setting:

- VTH[5:0], a 6-bit integer to set the high-side drain-source threshold voltage, V_{DSTH}, in 50 mV increments.

Config 5: Bridge monitor setting:

- AOL, Activate on-state open-load detection.
- CPM, selects VCP charge pump mode.
- OLT[3:0], a 4-bit integer to set the open-load threshold voltage, V_{OLTH}, in 25 mV increments.

Config 6: Bridge monitor setting:

- VLR, selects the VOOR voltage monitor level.
- VLM, selects the VIO voltage monitor level.
- VPT[5:0], a 6-bit integer to set the phase comparator threshold voltage, V_{PT}, as a ratio of the bridge voltage, V_{BB}, in 1.56% increments from 0 to 98.4%.

Config 7: Gate drive control (high-side timing):

- THR[3:0], a 4-bit integer to set the high-side rising (GHx low-to-high) I1 Time in 16 ns increments.
- THF[3:0], a 4-bit integer to set the high-side falling (GHx high-to-low) I1 Time in 16 ns increments.

Config 8: Gate drive control (high-side I1 Current):

- IHR1[3:0], a 4-bit integer to set the high-side rising (GHx low-to-high) I1 Current in 16 mA increments.
- IHF1[3:0], a 4-bit integer to set the high-side falling (GHx high-to-low) I1 Current in 16 mA increments.

Config 9: Gate drive control (high-side I2 current):

- IHR2[3:0], a 4-bit integer to set the high-side rising (GHx low-to-high) I2 Current in 16 mA increments.
- IHF2[3:0], a 4-bit integer to set the high-side falling (GHx high-to-low) I2 Current in 16 mA increments.

Config 10: Gate drive control (low-side timing):

- TLR[3:0], a 4-bit integer to set the low-side rising (GLx low-to-high) I1 Time in 16 ns increments.
- TLF[3:0], a 4-bit integer to set the low-side falling (GLx high-to-low) I1 Time in 16 ns increments.

Config 11: Gate drive control (low-side I1 current):

- ILR1[3:0], a 4-bit integer to set the low-side rising (GLx low-to-high) I1 Current in 16 mA increments.
- ILF1[3:0], a 4-bit integer to set the low-side falling (GLx high-to-low) I1 Current in 16 mA increments.

Config 12: Gate drive control (low-side I2 current):

- ILR2[3:0], a 4-bit integer to set the low-side rising (GLx low-to-high) I2 Current in 16 mA increments.
- ILF2[3:0], a 4-bit integer to set the low-side falling (GLx high-to-low) I2 Current in 16 mA increments.

Config 13: Sense amplifier offset and Watchdog timer:

- S3C, S2C, S1C, initiates current sense amplifier input offset calibration.
- WDC[1:0], a 2-bit integer to set number of acceptable attempt for mis-refresh.
- QAT[3:0], a 4-bit integer to set Q&A watchdog minimum and maximum timeout.

ALLEGRO microsystems
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Config 14: Sense amplifier gain:

- S3G[2:0], a 3-bit integer to set sense amplifier 3 gain between 7.5 and 25 V/V.
- S2G[2:0], a 3-bit integer to set sense amplifier 2 gain between 7.5 and 25 V/V.
- S1G[2:0], a 3-bit integer to set sense amplifier 1 gain between 7.5 and 25 V/V.

Config 15: NVM Write:

- SAV[1:0], Controls and reports saving the register contents of NVM.

Config 16: Q&A Watchdog:

- QA[7:0], a 7-bit pattern for the Q&A watchdog control.

Config 17: WD Mode:

- WDM[7:0], a 7-bit pattern for the watchdog control.

Stop-On Fault Registers

Two registers to control whether gate drive outputs are to remain enabled or be disabled in response to faults. See Diagnostics section for further detail of fault actions.

Stop on Fault 0:

One bit per fault type to define stop on fault behavior for OT, TW, LCD, LBD, LAD, VCPU, SE, VD, VLO and WD diagnostics.

Stop on Fault 1:

One bit per fault type to define stop on fault behavior for OC, DSO, GSU, VBU, VRO, VRU, VSO and VSU diagnostics.

Verification Registers

Five registers are used to manage the system and diagnostic verification features.

Verify Command 0:

Individual bits to initiate off-line verification tests for VDS, VREG, Bootstrap undervoltage, logic overvoltage, VBB, and VGS diagnostics.

Verify Command 1:

Individual bits to initiate off-line verification tests for phase disconnect, overcurrent, logic undervoltage, and open-load diagnostics.

Verify Command 2:

Individual bits to initiate off-line verification tests for TW, OT LSS disconnect, VCPU, VIO, and VOOR diagnostics.

Verify Result 0 (read only):

Individual bits holding the results of the phase disconnect, the watchdog errors and the LSS disconnect verification tests. When DSR = 0, these bits are reset on completion of a successful read of the register.

Verify Result 1 (read only):

Individual bits holding the results of gate drive off, phase state and sense amplifier verification tests. When DSR = 0 these bits are reset on completion of a successful read of the register.

Diagnostic Registers

In addition to the read-only status register, three read-only diagnostic registers provide detailed diagnostic management and reporting. When DSR = 0, any bits set in a diagnostic register are reset on completion of a successful read of that register. When DSR = 1, the register will not be reset. Reading one diagnostic register will not affect the fault bits in any other register. Reading the status register will not affect fault bits in any diagnostic register.

Diagnostic 0 (read only):

VGS undervoltage monitor bits for each gate drive output, a VCP undervoltage bit and composite bit indicating VIO or VOOR out-of-range.

Diagnostic 1 (read only):

Individual bits indicating faults detected by VREG diagnostic monitors and VDS monitors.

Diagnostic 2 (read only):

Individual bits indicating faults detected by bootstrap undervoltage, VBB, overcurrent, and open load diagnostic monitors.

Mask Registers

Three mask registers allow individual diagnostics to be disabled. If a bit is set to one in the mask registers, then the corresponding diagnostic will be completely disabled. No fault states for the disabled diagnostic will be generated, no fault flags or diagnostic bits will be set, and no action will be taken if the corresponding fault conditions are present.

Mask 0:

Individual bits to separately disable the VGS gate drive output diagnostics plus bits to disable the VCP undervoltage and composite VIO/VOOR out of range diagnostics.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Mask 1:

Individual bits to disable VDS diagnostic monitors for each gate drive output and the VREG monitor.

Mask 2:

Individual bits to disable VBB, logic, bootstrap, temperature, LSS disconnect, and logic regulator undervoltage diagnostic monitors.

Control Register

The Control register contains one control bit for each MOSFET and some system function settings:

- DG[1:0], a two-bit integer to select the signal output on the DIAG terminal.
- DSR, disables reset on serial transfer.
- CH, CL, MOSFET Control bits for Phase C.
- BH, BL, MOSFET Control bits for Phase B.
- AH, AL, MOSFET Control bits for Phase A.

Status Register

There is one status register in addition to the addressable registers. When any register transfer takes place, the first six bits output on SDO are always the most significant six bits of the status register irrespective of whether the addressed register is being read or written (see Serial Timing diagram).

The content of the remaining ten bits will depend on the state of the WR bit input on SDI. Except for the read-only registers, when WR is 1, the addressed register will be written and the remaining ten bits output on SDO will be the least significant nine bits of the status register followed by a parity bit. For the read-only registers, that is the two verification result registers and the three diagnostic registers, when WR is 1, the data bits will be ignored, no data will be written to the register and the remaining ten bits output on SDO will be the least significant nine bits of the status register followed by a parity bit. For both read-only and read/write registers, when WR is 0, the addressed register will be read, and the remaining ten bits will be the contents of the addressed register followed by a parity bit.

The read only status register provides a summary of the chip status by indicating if any diagnostic monitors have detected a fault. The most significant four bits of the status register indicate critical system faults. Bits 11 through 1 provide indicators for specific individual monitors and the contents of the three diagnostic registers. The contents and mapping to the diagnostic registers is listed in Table 9.

The first most significant bit in the register is the diagnostic status flag, FF. This is high if any bits in the status register are set. If there are no fault bits in the status register, then FF will be zero. When STRn goes low to start a serial write, SDO outputs the diagnostic status flag. This allows the main controller to poll the AMT49106 through the serial interface to determine if a fault has been detected. If no faults have been detected, then the serial transfer may be terminated without generating a serial read fault by ensuring that SCK remains high while STRn is low. When STRn goes high, the transfer will be terminated and SDO will go into its high impedance state.

The second most significant bit is the POR bit. At power-up or after a power-on-reset, the FF bit and the POR bit are set, indicating to the external controller that a power-on-reset has taken place. All other diagnostic bits are reset, and all other registers are returned to their default state. Note that a power-on-reset only occurs when the output of the internal logic regulator rises above its undervoltage threshold. Power-on-reset is not affected by the state of the VBB supply or VREG regulator output. In general, the VR, VRU, and VD bits may also be set following a power-on reset as the regulators will not have reached their respective rising undervoltage thresholds until after the register reset is completed.

Table 9: Status Register Mapping

Status Register Bit	Diagnostic	Related Diagnostic Register Bits
FF	Status Flag	None
POR	Power-on-Reset	None
SE	Serial Error	None
EE	EEPROM Error	None
OT	Overtemperature	None
TW	Temperature Warning	None
VS	VBB Out of Range	VSU, VSO
VLO	Logic OV	None
WD	Watchdog Error	QTO, QAE
VR	Regulator Monitor	VRU. VRO, VCPU
VD	VIO or VOOR Out of Range	VDO, VDU
LDF	Load Monitor	OC1, OC2, OC3, OL
BSU	Bootstrap UV	VA, VB, VC
GSU	VGS UV	AHU, BHU, CHU, ALU, BLU, CLU
DSO	VDS OV	AHO, BHO, CHO ALO, BLO, CLO

UV = Undervoltage, OV = Overvoltage

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

The third bit in the status register is the SE bit, which indicates that the previous serial transfer was not completed successfully.

The fourth bit in the Status register is the EE bit, which indicates that an EEPROM error was detected at device power-up.

Of the remaining bits, the contents of OT, TW, and VLO are determined by individual diagnostics. These bits along with the POR and SE bits will be reset on the completion of a successful serial write transaction if DSR = 0. If DSR = 1, the fault bits will not be affected. Resetting only affects latched fault bits for faults that are no longer present. For any static faults that are still present, for example overtemperature, the fault flag will remain set after the reset.

The contents of the remaining bits in the status register, VS, WD, VR, VD, LDF, BSU, GSU, and DSO are all derived from the contents of the diagnostic registers. These bits are only cleared when the corresponding contents of the diagnostic registers are reset, they cannot be reset by reading the status register. A fault indicated on any of the related diagnostic register bits will set the corresponding status register bit to 1. The related diagnostic register must then be read to determine the exact fault and clear the fault state if the fault condition has cleared.

Non-Volatile Memory

The values in the configuration and control registers are held in non-volatile EEPROM (NVM), allowing the AMT49106 to be pre-programmed with different user-defined register values for each application, thus avoiding the need to program the register contents at each power on.

The AMT49106 provides a simple method to write the contents of the registers into the NVM using the serial interface. When the SAV[1:0] bits in register 15 are changed from [01] to [10], in a single serial write, the present contents of registers 0 to 14, excluding register 0 bit 9 (GTS), registers 18 to 19, 25 to 27 and 31 are saved (written to NVM) as a single operation. The save sequence takes typically 400 ms to complete. It is not possible to save single register values. Although the motor may be operating during the save sequence, it is recommended that the motor drive is disabled before starting a save sequence to avoid any corruption caused by the electrical noise or any faults from the motor.

Note that the GTS bit (register 0[9]) is not saved. This is to avoid a lockout condition where the AMT49106 is commanded to go to sleep as soon as the wake-up sequence is complete.

The register save sequence requires a programming voltage V_{PP} to be applied to the VBB terminal. V_{PP} must be present on the VBB terminal for a period, t_{PRS}, before the save sequence is started. V_{PP} must remain on VBB until the save sequence is completed.

During the save sequence, the SPI remains active for read only. Any attempt to write to the registers during the save sequence will cause the FF and SE bits to be set in the Status register.

During the save sequence, the AMT49106 will automatically complete all the necessary steps to ensure that the NVM is correctly programmed and will complete the sequence by verifying that the contents of the NVM have been securely programmed. On successful completion of a save sequence, the SAV[1:0] bits will be set to [01]. Register 15 should be read to determine if the save has completed successfully. If SAV[1:0] is reset to [00], then the save sequence has been terminated and has not completed successfully.

If V_{PP} drops to an unacceptably low level during a save sequence, the sequence will be terminated and SAV[1:0] will be reset to 00.

To externally verify the data saved in the NVM, the VBB supply must be cycled off, then on to cause a power-on reset. Following a power-on reset, the contents of the NVM are copied to the serial registers which can then be read through the serial interface and verified.

Refer to the NVM - Programming Parameters section of the Electrical Characteristics table for the permissible number of EEPROM write cycles and the maximum junction temperature limit that applies during programming.

ALLEGRO microsystems
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0: Config 0	0	0	0	0	0	WR	GTS	OCQ		DT5	DT4	DT3	DT2	DT1	DT0	P
							0	0	0	1	1	1	1	1	1	
1: Config 1	0	0	0	0	1	WR	OCT3	OCT2	OCT1	OCT0	TOC4	TOC3	TOC2	TOC1	TOC0	P
							0	1	0	1	0	1	1	1	1	

*Power-on reset value shown below each input register bit.

Config 0

GTS Go to sleep command

GTS	State	Default
0	Awake	D
1	Sleep (if ENABLE low)	
0 → 1	Wake up	

OCQ Overcurrent time qualifier mode

OCQ	Qualifier	Default
0	Debounce	D
1	Blanking	

DT[5:0] Dead time.

$t_{DEAD} = n \times 50$ ns

where where n is a positive integer defined by DT[5:0]. For example, for the power-on reset condition, DT[5:0] = [11 1111], t_{DEAD} = 3.15 µs.

The range of t_{DEAD} is 100 ns to 3.15 µs. Selecting a value of 1 or 2 will set the dead time to 100 ns. Setting DT = 0 disables the dead time.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Config 1

OCT[3:0] Overcurrent threshold.

$V_{OCT} = (n + 1) \times 150$ mV

where n is a positive integer defined by OCT[3:0], e.g. for the power-on-reset condition OCT[3:0] = [0101] then V_{OCT} = 0.9 V. The range of V_{OCT} is 0.15 to 2.4 V.

TOC[4:0] Overcurrent qualify time.

$t_{OCQ} = n \times 500$ ns

where n is a positive integer defined by TOC[4:0], e.g. for the power-on-reset condition TOC[4:0] = [0 1111] then t_{OCQ} = 7.5 µs. The range of t_{OCQ} is 0 to 15.5 µs.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2: Config 2	0	0	0	1	0	WR	VDQ			TVD5	TVD4	TVD3	TVD2	TVD1	TVD0	P
							0	0	0	0	1	0	0	0	0	
3: Config 3	0	0	0	1	1	WR				VTL5	VTL4	VTL3	VTL2	VTL1	VTL0	P
							0	0	0	0	1	1	0	0	0	

*Power-on reset value shown below each input register bit.

Config 2

VDQ VDS and VGS Fault qualifier mode.

VDQ	VDS and VGS Fault Qualifier	Default
0	Debounce	D
1	Blank	

TVD[5:0] VDS and VGS qualification time.

$t_{VDQ} = n \times 100$ ns

where n is a positive integer defined by TVD[5:0].
e.g. for the power-on-reset condition
TVD[5:0] = [01 0000] then t_{VDQ} = 1.6 µs.
The range of t_{VDQ} is 0.6 to 6.3 µs.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Config 3

VTL[5:0] Low-side VDS overvoltage threshold.

$V_{DSTL} = n \times 50$ mV

where n is a positive integer defined by VTL[5:0],
e.g. for the power-on-reset condition
VTL[5:0] = [01 1000] then V_{DSTL} = 1.2 V.
The range of V_{DSTL} is 0 to 3.15 V.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
4: Config 4	0	0	1	0	0	WR				VTH5	VTH4	VTH3	VTH2	VTH1	VTH0	P
							0	0	0	0	1	1	0	0	0	
5: Config 5	0	0	1	0	1	WR	AOL	CPM1	CPM0			OLT3	OLT2	OLT1	OLT0	P
							0	0	0	0	0	1	0	0	0	

*Power-on reset value shown below each input register bit.

Config 4

VTH[5:0] High-side VDS overvoltage threshold.

$V_{DSTH} = n \times 50$ mV

where n is a positive integer defined by VTH[5:0], e.g. for the power-on-reset condition VTH[5:0] = [01 1000] then V_{DSTH} = 1.2 V. The range of V_{DSTH} is 0 to 3.15 V.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Config 5

AOL On-state open-load detect.

AOL	On-State Open-Load Detect	Default
0	Inactive	D
1	Active	

CPM VCP Charge pump mode.

CPM1	CPM0	VCP Charge pump mode	Default
0	0	Auto 5 mA / 200 µA	D
0	1	200 µA	
1	0	5 mA	
1	1	Off	

OLT[3:0] Open-load threshold.

$V_{OLTH} = (n + 1) \times 25$ mV

where n is a positive integer defined by OLT[3:0], e.g. for the power-on-reset condition OL[3:0] = [1000] then V_{OLT} = 225 mV. The range of V_{OLTH} is 25 to 400 mV.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
6: Config 6	0	0	1	1	0	WR	VLR	VLM		VPT5	VPT4	VPT3	VPT2	VPT1	VPT0	P
							0	0	0	1	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Config 6

VLR VOOR Voltage Monitor.

VLR	Nominal V_{OOR} Voltage	Default
0	3.3 V	D
1	5 V	

VLM VIO Voltage Monitor.

VLM	Nominal V_{IO} Voltage	Default
0	3.3 V	D
1	5 V	

VPT[5:0] Phase comparator threshold.

$V_{PT} = (n / 64) \times V_{BB}$

where n is a positive integer defined by VPT[5:0], e.g. for the power-on-reset condition VPT[5:0] = [10 0000] then V_{PT} = 50% V_{BB}. The range of V_{PT} is 0 to 98.4% V_{BB}.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
7:Config 7	0	0	1	1	1	WR		THR3	THR2	THR1	THR0	THF3	THF2	THF1	THF0	P
							0	0	0	0	0	0	0	0	0	
8:Config 8	0	1	0	0	0	WR		IHR13	IHR12	IHR11	IHR10	IHF13	IHF12	IHF11	IHF10	P
							0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Config 7

THR[3:0] High-side rising t1 Time.

$t_1 = 60\ \text{ns} + (n \times 16\ \text{ns})$

where n is a positive integer defined by THR[3:0], e.g. if THR[3:0] = [0001] then t_1 = 76 ns. The range of t_1 is 60 to 300 ns.

THF[3:0] High-side falling t1 Time.

$t_1 = 60\ \text{ns} + (n \times 16\ \text{ns})$

where n is a positive integer defined by THF[3:0], e.g. if THF[3:0] = [0001] then t_1 = 76 ns. The range of t_1 is 60 to 300 ns.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Config 8

IHR1[3:0] High-side rising I1 Current.

$I_1 = n \times -16\ \text{mA}$

where n is a positive integer defined by IHR1[3:0], e.g. if IHR1[3:0] = [1000] then I_1 = –128 mA. The range of I_1 is –16 to –240 mA. Selecting a value of 0 will set maximum gate drive to turn on the MOSFET as quickly as possible.

IHF1[3:0] High-side falling I1 Current.

$I_1 = n \times 16\ \text{mA}$

where n is a positive integer defined by IHF1[3:0], e.g. if IHF1[3:0] = [1000] then I_1 = 128 mA. The range of I_1 is 16 to 240 mA. Selecting a value of 0 will set maximum gate drive to turn off the MOSFET as quickly as possible.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
9:Config 9	0	1	0	0	1	WR		IHR23	IHR22	IHR21	IHR20	IHF23	IHF22	IHF21	IHF20	P
							0	0	0	0	0	0	0	0	0	
10:Config 10	0	1	0	1	0	WR		TLR3	TLR2	TLR1	TLR0	TLF3	TLF2	TLF1	TLF0	P
							0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Config 9

IHR2[3:0] High-side rising I2 Current.

$I_2 = n \times -16$ mA

where n is a positive integer defined by IHR2[3:0], e.g. if IHR2[3:0] = [1000] then $I_2 = -128$ mA. The range of I_2 is –16 to –240 mA. Selecting a value of 0 will set maximum gate drive to turn on the MOSFET as quickly as possible.

IHF2[3:0] High-side falling I2 Current.

$I_2 = n \times 16$ mA

where n is a positive integer defined by IHF2[3:0], e.g. if IHF2[3:0] = [1000] then $I_2 = 128$ mA. The range of I_2 is 16 to 240 mA. Selecting a value of 0 will set maximum gate drive to turn off the MOSFET as quickly as possible.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Config 10

TLR[3:0] Low-side rising t1 Time.

$t_1 = 60$ ns + ($n \times 16$ ns)

where n is a positive integer defined by TLR[3:0], e.g. if TLR[3:0] = [0001] then $t_1 = 76$ ns. The range of t_1 is 60 to 300 ns.

TLF[3:0] Low-side falling t1 Time.

$t_1 = 60$ ns + ($n \times 16$ ns)

where n is a positive integer defined by TLF[3:0], e.g. if TLF[3:0] = [0001] then $t_1 = 76$ ns. The range of t_1 is 60 to 300 ns.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
11:Config 11	0	1	0	1	1	WR		ILR13	ILR12	ILR11	ILR10	ILF13	ILF12	ILF11	ILF10	P
							0	0	0	0	0	0	0	0	0	
12:Config 12	0	1	1	0	0	WR		ILR23	ILR22	ILR21	ILR20	ILF23	ILF22	ILF21	ILF20	P
							0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Config 11

ILR1[3:0] Low-side rising I1 Current.

$I_1 = n \times -16$ mA

where n is a positive integer defined by ILR1[3:0], e.g. if ILR1[3:0] = [1000] then $I_1 = -128$ mA. The range of I_1 is –16 to –240 mA. Selecting a value of 0 will set maximum gate drive to turn on the MOSFET as quickly as possible.

ILF1[3:0] Low-side falling I1 Current.

$I_1 = n \times 16$ mA

where n is a positive integer defined by ILF1[3:0], e.g. if ILF1[3:0] = [1000] then $I_1 = 128$ mA. The range of I_1 is 16 to 240 mA. Selecting a value of 0 will set maximum gate drive to turn off the MOSFET as quickly as possible.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Config 12

ILR2[3:0] Low-side rising I2 Current.

$I_2 = n \times -16$ mA

where n is a positive integer defined by ILR2[3:0], e.g. if ILR2[3:0] = [1000] then $I_2 = -128$ mA. The range of I_1 is –16 to –240 mA. Selecting a value of 0 will set maximum gate drive to turn on the MOSFET as quickly as possible.

ILF2[3:0] Low-side falling I2 Current.

$I_2 = n \times 16$ mA

where n is a positive integer defined by ILF2[3:0], e.g. if ILF2[3:0] = [1000] then $I_2 = 128$ mA. The range of I_2 is 16 to 240 mA. Selecting a value of 0 will set maximum gate drive to turn off the MOSFET as quickly as possible.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
13:Config 13	0	1	1	0	1	WR	S3C	S2C	S1C	WDC1	WDC0	QAT3	QAT2	QAT1	QAT0	P
							0	0	0	0	0	0	0	0	0	
14:Config 14	0	1	1	1	0	WR	S3G2	S3G1	S3G0	S2G2	S2G1	S2G0	S1G2	S1G1	S1G0	P
							0	1	0	0	1	0	0	1	0	

*Power-on reset value shown below each input register bit.

Config 13

S3C Sense amplifier 3 input offset calibrate

S2C Sense amplifier 2 input offset calibrate

S1C Sense amplifier 1 input offset calibrate

A zero to one transition initiates calibration cycle.

WDC[1:0] Watchdog failure count threshold.

WDC	Watchdog Fail Count	Default
0	0	D
1	1	
2	3	
3	7	

QAT[3:0] Q&A watchdog timeout.

QAT	Minimum	Maximum	Default
0	0.1 ms	0.2 ms	D
1	0.2 ms	0.4 ms	
2	0.4 ms	0.8 ms	
3	0.6 ms	1.2 ms	
4	0.8 ms	1.6 ms	
5	1 ms	2 ms	
6	2 ms	4 ms	
7	4 ms	8 ms	
8	6 ms	12 ms	
9	8 ms	16 ms	
10	10 ms	20 ms	
11	12 ms	24 ms	
12	14 ms	28 ms	
13	16 ms	32 ms	
14	18 ms	36 ms	
15	20 ms	40 ms	

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Config 14

S3G[2:0] Sense amplifier 3 gain.

S3G	Gain	Default
0	7.5	
1	10	
2	12.5	D
3	15	
4	17.5	
5	20	
6	22.5	
7	25	

S2G[2:0] Sense amplifier 2 gain.

S2G	Gain	Default
0	7.5	
1	10	
2	12.5	D
3	15	
4	17.5	
5	20	
6	22.5	
7	25	

S1G[2:0] Sense amplifier 1 gain.

S1G	Gain	Default
0	7.5	
1	10	
2	12.5	D
3	15	
4	17.5	
5	20	
6	22.5	
7	25	

where SxG is a positive integer defined by SxG[2:0].

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
15: NVM Write	0	1	1	1	1	WR	SAV1	SAV0								P
							0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Write NVM Control

SAV[1:0] Save parameters to Non-Volatile Memory (NVM)

When SAV[1:0] are changed from [01] to [10], the present contents of registers 0 to 14, excluding register 0 bit 9 (GTS), registers 18 to 19, 25 to 27 and 31 are written to NVM.
When the NVM save has completed successfully, SAV[1:0] bits will be set to [01] and can be read to verify completion of the write. If SAV[1:0] is reset to [00], the save has not completed successfully.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
16: Q&A Watchdog	1	0	0	0	0	WR		QA7	QA6	QA5	QA4	QA3	QA2	QA1	QA0	P
							0	0	0	0	0	0	0	0	0	
17: WD Mode	1	0	0	0	1	WR		WDM7	WDM6	WDM5	WDM4	WDM3	WDM2	WDM0	WDM0	P
							0	1	0	1	0	1	0	1	0	

*Power-on reset value shown below each input register bit.

Q&A Watchdog

QA[7:0] Q&A watchdog control register

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Q&A Watchdog look-up table

Address[3:0]	Answer Code[7:0]
0x0	0xA5
0x1	0x1D
0x2	0xD7
0x3	0x6E
0x4	0xFE
0x5	0xF3
0x6	0x3E
0x7	0xC4
0x8	0xAD
0x9	0x8F
0xA	0x2F
0xB	0x09
0xC	0xC6
0xD	0xCA
0xE	0x46
0xF	0x10

Number is written in hexadecimal

Watchdog Mode

WDM[7:0] Watchdog Mode Selector

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Mode confirmation (Read back)

WDM[7:0]	Device Mode	Default
0xAA	Bridge Disable (Gate Drive Outputs Low)	D
0x55	Q&A Watchdog Active	
0xEE	Q&A watchdog Inactive	

Number is written in hexadecimal

Mode Change (Write)

Mode	SEQ0	SEQ1	SEQ2
Bridge Disable Mode	0xA0	0x23	0x61
Q&A Watchdog Active	0xA1	0x78	0x98
Bridge Active & Q&A watchdog disabled	0xA2	0xCD	0x88

Number is written in hexadecimal

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
18: Stop on Fault 0	1	0	0	1	0	WR	FOT	FTW		FLSS	FCPU	FSE	FVDD	FVLO	FWD	P
							1	1	0	0	0	1	1	1	1	
19: Stop on Fault 1	1	0	0	1	1	WR	FOC		FDSO	FGSU	FVBU	FVRO	FVRU	FVSO	FVSU	P
							1	0	1	1	1	1	1	1	1	

*Power-on reset value shown below each input register bit.

Stop on Fault 0

- FOT Overtemperature
- FTW Temperature Warning
- FLSS LSS Disconnect
- FCPU VCP Undervoltage
- FSE Serial Error
- FVDD VIO or VOOR Out of Range
- FVLO Logic Overvoltage
- FWD WD Error

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Stop on Fault 1

- FOC Overcurrent
- FDSO VDS Overvoltage
- FGSU VGS Undervoltage
- FVBU Bootstrap Undervoltage
- FVRO VREG Overvoltage
- FVRU VREG Undervoltage
- FVSO VBB Overvoltage
- FVSU VBB Undervoltage

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
20: Verify Command 0	1	0	1	0	0	WR			YDO	YRO	YRU	YBU	YSO	YSU	YGU	P
							0	0	0	0	0	0	0	0	0	
21: Verify Command 1	1	0	1	0	1	WR	YPH	YPL	YOC	YLO	YOL	YPS1	YPS0	YSK	YSC	P
							0	0	0	0	0	0	0	0	0	
22: Verify Command 2	1	0	1	1	0	WR	YTW	YOT		YLS	YCP	YIO	YIU	YMO	YMU	P
							0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Verify Command 0

YDO VDS Overvoltage
YRO VREG Overvoltage
YRU VREG Undervoltage
YBU Bootstrap Capacitor Undervoltage
YSO VBB Supply Overvoltage
YSU VBB Supply Undervoltage
YGU VGS Undervoltage

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Verify Command 1

YPH Phase Disconnect High-Side
YPL Phase Disconnect Low-Side
YOC Overcurrent
YLO Logic Input Overvoltage
YOL On-State Open Load

YPS[1:0] Phase diagnostic select.

YPS1	YPS0	Signal on DIAG output	Default
0	0	Phase B Disconnect	D
0	1	Phase A Disconnect	
1	0	Phase C Disconnect	
1	1	Off-state open load*	

YSK I_{SD} (2.5 mA) sink on phase selected by YPS*
YSC I_{SU} (–410 µA) source on phase selected by YPS*

* When YPS = 3, Phase B has a fixed 2.5 mA sink and the source current on phases A and C are common and set by YSC.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Verify Command 2

YTW Temperature Warning
YOT Overtemperature
YLS LSS Disconnect
YIO VIO Overvoltage
YIU VIO Undervoltage
YMO VOOR Overvoltage
YMU VOOR Undervoltage
YCP VCP Undervoltage

P Parity bit. Ensures an odd number of 1s in any serial transfer.

For All Verify Command Registers

Yxx	Verification	Default
0	Inactive	D
1	Active and Initiate	

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
23: Verify Result 0	1	0	1	1	1	WR	PCD	PBD	PAD	QAE	QTO		LCD	LBD	LAD	P
							0	0	0	0	0	0	0	0	0	
24: Verify Result 1	1	1	0	0	0	WR			GDO	SCS	SBS	SAS	S3D	S2D	S1D	P
							0	0	1	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Verify Result 0 (read only)

PCD Phase C disconnect

PBD Phase B disconnect

PAD Phase A disconnect

QAE Q&A watchdog Answer error

QTO Q&A watchdog timeout

LCD LSSC disconnect

LBD LSSB disconnect

LAD LSSA disconnect

xxx	Verification Result	Default
0	Not detected	D
1	Detected	

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Verify Result 1 (read only)

GDO All gate drives off

SCS Phase C state

SBS Phase B state

SAS Phase A state

S3D Sense amp 3 disconnect

S2D Sense amp 2 disconnect

S1D Sense amp 1 disconnect

xxx	Verification Result	Default
0	Not detected	D
1	Detected	

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
25: Mask 0	1	1	0	0	1	WR	VCPU	VDU	VDO	CHU	CLU	BHU	BLU	AHU	ALU	P
							0	0	0	0	0	0	0	0	0	
26: Mask 1	1	1	0	1	0	WR	VRO	VRU		CHO	CLO	BHO	BLO	AHO	ALO	P
							0	0	0	0	0	0	0	0	0	
27: Mask 2	1	1	0	1	1	WR	VS	VLO	BSU	TW			LCD	LBD	LAD	P
							0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Mask 0

VCPU VCP undervoltage
VDU VIO or VOOR undervoltage
VDO VIO or VOOR overvoltage
CHU Phase C high-side VGS undervoltage
CLU Phase C low-side VGS undervoltage
BHU Phase B high-side VGS undervoltage
BLU Phase B low-side VGS undervoltage
AHU Phase A high-side VGS undervoltage
ALU Phase A low-side VGS undervoltage

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Mask 1

VRO VREG Overvoltage
VRU VREG Undervoltage
CHO Phase C high-side VDS overvoltage
CLO Phase C low-side VDS overvoltage
BHO Phase B high-side VDS overvoltage
BLO Phase B low-side VDS overvoltage
AHO Phase A high-side VDS overvoltage
ALO Phase A low-side VDS overvoltage

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Mask 2

VS VBB out of range
VLO Logic Overvoltage
BSU Bootstrap Undervoltage
TW Temperature Warning
LCD Phase C LSS disconnect
LBD Phase B LSS disconnect
LAD Phase A LSS disconnect

P Parity bit. Ensures an odd number of 1s in any serial transfer.

For All Mask Registers

xxx	Fault Mask	Default
0	Fault detection permitted	D
1	Fault detection disabled	

If a bit is set to one in the mask registers, then the corresponding diagnostic will be completely disabled. No fault states for the disabled diagnostic will be generated, no fault flags or diagnostic bits will be set, and no action will be taken if the corresponding fault conditions are present.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
28: Diagnostic 0	1	1	1	0	0	WR	VCPU	VDU	VDO	CHU	CLU	BHU	BLU	AHU	ALU	P
							0	0	0	0	0	0	0	0	0	
29: Diagnostic 1	1	1	1	0	1	WR	VRO	VRU		CHO	CLO	BHO	BLO	AHO	ALO	P
							0	0	0	0	0	0	0	0	0	
30: Diagnostic 2	1	1	1	1	0	WR	VC	VB	VA	VSO	VSU	OC3	OC2	OC1	OL	P
							0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Diag 0 (read only)

VCPU VCP undervoltage

VDU VIO or VOOR undervoltage

VDO VIO or VOOR overvoltage

CHU Phase C high-side VGS undervoltage

CLU Phase C low-side VGS undervoltage

BHU Phase B high-side VGS undervoltage

BLU Phase B low-side VGS undervoltage

AHU Phase A high-side VGS undervoltage

ALU Phase A low-side VGS undervoltage

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Diag 1 (read only)

VRO VREG overvoltage

VRU VREG undervoltage

CHO Phase C high-side VDS overvoltage

CLO Phase C low-side VDS overvoltage

BHO Phase B high-side VDS overvoltage

BLO Phase B low-side VDS overvoltage

AHO Phase A high-side VDS overvoltage

ALO Phase A low-side VDS overvoltage

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Diag 2 (read only)

VC Phase C bootstrap undervoltage

VB Phase B bootstrap undervoltage

VA Phase A bootstrap undervoltage

VSO VBB overvoltage

VSU VBB undervoltage

OC3 Overcurrent on sense amp 3

OC2 Overcurrent on sense amp 2

OC1 Overcurrent on sense amp 1

OL Open load

P Parity bit. Ensures an odd number of 1s in any serial transfer.

For All Diagnostic Registers

xxx	Status	Default
0	No fault detected	D
1	Fault detected	

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
31: Control	1	1	1	1	1	WR	DG1	DG0	DSR	CH	CL	BH	BL	AH	AL	P
							0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Control

DG[1:0] Selects signal routed to DIAG.

DG1	DG0	Signal on DIAG Pin	Default
0	0	Fault – low true	D
0	1	Pulse Fault	
1	0	Temperature	
1	1	Clock	

DSR Disable Serial Reset.

DSR	Reset on serial read	Default
0	Enabled	D
1	Disabled	

CH Phase C, High-side gate drive

CL Phase C, Low-side gate drive

BH Phase B, High-side gate drive

BL Phase B, Low-side gate drive

AH Phase A, High-side gate drive

AL Phase A, Low-side gate drive

See Table 2 and Table 3 for control logic operation.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Status	FF	POR	SE	EE	OT	TW	VS	VLO	WD	VR	VD	LDF	BSU	GSU	DSO	P
	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Status

FF Status register flag

POR Power-on-reset

SE Serial Error

EE EEPROM fault

OT Overtemperature

TW High temperature warning

VS VBB out of range

VLO Logic overvoltage

WD Watchdog error

VR Regulator voltage out of range

VD VIO or VOOR out of range

LDF Load fault

BSU Bootstrap undervoltage

GSU VGS undervoltage

DSO VDS overvoltage

xxx	Status
0	No fault detected
1	Fault detected

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Status Register Bit Mapping

Status Register Bit	Related Diagnostic Register Bits
FF	None
POR	None
SE	None
EE	None
OT	None
TW	None
VS	VSU, VSO
VLO	None
WD	QTO, QAE
VR	VRU, VRO, VCPU
VD	VDU, VDO
LDF	OC1, OC2, OC3, OL [1]
BSU	VA, VB, VC
GSU	AHU, ALU, BHU, BLU, CHU, CLU
DSO	AHO, ALO, BHO, BLO, CHO, CLO

[1] LDF bit set in response to on-state open-load conditions but not off-state open load conditions.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

APPLICATION INFORMATION

Bootstrap Capacitor Selection

C_{BOOT}, must be correctly selected to ensure proper operation of the device. Too large and time will be wasted charging the capacitor, resulting in a limit on the PWM frequency. Too small and there can be a large voltage drop at the time the charge is transferred from C_{BOOT} to the MOSFET gate.

To keep the voltage drop due to charge sharing small, the charge in the bootstrap capacitor, Q_{BOOT}, should be much larger than Q_{GATE}, the charge required by the gate:

$$Q_{BOOT} \gg Q_{GATE}$$

A factor of 20 is a reasonable value:

$$Q_{BOOT} = C_{BOOT} \times V_{BOOT} = Q_{GATE} \times 20$$

or

$$C_{BOOT} = \frac{Q_{GATE} \times 20}{V_{BOOT}}$$

where V_{BOOT} is the voltage across the bootstrap capacitor.

The voltage drop, ΔV, across the bootstrap capacitor as the MOSFET is being turned on, can be approximated by:

$$\Delta V = \frac{Q_{GATE}}{C_{BOOT}}$$

So for a factor of 20, ΔV will be 5% of V_{BOOT}.

The maximum voltage across the bootstrap capacitor under normal operating conditions is V_{REG}(max). However, in some circumstances, the voltage may transiently reach a maximum of 18 V, which is the clamp voltage of the Zener diode between the Cx terminal and the Sx terminal. In most applications with a good ceramic capacitor, the working voltage can be limited to 16 V (rated voltage).

VREG Capacitor Selection

The internal reference, VREG, supplies current for the low-side gate drive circuits and the charging current for the bootstrap capacitors. When a low-side MOSFET is turned on, the gate-drive circuit will provide the high transient current to the gate that is necessary to turn the MOSFET on quickly. This current, which can be several hundred milliamperes, cannot be provided directly by the limited output of the VREG regulator but must be supplied by an external capacitor connected to VREG.

The turn on current for the high-side MOSFET is similar in value, but is mainly supplied by the bootstrap capacitor. However, the bootstrap capacitor must then be recharged from the VREG regulator output. Unfortunately, the bootstrap recharge can occur a very short time after the low-side turn-on occurs. This means that the value of the capacitor connected between VREG and AGND should be high enough to minimize the transient voltage drop on VREG for the combination of a low-side MOSFET turn-on and a bootstrap capacitor recharge. For block commutation control (trapezoidal drive), where only one high side and one low side is switching during each PWM period, a minimum value of 20 × C_{BOOT} is reasonable. For sinusoidal control schemes, a minimum value of 40 × C_{BOOT} is recommended. The maximum working voltage of the VREG capacitor will never exceed V_{REG}, so it can be as low as 15 V. This capacitor should be placed as close as possible to the VREG terminal.

Supply Decoupling

Since this is a switching circuit, there will be current spikes from all supplies at the switching points. As with all such circuits, the power supply connections should be decoupled by ceramic capacitors to ground. These should be connected as close as possible to the supply terminals, VBB and VIO, and the ground terminal, GND. It is recommended that 100 nF and 470 nF capacitors are fitted to VBB and VIO respectively.

Power Dissipation

In applications where a high ambient temperature is expected, the on-chip power dissipation may become a critical factor. Careful attention should be paid to ensure the operating conditions allow the AMT49106 to remain in a safe range of junction temperature.

The power consumed by the AMT49106, P_D, can be estimated by:

$$P_D = P_{BIAS} + P_{CPUMP} + P_{SWITCHING}$$
$$P_{BIAS} = (V_{BB} \times I_{BB}) + (V_{IO} \times I_{IOQ})$$
$$P_{CPUMP} = ((3 \times V_{BB}) - V_{REG}) \times I_{AVE} \quad (for\ V_{BB} < 7\ V)$$
$$P_{CPUMP} = ((2 \times V_{BB}) - V_{REG}) \times I_{AVE} \quad (for\ V_{BB} < 16\ V)$$
$$P_{CPUMP} = (V_{BB} - V_{REG}) \times I_{AVE} \quad (for\ V_{BB} > 16\ V)$$

where: $I_{AVE} = Q_{GATE} \times N \times f_{PWM}$

$$P_{SWITCHING} = Q_{GATE} \times V_{REG} \times N \times f_{PWM} \times Ratio$$

where: $$Ratio = \frac{10}{(R_{GATE} + 10)}$$

and N = number of MOSFETs switching during a PWM cycle.

ALLEGRO microsystems
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

INPUT/OUTPUT STRUCTURES

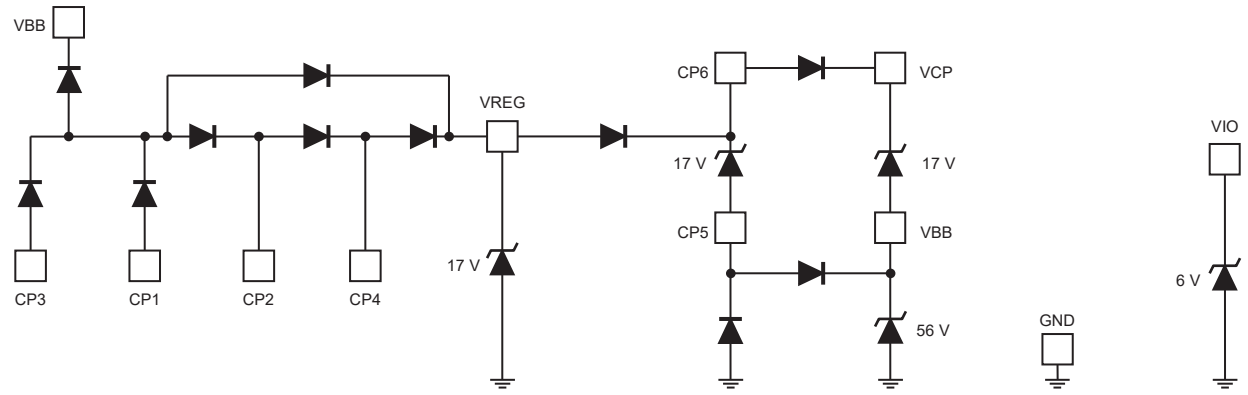


Figure 17a: Supplies

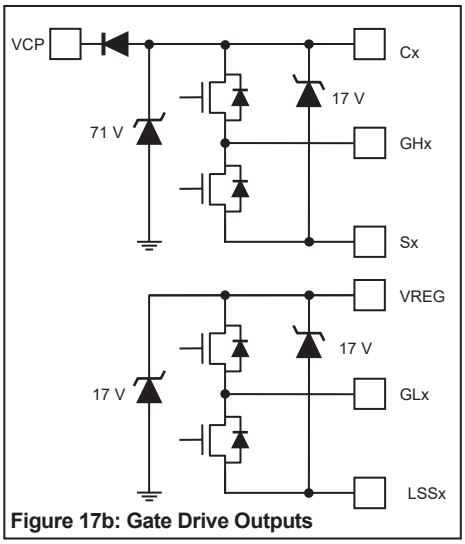


Figure 17b: Gate Drive Outputs

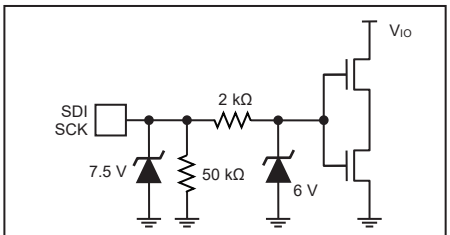


Figure 17c: Logic Inputs with Pull-Down

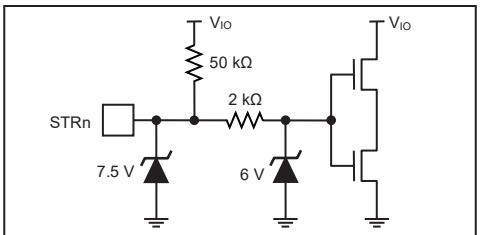


Figure 17d: Logic Inputs with Pull-Up

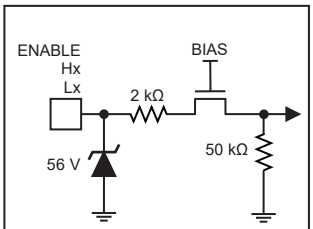


Figure 17e: HV Logic Inputs

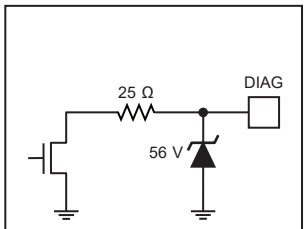


Figure 17f: DIAG Output

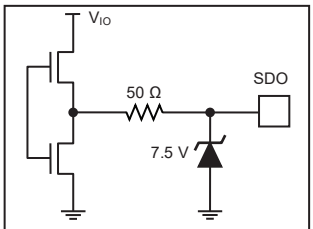


Figure 17g: SDO, SxL Outputs

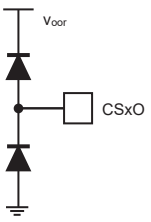


Figure 17h: CSxO Outputs

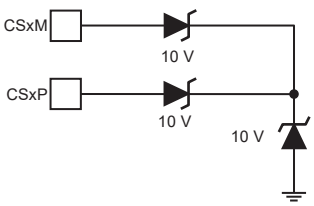


Figure 17i: CSxM, CSxP Inputs

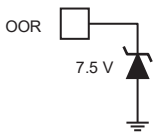
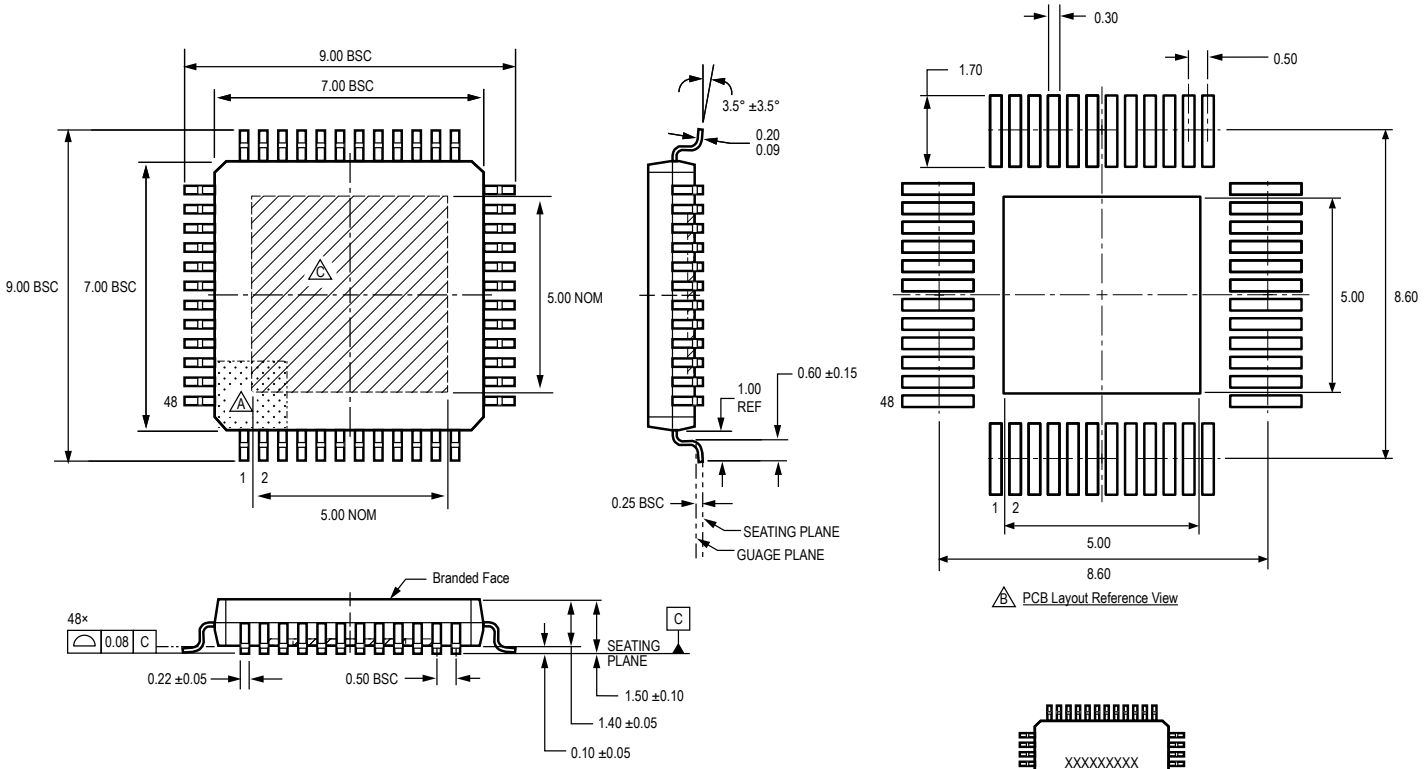


Figure 17j: VOOR Input

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000386, Rev. 5 or JEDEC MS-026 BBCHD)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Reference land pattern layout (reference IPC7351 QFP50P900X900X160-48M); adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

C Exposed thermal pad (bottom surface); exact dimensions may vary with device

D Branding scale and appearance at supplier discretion

B PCB Layout Reference View

D Standard Branding Reference View
Line 1, 2, 3: Maximum 9 characters per line

Line 1: Part Number
Line 2: Logo A, 4-digit Date Code
Line 3: Assembly Lot Number

Figure 18: JP Package, 48-Pin LQFP with Exposed Thermal Pad

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Revision History

Number	Date	Description
–	May 29, 2020	Initial release
1	July 9, 2020	Updated VBB Quiescent Current I_{BBS} test conditions (page 6), Pull-Up On-Resistance maximum values (page 7), Reset Shutdown Time characteristic (page 9); removed Input Common Mode Range characteristic (page 10); updated DC Common-Mode Rejection typical value (page 10), Logic Overvoltage when VLM = 1 minimum and maximum values, VOOR Undervoltage when VLR = 1 minimum values, VOOR Overvoltage when VLR = 1 minimum and maximum values (page 11), VDS Threshold High-Side and Low-Side values, VDS and VGS Quality Time values, DIAG Output: Temperature Sink Current values, DIAG Output: Temperature Source Current values (page 12); added footnote 13 to Temperature Warning Threshold, Temperature Warning Hysteresis, Overtemperature Threshold, Overtemperature Hysteresis (page 12); updated Bridge: Phase Disconnected section (pages 41-42).
2	September 10, 2020	Updated V_{OROLON} and $V_{OROLOFF}$ minimum values (page 11)
3	February 17, 2021	Added Input Common-Mode Range (DC) characteristic (page 10) and Logic Truth Tables footnote (page 19); updated Turn-Off and Turn-On Time test conditions (page 7), Phase Output Leakage Current minimum value (page 8), Input Pull-Down ENABLE minimum value (page 9), Input Offset Voltage test conditions, Output Offset Ratio minimum and maximum values (page 10), VCP Undervoltage Hysteresis maximum value (page 11), VDS and VGS Qualify Time (page 12), Sleep Mode section (page 27), and Supply Decoupling section (page 71).
4	March 9, 2021	Added footnotes to DIAG Output: Temperature Range and Temperature Slope (page 12)
5	May 5, 2021	Updated ASIL status (page 1)
6	May 26, 2022	Updated package drawing (page 73)
7	February 17, 2023	Updated Gain Drift Over Temperature maximum value (page 10) and Gate Drive Undervoltage Warning test conditions (page 11)

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com