AK4115

High Feature 192kHz 24bit Digital Audio Interface Transceiver

GENERAL DESCRIPTION

The AK4115 is a 24-bit stereo digital audio transceiver that supports sampling rates up to 216kHz. The channel status bit decoder supports both consumer and professional modes and can automatically detect Non-PCM bit streams such as Dolby Digital or MPEG. The AK4115 supports a wide array of features a couple of them being; differential cable driver and receiver support, and an internal PLL that can support clock sources such as bi-phase and "word clock". Control of AK4115 is achieved though a μP or pin-strapping (parallel mode) and it is packaged in a space- saving 64pin-LQFP.

* Dolby Digital is a trademark of Dolby Laboratories.

FEATURES

- **AES3, IEC60958, S/PDIF, EIAJ CP1201 Compatible**
- **Very Low Jitter Analog PLL**
- **Synchronous / Asynchronous Mode**
- **Include Two X'tal Oscillators**
- **Clock Source: PLL or External Clock**
  - **Reference Clock for PLL:**
    - **Biphase signal: 22kHz to 216kHz**
    - **External Clock (ELRCK pin): 22kHz to 216kHz**
- **8-channel Receiver input**
  - **One channel supports Differential Input**
- **2-channel Transmission output (Through output or DIT)**
  - **One channel supports Differential Output (RS422 Line Output Buffer)**
- **Auxiliary Digital Input**
- **De-emphasis for 32kHz, 44.1kHz and 48kHz**
- **Detection Functions**
  - **Non-PCM Bit Stream Detection**
  - **DTS-CD Bit Stream Detection**
  - **Sampling Frequency Detection:**
    (22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz, 64kHz, 88.2kHz, 96kHz, 176.4kHz and 192kHz)
  - **Unlock & Parity Error Detection**
  - **DAT Start ID Detection**
- **Up to 24bit Audio Data Format**
- **Audio Interface: Master or Slave Mode**
- **192-bit Channel Status Buffer**
- **Burst Preamble bit Pc and Pd Buffer for Non-PCM bit stream**
- **Q-subcode Buffer for CD bit stream**
- **Serial μP Interface: 4-wire or I^2C (max. 400kHz)**
- **Two Master Clock Outputs: 64fs/128fs/256fs/512fs**
- **Operating Voltage: 2.7 to 3.6V with 5V Logic Tolerance**
- **Package: 64pin LQFP**
- **Ta: -20 to 85°C**

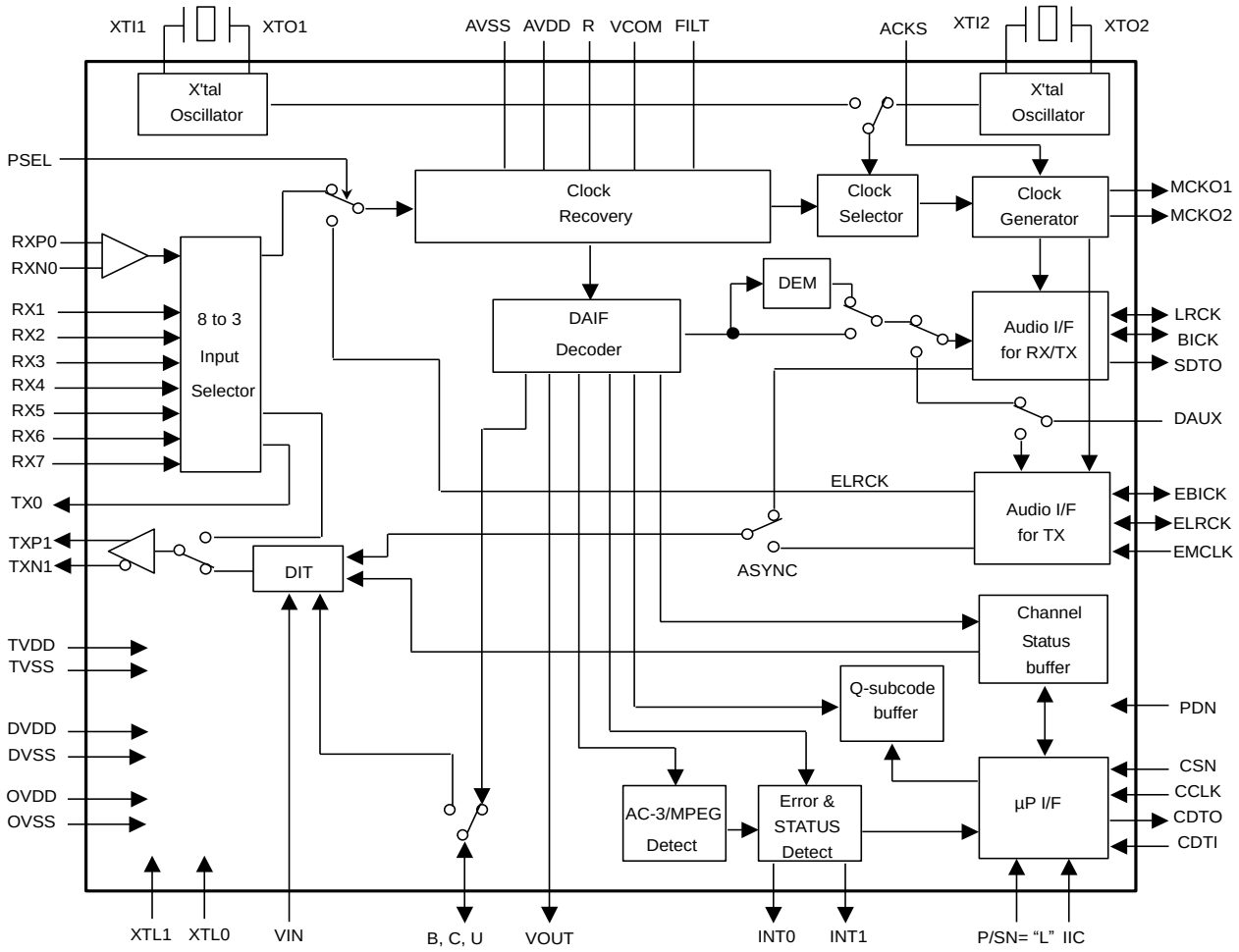


Figure 1. AK4115 Block Diagram in serial mode

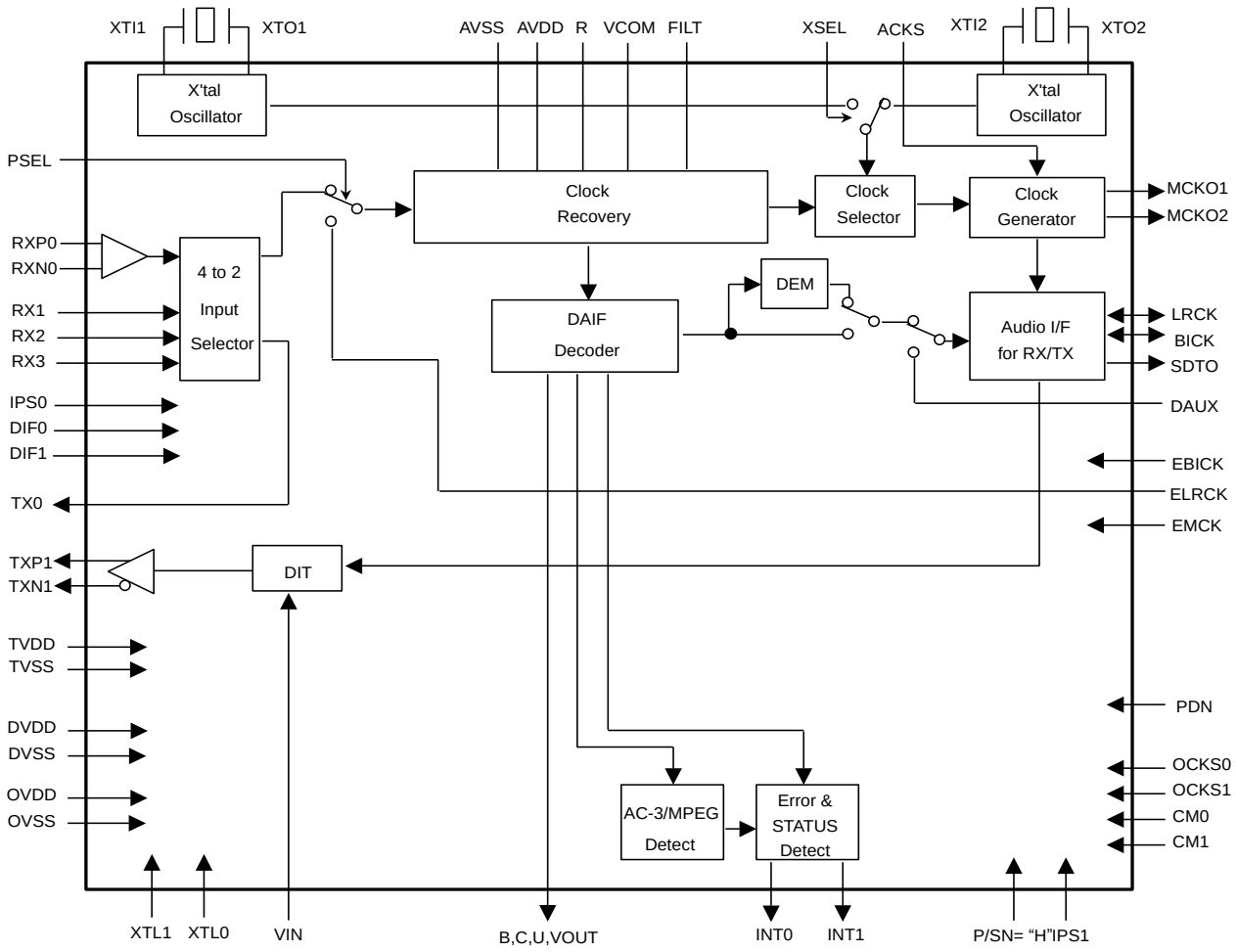
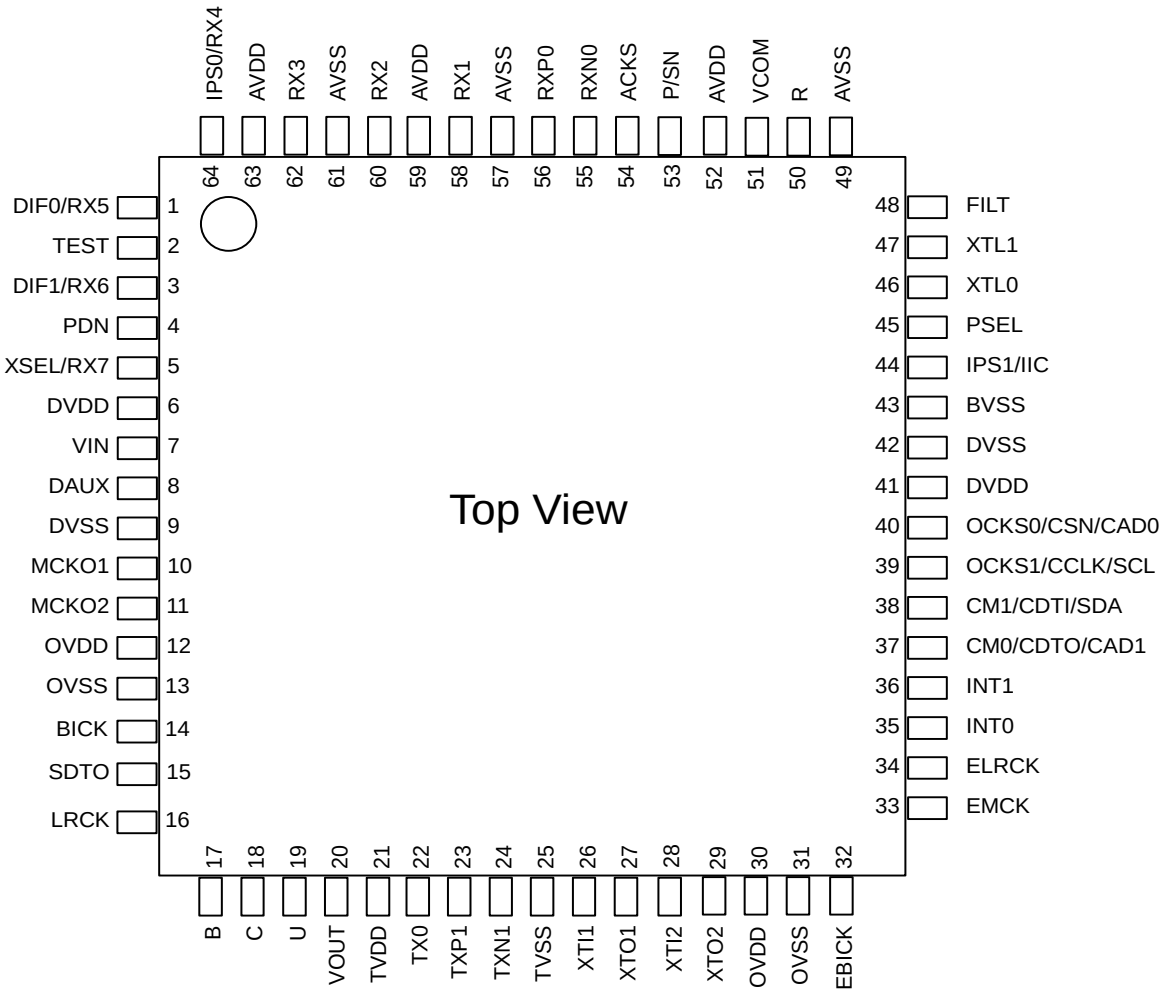


Figure 2. AK4115 Block Diagram in parallel mode

■ Ordering Guide

AK4115VQ	-20 ~ +85 °C	64pin LQFP (0.5mm pitch)
AK4115	Evaluation board for AK4115	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	DIF0	I	Audio Data Interface Format #0 Pin in parallel mode
	RX5	I	Receiver Channel #5 Pin in serial mode (Internal biased pin)
2	TEST	I	TEST Pin This pin must be connected to AVSS.
3	DIF1	I	Audio Data Interface Format #1 Pin in parallel mode
	RX6	I	Receiver Channel #6 Pin in serial mode (Internal biased pin)
4	PDN	I	Power-Down Mode Pin When "L", the AK4115 is powered-down and reset.
5	XSEL	I	X'tal Oscillator Selection Pin in parallel mode "L": X'tal #1 is powered-up. "H": X'tal #2 is powered-up. XSEL pin and XSEL bit are ORed.
	RX7	I	Receiver Channel #7 Pin in serial mode (Internal biased pin)
6	DVDD	-	Digital Power Supply Pin, 3.3V
7	VIN	I	V-bit Input Pin for Transmitter Output
8	DAUX	I	Auxiliary Audio Data Input Pin
9	DVSS	-	Digital Ground Pin
10	MCKO1	O	Master Clock Output #1 Pin
11	MCKO2	O	Master Clock Output #2 Pin
12	OVDD	-	Digital Power Supply Pin, 3.3V
13	OVSS	-	Digital Ground Pin
14	BICK	I/O	Audio Serial Data Clock Pin
15	SDTO	O	Audio Serial Data Output Pin
16	LRCK	I/O	Channel Clock Pin
17	B	I/O	Block-Start Input/Output Pin
18	C	I/O	C-bit Input/Output Pin
19	U	I/O	U-bit Input/Output Pin
20	VOUT	O	V-bit Output Pin for Receiver
21	TVDD	-	Input tolerance & TX Output Buffer Power Supply Pin, 3.3V or 5V
22	TX0	O	Transmit Channel (Through Data) Output #0 Pin
23	TXP1	O	Transmit Channel Positive Output #1 Pin
24	TXN1	O	Transmit Channel Negative Output #1 Pin
25	TVSS	-	Input & TX Output Buffer Ground pin
26	XTI1	I	X'tal #1 Input Pin
27	XTO1	O	X'tal #1 Output Pin
28	XTI2	I	X'tal #2 Input Pin
29	XTO2	O	X'tal #2 Output Pin
30	OVDD	-	Digital Power Supply Pin, 3.3V
31	OVSS	-	Digital Ground Pin
32	EBICK	I/O	External Serial Data Clock Pin
33	EMCK	I	External Master Clock Input Pin
34	ELRCK	I/O	External Channel Clock Pin
35	INT0	O	Interrupt #0 Pin
36	INT1	O	Interrupt #1 Pin

Note 1. Do not allow digital input pins except internal biased pins to float.

PIN/FUNCTION (Continued)

No.	Pin Name	I/O	Function
37	CM0	I	Master Clock Operation Mode #0 Pin in parallel mode
	CDTO	O	Control Data Output Pin in serial mode, IIC pin = "L".
	CAD1	I	Chip Address #1 Pin in serial mode, IIC pin = "H".
38	CM1	I	Master Clock Operation Mode #1 Pin in parallel mode
	CDTI	I	Control Data Input Pin in serial mode, IIC pin = "L".
	SDA	I/O	Control Data Pin in serial mode, IIC pin = "H". An external pull-up resistor is required.
39	OCKS1	I	Output Clock Select #1 Pin in parallel mode
	CCLK	I	Control Data Clock Pin in serial mode, IIC pin = "L"
	SCL	I	Control Data Clock Pin in serial mode, IIC pin = "H" An external pull-up resistor is required.
40	OCKS0	I	Output Clock Select #0 Pin in parallel mode
	CSN	I	Chip Select Pin in serial mode, IIC pin = "L".
	CAD0	I	Chip Address #0 Pin in serial mode, IIC pin = "H".
41	DVDD	-	Digital Power Supply Pin, 3.3V
42	DVSS	-	Digital Ground Pin
43	BVSS	-	Substrate Ground Pin
44	IPS1	I	Input Channel Select #1 Pin in parallel mode
	IIC	I	IIC Select Pin in serial mode "L": 4-wire Serial, "H": I^2C
45	PSEL	I	PLL Source Select Pin "L": S/PDIF Input, "H": ELRCK Input Clock PSEL pin and PSEL bit are ORed in serial mode.
46	XTL0	I	X'tal Frequency Select #0 Pin
47	XTL1	I	X'tal Frequency Select #1 Pin
48	FILT	O	PLL Loop Filter Pin
49	AVSS	-	Analog Ground Pin
50	R	O	External Resistor Pin 10kΩ ±1% resistor should be connected to AVSS externally.
51	VCOM	O	Common Voltage Output Pin 4.7μF capacitor should be connected to AVSS externally.
52	AVDD	-	Analog Power Supply Pin, 3.3V
53	P/SN	I	Parallel/Serial Select Pin "L": Serial Mode, "H": Parallel Mode
54	ACKS	I	Master Clock Frequency Auto Setting Mode Pin. "L": Disable, "H": Enable ACKS pin and ACKS bit are ORed in serial mode.
55	RXN0	I	Receiver Channel #0 Negative Input Pin (Internal biased pin) In serial mode, this channel is selected as default channel.
56	RXP0	I	Receiver Channel #0 Positive Input Pin (Internal biased pin) In serial mode, this channel is selected as default channel.
57	AVSS	-	Analog Ground Pin
58	RX1	I	Receiver Channel #1 Pin (Internal biased pin)
59	AVDD	-	Analog Power Supply Pin, 3.3V
60	RX2	I	Receiver Channel #2 Pin (Internal biased pin)
61	AVSS	-	Analog Ground Pin
62	RX3	I	Receiver Channel #3 Pin (Internal biased pin)
63	AVDD	-	Analog Power Supply Pin, 3.3V
64	IPS0	I	Input Channel Select #0 Pin in parallel mode
	RX4	I	Receiver Channel #4 Pin in serial mode (Internal biased pin)

Note 1. Do not allow digital input pins except internal biased pins to float.

■ Handling of Unused Pin

The unused I/O pin should be processed appropriately as below.

1. Serial Mode (P/SN pin = "L")

Classification	Pin Name	Setting
Analog Input	RXP0, RXN0, RX7-1	These pins should be open.
	TEST	This pin should be connected to AVSS.
Analog Output	FILT	This pin should be open.
Digital Input	VIN, DAUX, XTI1, XTI2, EMCK	These pin should be connected to DVSS.
Digital Output	MCKO1, MCKO2, VOUT, TX0, TXP1, TXN1, XTO1, XTO2, INT0, INT1, CDTO (IIC pin = "L")	These pins should be open.
Digital Input/Output	B, U, C	These pins should be open when BCU_IC bit is "1". These pins should be DVSS when BCU_IO bit is "0".
	EBICK, ELRCK	These pins should be open in master mode. These pins should be connected to DVSS in slave mode.

2. Parallel Mode (P/SN pin = "H")

Classification	Pin Name	Setting
Analog Input	RXP0, RXN0, RX3-1	These pins should be open.
	TEST	This pin should be connected to AVSS.
Analog Output	FILT	This pin should be open.
Digital Input	VIN, DAUX, XTI1, XTI2, EMCK, EBICK, ELRCK	These pin should be connected to DVSS.
Digital Output	MCKO1, MCKO2, VOUT, TX0, TXP1, TXN1, XTO1, XTO2, INT0, INT1, B, U, C	These pins should be open.

ABSOLUTE MAXIMUM RATINGS

(AVSS=OVSS=DVSS=TVSS=BVSS=0V; Note 2)

Parameter		Symbol	min	max	Units
Power Supplies:	Analog	AVDD	-0.3	4.6	V
	Digital	DVDD	-0.3	4.6	V
	Logic Output Buffer	OVDD	-0.3	4.6	V
	Input tolerance and TX Buffer	TVDD	-0.3	6.0	V
	| BVSS – AVSS | (Note 3)	ΔGND1	-	0.3	V
	| BVSS – OVSS | (Note 3)	ΔGND2	-	0.3	V
	| BVSS – DVSS | (Note 3)	ΔGND3	-	0.3	V
	| BVSS – TVSS | (Note 3)	ΔGND4	-	0.3	V
Input Current (Any pins except supplies)		IIN	-	±10	mA
Input Voltage (Note 4)		VIN	-0.3	"TVDD+0.3" or 6.0	V
Ambient Temperature (Power applied)		Ta	-20	85	°C
Storage Temperature		Tstg	-65	150	°C

Note 2. All voltages with respect to ground.

Note 3. AVSS, OVSS, DVSS, BVSS and TVSS must be connected to the same ground plane.

Note 4. All input pins. The maximum value is low value either "TVDD+0.3V" or "6.0V".
Pull-up resistor at SDA and SCL pins should be connected to (TVDD+0.3)V or less voltage.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS=OVSS=DVSS=TVSS=BVSS=0V; Note 2)

Parameter		Symbol	min	typ	max	Units
Power Supplies: (Note 5)	Analog	AVDD	2.7	3.3	3.6	V
	Digital	DVDD	2.7	3.3	3.6	V
	Logic Output Buffer	OVDD	2.7	3.3	3.6	V
	Input tolerance and TX Buffer	TVDD	DVDD	5.0	5.5	V
	Difference	AVDD – DVDD	-0.3	0	0.3	V
		AVDD – OVDD	-0.3	0	0.3	V
		OVDD – DVDD	-0.3	0	0.3	V

Note 2. All voltages with respect to ground.

Note 5. The power up sequence among AVDD, DVDD, OVDD and TVDD is not critical.

*AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

S/PDIF RECEIVER CHARACTERISTICS

(Ta=25°C; AVDD=OVDD=DVDD=2.7~3.6V; TVDD=2.7~5.5V)

Parameter	Symbol	min	typ	max	Units
Input Resistance	Zin	-	10	-	kΩ
Input Voltage	VTH	200	-	-	mVpp
Input Sample Frequency	fs	22	-	216	kHz
Time deviation Jitter					
RX input (PSEL = "0")		-	100	-	ps RMS
ELRCK input (PSEL = "1")		-	300	-	ps RMS
Cycle - to - Cycle Jitter					
RX input (PSEL = "0")		-	70	-	ps RMS
ELRCK input (PSEL = "1")		-	70	-	ps RMS

DC CHARACTERISTICS

(Ta=25°C; AVDD=OVDD=DVDD=2.7~3.6V; TVDD=2.7~5.5V; unless otherwise specified)

Parameter	Symbol	min	typ	max	Units
Power Supply Current					
Normal operation: PDN pin = "H" (Note 6)					
AVDD+DVDD+OVDD:		-	28	42	mA
TVDD:		-	30	45	mA
Power down: PDN pin = "L" (Note 7)					
AVDD+DVDD+OVDD+TVDD:		-	10	100	μA
High-Level Input Voltage	VIH	70%DVDD	-	TVDD	V
Low-Level Input Voltage	VIL	DVSS-0.3	-	30%DVDD	V
Input Level at AC coupling (Only ELRCK pin)	VAC	0.5	-	TVDD	Vpp
Except for TX0, TXN1 and TXP1 pins					
High-Level Output Voltage (Iout=-400μA)	VOH	OVDD-0.4	-	-	V
Low-Level Output Voltage					
(Except SDA pin: Iout=400μA)	VOL	-	-	0.4	V
(SDA pin: Iout= 3mA)	VOL	-	-	0.4	V
TX0 Output Level					
Output Level (Note 8)	VTXO0	0.4	0.5	0.6	V
TXN1 and TXP1 pins					
Professional mode (TVDD= 4.5 ~ 5.5V)					
Output Impedance (Rp + Rn + R1) (Note 9)	RTXPN	88	110	132	Ω
Consumer Mode (TVDD = 2.7 ~ 5.5V)					
Output Level (Note 10)	VTXO1	0.4	0.5	0.6	V
Input Leakage Current	Iin	-	-	± 10	μA

Note 6. AVDD, OVDD, DVDD = 3.3V, TVDD=5.0V, C_L=20pF, fs=216kHz, X'tal=24.576MHz, Clock Operation Mode 2, OCKS1=1, OCKS0=1, TX0 output circuit: Figure 23, TX1 output circuit: Figure 25.
AVDD=10mA (typ), OVDD+DVDD=18mA (typ)

Note 7. RX inputs are open and all digital input pins are held TVDD or DVSS.

Note 8. By using Figure 23 or Figure 24.

Note 9. Rp: Output impedance of TXP1, Rn: Output impedance of TXN1, R1 = 75Ω. By using Figure 25.

Note 10. By using Figure 26

SWITCHING CHARACTERISTICS

(Ta=25°C; AVDD=OVDD=DVDD=2.7~3.6V, TVDD=2.7~5.5V; C_L=20pF)

Parameter			Symbol	min	typ	max	Units
Master Clock Timing							
Crystal Resonator		Frequency	fXTAL	11.2896	-	24.576	MHz
External Clock		Frequency	fECLK	11.2896	-	27.648	MHz
		Duty	dECLK	40	50	60	%
MCKO1 Output		Frequency	fMCK1	2.816	-	27.648	MHz
		Duty	dMCK1	40	50	60	%
MCKO2 Output		Frequency	fMCK2	1.408	-	27.648	MHz
		Duty	dMCK2	40	50	60	%
PLL Clock Recover Frequency (RX7-0)			fpll	22	-	216	kHz
LRCK Frequency			fs	22	-	216	kHz
Duty Cycle (at Slave Mode)			dLCK	45	-	55	%
Duty Cycle (at Master Mode)			dLCK	-	50	-	%
Audio Interface Timing 1							
Slave Mode							
BICK Period			tBCK	72	-	-	ns
BICK Pulse Width Low			tBCKL	27	-	-	ns
Pulse Width High			tBCKH	27	-	-	ns
LRCK Edge to BICK "↑" (Note 11)			tLRB	15	-	-	ns
BICK "↑" to LRCK Edge (Note 11)			tBLR	15	-	-	ns
LRCK to SDTO (MSB) (3.0V ≤ DVDD,OVDD ≤ 3.6V)			tLRM	-	-	20	ns
BICK "↓" to SDTO (3.0V ≤ DVDD,OVDD ≤ 3.6V)			tBSD	-	-	20	ns
LRCK to SDTO (MSB) (2.7V ≤ DVDD,OVDD < 3.0V)			tLRM	-	-	25	ns
BICK "↓" to SDTO (2.7 V≤ DVDD,OVDD < 3.0V)			tBSD	-	-	25	ns
DAUX Hold Time			tDXH	15	-	-	ns
DAUX Setup Time			tDXS	15	-	-	ns
Master Mode							
BICK Frequency			fBCK	-	64fs	-	Hz
BICK Duty			dBCK	-	50	-	%
BICK "↓" to LRCK			tMBLR	-15	-	15	ns
BICK "↓" to SDTO			tBSD	-	-	15	ns
DAUX Hold Time			tDXH	15	-	-	ns
DAUX Setup Time			tDXS	15	-	-	ns
Master Clock Timing 2							
EMCK		Frequency	fECLK2	2.816	-	27.648	MHz
		Duty	dECLK2	40	50	60	%
ELRCK		PLL Lock Range	fEPLL	22	-	216	kHz
		Frequency	fs	22	-	216	kHz
		Duty	dLCK	40	50	60	%
Audio Interface Timing 2							
Slave Mode							
EBICK Period			tEBCK	72	-	-	ns
EBICK Pulse Width Low			tEBCKL	27	-	-	ns
Pulse Width High			tEBCKH	27	-	-	ns
ELRCK Edge to BICK "↑" (Note 12)			tELRB	15	-	-	ns
EBICK "↑" to ELRCK Edge (Note 12)			tEBLR	15	-	-	ns
DAUX Hold Time			tEDXH	15	-	-	ns
DAUX Setup Time			tEDXS	15	-	-	ns
Master Mode							
EBICK Frequency			fEBCK	-	64fs	-	Hz
EBICK Duty			dEBCK	-	50	-	%
EBICK "↓" to ELRCK			tEMBLR	-15	-	15	ns
DAUX Hold Time			tEDXH	15	-	-	ns
DAUX Setup Time			tEDXS	15	-	-	ns

Note 11. BICK rising edge must not occur at the same time as LRCK edge.

Note 12. EBICK rising edge must not occur at the same time as ELRCK edge.

SWITCHING CHARACTERISTICS (Continued)

(Ta=25°C; AVDD=OVDD=DVDD=2.7~3.6V, TVDD=2.7~5.5V; C_L=20pF)

Parameter	Symbol	min	typ	max	Units
Control Interface Timing (4-wire serial mode)					
CCLK Period	tCCK	200	-	-	ns
CCLK Pulse Width Low	tCCKL	80	-	-	ns
Pulse Width High	tCCKH	80	-	-	ns
CDTI Setup Time	tCDS	50	-	-	ns
CDTI Hold Time	tCDH	50	-	-	ns
CSN "H" Time	tCSW	150	-	-	ns
CSN "↓" to CCLK "↑"	tCSS	50	-	-	ns
CCLK "↑" to CSN "↑"	tCSH	50	-	-	ns
CDTO Delay	tDCD	-	-	45	ns
CSN "↑" to CDTO Hi-Z	tCCZ	-	-	70	ns
Control Interface Timing (I^2C Bus mode):					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	µs
Clock Low Time	tLOW	1.3	-	-	µs
Clock High Time	tHIGH	0.6	-	-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	µs
SDA Hold Time from SCL Falling (Note 13)	tHD:DAT	0	-	-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	µs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	µs
Capacitive load on bus	Cb	-	-	400	pF
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns
Reset Timing					
PDN Pulse Width	tPW	150	-	-	ns

Note 13. Data must be held for sufficient time to bridge the 300ns transition time of SCL.
Note 14. I^2C-bus is a tradmark of NXP B.V.

■ Timing Diagram

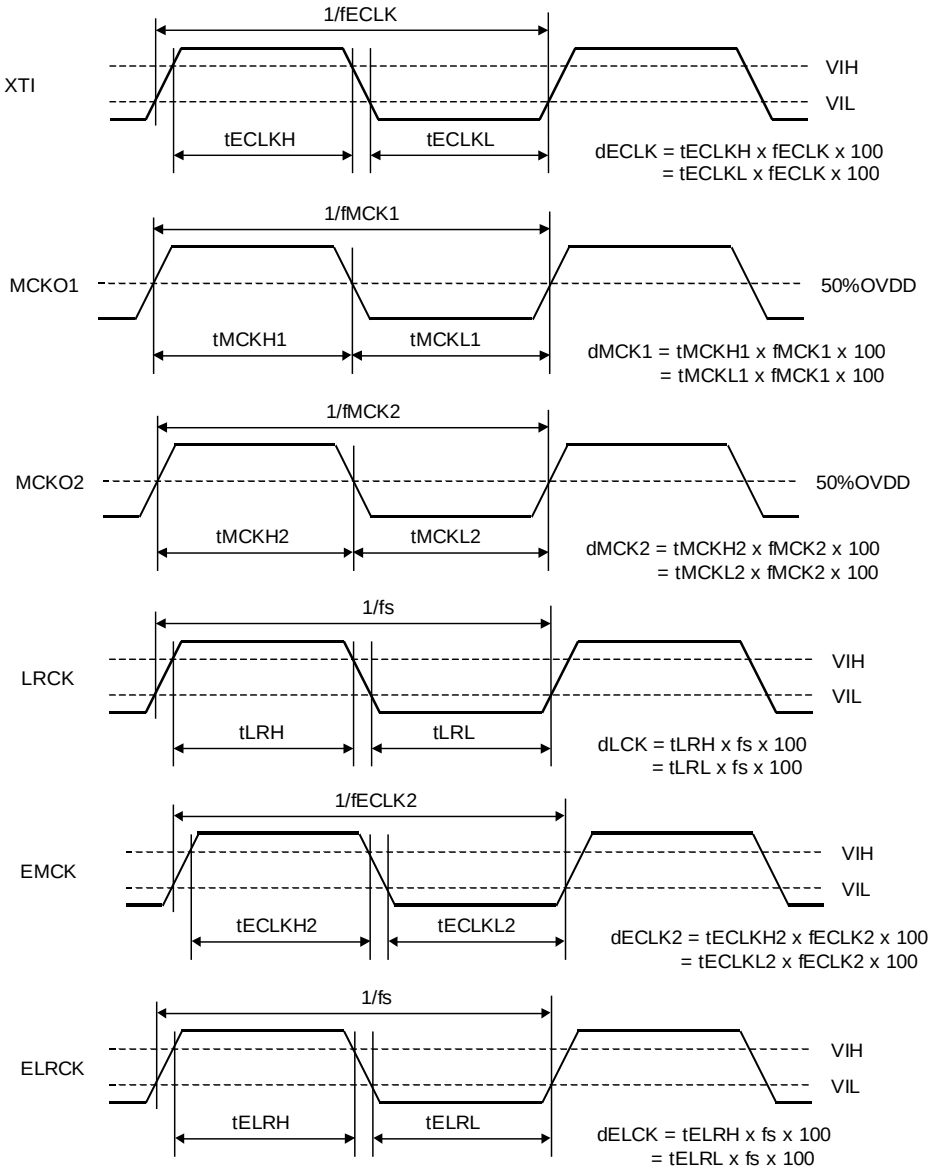


Figure 3. Clock Timing

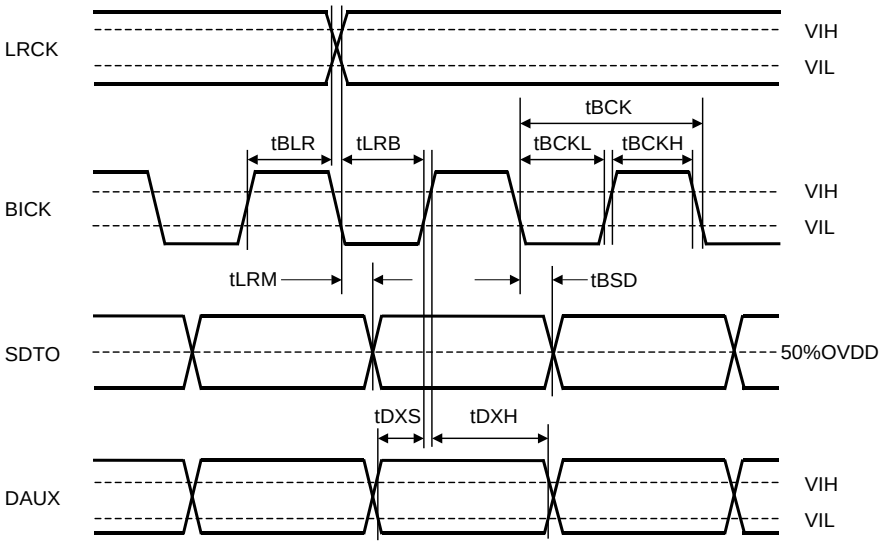


Figure 4. Serial Interface Timing 1 (Slave Mode)

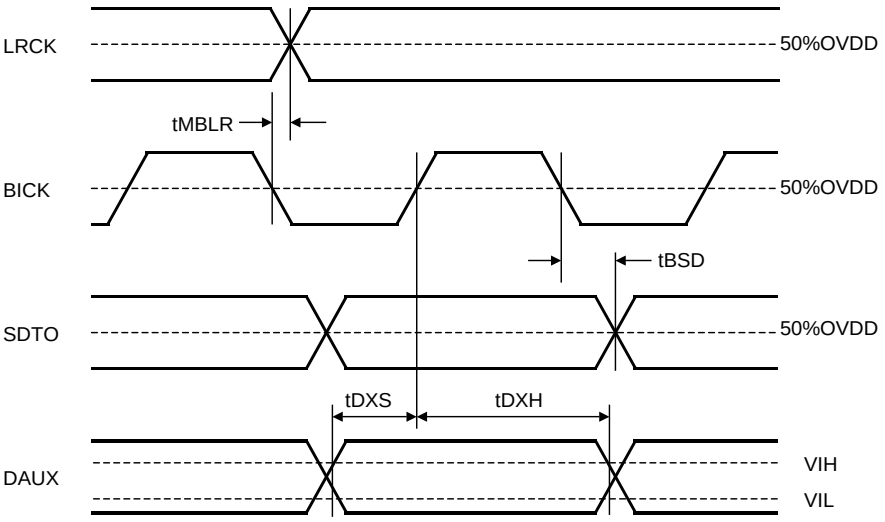


Figure 5. Serial Interface Timing 1 (Master Mode)

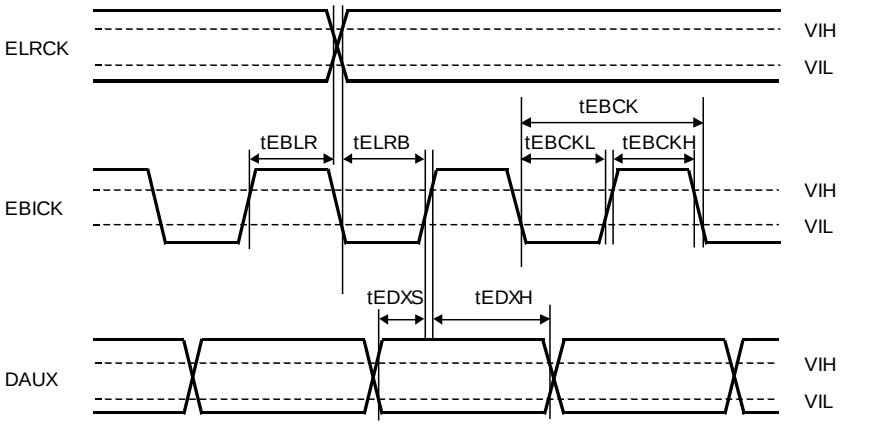


Figure 6. Serial Interface Timing 2 (Slave Mode)

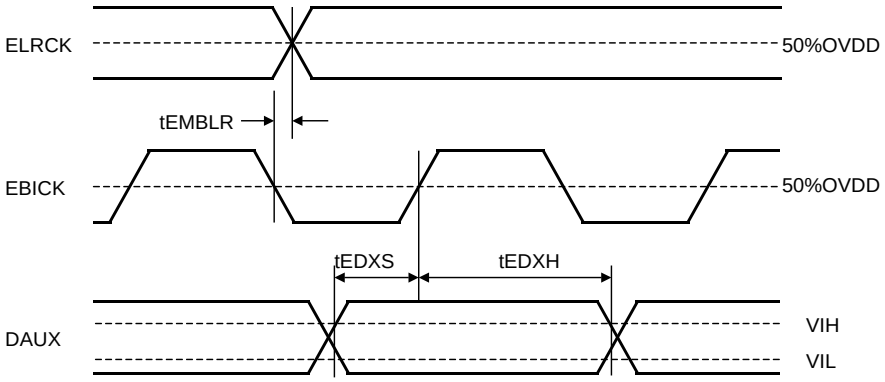


Figure 7. Serial Interface Timing 2 (Master Mode)

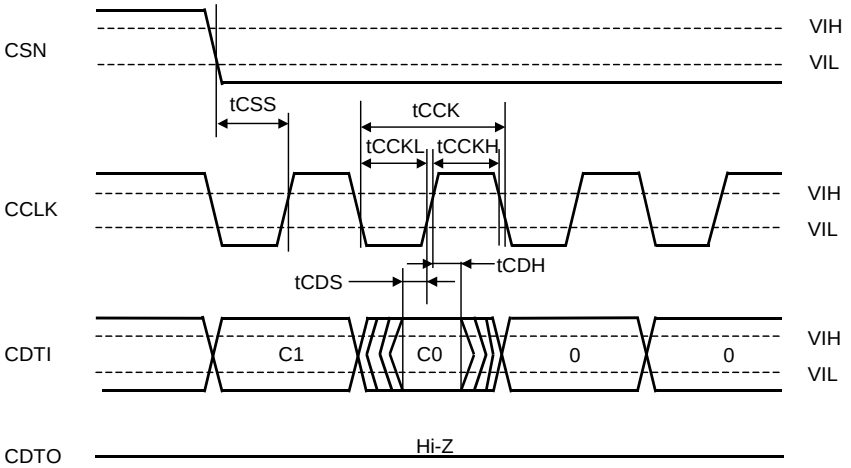


Figure 8. WRITE/READ Command Input Timing in 4-wire serial mode

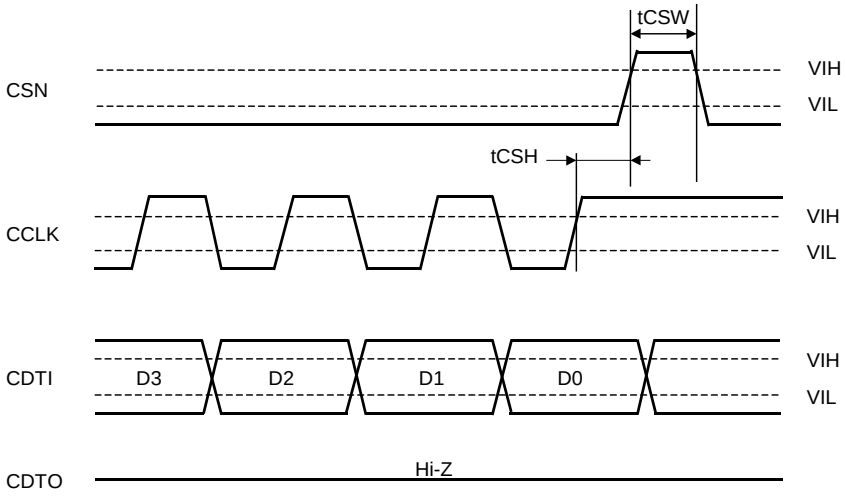


Figure 9. WRITE Data Input Timing in 4-wire serial mode

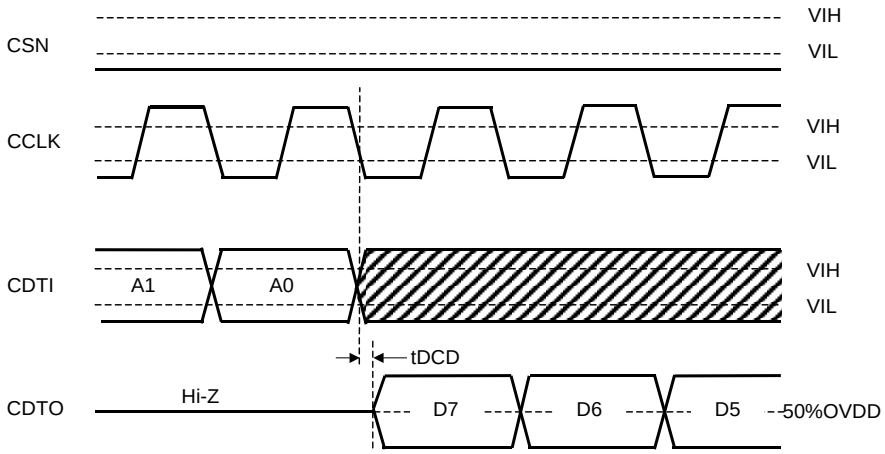


Figure 10. READ Data Output Timing 1 in 4-wire serial mode

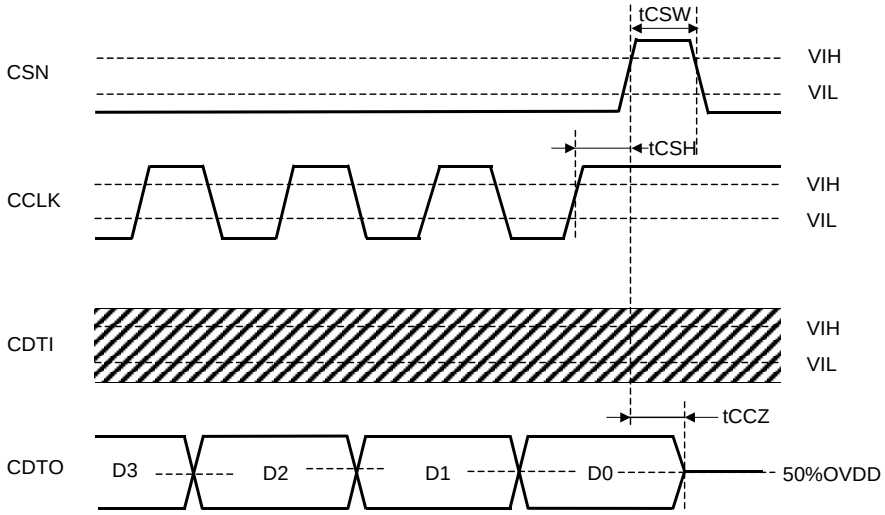


Figure 11. READ Data Input Timing 2 in 4-wire serial mode

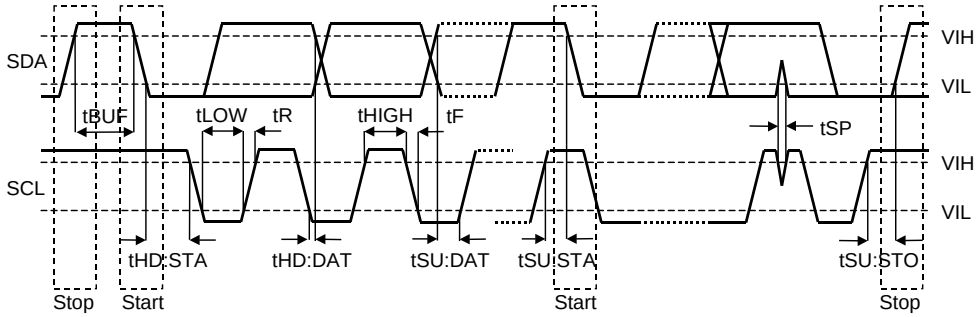


Figure 12. I^{2}C Bus mode Timing

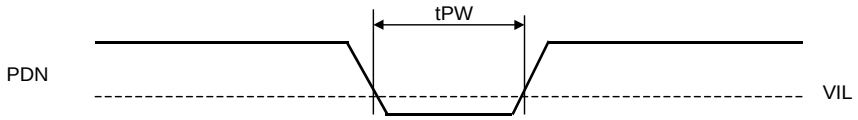


Figure 13. Power Down & Reset Timing

OPERATION OVERVIEW

■ Non-PCM (Dolby Digital, MPEG, etc) and DTS-CD Bitstream Detection

The AK4115 has a non-PCM bitstream auto-detection function, When the 32-bit mode Non-PCM preamble based on Dolby "Dolby Digital Data Stream in IEC 60958 Interface" is detected, the NPCM bit sets to "1". The 96-bit sync code consists of 0x0000, 0x0000, 0x0000, 0x0000, 0xF872 and 0x4E1F. Detection of this pattern will set the NPCM bit to "1". Once the NPCM bit is set to "1", it will remain "1" until 4096 frames pass through the chip without an additional sync pattern being detected. When those preambles are detected, the burst preambles Pc (burst information: Figure 51) and Pd (length code: Figure 52) that follow those sync codes are stored to registers. The AK4115 has also a DTS-CD bitstream auto-detection function. When the AK4115 detects DTS-CD bitstream, the DTSCD bit sets to "1". If the next sync code does not occur within 4096frames, the DTSCD bit sets to "0" until no-PCM bitstream is detected again. The ORed value of NPCM and DTSCD bits are output to AUTO bit. The AK4115 detects the 14-bit sync word and the 16-bit sync word of a DTS-CD bitstream, the detection function can be set ON/OFF by DTS14 and DTS16 bits in serial mode. In parallel mode, the logical OR value of the AUTO and DTS-CD bits are outputted to the INT1 pin. The DTS-CD bit detects both the 14-bit sync word and the 16-bit sync word.

■ 216kHz Clock Recovery

The integrated low jitter PLL has a wide lock range from 22kHz to 216kHz. The AK4115 has a sampling frequency detection function (22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz, 64kHz, 88.2kHz, 96kHz, 176.4kHz and 192kHz) that uses either a clock comparison against the X'tal oscillator from the setting of XTL1-0, or the channel status information. The PLL loses lock when the received sync interval is incorrect.

■ Reference Clock for PLL

The reference clock for the PLL can select the bi-phase signal or the clock supplied from the ELRCK pin. The bi-phase signals are supplied to RX7-0 pins and the ELRCK pin is supplied to a sampled clock (1fs) from the word clock (typically used by studio equipment). This is selected by the PSEL bit or the PSEL pin. PSEL bit and PSEL pin are ORed internally.

PSEL	Reference Clock for PLL	
0	RX Input	Default
1	ELRCK Input	

Table 1. Setting of PLL Reference Clock

■ PLL Lock Time

The lock time at PSEL = "0" depends on sampling frequency (fs) and FAST bit (See Table 2). FAST bit is useful at lower sampling frequency and is fixed to "1" in parallel mode. When PSEL is "1", the lock time is 35ms (max) and is not related to the setting of the FAST bit. The lock time in Table 2 does not include the power-up time of VCOM voltage. Therefore, the power-up time of VCOM voltage must be added when PDN pin changes from "L" to "H". The power-up time of VCOM voltage is max. 15ms (Capacitor value of VCOM pin = 4.7μF).

PSEL	FAST bit	PLL Lock Time	
0	0	≤ (20ms + 384/fs)	Default
0	1	≤ (20ms + 1/fs)	
1	-	≤ 35ms	

Table 2. PLL Lock Time (fs: Sampling Frequency)

■ Word Clock (Studio Sync Clock)

The word clock is used to synchronize clocks among studio equipment and is always synchronized to the sampling frequency (1fs). The internal PLL generates MCLK, BICK and LRCK from the word clock supplied to the ELRCK pin. The PLL lock range is 22kHz to 216kHz. The word clock (ELRCK pin) can receive signal levels of 0.5Vpp(min) when AC coupled. In master mode, the clock phase between ELRCK pin and LRCK pin is within ± 5%. When the AK4115 is supplied with a bi-phase signal and a word clock (ELRCK), the phase error between the LRCK and ELRCK is within ±1/(128fs). Therefore, use LRCK and not ELRCK for the serial data output stream. When the word clock is not synchronized to the bi-phase signal, WSYNC bit should be set to "0".

■ DIT/DIR Mode

The AK4115 operates in either synchronous mode or asynchronous mode. In synchronous mode, transmitter and receiver are operated by the same clock source. In asynchronous mode, transmitter and receiver are operated by different a sampling frequencies that are selected by the ASYNC bit. Frequency multiples are not required in asynchronous mode.

1. Synchronous Mode: ASYNC bit = "0"

PSEL and CM1-0 select the clock source and the data source for SDTO. In Mode 2, the clock source is switched from PLL to X'tal when the PLL goes to the unlock state. In Mode 3, the clock source is fixed to X'tal, but PLL is also operation and the recovered data such as channel status bit can be monitored. For Mode 2 and Mode 3, it is recommended that the frequency of X'tal is different from the recovered frequency of the PLL. In Modes 4-6, the PLL source is ELRCK and MCKO1/2, BICK and LRCK are generated by the PLL. The data source of SDTO is always DAUX.

Mode	PSEL	CM1	CM0	UNLOCK	PLL Status	X'tal Status	Clock source	Clock I/O	SDTO
0	0	0	0	-	ON	ON (Note 16)	PLL (RX)	Note 17	RX
1	0	0	1	-	OFF	ON	X'tal	Note 17	DAUX
2	0	1	0	0	ON	ON	PLL (RX)	Note 17	RX
				1	ON	ON	X'tal	Note 17	DAUX
3	0	1	1	-	ON	ON	X'tal	Note 17	DAUX
4	1	0	0	-	ON	ON (Note 16)	PLL (ELRCK)	Note 17	DAUX
5	1	0	1	-	OFF	ON	X'tal	Note 17	DAUX
6	1	1	0	0	ON	ON	PLL (ELRCK)	Note 17	DAUX
				1	ON	ON	X'tal	Note 17	DAUX

Note 15. ON: Oscillation (Power-up), OFF: STOP (Power-down)
Note 16: When the X'tal is not used as clock comparison for fs detection (i.e. XTL1,0= "1,1"), the X'tal is OFF.
Note 17. MCKO1/2, BICK, LRCK

Table 3. Clock operation for DIT/DIR in synchronous mode

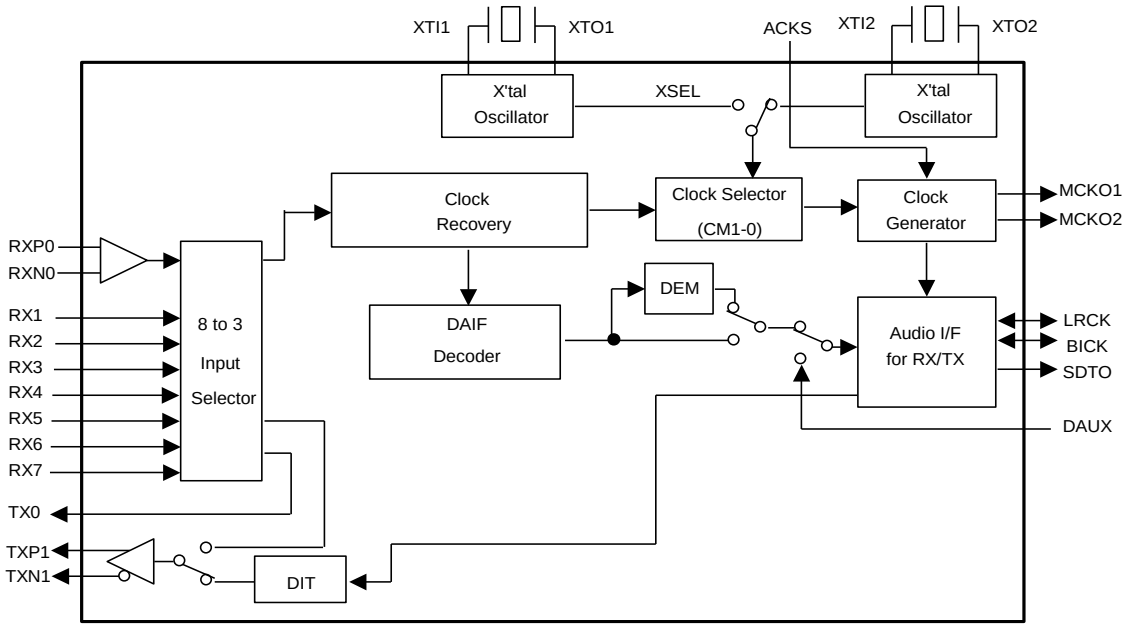


Figure 14. Clocks for DIT/DIR in synchronous mode (PSEL bit = "0")

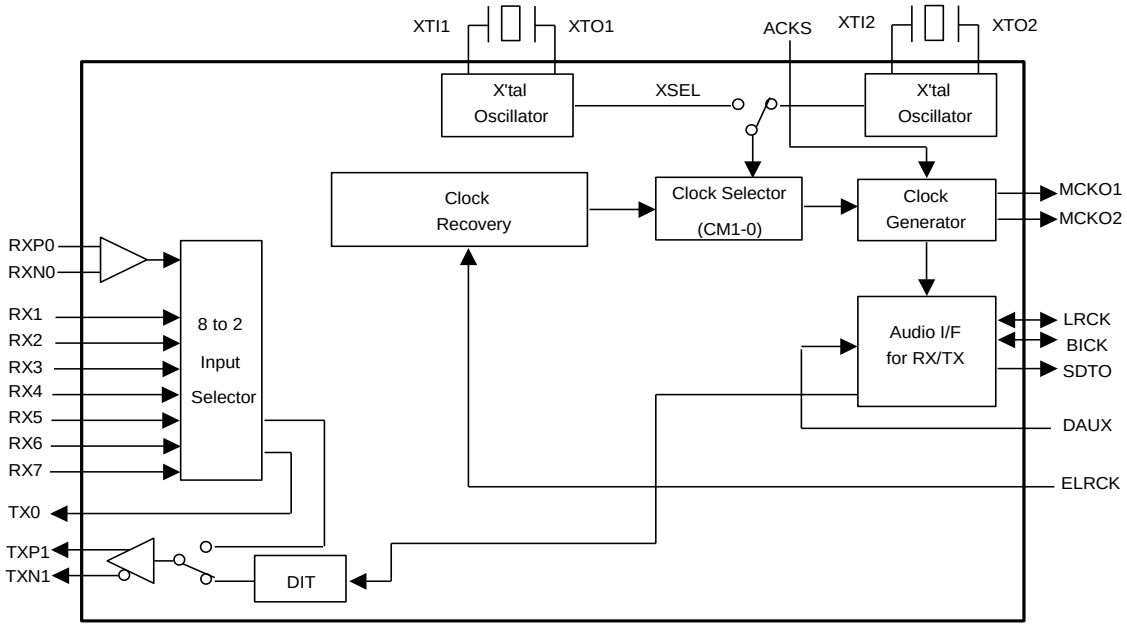


Figure 15. Clocks for DIT/DIR in synchronous mode (PSEL bit = "1")

2. Asynchronous Mode: ASYNC bit = "1", PSEL = "0"

When ASYNC bit is "1", DIT and DIR can operate at different sample rates(non-multiples). In Mode1, Mode2 (When the PLL is the unlock state) and Mode3, SDTO is fixed "L". The input timing of DAUX should be synchronized with ELRCK and EBCIK. The master clock of TX can be selected to either X'tal or EMCK by the MSEL bit (See Table 4).

MSEL bit	Master Clock	
0	X'tal	Defalut
1	EMCK	

Table 4. Master clock setting for TX in asynchronous mode.

Mode	CM1	CM0	UNLOCK	PLL Status	X'tal Status	RX			TX	
						Clock Source	Clock I/O	SDTO	Clock Source	Clock I/O
0	0	0	-	ON	ON (Note 19)	PLL (RX)	Note 20	RX	X'tal or EMCK (Note 22)	Note 21
1	0	1	-	OFF	ON	X'tal	Note 20	"L"	X'tal or EMCK	Note 21
2	1	0	0	ON	ON	PLL (RX)	Note 20	RX	X'tal or EMCK	Note 21
			1	ON	ON	X'tal	Note 20	"L"	X'tal or EMCK	Note 21
3	1	1	-	ON	ON	X'tal	Note 20	"L"	X'tal or EMCK	Note 21

Note 18. ON: Oscillation (Power-up), OFF: STOP (Power-down)
Note 19. When the X'tal is not used as clock comparison for sampling frequency detection (i.e. XTL1,0 = "1,1"), the X'tal is OFF.
Note 20. MCKO1/2, BICK, LRCK
Note 21. EMCK or X'tal, EBICK, ELRCK, DAUX
Note 22. When X'tal is OFF, the clock source supports EMCK only.

Table 5. Clock operation for DIT/DIR in asynchronous mode

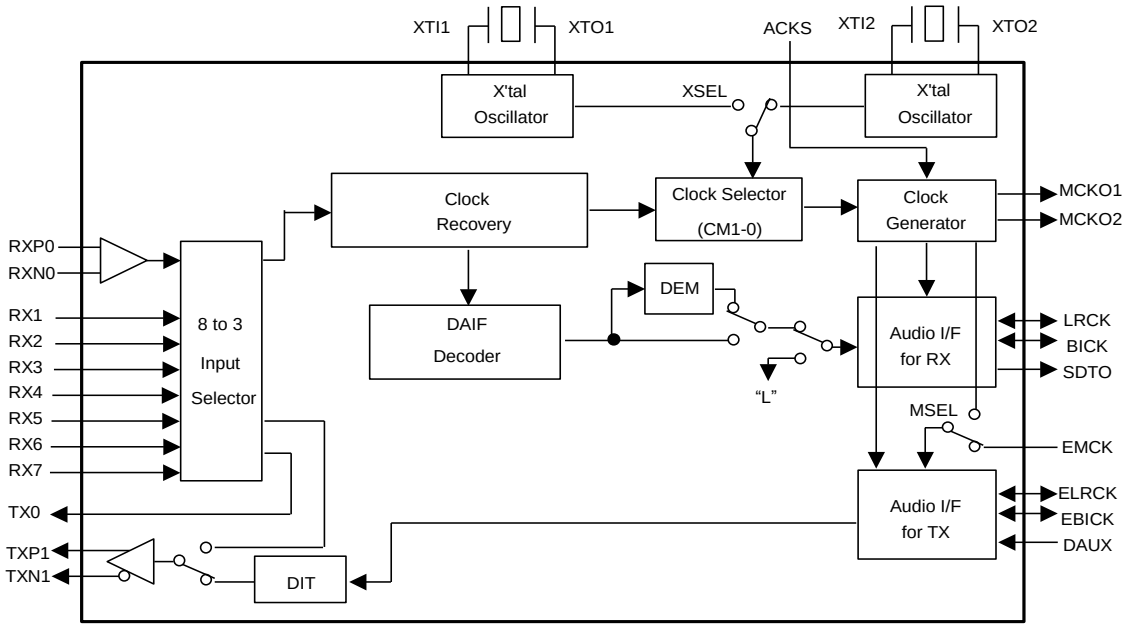


Figure 16. Clocks for DIT/DIR in asynchronous mode

■ Block start, Channel status bit, User bit and Validity bit

The AK4115 can control and monitor block start, channel status bits, user bits and validity bit for RX and TX. B, C and U pins are bi-directional and the direction of input/output can be selected by the BCU_IO bit. B, C, U and VOUT pins become "L" (BCU_IO bit = "1") in an unlocked state of Mode 2.

a. Serial mode & Except AES3 mode (P/SN pin = "L", AES3 bit = "0")

ASYNC bit	BCU_IO bit	Block Start (B pin)	RX			TX		
			Channel Status bit	User bit	Validity bit	Channel Status bit	User bit	Validity bit
0	0	Input	CR191-0 bits	N/A	VOUT pin VRX bit (Note 24)	C pin CT191-0 bits (Note 25)	U pin	VIN pin VTX bit (Note 26)
	1	Output	C pin CR191-0 bits (Note 23)	U pin	VRX bit VOUT pin (Note 24)	CT191-0 bits	All "0" data (Note 27)	VIN pin VTX bit (Note 26)
1	0	Input	CR191-0 bits	N/A	VRX bit	C pin CT191-0 bits (Note 25)	U pin	VIN pin VTX bit (Note 26)
	1	Output	In case that No DAUX input exists			In case that No RX input exists		
			C pin CR191-0 bits (Note 23)	U pin	VOUT pin VRX bit (Note 24)	CT191-0 bits	All "0" data	VTX bit

Note 23. Channel status bit for RX can be monitored by both C pin and CR191-0 bits.
Note 24. Validity bit for RX can be monitored by both VOUT pin and VRX bit.
Note 25. C pin and CT191-0 bits are ORed internally.
Note 26. VIN pin and VTX bit are ORed internally.
Note 27. When UDIT bit is "1", the recovered U bits are used for DIT(DIR-DIT loop mode of U bit).

Table 6. Block start, Channel Status bit, User bit and Validity bit in serial mode except AES3 mode (N/A: Not available)

When the RX and the DAUX of TX path run at the same time under the condition which is in asynchronous mode (ASYNC bit = "1") and the B, C, U pins are set as output (BCU_IO bit = "1" and BCU bit = "1"), the DIT output that is operating asynchronously with RX becomes abnormal at regular intervals. In this case, the RX input side operates normally. This phenomenon has no constraint of AES 3 bit setting.
This occurs because the Block-Start, Channel Status, and User data decoded from the RX input are internally written to the same assigned data of the TX frame data.
When using RX path and DAUX of TX path at the same time, set the B, C, U pins to Low output by setting BCU_IO bit = "1" (output) and BCU bit = "0", or set the B, C, U pins to input direction by setting BCU_IO bit = "0" (input) and BCU bit = "1".

b. Serial mode & AES3 mode (P/SN pin = “L”, AES3 bit = “1”, ASYNC bit = “0”)

DIF1 bit	BCU_IO bit	Block Start (B pin)	RX			TX		
			Channel Status bit	User bit	Validity bit	Channel Status bit	User bit	Validity bit
0	0	Input	CR191-0 bits SDTO pin (Note 28)	SDTO pin	VOUT pin VRX bit SDTO pin (Note 31)	C pin CT191-0 bits (Note 32)	U pin	VIN pin VTX bit (Note 34)
	1	Output	C pin CR191-0 bits SDTO pin (Note 29)	U pin SDTO pin (Note 30)	VOUT pin VRX bit SDTO pin (Note 31)	CT191-0 bits	All “0” data (Note 35)	VIN pin VTX bit (Note 34)
1	0	Input	CR191-0 bits SDTO pin (Note 28)	SDTO pin	VOUT pin VRX bit SDTO pin (Note 31)	CT191-0 bits DAUX pin (Note 33)	DAUX pin	DAUX pin
	1	Output	C pin CR191-0 bits SDTO pin (Note 29)	U pin SDTO pin (Note 30)	VOUT pin VRX bit SDTO pin (Note 31)	CT191-0 bits DAUX pin (Note 33)	DAUX pin	DAUX pin

Note 28. Channel status bit for RX can be monitored by CR191-0 bits and SDTO pin.
Note 29. Channel status bit for RX can be monitored by C pin, CR191-0 bits and SDTO pin.
Note 30. User bit for RX can be monitored by U pin and SDTO pin.
Note 31. Validity bit for RX can be monitored by VOUT pin, VRX bit and SDTO pin.
Note 32. C pin and CT191-0 bits are ORed internally.
Note 33. Channel status bit can select either CT191-0 bits or DAUX pin by the setting of CTX bit.
Note 34. VIN pin and VTX bit are ORed internally.
Note 35. When UDIT bit is “1”, the recovered U bits are used for DIT(DIR-DIT loop mode of U bit).

Table 7. Block start, Channel Status bit, User bit and Validity bit in serial mode & AES3 mode

c. Parallel mode (P/SN pin = “H”)

Block Start (B pin)	RX			TX		
	Channel Status bit	User bit	Validity bit	Channel Status bit	User bit	Validity bit
Output	C pin	U pin	VOUT pin	Default value of CT191-0 bits	All “0” data	VIN pin

Table 8. Block start, Channel Status bit, User bit and Validity bit in parallel mode

1. Channel Status bit

1-1. RX

The data recovered from the bi-phase input signal is stored in CR191-0 bits. When the BCU_IO bit = "1", the channel status bits are available on the C pin according to the block signal timing. The channel status bits are outputted from SDTO pin with audio data in AES3 mode.

1-2. TX

The channel status bit can controlled by the CT191-0 bits. When BCU_IO bit is "0", the channel status bits are also controlled by C pin. CT191-0 bits and the signal on the C pin are ORed internally.

The input to C pin is ignored in AES3 mode. When CTX bit is set to "0", the channel status bits on DAUX pin are outputted with audio data from TX. When CTX bit is set to "1", the values of CT191-0 bits are outputted with audio data from TX.

When the CCRE bit is "1" and AK4115 is in professional mode (bit0 = "1"), the CRC code can be generated according to the professional mode definition in the AES3 standard. When the CCRE bit is "0", the CRC data is not generated and the data from the CT191-0 bits is passed to the TX directly. In the consumer mode (bit0 = "0"), the CRC code is not generated.

In the consumer mode (bit0 = "0"), bits20-23(audio channel) must be controlled by the CT20 bit. When the CT20 bit is "1", the AK4115 corresponds to "stereo mode", bits20-23 are set to "1000"(left channel) in sub-frame 1, and is set to "0100"(right channel) in sub-frame 2. When the CT20 bit is "0", bits20-23 is set to "0000" in both sub-frame 1 and sub-frame 2.

All CR191-0 bits are transferred to CT191-0 bits when the CTRAN bit changes from "0" to "1". The transferred CT191-0 bits are valid after the next block start signal is detected. CTRAN bit goes to "0" after finishing the transfer. Don't write to the CT191-0 bits when the CTRAN bit = "1".

2. User bit

2-1. RX

When the BCU_IO bit is "1", the recovered user bit is available on the U pin according to block start timing. The user bits are outputted from SDTO pin with audio data in AES3 mode.

2-2. TX

When the BCU_IO bit is "0", the user bit is sent to the U pin according to block start timing. When BCU_IO bit is "1" and the ASYNC bit is "0"(synchronous mode), the user bit is controlled by the UDIT bit. When the UDIT bit is "0", user bit is set to "0". When the UDIT bit is "1", the recovered U bits are used for DIT(DIR-DIT loop mode of U bit). This mode (UDIT bit = "1") is enabled when the PLL is locked. The input to U pin is ignored in AES3 mode and the user bits on DAUX pin are outputted with audio data from TX.

3. Validity bit

3-1. RX
In synchronous mode, the validity bit is available on the VOUT pin according to block start timing. In asynchronous mode, the validity bit is available on the VOUT pin according to LRCK timing. The VRX bit is available in both modes. The validity bit is outputted from SDTO pin with audio data in AES3 mode.

3-2. TX

The validity bit is controlled by the VIN pin or the VTX bit. Since the validity bit does not usually update every sub-frame cycle, it can be controlled by the VIN pin according to LRCK timing in synchronous mode. In asynchronous mode, it can be controlled by the VIN pin according to ELRCK timing. When the validity bit timing is synchronized with the block start timing , the BCU_IO bit should be "0". In asynchronous mode, the validity bit cannot be controlled by the VIN pin when BCU_IO bit is set to "0".

The input to VIN pin and VTX bit are ignored in AES3 mode and the validity bit on DAUX is outputted with audio data from TX.

4. Block Start Signal Timing

In synchronous mode, the block start signal timing depends on LRCK. In asynchronous mode, it depends on ELRCK. The channel status, user and validity bits are captured with the current audio sample. When the block start signal is an input (BCU_IO bit = "0"), the block start signal should stay high for more than one sub-frame. When the block start signal is an output (BCU_IO bit = "1"), the block start signal goes high at the start of frame 0 and remains high until the end of frame 39.

The input to B pin is ignored in AES3 mode and the B bit on DAUX is used as the block start timing.

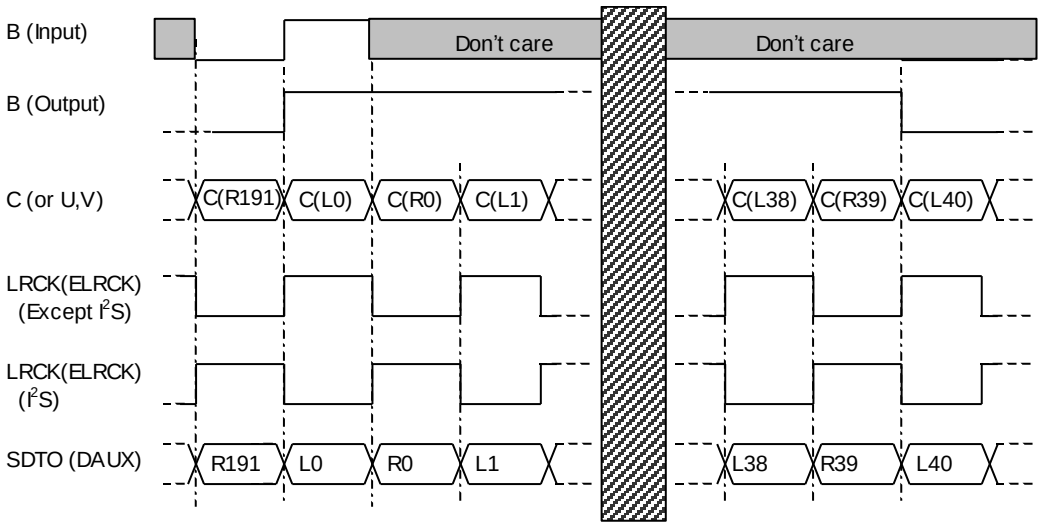


Figure 17. B, C, U, V Input/output timings

■ Master Clock Output

The AK4115 has two master clock outputs, MCKO1 and MCKO2. MCKO2 has two modes. These modes can be selected by the XMCK bit.

1) When XMCK bit = "0"

These clocks are derived from either the recovered clock or the X'tal oscillator. The frequencies of the master clock outputs (MCKO1 and MCKO2) are set by OCKS0 and OCKS1 as shown in Table 9. The 512fs clock is changed into the 256fs clock when sampling frequency is 96kHz or 192kHz. The 512fs or 256fs clock is changed into the 128fs clock when sampling frequency is 192kHz.

No.	OCKS1	OCKS0	MCKO1 pin	MCKO2 pin	X'tal	fs (max)	
0	0	0	256fs	256fs	256fs	96 kHz	Default
1	0	1	256fs	128fs	256fs	96 kHz	
2	1	0	512fs	256fs	512fs	48 kHz	
3	1	1	128fs	64fs	128fs	192 kHz	

Table 9. Master Clock Output Frequency

2) When XMCK bit = "1"

MCKO2 outputs the input clock of the XTI pin. The settings of CM1-0 and OCKS1-0 bits are ignored. The output frequency can be set by the DIV bit. MCKO1 outputs a clock that is selected by the CM1-0 bits and OCKS1-0 bits.

XMCK bit	DIV bit	MCKO2 Clock Source	MCKO2 Frequency
1	0	X'tal (Note 36)	x 1
1	1	X'tal (Note 36)	x 1/2

Note 36. MCKO2 Clock Source is selected by XSEL bit.

Table 10. Select output frequency of MCKO2

■ Master Clock Auto Setting Mode

The master clock auto setting mode detects the MCLK/LRCK ratio (selects Normal/Double/Quad automatically). When ACKS is "1", this mode is enabled. The frequencies of MCKO1 and MCKO2 are shown in Table 11. In this mode, the settings of OCKS1-0 are ignored. This mode is only supported when the sampling frequency detection circuit is enabled in PLL mode.(refer to "Sampling Frequency and Pre-emphasis Detection" section.) When ELRCK is selected and XTL1-0 = "11", this mode is not supported. In X'tal mode, the frequencies of MCKO1/MCKO2 depend upon OCKS1-0. The ACKS pin and ACKS bit are ORed internally.

Mode	MCKO1	MCKO2	Sampling Frequency Range
Normal Speed	512fs	256fs	22kHz to 48kHz
Double Speed	256fs	128fs	64kHz to 96kHz
Quad Speed	128fs	64fs	176.4kHz to 216kHz

Table 11. Master Clock Frequency Select (Master Clock Auto Setting Mode)

■ X’tal Oscillator

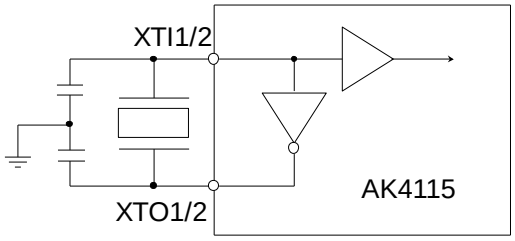
The AK4115 has two X’tal oscillators. They can not operate at the same time. The operation of the X’tal oscillator is selected by the XSEL bit or the XSEL pin.

XSEL	Status	
	X’tal #1	X’tal #2
0	Power-Up	Power-Down
1	Power-Down	Power-Up

Table 12. Setting of X’tal oscillator

The following circuits are available to feed the clock to the XTI1/2 pins of AK4115.

1) X’tal



Note: External capacitance depends upon the crystal oscillator (typ. 5-10pF)

Figure 18. X’tal mode

2) External clock

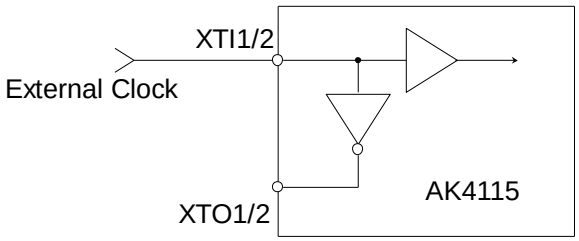


Figure 19. External clock mode

3) Fixed to the Clock Operation Mode 0

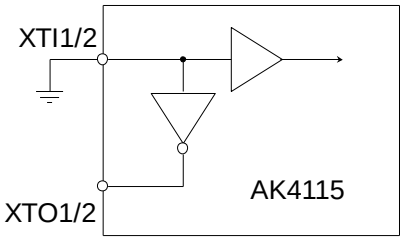


Figure 20. OFF mode

■ Sampling Frequency and Pre-emphasis Detection

The AK4115 has two methods for detecting the sampling frequency:

1. Clock comparison between the recovered clock and X'tal oscillator
2. Sampling frequency information from channel status

The method is selected by the XTL1,0 pins. When XTL1, 0 = "1,1", the sampling frequency is detected by the channel status sampling frequency information. The detected frequency is available on the FS3-0 bits.

XTL1	XTL0	X'tal Frequency		
		X'tal #1	X'tal #2	
0	0	11.2896MHz	12.288MHz	Default
0	1	12.288MHz	11.2896MHz	
1	0	24.576MHz	22.5792MHz	
1	1	(Use channel status)	(Use channel status)	

Table 13. Reference X'tal frequency

Register output				fs	Except XTL1, 0 = "1,1"	XTL1, 0 = "1, 1"		
					Clock comparison (Note 37)	Consumer mode (Note 38)	Professional mode (Note 39)	
FS3	FS2	FS1	FS0			Byte3 Bit3,2,1,0	Byte0 Bit7,6	Byte4 Bit6,5,4,3
0	0	0	0	44.1kHz	44.1kHz ± 3%	0 0 0 0	0 1	0 0 0 0
0	0	0	1	Reserved	-	0 0 0 1	(Others)	
0	0	1	0	48kHz	48kHz ± 3%	0 0 1 0	1 0	0 0 0 0
0	0	1	1	32kHz	32kHz ± 3%	0 0 1 1	1 1	0 0 0 0
0	1	0	0	22.05kHz	22.05kHz ± 3%	0 1 0 0	0 0	1 0 0 1
0	1	1	0	24kHz	24kHz ± 3%	0 1 1 0	0 0	0 0 0 1
1	0	1	1	64kHz	64kHz ± 3%			
1	0	0	0	88.2kHz	88.2kHz ± 3%	1 0 0 0	0 0	1 0 1 0
1	0	1	0	96kHz	96kHz ± 3%	1 0 1 0	0 0	0 0 1 0
1	1	0	0	176.4kHz	176.4kHz ± 3%	1 1 0 0	0 0	1 0 1 1
1	1	1	0	192kHz	192kHz ± 3%	1 1 1 0	0 0	0 0 1 1

Note 37: At least ±3% range is identified as the value in the Table 14. In case of intermediate frequency of those two, FS3-0 bits indicate no value. When the frequency is ≥ 3% over 192kHz or ≤ 3% under 22kHz, FS3-0 bits may indicate "0001", "0101", "0111" or "1001".

Note 38: In consumer mode, Byte3 Bit3-0 are copied to FS3-0 bits.

Note 39. In professional mode, FS3-0 bit indicates "0001" except for frequency shown by Table 14.

Table 14. fs Information

The pre-emphasis information is detected and reported on PEM bit. This information is extracted from channel 1 by default. It can be switched to channel 2 by the CS12 bit in control register.

PEM	Pre-emphasis	Byte 0 Bits 3-5
0	OFF	≠ 0X100
1	ON	0X100

Table 15. PEM in Consumer Mode

PEM	Pre-emphasis	Byte 0 Bits 2-4
0	OFF	≠110
1	ON	110

Table 16. PEM in Professional Mode

■ De-emphasis Filter Control

The AK4115 includes a digital de-emphasis filter (tc=50/15μs). This is an IIR filter corresponds to four sampling frequencies (32kHz, 44.1kHz and 48kHz). When DEAU bit="1", the de-emphasis filter is enabled automatically by the sampling frequency and pre-emphasis information in the channel status. The AK4115 is in this mode by default. In parallel control mode, the AK4115 is always placed in this mode and the status bits in channel 1 control the de-emphasis filter. In serial control mode, DEM0/1 bits control the de-emphasis filter when the DEAU bit is "0". The internal de-emphasis filter is bypassed and the recovered data is available without any change if either the pre-emphasis or de-emphasis mode is OFF. When the PEM bit is "0", the internal de-emphasis filter is always bypassed.

PEM	FS3	FS2	FS1	FS0	Mode
1	0	0	0	0	44.1kHz
1	0	0	1	0	48kHz
1	0	0	1	1	32kHz
1	(Others)				OFF
0	x	x	x	x	OFF

Table 17. De-emphasis Auto Control at DEAU bit = "1" (Default)

PEM	DEM1	DEM0	Mode	
1	0	0	44.1kHz	
1	0	1	OFF	Default
1	1	0	48kHz	
1	1	1	32kHz	
0	x	x	OFF	

Table 18. De-emphasis Manual Control at DEAU bit = "0"

■ System Reset and Power-Down

The AK4115 has a power-down mode for all circuits by PDN pin and can be partially powerd-down by PWN bit. The RSTN bit initializes the register and resets the internal timing. In parallel mode, only the control by PDN pin is enabled. The AK4115 should be reset once by bringing PDN pin = "L" upon power-up.

PDN Pin:

All analog and digital circuits are placed in power-down and reset mode by bringing PDN pin= "L". All the registers are initialized, and clocks are stopped. Reading/Writing to the registers is disabled.

RSTN Bit (Address 00H; D0):

All the registers except PWN and RSTN bits are initialized by bringing RSTN bit = "0". The internal timing is also initialized. Writing to registers is not available except the PWN and RSTN bits. Reading from the registers is disabled.

PWN Bit (Address 00H; D1):

The clock recovery is initialized by bringing PWN bit = "0". In this case, the clocks are stopped. The registers are not initialized and the mode settings are maintained. Writing and reading to the registers are enabled.

■ Bi-phase Input

Eight receiver inputs (RX7-0) are available in serial mode and four receiver inputs (RX3-0) are available in parallel mode. Each input includes an amplifier for unbalanced mode that can accept a signal of 200mVpp or more. IPS2-0 selects the receiver channel.

IPS2 bit	IPS1 bit	IPS0 bit	INPUT Data	
0	0	0	RX0	Default
0	0	1	RX1	
0	1	0	RX2	
0	1	1	RX3	
1	0	0	RX4	
1	0	1	RX5	
1	1	0	RX6	
1	1	1	RX7	

Table 19. Recovery Data Select in serial mode

IPS1 pin	IPS0 pin	INPUT Data
0	0	RX0
0	1	RX1
1	0	RX2
1	1	RX3

Table 20. Recovery Data Select in parallel mode

■ Bi-phase Output

The AK4115 has two transmitter outputs, TX0 and TX1. TX0 is a loop-through output that is selected from the RX input. TX0 output is selected from RX7-0 by the OPS00, OPS01 and OPS02 bits. In parallel mode, the source of the loop-through output from TX0 is fixed to RX0.

TX1 accepts output from RX7-0 or the transmitter (DIT; the data from DAUX is transformed to IEC60958 format.). TX1 also has a true RS422 line driver (differential output). The source of the loop-through output from TX1 is selected from RX7-0 by the OPS10, OPS11 and OPS12 bits. When the DIT bit is set to "1", TX1 is transmitted to DAUX data. In parallel mode, TX1 is fixed to DIT.

OPS02	OPS01	OPS00	Output Data	
0	0	0	RX0	Default
0	0	1	RX1	
0	1	0	RX2	
0	1	1	RX3	
1	0	0	RX4	
1	0	1	RX5	
1	1	0	RX6	
1	1	1	RX7	

Table 21. Output Data Select for TX0

DIT	OPS12	OPS11	OPS10	Output Data	
0	0	0	0	RX0	
0	0	0	1	RX1	
0	0	1	0	RX2	
0	0	1	1	RX3	
0	1	0	0	RX4	
0	1	0	1	RX5	
0	1	1	0	RX6	
0	1	1	1	RX7	
1	x	x	x	DAUX	Default

Table 22. Output Data Select for TX1

■ Bi-phase signal input circuit

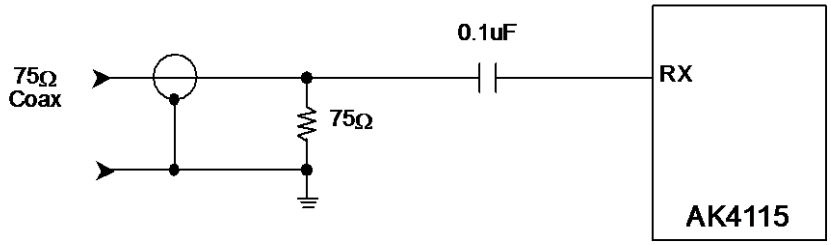


Figure 21. Consumer Input Circuit (Coaxial Input)

Note: For coaxial input, if a coupling level to this input from the next RX input line pattern exceeds 50mV, there may be an incorrect operation. In this case, it is possible to lower the coupling level by adding this decoupling capacitor.

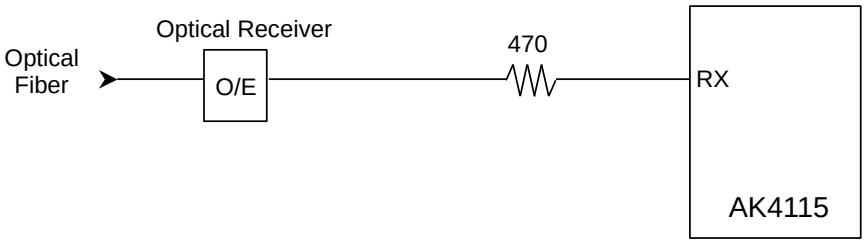


Figure 22. Consumer Input Circuit (Optical Input)

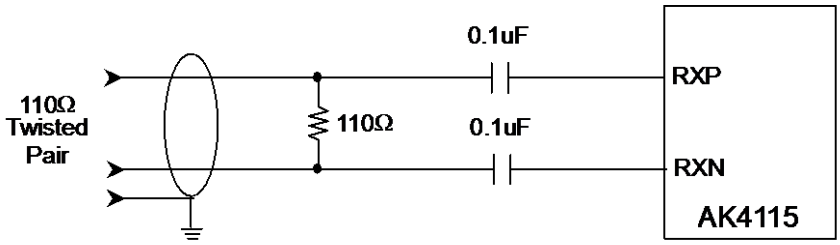


Table 23. Professional Input Circuit (Balanced Input)
Note. When RXN pin is unused, RXN pin must be AC-coupled to ground.

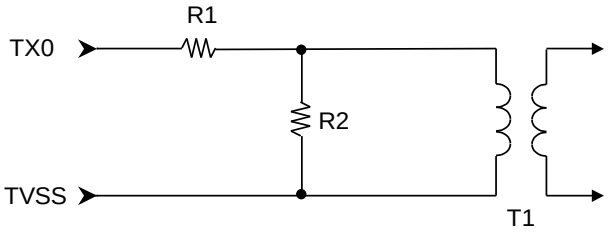
For coaxial input in serial mode, the input level of RX line is small, so care must be taken to avoid crosstalk among the RX input lines. In this case, a shield is recommended between the input lines. In parallel mode, RX3-0 is available and RX7-4 change to other pins for audio format control. Those pins must be fixed to “H” or “L”.

■ Bi-phase signal output circuit

The AK4115 includes two TX output buffers. The output level is proportional to TVDD voltage. The T1 in Figure 23, Figure 24, Figure 25 and Figure 26 is a transformer of 1:1. The resistor values should use ±1% accuracy.

1. Line Driver of TX0

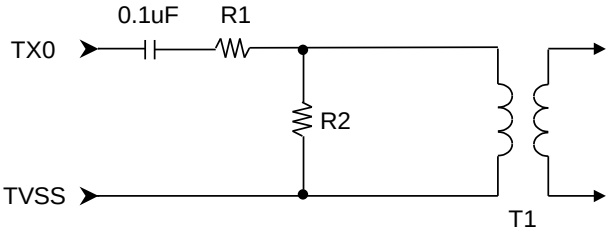
The output level of TX0 is 0.5V ± 20% using the external resistor network in consumer mode.



TVDD	R1	R2
3.3V	240Ω	150Ω
3.0V	220Ω	150Ω
5.0V	430Ω	150Ω

Figure 23. TX0 External Resistor Network 1

Note: When the AK4115 is in the power-down mode (PDN pin = "L"), power supply current can be reduced by using an AC coupling capacitor as shown in Figure 24, since TX1 output is undetermined in power-down mode.



TVDD	R1	R2
3.3V	240Ω	150Ω
3.0V	220Ω	150Ω
5.0V	430Ω	150Ω

Figure 24. TX0 External Resistor Network 2

2. Line Driver of TX1

2-1. Professional Mode (TVDD = 4.5V ~ 5.5V)

The TX1 has an RS422 line driver when TVDD is 5V±10%. The AES3 specification states that the line driver shall have a balanced output with an internal impedance of 110 ohms ±20% and also requires a balanced output drive capability of 2 to 7 volts peak-to-peak into 110 ohm load. The internal impedance of the RS422 driver along with a series resistors of 75 ohms realizes this requirement.

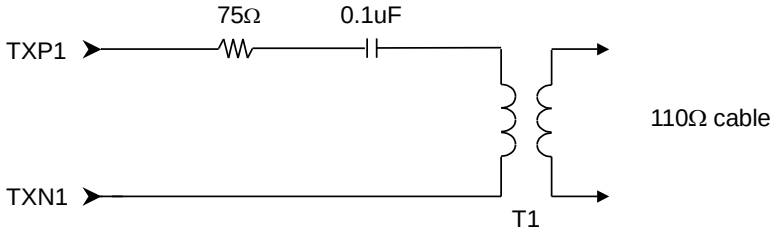
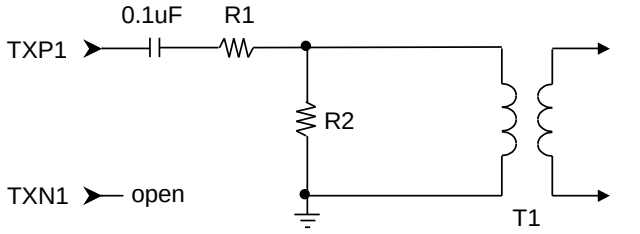


Figure 25. Professional Output Driver Circuit

2-2. Consumer Mode (TVDD = 2.7V ~ 5.5V)

For consumer use , the specifications require an output impedance of 75 ohms ±20% and a driver level of 0.5 ± 20% volts peak to peak. A combination of R1 in parallel with R2 meets this requirement. The outputs can be set to ground by resetting the device or a software mute.



TVDD	R1	R2
3.3V	270Ω	150Ω
3.0V	240Ω	150Ω
5.0V	430Ω	150Ω

Figure 26. Consumer Output Driver Circuit at AC coupling

■ PLL Loop Filter

C1 and R should be connected in series and attached between FILT pin and AVSS in parallel with C2. The value of PLL Loop Filter includes temperature deviation. Be careful to minimize the noise into the FILT pin. When the Studio Sync mode is not used, FILT pin can be open.

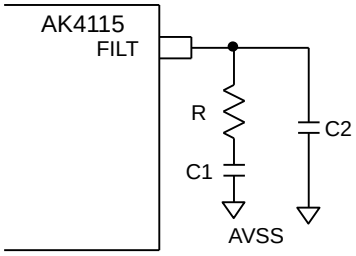


Figure 27. PLL Loop Filter

R [Ω]	C1 [nF]	C2 [pF]
24k ± 5%	10 ± 30%	100 ± 30%

Table 24. Value of PLL Loop Filter

■ Q-subcode buffers

The AK4115 has a Q-subcode buffer for CD applications. The AK4115 takes the Q-subcode into registers by the following method.

1. The sync word (S0,S1) is constructed of at least 16 “0”s.
2. The start bit is “1”.
3. Those 7bits Q-W follows to the start bit.
4. The distance between two start bits are 8-16 bits.

The QINT bit in the control register goes to “1” when the new Q-subcode differs from old one, and goes to “0” when the QINT bit is read.

	1	2	3	4	5	6	7	8	*
S0	0	0	0	0	0	0	0	0	0…
S1	0	0	0	0	0	0	0	0	0…
S2	1	Q2	R2	S2	T2	U2	V2	W2	0…
S3	1	Q3	R3	S3	T3	U3	V3	W3	0…
:	:	:	:	:	:	:	:	:	:
S97	1	Q97	R97	S97	T97	U97	V97	W97	0…
S0	0	0	0	0	0	0	0	0	0…
S1	0	0	0	0	0	0	0	0	0…
S2	1	Q2	R2	S2	T2	U2	V2	W2	0…
S3	1	Q3	R3	S3	T3	U3	V3	W3	0…
:	:	:	:	:	:	:	:	:	:

↑ Q

(*) number of "0" : min=0; max=8.

Figure 28. Configuration of U-bit(CD)

Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10	Q11	Q12	Q13	Q14	Q15	Q16	Q17	Q18	Q19	Q20	Q21	Q22	Q23	Q24	Q25
CTRL				ADRS				TRACK NUMBER								INDEX							

Q26	Q27	Q28	Q29	Q30	Q31	Q32	Q33	Q34	Q35	Q36	Q37	Q38	Q39	Q40	Q41	Q42	Q43	Q44	Q45	Q46	Q47	Q48	Q49
MINUTE								SECOND								FRAME							

Q50	Q51	Q52	Q53	Q54	Q55	Q56	Q57	Q58	Q59	Q60	Q61	Q62	Q63	Q64	Q65	Q66	Q67	Q68	Q69	Q70	Q71	Q72	Q73
ZERO								ABSOLUTE MINUTE								ABSOLUTE SECOND							

Q74	Q75	Q76	Q77	Q78	Q79	Q80	Q81	Q82	Q83	Q84	Q85	Q86	Q87	Q88	Q89	Q90	Q91	Q92	Q93	Q94	Q95	Q96	Q97
ABSOLUTE FRAME								CRC															

G(x)=x^16+x^12+x^5+1

Figure 29. Q-subcode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
40H	Q-subcode Address / Control	Q9	Q8	. . .	. . .	. . .	. . .	Q3	Q2
41H	Q-subcode Track	Q17	Q16	. . .	. . .	. . .	. . .	Q11	Q10
42H	Q-subcode Index	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
43H	Q-subcode Minute	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
44H	Q-subcode Second	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
45H	Q-subcode Frame	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
46H	Q-subcode Zero	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
47H	Q-subcode ABS Minute	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
48H	Q-subcode ABS Second	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
49H	Q-subcode ABS Frame	Q81	Q80	. . .	. . .	. . .	. . .	Q75	Q74

Figure 30. Q-subcode register

■ Error Handing for RX (PSEL = “0”)

The followings nine events the INT0 and INT1 pins to trigger the interrupt condition. When the PLL is OFF (Clock Operation Mode 1), INT0 and INT1 pins go to “L”.

1. UNLCK : PLL unlock state detect
   “1” when the PLL loses lock. The AK4115 loses lock when the time between two preambles is not correct or when those preambles are not correct.

2. PAR : Parity error or bi-phase coding error detection
   “1” when parity error or bi-phase coding error is detected, updated every sub-frame cycle.

3. AUTO : Non-Linear PCM or DTS-CD Bit Stream detection
   The OR function of NPCM and DTSCD bits.is available at the AUTO bit.

4. VRX : Validity flag detection
   “1” when validity flag is detected. Updated every sub-frame cycle.

5. AUDION : Non-audio detection
   “1” when the “AUDION” bit in recovered channel status indicates “1”. Updated every block cycle.

6. STC : Sampling frequency or pre-emphasis information change detection
   When either FS3-0 bit or PEM bit is changed, it maintains “1” during 1 sub-frame.

7. QINT : U-bit Sync flag
   “1” when the Q-subcode differs from the old one. Updated every sync code cycle for Q-subcode.

8. CINT : Channel status sync flag
   “1” when received C bit differs from the old one. Updated every block cycle.

9. DAT : DAT Start ID detect
   “1” when the category code indicates “DAT” and “DAT Start ID” is detected. When DCNT bit is “1”, it does not indicate “1” even if “DAT Start ID” is detected again within “3841 x LRCK”.
   When “DAT Start ID” is detected again after “3840 x LRCK” passed, it indicates “1”. When DCNT bit is “0”, it indicates “1” every “DAT Start ID” detection.

1. Parallel Mode

In parallel mode, the INT0 pin outputs the ORed signal between UNLCK and PAR. The INT1 pin outputs the ORed signal between AUTO and AUDION. Once INT0 goes ”H”, it maintains “H” for 1024/fs cycles after all error events are removed. Table 25 shows the state of each output pins when the INT0/1 pin is “H”.

Event				Pin			
UNLCK	PAR	AUTO	AUDION	INT0	INT1	SDTO	VOUT
1	x	x	x	“H”	Note 40	“L”	“L”
0	1	x	x			Previous Data	Output
0	0	x	x	“L”		Output	Output
x	x	1	x	Note 41	“H”	Note 42	Note 43
x	x	x	1				
x	x	0	0		“L”		

Note 40. INT1 pin outputs “L” or “H” in accordance with the ORed signal between AUTO and AUDION.

Note 41. INT0 pin outputs “L” or “H” in accordance with the ORed signal between UNLCK and PAR.

Note 42. SDTO pin outputs “L”, “Previous Data” or “Normal Data” in accordance with the ORed signal between UNLCK and PAR.

Note 43. VOUT pin outputs “L” or “Normal operation” in accordance with the ORed signal between PAR and UNCLK.

Table 25. Error Handling in parallel mode (x: Don’t care)

2. Serial Mode

In serial mode, the INT1 and INT0 pins output an ORed signal based on the above nine interrupt events. When masked, the interrupt event does not affect the operation of the INT1-0 pins (the masks do not affect the registers in 07H and DAT bit). Once INT0 pin goes to “H”, it remains “H” for 1024/fs (this value can be changed by the EFH1-0 bits) after all events not masked by mask bits are cleared. INT1 pin immediately goes to “L” when those events are cleared.

UNLCK, PAR, AUTO, AUDION and VRX bits in Address=07H indicate the interrupt status events above in real time. Once QINT, CINT and DAT bits go to “1”, it stays “1” until the register is read.

When the AK4115 loses lock, the channel status bit, user bit, Pc and Pd are initialized. In this initial state, INT0 pin outputs the ORed signal between UNLCK and PAR bits. INT1 pin outputs the ORed signal between AUTO and AUDION bits.

Event			Pin		
UNLCK	PAR	Others	SDTO	VOUT	TX
1	x	x	“L”	“L”	Output
0	1	x	Previous Data	Output	Output
x	x	x	Output	Output	Output

Table 26. Error Handling in serial mode (x: Don’t care)

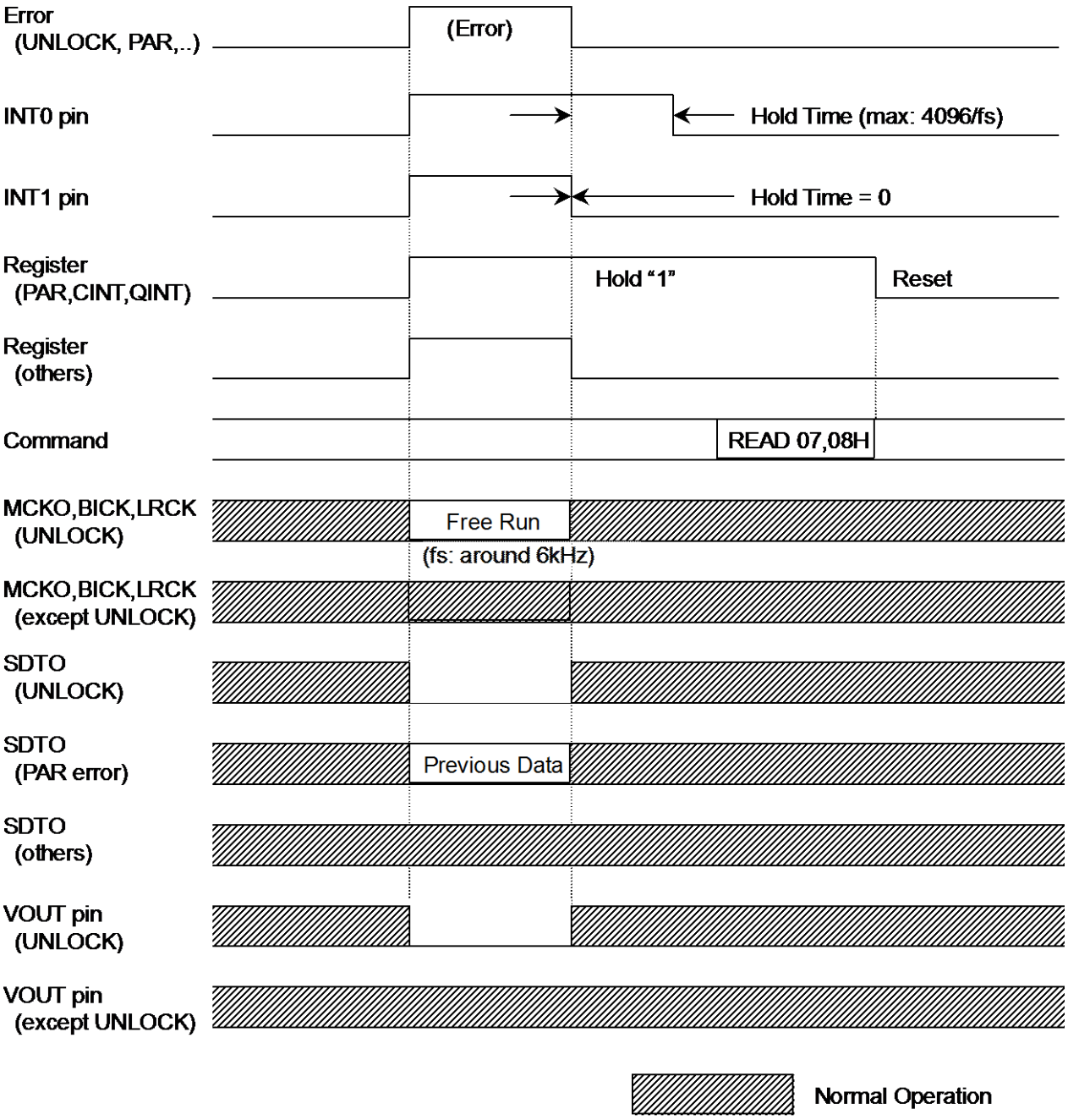


Figure 31. INT0/1 pin timing

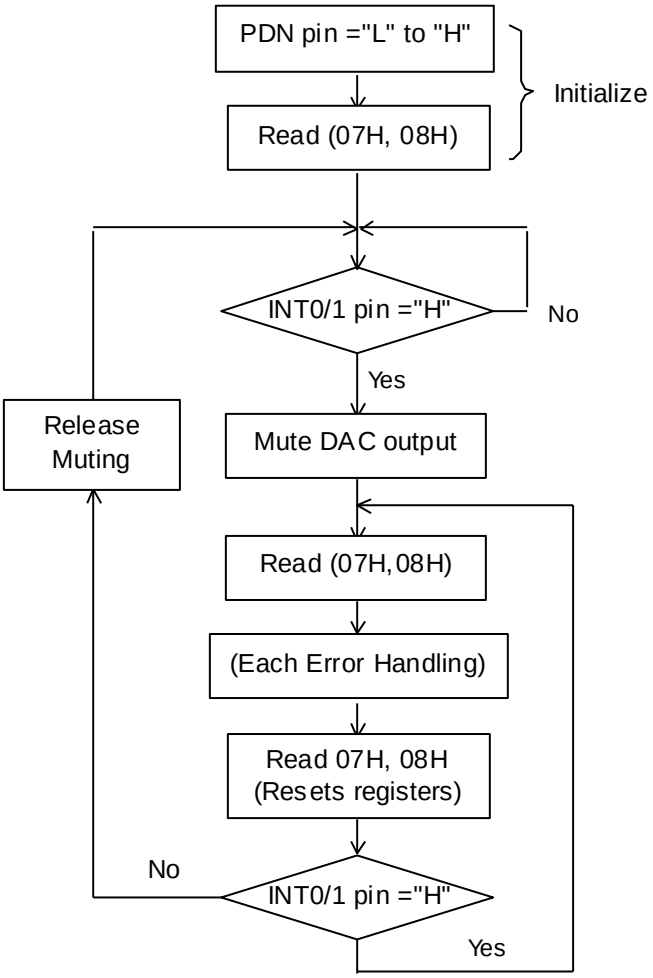


Figure 32. Error Handling Sequence Example 1

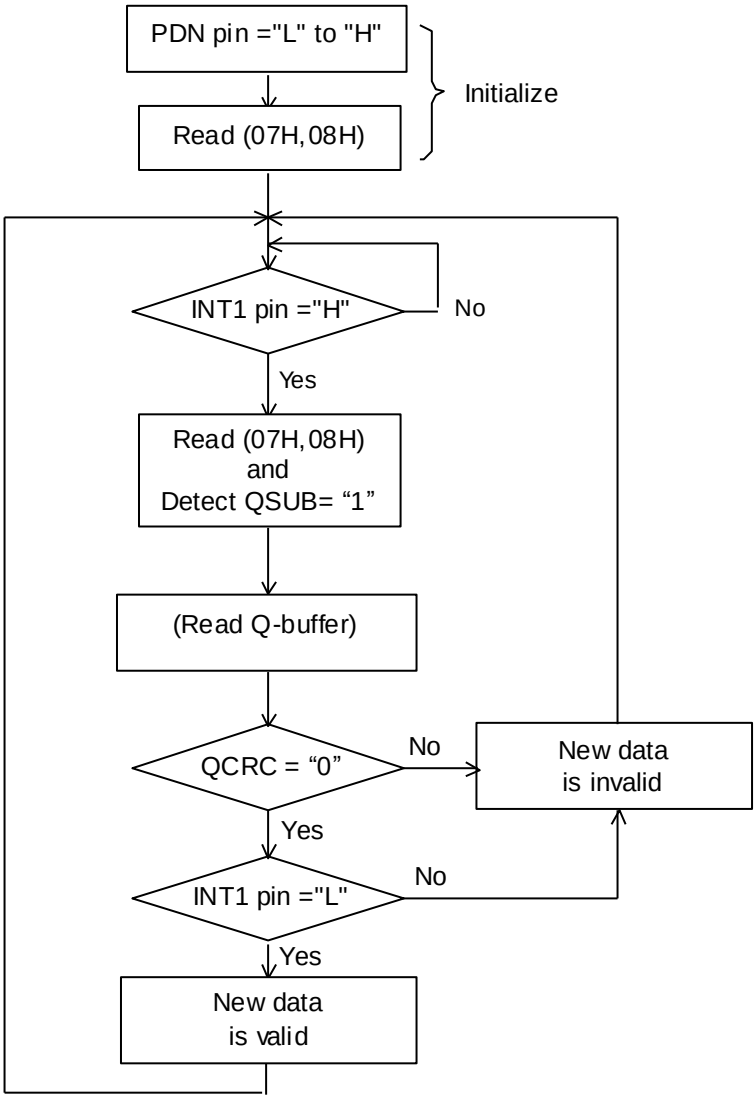


Figure 33. Error Handling Sequence Example (for Q/CINT)

■ Error Handing for ELRCK (PSEL = "1")

The followings two events cause the INT0 and INT1 pins to show the status of the interrupt conditions. When the PLL is OFF (Clock Operation Mode 1), the INT0 and INT1 pins go to "L".

1. UNLCK : PLL unlock state detect
   "1" when the PLL loses lock.
   The AK4115 loses lock when the phase difference between the current ELRCK and the previous ELRCK is more than 5% after "4 x fs".
   The PLL is locked when the phase difference between the current ELRCK and the pervious ELRCK is less than 2% after "256 x fs".
   When the PLL loses lock, the PLL goes to a free running state. The sampling frequency is typically 11kHz in this case.

2. FS3-0 : Sampling frequency detection
   FS3-0 bits are updated every "128 x fs". When FS3-0 bits are changed, the STC bit is not changed and the INT0 and INT1 pins go to "H" after "1 x fs"

In this mode, INT0 does not have the hold function. Therefore, INT0 and INT1 go to "L" at the same time when those events are removed. Each INT0/1 pins can mask those two events individually.

1. Parallel Mode

In parallel mode, INT0 triggers UNLCK, and INT1 triggers when FS3-0 bits are changed. INT0 and INT1 go "L" after each event is removed.

2. Serial Mode

In serial mode, INT1 and INT0 outputs an ORed signal based on the two interrupt events shown above. When masked, the interrupt event does not affect operation of the INT1-0.

Event		Pin	
UNLCK	Change of FS3-0 bits	SDTO	TX
1	x	"L"	Output
0	1	Output	Output

Table 27. Error Handling (x: Don't care)

■ Audio Serial Interface Format

1. LRCK, BICK, SDTO and DAUX

In serial mode, the DIF2-0 bits can select eight serial audio data formats as shown in Table 28. In parallel mode, the DIF0 and DIF1 pins can select four serial audio data format as shown in Table 29. In Mode0-7, the serial data is MSB-first, 2's complement format. The SDTO is clocked out on the falling edge of BICK and DAUX is latched on the rising edge of BICK. BICK outputs 64fs clock in Mode 0-5. Mode 6-7 are Slave Modes, and BICK is available up to 128fs at fs=48kHz. If the data word length is equal or less than 20bit (Mode0-2), the LSBs in the sub-frame are truncated. In Mode 3-7, the last 4LSBs are auxiliary data (see Figure 34).

When the Parity Error, Bi-phase Error or Frame Length Error occurs in a sub-frame, the AK4115 continues to output the last normal sub-frame data from SDTO repeatedly until the error is removed. When the Unlock Error occurs, AK4115 outputs "0" from SDTO. If DAUX is used, the data is transformed and outputted from SDTO. DAUX is used in Clock Operation Mode 1, 3 and unlock state of Mode 2.

The input data format to DAUX should be left justified except in Mode5 and 7(Table 28). In Mode5 or 7, both the input data format of DAUX and output data format of SDTO are I^2S. Mode 6 and 7 are Slave Modes that corresponds to the Master Mode of Mode4 and 5. In Slave Mode, LRCK and BICK should be synchronized with MCKO1/2.

When AES3 bit is set to "1", SDTO becomes AES3 mode. The serial data is LSB-first, 2's complement format. The V, C, U and B bits behind the audio data are added. The B bit goes to "1" when the B-sync in preamble is detected (Figure 39).

When DAUX is sent to SDTO, the data format depends on DIF0 bit. When DIF0 bit is set to "0", the received MSB-first, 24bit MSB justified is converted to LSB-first, 24bit MSB justified. Then the only audio data is converted and V, U, C and B bits set to "0". When DIF0 bit is set to "1", the AES3 format received from DAUX pin is maintained and is sent to SDTO pin. Mode 8-9 support only synchronous mode (ASYNC bit = "0").

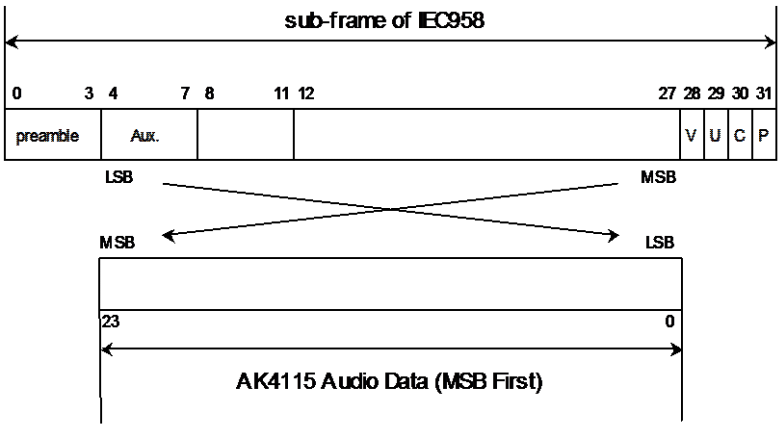


Figure 34. Bit configuration

Mode	AES3 bit	DIF2 bit	DIF1 bit	DIF0 bit	DAUX	SDTO	LRCK		BICK		
								I/O		I/O	
0	0	0	0	0	24bit, Left justified	16bit, Right justified	H/L	O	64fs	O	
1	0	0	0	1	24bit, Left justified	18bit, Right justified	H/L	O	64fs	O	
2	0	0	1	0	24bit, Left justified	20bit, Right justified	H/L	O	64fs	O	
3	0	0	1	1	24bit, Left justified	24bit, Right justified	H/L	O	64fs	O	
4	0	1	0	0	24bit, Left justified	24bit, Left justified	H/L	O	64fs	O	
5	0	1	0	1	24bit, I^2S	24bit, I^2S	L/H	O	64fs	O	
6	0	1	1	0	24bit, Left justified	24bit, Left justified	H/L	I	64-128fs	I	Default
7	0	1	1	1	24bit, I^2S	24bit, I^2S	L/H	I	64-128fs	I	
8	1	0	0	0	24bit, Left justified	AES3 Mode	H/L	O	64fs	O	
9	1	0	0	1	AES Mode	AES3 Mode	H/L	O	64fs	O	

Table 28. Audio data format in serial mode

Mode	DIF1 pin	DIF0 pin	DAUX	SDTO	LRCK		BICK	
						I/O		I/O
4	0	0	24bit, Left justified	24bit, Left justified	H/L	O	64fs	O
5	0	1	24bit, I^2S	24bit, I^2S	L/H	O	64fs	O
6	1	0	24bit, Left justified	24bit, Left justified	H/L	I	64-128fs	I
7	1	1	24bit, I^2S	24bit, I^2S	L/H	I	64-128fs	I

Table 29. Audio data format in parallel mode

2. EMCK, ELRCK, EBICK and DAUX

In asynchronous mode, the audio data format of DAUX is selected by EDIF1-0 bits. The clock source of master clock selects X'tal or EMCK by the MSEL bit. In parallel mode, this function is not supported.

Mode	EDIF1 bit	EDIF0 bit	DAUX	ELRCK		EBICK		
					I/O		I/O	
4	0	0	24bit, Left justified	H/L	O	64fs	O	
5	0	1	24bit, I^2S	L/H	O	64fs	O	
6	1	0	24bit, Left justified	H/L	I	64-128fs	I	Default
7	1	1	24bit, I^2S	L/H	I	64-128fs	I	

Table 30. Audio data format in asynchronous mode

In asynchronous mode, the frequecny of EMCK/X'tal selects 128fs, 256fs or 512fs. It is controlled by ECKS1-0 bit.

ECKS1	ECKS0	EMCK Frequency	fs(max)	
0	0	512fs	54kHz	
0	1	256fs	108kHz	Default
1	0	128fs	216kHz	
1	1	N/A	-	

Table 31. EMCK Frequency

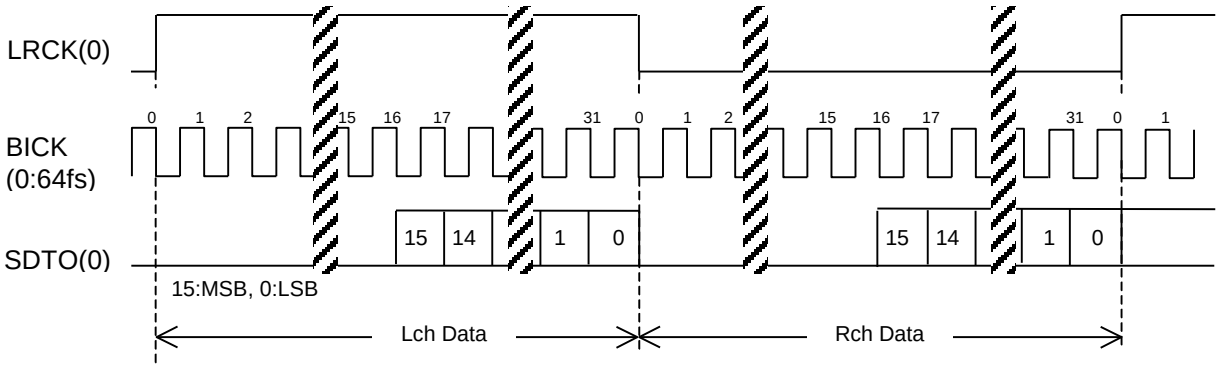


Figure 35. Mode 0 Timing

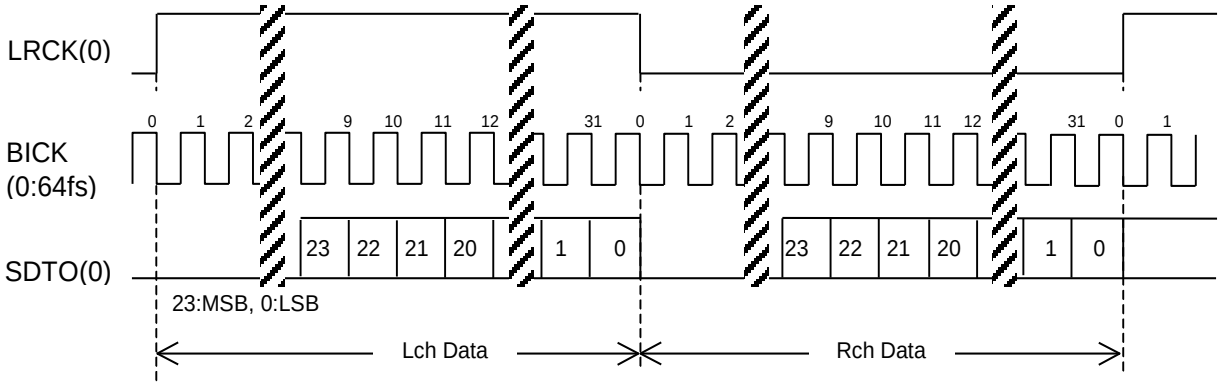


Figure 36. Mode 3 Timing

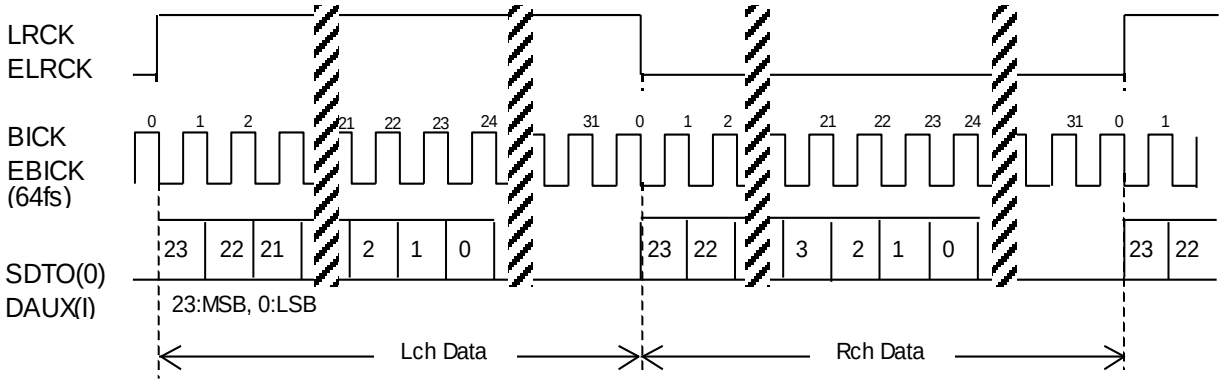


Figure 37. Mode 4, 6 Timing

Mode4 : LRCK, BICK, ELRCK, EBICK : Output
Mode6 : LRCK, BICK, ELRCK, EBICK: Input

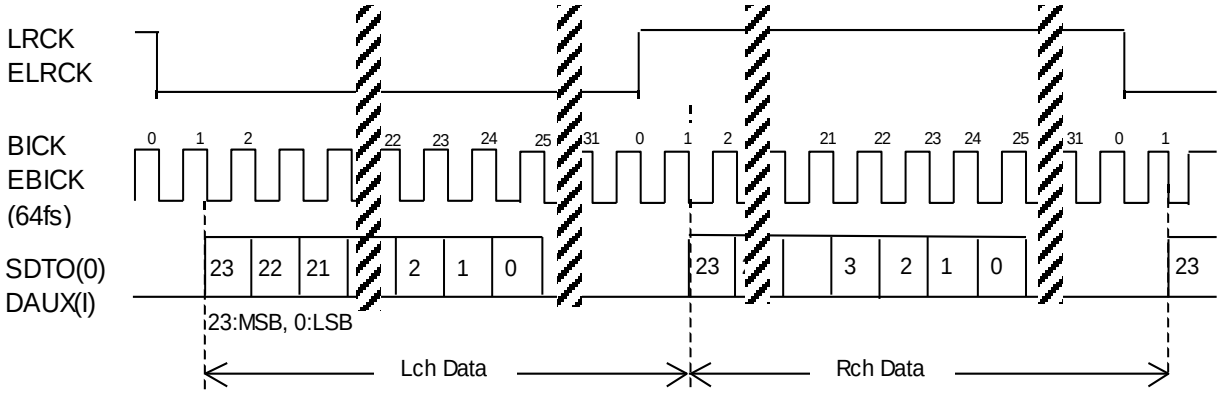


Figure 38. Mode 5, 7 Timing

Mode5 : LRCK, BICK, ELRCK, EBICK : Output
Mode7 : LRCK, BICK, ELRCK, EBICK : Input

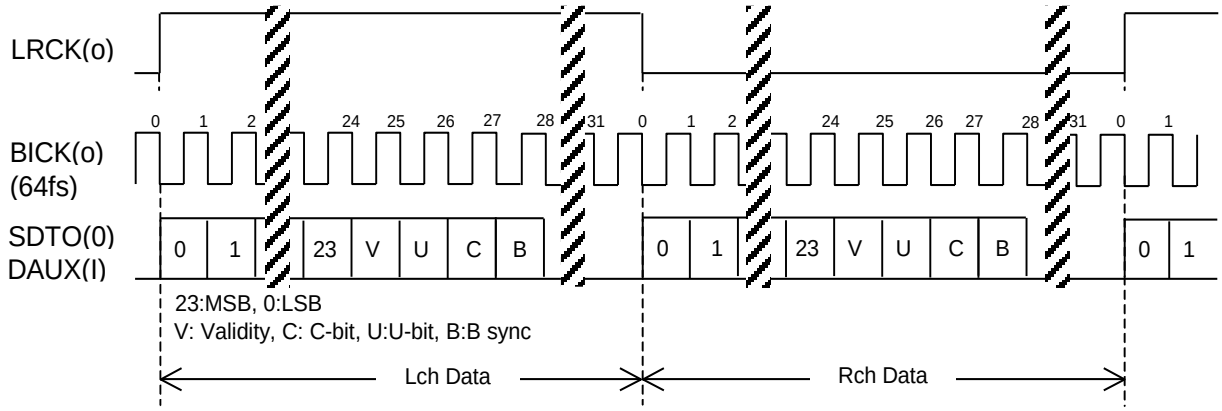
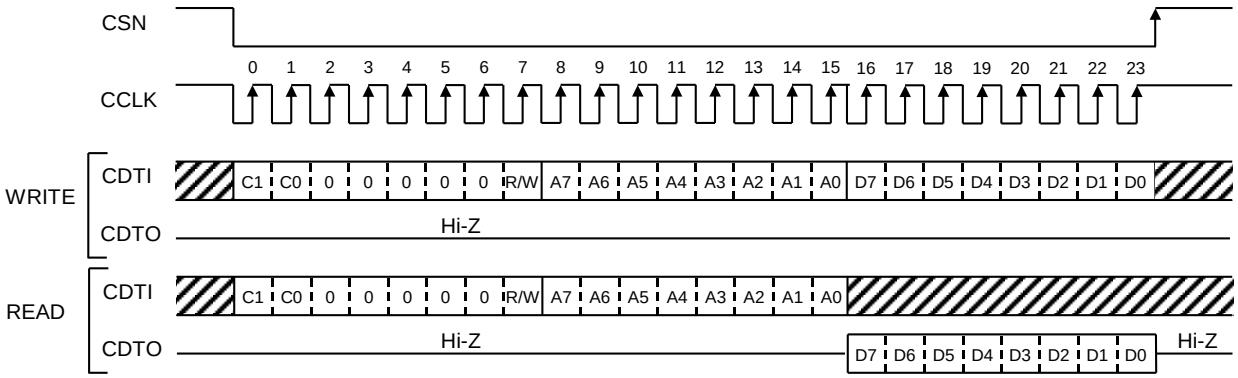


Figure 39. AES3 Mode

■ Serial Control Interface

1. 4-wire serial control mode (IIC pin = "L")

The internal registers may be either written or read by the 4-wire μP interface pins: CSN, CCLK, CDTI & CDTO. The data on this interface consists of Chip address (2-bits, C1-0 are fixed to "00"), Read/Write (1bit), Register address (MSB first, 8-bits) and Control data (MSB first, 8-bits). Address and data is clocked in on the rising edge of CCLK and data is clocked out on the falling edge. For write operations, data is latched after the 24th rising edge of CCLK, after a high-to-low transition of CSN. For read operations, the CDTO output goes high impedance after a low-to-high transition of CSN. The maximum speed of CCLK is 5MHz. PDN pin = "L" resets the registers to their default values. When the state of P/SN pin is changed, the AK4115 should be reset by PDN pin = "L". CSN should be brought "H" after each word.



C1-C0: Chip Address (Fixed to "00")
R/W: READ/WRITE (0:READ, 1:WRITE)
A7-A0: Register Address
D7-D0: Control Data

Figure 40. 4-wire Serial Control I/F Timing

2. I²C bus control mode (IIC pin = "H")

AK4115 supports a fast-mode I²C-bus system (max : 400kHz).

2-1. Data transfer

All commands are preceded by a START condition. After the START condition, a slave address is sent. After the AK4115 recognizes the START condition, the device interfaced to the bus waits for the slave address to be transmitted over the SDA line. If the transmitted slave address matches an address for one of the devices, the designated slave device pulls the SDA line to LOW (ACKNOWLEDGE). The data transfer is always terminated by a STOP condition generated by the master device.

2-1-1. Data validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW except for the START and the STOP condition.

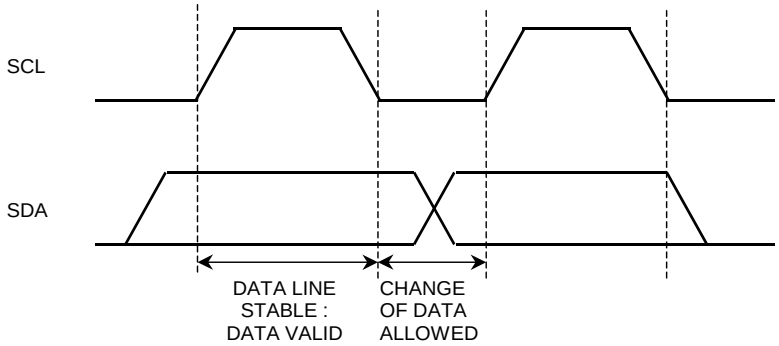


Figure 41. Data transfer

2-1-2. START and STOP condition

A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition. All sequences start from the START condition.
A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition. All sequences end by the STOP condition.

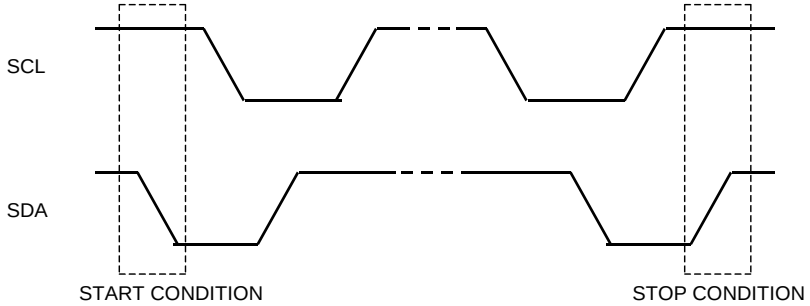


Figure 42. START and STOP conditions

2-1-3. ACKNOWLEDGE

ACKNOWLEDGE is a software convention used to indicate successful data transfers. The transmitting device will release the SDA line (HIGH) after transmitting eight bits. The receiver must pull down the SDA line during the acknowledge clock pulse so that that it remains stable "L" during "H" period of this clock pulse. The AK4115 will generates an acknowledge after each byte has been received.
In the read mode, the slave, AK4115 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no STOP condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the STOP condition.

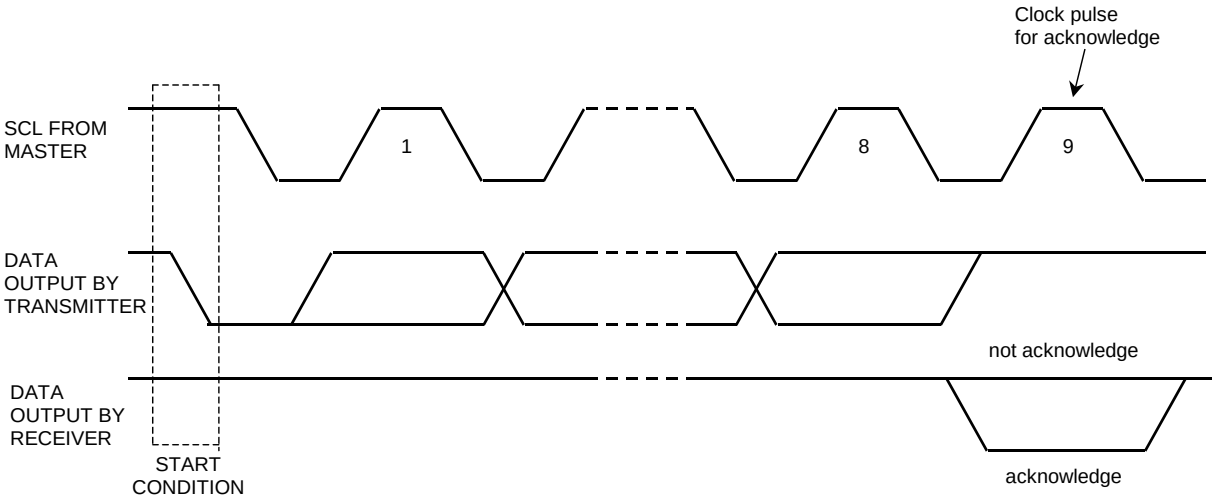


Figure 43. Acknowledge on the I^2C-bus

2-1-4. FIRST BYTE

The first byte, which includes seven bits of slave address and one bit of R/W bit, is sent after the START condition. If the transmitted slave address matches an address for one of the device, the receiver who has been addressed pulls down the SDA line.
The most significant five bits of the slave address are fixed as "00100". The next two bits are CAD1 and CAD0 (device address bits). These two bits identify the specific device on the bus. The hard-wired input pins (CAD1 pin and CAD0 pin) set them. The eighth bit (LSB) of the first byte (R/W bit) defines whether a write or read condition is requested by the master. A "1" indicates that the read operation is to be executed. A "0" indicates that the write operation is to be executed.

0	0	1	0	0	CAD1	CAD0	R/W

(Those CAD1/0 should match with CAD1/0 pins.)

Figure 44. The First Byte

2-2. WRITE Operations

Set R/W bit = "0" for the WRITE operation of AK4115.
After receipt the start condition and the first byte, the AK4115 generates an acknowledge, and awaits the second byte (register address). The second byte consists of the address for control registers of AK4115. The format is MSB first, 8-bits.

A7	A6	A5	A4	A3	A2	A1	A0

Figure 45. The Second Byte

After receipt of the second byte, the AK4115 generates an acknowledge, and awaits the third byte. Those data after the second byte contain control data. The format is MSB first, 8-bits.

D7	D6	D5	D4	D3	D2	D1	D0

Figure 46. Byte structure after the second byte

The AK4115 is capable of more than one byte write operation by one sequence.
After receipt of the third byte, the AK4115 generates an acknowledge, and awaits the next data again. The master can transmit more than one word instead of terminating the write cycle after the first data word is transferred. After the receipt of each data, the internal 5-bit address counter is incremented by one, and the next data is taken into next address automatically. If the address exceed 49H prior to generating the stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

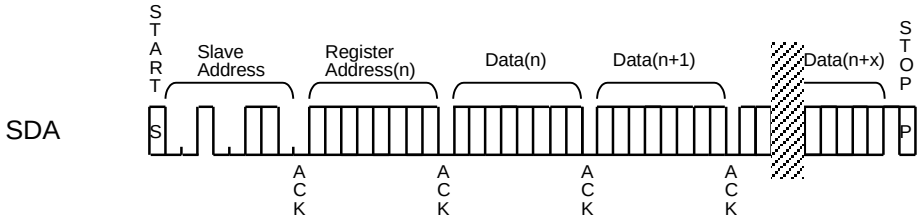


Figure 47. WRITE Operation

2-3. READ Operations

Set R/W bit = "1" for the READ operation of AK4115.
After transmission of a data, the master can read next address's data by generating the acknowledge instead of terminating the write cycle after the receipt the first data word. After the receipt of each data, the internal 5-bit address counter is incremented by one, and the next data is taken into next address automatically. If the address exceed 49H prior to generating the stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.
The AK4115 supports two basic read operations: CURRENT ADDRESS READ and RANDOM READ.

2-3-1. CURRENT ADDRESS READ

The AK4115 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next CURRENT READ operation would access data from the address n+1.
After receipt of the slave address with R/W bit set to "1", the AK4115 generates an acknowledge, transmits 1byte data which address is set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but generate the stop condition, the AK4115 discontinues transmission.

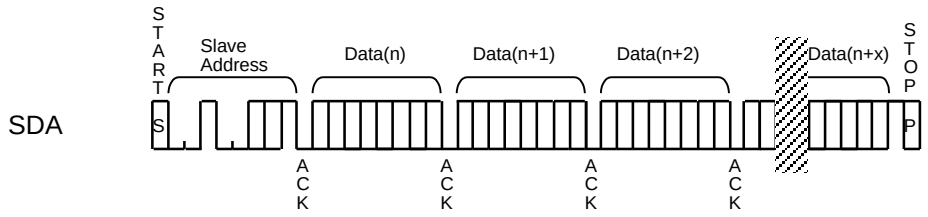


Figure 48. CURRENT ADDRESS READ

2-3-2. RANDOM READ

Random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit set to "1", the master must first perform a "dummy" write operation.
The master issues the start condition, slave address(R/W="0") and then the register address to read. After the register address's acknowledge, the master immediately reissues the start condition and the slave address with the R/W bit set to "1". Then the AK4115 generates an acknowledge, 1byte data and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but generate the stop condition, the AK4115 discontinues transmission.

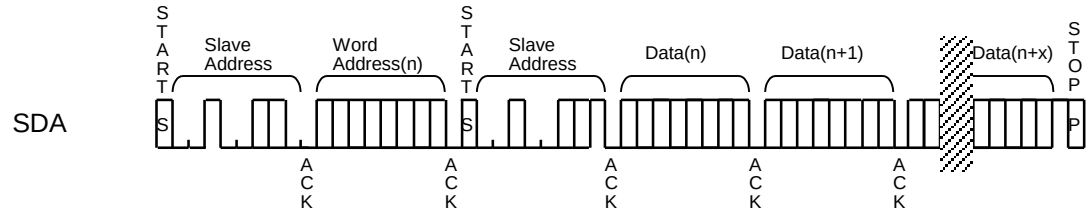


Figure 49. RANDOM READ

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	CLK & Power Down Control	CS12	BCU	CM1	CM0	OCKS1	OCKS0	PWN	RSTN
01H	Format & De-em Control	AES3	DIF2	DIF1	DIF0	DEAU	DEM1	DEM0	ACKS
02H	Input/ Output Control 0	TX1E	OPS12	OPS11	OPS10	TX0E	OPS02	OPS01	OPS00
03H	Input/ Output Control 1	EFH1	EFH0	UDIT	BCU_IO	DIT	IPS2	IPS1	IPS0
04H	INT0 MASK	MQIT0	MAUT0	MCIT0	MULK0	MV0	MSTC0	MAUD0	MPAR0
05H	INT1 MASK	MQIT1	MAUT1	MCIT1	MULK1	MV1	MSTC1	MAUD1	MPAR1
06H	DAT Mask & DTS Detect	DIV	XMCK	FAST	DCNT	DTS16	DTS14	MDAT1	MDAT0
07H	Receiver Status 0	QINT	AUTO	CINT	UNLCK	VRX	STC	AUDION	PAR
08H	Receiver Status 1	FS3	FS2	FS1	FS0	PEM	DAT	DTSCD	NPCM
09H	Receiver Status 2	0	0	0	0	0	0	QCRC	CCRC
0AH	Clock Control	TX1NE	0	MCK2E	MCK1E	ASYNC	WSYNC	XSEL	PSEL
0BH	TX Control	MSEL	ECKS1	ECKS0	EDIF1	EDIF0	CTRAN	CCRE	VTX
0CH	RX Channel Status Byte 0	CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
•	•	•	•	•	•	•	•	•	•
23H	RX Channel Status Byte 23	CR191	CR190	CR189	CR188	CR187	CR186	CR185	CR184
24H	TX Channel Status Byte 0	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0
•	•	•	•	•	•	•	•	•	•
3BH	TX Channel Status Byte 23	CT191	CT190	CT189	CT188	CT187	CT186	CT185	CT184
3CH	Burst Preamble Pc Byte 0	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
3DH	Burst Preamble Pc Byte 1	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8
3EH	Burst Preamble Pd Byte 0	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
3FH	Burst Preamble Pd Byte 1	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8
40H	Q-subcode Address / Control	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2
41H	Q-subcode Track	Q17	Q16	Q15	Q14	Q13	Q12	Q11	Q10
42H	Q-subcode Index	Q25	Q24	Q23	Q22	Q21	Q20	Q19	Q18
43H	Q-subcode Minute	Q33	Q32	Q31	Q30	Q29	Q28	Q27	Q26
44H	Q-subcode Second	Q41	Q40	Q39	Q38	Q37	Q36	Q35	Q34
45H	Q-subcode Frame	Q49	Q48	Q47	Q46	Q45	Q44	Q43	Q42
46H	Q-subcode Zero	Q57	Q56	Q55	Q54	Q53	Q52	Q51	Q50
47H	Q-subcode ABS Minute	Q65	Q64	Q63	Q62	Q61	Q60	Q59	Q58
48H	Q-subcode ABS Second	Q73	Q72	Q71	Q70	Q69	Q68	Q67	Q66
49H	Q-subcode ABS Frame	Q81	Q80	Q79	Q78	Q77	Q76	Q75	Q74
4AH	Optional Control	0	0	0	0	0	0	CTX	0

Notes:

When PDN pin goes “L”, the registers are initialized to their default values.
When RSTN bit goes “0”, the internal timing is reset and the registers are initialized to their default values.
All data can be written to the register even if PWN bit is “0”.
Data must not be written to addresses 4BH through FFH.

■ Register Definitions

Reset & Initialize

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	CLK & Power Down Control	CS12	BCU	CM1	CM0	OCKS1	OCKS0	PWN	RSTN
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	1	0	0	0	0	1	1

RSTN: Timing Reset & Register Initialize
- 0: Reset & Initialize
- 1: Normal Operation (Default)

PWN: Power Down
- 0: Power Down
- 1: Normal Operation (Default)

OCKS1-0: Master Clock Frequency Select (See Table 9)

CM1-0: Master Clock Operation Mode Select (See Table 3 and Table 5)

BCU: Block start & C/U Output Mode when BCU_IO bit is "1"

When using DIT and DIR at the same time in asynchronous mode (ASYNC bit = "1") both BCU_IO bit = "1" and BCU bit = "1" settings are prohibited.
- 0: B, C and U pins output "L".
- 1: B, C, and U pins output the data recovered from biphase signal. (Default)

When BCU_IO bit is "0", BCU bit is ignored.

CS12: Channel Status Select
- 0: Channel 1 (Default)
- 1: Channel 2

Selects which channel status is used to derive C-bit buffers, AUDION, PEM, FS3, FS2, FS1, FS0, Pc and Pd. The de-emphasis filter is controlled by channel 1 in the Parallel Mode.

Format & De-emphasis Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Format & De-em Control	AES3	DIF2	DIF1	DIF0	DEAU	DEM1	DEM0	ACKS
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	1	1	0	1	0	1	0

ACKS: Master clock Auto Setting Mode
- 0: Disable (Default)
- 1: Enable

DEM1-0: 32, 44.1, 48kHz De-emphasis Control (See Table 18)

DEAU: De-emphasis Auto Detect Enable
- 0: Disable
- 1: Enable (Default)

DIF2-0, AES3: Audio Data Format Control (See Table 28)

Input/Output Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Input/ Output Control 0	TX1E	OPS12	OPS11	OPS10	TX0E	OPS02	OPS01	OPS00
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	0	0	1	0	0	0

OPS02-00: Output Through Data Select for TX0 pin (See Table 21)
TX0E: TX0 Output Enable
0: Disable. TX0 outputs "L".
1: Enable (Default)
OPS12-10: Output Through Data Select for TX1 pin (See Table 22)
TX1E: TXP1/TXN1 pins Output Enable
0: Disable. TXP1 pin outputs "L". TXN1 pin outputs "H".
1: Enable (Default)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Input/ Output Control 1	EFH1	EFH0	UDIT	BCU_IO	DIT	IPS2	IPS1	IPS0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	1	0	1	1	0	0	0

IPS2-0: Input Recovery Data Select (See Table 19)
DIT: Through data/Transmit data select for TXP1/N1 pins
0: Through data (RX data).
1: Transmit data (DAUX data). (Default)
BCU_IO: Select I/O of B, C and U pins
When using DIT and DIR at the same time in asynchronous mode (ASYNC bit = "1") both BCU_IO bit = "1" and BCU bit = "1" settings are prohibited.

0: Input
1: Output (Default)
UDIT: U bit control for DIT
0: U bit is fixed to "0". (Default)
1: Recovered U bit is used for DIT (loop mode for U bit)
EFH1-0: Interrupt 0 Pin Hold Count Select
00: 512 LRCK 01: 1024 LRCK (Default)
10: 2048 LRCK 11: 4096 LRCK

Mask Control for INT0

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	INT0 MASK	MQIT0	MAUT0	MCIT0	MULK0	MVRX0	MSTC0	MAUD0	MPAR0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	0	1	1	1	0

MPAR0: Mask enable for PAR bit
0: Mask disable (Default)
1: Mask enable
MAUD0:Mask enable for AUDION bit
0: Mask disable
1: Mask enable (Default)
MSTC0: Mask enable for STC bit
0: Mask disable
1: Mask enable (Default)
MVRX0:Mask enable for VRX bit
0: Mask disable
1: Mask enable (Default)
MULK0:Mask enable for UNLCK bit
0: Mask disable (Default)
1: Mask enable
MCIT0: Mask enable for CINT bit
0: Mask disable
1: Mask enable (Default)
MAUT0:Mask enable for AUTO bit
0: Mask disable
1: Mask enable (Default)
MQIT0: Mask enable for QINT bit
0: Mask disable
1: Mask enable (Default)

When mask is set to “1”, corresponding event does not affect INT0 pin operation.

Mask Control for INT1

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	INT1 MASK	MQIT1	MAUT1	MCIT1	MULK1	MVRX1	MSTC1	MAUD	MPAR1
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	1	1	1	1	0	1

MPAR1: Mask enable for PAR bit
0: Mask disable
1: Mask enable (Default)
MAUD1:Mask enable for AUDION bit
0: Mask disable (Default)
1: Mask enable
MSTC1: Mask enable for STC bit
0: Mask disable
1: Mask enable (Default)
MVRX1:Mask enable for VRX bit
0: Mask disable
1: Mask enable (Default)
MULK1:Mask enable for UNLCK bit
0: Mask disable
1: Mask enable (Default)
MCIT1: Mask enable for CINT bit
0: Mask disable
1: Mask enable (Default)
MAUT1:Mask enable for AUTO bit
0: Mask disable (Default)
1: Mask enable
MQIT1: Mask enable for QINT bit
0: Mask disable
1: Mask enable (Default)

When mask is set to “1”, corresponding event does not affect INT1 pin operation.

DAT Mask & DTS Detect

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	DAT Mask & DTS Detect	DIV	XMCK	FAST	DCNT	DTS16	DTS14	MDAT1	MDAT0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	1	1	1	1	1

MDAT0: Mask enable for DAT bit
0: Mask disable
1: Mask enable (Default)
The factor which mask bit is set to "0" affects INT0 pin operation.
MDAT1: Mask enable for DAT bit
0: Mask disable
1: Mask enable (Default)
The factor which mask bit is set to "0" affects INT1 pin operation.
DTS14: DTS-CD 14bit Sync Word Detect
0: Disable
1: Enable (Default)
DTS16: DTS-CD 16bit Sync Word Detect
0: Disable
1: Enable (Default)
DCNT: DAT Start ID Counter
0: Disable
1: Enable (Default)
FAST: Select PLL Lock Time when the biphase signal is recovered.
0: ≤ (20ms + 384/fs) (Default)
1: ≤ (20ms + 1/fs)
XMCK: Select output frequency of MCKO2 (See Table 10)
0: Depends on CM1-0 bits and OCKS1-0 bits (Default)
1: Fixed to X'tal Mode
DIV: MCKO2 Output Frequency Select at X'tal Mode (See Table 10)
0: Same frequency as X'tal (Default)
1: Half frequency of X'tal

Receiver Status 0

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	Receiver status 0	QINT	AUTO	CINT	UNLCK	VRX	STC	AUDION	PAR
R/W		RD	RD	RD	RD	RD	RD	RD	RD
Default		0	0	0	0	0	0	0	0

PAR: Parity Error or Bi-phase Error Status
0: No Error
1: Error
This bit goes to "1", if a Parity Error or Biphase Error is detected in the sub-frame.

AUDION: Audio Bit Output
0: Audio
1: Non Audio
This bit is made by encoding channel status bits.

STC: Sampling Frequency or Pre-emphasis Information Change Detection
0: No detect
1: Detect
This bit goes to "1" when either the FS3-0 or PEM bit changes.

VRX: Validity of channel status for RX
0: Valid
1: Invalid

UNLCK: PLL Lock Status
0: Lock
1: Unlock

CINT: Channel Status Buffer Interrupt
0: No change
1: Changed
This bit goes to "1" when C-bit stored in register addresses 0CH to 24H changes.

AUTO: Non-PCM/DTSCD Bitstream Detection
0: PCM Detected
1: Non-PCM/DTSCD Detected

QINT: Q-subcode Buffer Interrupt
0: No change
1: Changed
This bit goes to "1" when Q-subcode stored in register addresses 40H to 49H changes.

STC, QINT, CINT and PAR bits are initialized when 07H is read.

Receiver Status 1

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	Receiver status 1	FS3	FS2	FS1	FS0	PEM	DAT	DTSCD	NPCM
R/W		RD	RD	RD	RD	RD	RD	RD	RD
Default		0	0	0	1	0	0	0	0

NPCM: Non-PCM Bit Stream Auto Detection
0: No detect
1: Detect
DTSCD: DTS-CD Bit Stream Auto Detection
0: No detect
1: Detect
DAT: DAT Start ID Detect
0: No detect
1: Detect
DAT bit is initialized when 08H is read.
PEM: Pre-emphasis Detect
0: OFF
1: ON
This bit is made by encoding channel status bits.
FS3-0: Sampling Frequency detection (See Table 14)

Receiver Status 1

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	Receiver status 1	0	0	0	0	0	0	QCRC	CCRC
R/W		RD	RD	RD	RD	RD	RD	RD	RD
Default		0	0	0	0	0	0	0	0

CCRC: Cyclic Redundancy Check for Channel Status
0: No error
1: Error
This bit is enabled only in professional mode and only for the channel selected by the CS12 bit.
QCRC: Cyclic Redundancy Check for Q-subcode
0: No error
1: Error

Clock Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	Clock Control	TX1NE	0	MCK2E	MCK1E	ASYNC	WSYNC	XSEL	PSEL
R/W		R/W	RD	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	1	1	0	0	0	0

PSEL: Setting of PLL reference clock (See Table 1)
XSEL: Setting of X'tal oscillator (See Table 12)
WSYNC: Synchronization between the biphase signal and ELRCK
0: Disable (Default)
1: Enable
ASYNC: Setting of synchronous / asynchronous mode for DIT/DIR
0: Synchronous mode (Default)
1: Asynchronous mode
MCK1E: Setting of MCKO1 output
0: Disable. Output "L".
1: Enable (Default)
MCK2E: Setting of MCKO2 output
0: Disable. Output "L".
1: Enable (Default)
TX1NE: Setting of TXN1 pin.
0: Disable. Output "L". This mode is useful for consumer.
1: Enable (Default)

TX Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0BH	TX Control	MSEL	ECKS1	ECKS0	EDIF1	EDIF0	CTRAN	CCRE	VTX
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	1	1	0	0	1	0

VTX: Setting of Validity bit for TX
0: Valid (Default)
1: Invalid
CCRE: CCRC Enable at professional mode
0: CCRC data is not generated.
1: CCRC data is generated in professional mode. In consumer mode, CCRC data is not generated. (Default)
CTRAN: Transfer mode of CR191-0 bits
0: Not transfer or finish to transfer (Default)
1: Transfer
All CR191-0 bits is transferred to CT191-0 bits when CTRAN bit changes "0" to "1". The transferred CT191-0 bits are valid after next block start signal is detected. CTRAN bit goes to "0" after finishing the transfer.
EDIF1-0: Setting of audio interface mode in asynchronous mode. (See Table 30)
ECK1-0: Setting of EMCK input frequency (See Table 31)
MSEL: Master clock setting for TX in asynchronous mode (See Table 4)

Receiver Channel Status

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0CH	RX Channel Status Byte 0	CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
•	•	•	•	•	•	•	•	•	•
23H	RX Channel Status Byte 23	CR191	CR190	CR189	CR188	CR187	CR186	CR185	CR184
R/W		RD							
Default		Not initialized							

CR191-0: Receiver Channel Status Byte 23-0

Transmitter Channel Status

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
24H	TX Channel Status Byte 0	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0
R/W		R/W							
Default		0	0	0	0	0	1	0	0
25H	TX Channel Status Byte 1	CT15	CT14	CT13	CT12	CT11	CT10	CT9	CT8
•	•	•	•	•	•	•	•	•	•
3BH	TX Channel Status Byte 23	CT191	CT190	CT189	CT188	CT187	CT186	CT185	CT184
R/W		R/W							
Default		0							

CT7-0: Transmitter Channel Status Byte 0
Default: “00000100”
CT191-8: Transmitter Channel Status Byte 23-1
Default: “00000000”

Burst Preamble Pc/Pd in non-PCM encoded Audio Bitstreams

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
3CH	Burst Preamble Pc Byte 0	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
3DH	Burst Preamble Pc Byte 1	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8
3EH	Burst Preamble Pd Byte 0	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
3FH	Burst Preamble Pd Byte 1	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8
R/W		RD							
Default		Not initialized							

PC15-0: Burst Preamble Pc Byte 0 and 1
PD15-0: Burst Preamble Pd Byte 0 and 1

Q-subcode Buffer

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
40H	Q-subcode Address / Control	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2
41H	Q-subcode Track	Q17	Q16	Q15	Q14	Q13	Q12	Q11	Q10
42H	Q-subcode Index	Q25	Q24	Q23	Q22	Q21	Q20	Q19	Q18
43H	Q-subcode Minute	Q33	Q32	Q31	Q30	Q29	Q28	Q27	Q26
44H	Q-subcode Second	Q41	Q40	Q39	Q38	Q37	Q36	Q35	Q34
45H	Q-subcode Frame	Q49	Q48	Q47	Q46	Q45	Q44	Q43	Q42
46H	Q-subcode Zero	Q57	Q56	Q55	Q54	Q53	Q52	Q51	Q50
47H	Q-subcode ABS Minute	Q65	Q64	Q63	Q62	Q61	Q60	Q59	Q58
48H	Q-subcode ABS Second	Q73	Q72	Q71	Q70	Q69	Q68	Q67	Q66
49H	Q-subcode ABS Frame	Q81	Q80	Q79	Q78	Q77	Q76	Q75	Q74
R/W		RD							
Default		Not initialized							

Optional Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
4AH	Optional Control	0	0	0	0	0	0	CTX	0
R/W		RD	RD	RD	RD	RD	RD	R/W	RD
Default		0	0	0	0	0	0	0	0

CTX: Setting of channel status information for AES3 mode
0: Channel status information on DAUX is sent from TX (Default)
1: Channel status information in control registers (CTX191-0 bits) is sent from TX.

■ Burst Preambles in non-PCM Bitstreams

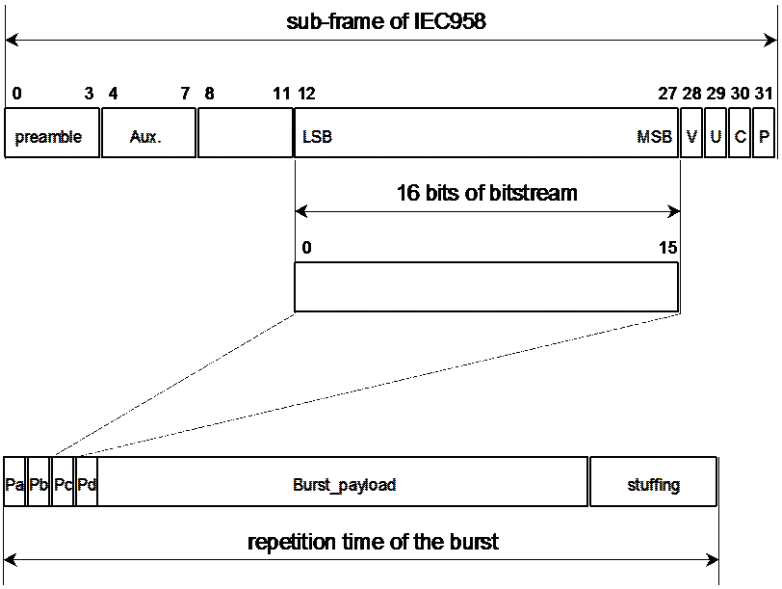


Figure 50. Data structure in IEC60958

Preamble word	Length of field	Contents	Value
Pa	16 bits	sync word 1	0xF872
Pb	16 bits	sync word 2	0x4E1F
Pc	16 bits	Burst info	see Table 33
Pd	16 bits	Length code	numbers of bits

Table 32. Burst preamble words

Bits of Pc	Value	Contents	Repetition time of burst in IEC60958 frames
0-4		data type	
	0	NULL data	≤4096
	1	Dolby AC-3 data	1536
	2	reserved	
	3	PAUSE	
	4	MPEG-1 Layer1 data	384
	5	MPEG-1 Layer2 or 3 data or MPEG-2 without extension	1152
	6	MPEG-2 data with extension	1152
	7	MPEG-2 AAC ADTS	1024
	8	MPEG-2, Layer1 Low sample rate	384
	9	MPEG-2, Layer2 or 3 Low sample rate	1152
	10	reserved	
	11	DTS type I	512
	12	DTS type II	1024
	13	DTS type III	2048
	14	ATRAC	512
	15	ATRAC2/3	1024
	16-31	reserved	
5, 6	0	reserved, shall be set to “0”	
7	0	error-flag indicating a valid burst_payload	
	1	error-flag indicating that the burst_payload may contain errors	
8-12		data type dependent info	
13-15	0	bit stream number, shall be set to “0”	

Table 33. Fields of burst info Pc

■ Non-PCM Bitstream timing

1) When Non-PCM preamble is not coming within 4096 frames,

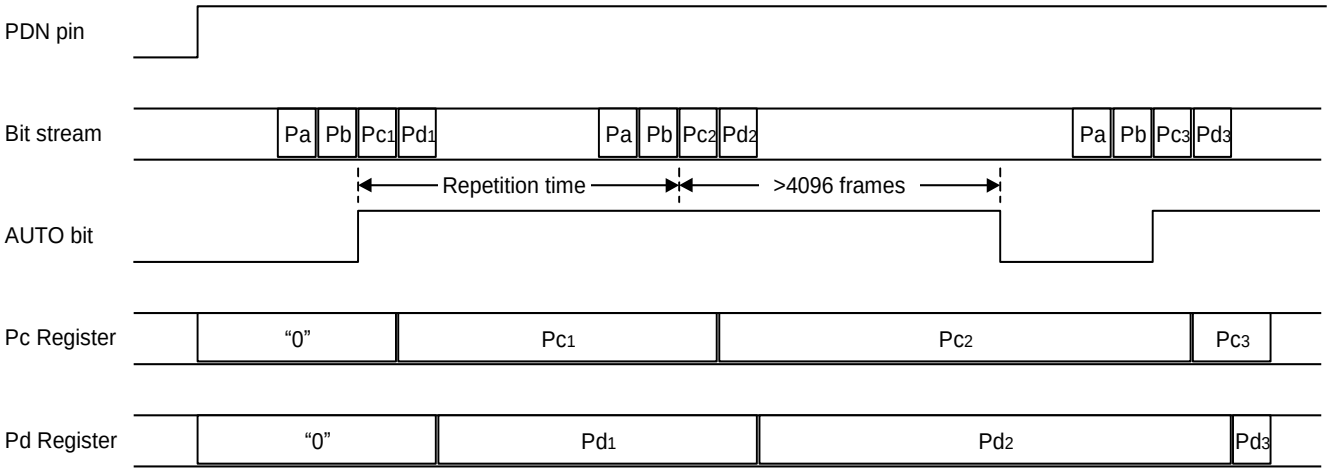


Figure 51. Timing example 1

2) When Non-PCM bitstream stops (when MULK0=0),

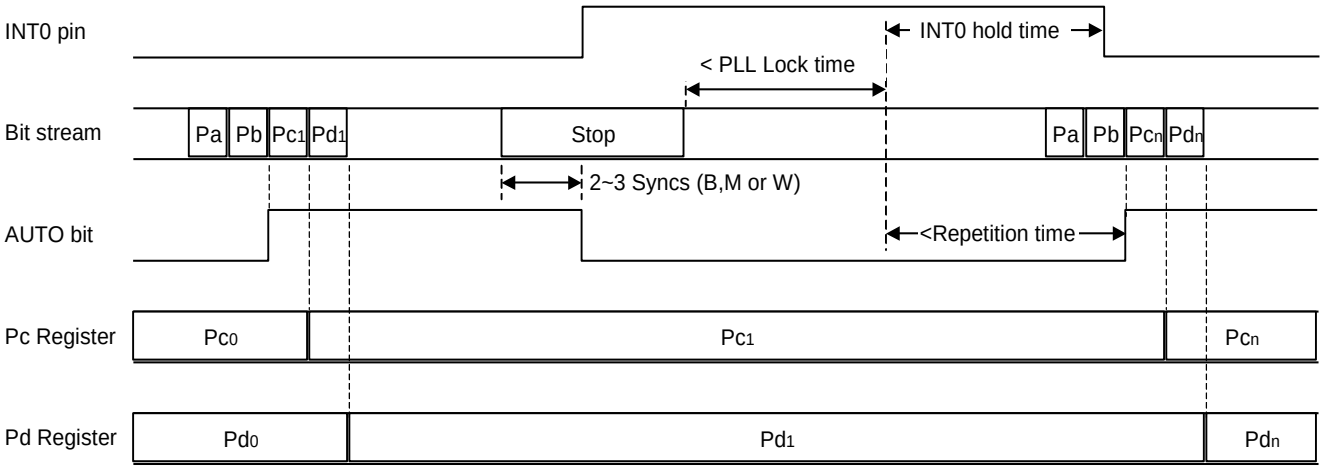


Figure 52. Timing example 2

SYSTEM DESIGN

Figure 53 shows the example of system connection diagram for 4-wire serial mode.

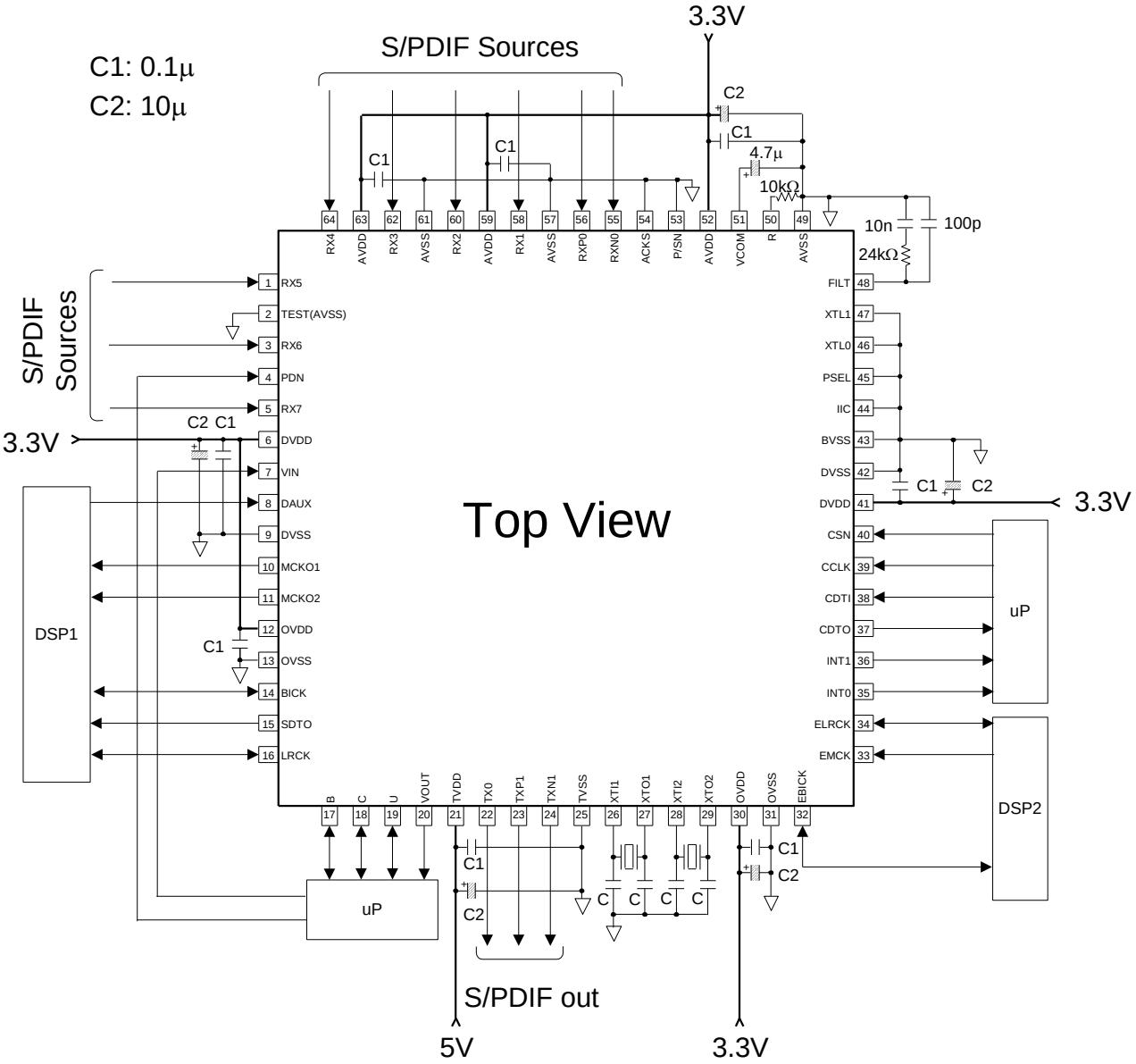


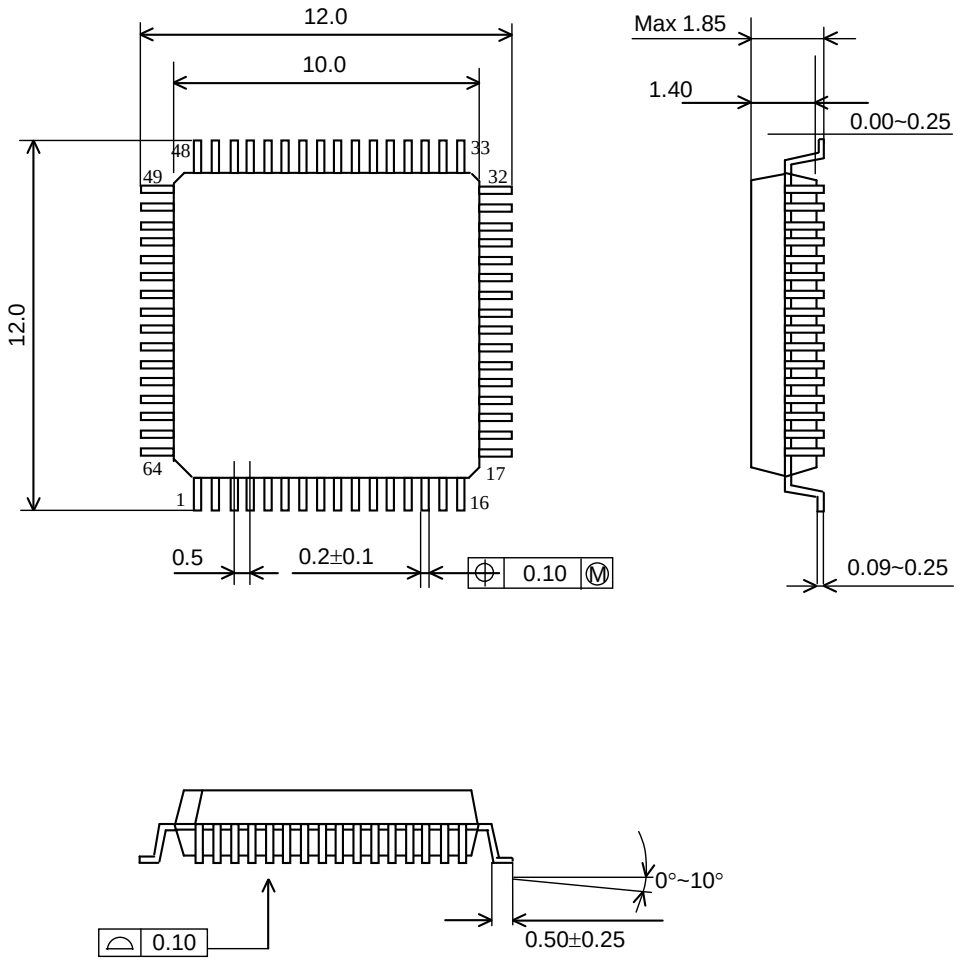
Figure 53. Typical Connection Diagram (4-wire serial mode)

Notes:

- For setting of XTL0 and XTL1, refer the Table 13.
- "C" depends on the crystal.
- AVSS, BVSS, TVSS, OVSS and DVSS must be connected the same ground plane.
- Digital signals, especially clocks, should be kept away from the R and FILT pins in order to avoid an effect to the clock jitter performance.

PACKAGE

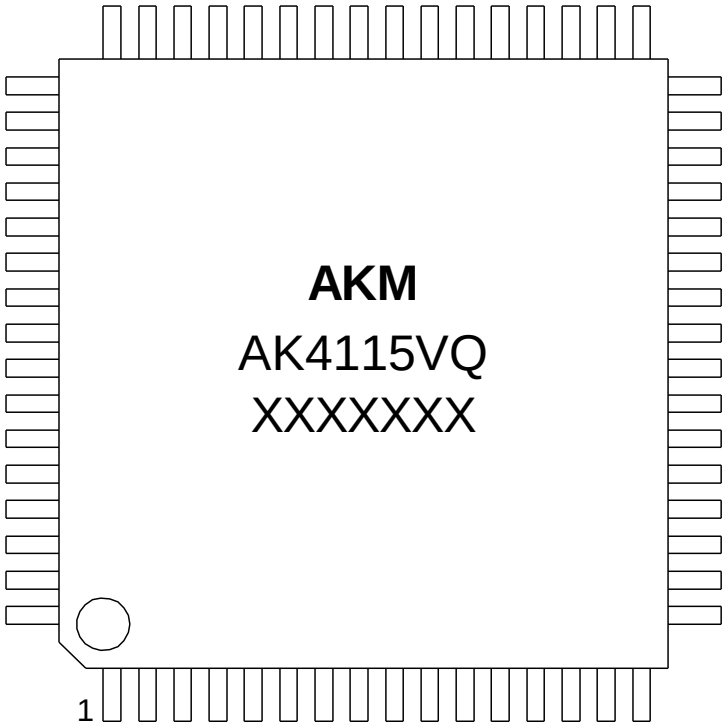
64pin LQFP(Unit: mm)



■ Material & Lead finish

Package molding compound: Epoxy
Lead frame material: Cu
Lead frame surface treatment: Solder (Pb free) plate

MARKING



XXXXXXX: Date code identifier

REVISION HISTORY

Date (Y/M/D)	Revision	Reason	Page	Contents
06/12/13	00	First Edition		
10/09/28	01	Error Correction	7	■ Handling of Unused Pin 1. Serial Mode (P/SN pin = "L") The condition of CDTO pin was added. 2. Parallel Mode (P/SN pin = "H") The CDTO pin was deleted.
			56	0AH, D5: MCK1E → MCK2E
		Specification Change	62	PACKAGE The package dimensions were changed.
18/09/12	02	Description Change	20	Descriptions were added on Table 6.
		Description Addition	49,50	Descriptions were added. BCU bit and BCU_IO bit
		Description Change	54	AUTO bit 0: PCM Detected 1: Non-PCM/DTSCD Detected
		Error Correction	56	R/W attribute of MSEL and ECKS1 bits were changed. RD → R/W

IMPORTANT NOTICE

0. Asahi Kasei Microdevices Corporation ("AKM") reserves the right to make changes to the information contained in this document without notice. When you consider any use or application of AKM product stipulated in this document ("Product"), please make inquiries the sales office of AKM or authorized distributors as to current status of the Products.
1. All information included in this document are provided only to illustrate the operation and application examples of AKM Products. AKM neither makes warranties or representations with respect to the accuracy or completeness of the information contained in this document nor grants any license to any intellectual property rights or any other rights of AKM or any third party with respect to the information in this document. You are fully responsible for use of such information contained in this document in your product design or applications. AKM ASSUMES NO LIABILITY FOR ANY LOSSES INCURRED BY YOU OR THIRD PARTIES ARISING FROM THE USE OF SUCH INFORMATION IN YOUR PRODUCT DESIGN OR APPLICATIONS.
2. The Product is neither intended nor warranted for use in equipment or systems that require extraordinarily high levels of quality and/or reliability and/or a malfunction or failure of which may cause loss of human life, bodily injury, serious property damage or serious public impact, including but not limited to, equipment used in nuclear facilities, equipment used in the aerospace industry, medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, devices related to electric power, and equipment used in finance-related fields. Do not use Product for the above use unless specifically agreed by AKM in writing.
3. Though AKM works continually to improve the Product's quality and reliability, you are responsible for complying with safety standards and for providing adequate designs and safeguards for your hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of the Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption.
4. Do not use or otherwise make available the Product or related technology or any information contained in this document for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). When exporting the Products or related technology or any information contained in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. The Products and related technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
5. Please contact AKM sales representative for details as to environmental matters such as the RoHS compatibility of the Product. Please use the Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. AKM assumes no liability for damages or losses occurring as a result of noncompliance with applicable laws and regulations.
6. Resale of the Product with provisions different from the statement and/or technical features set forth in this document shall immediately void any warranty granted by AKM for the Product and shall not create or extend in any manner whatsoever, any liability of AKM.
7. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of AKM.