ADC32RF8x Dual-Channel, 3-GSPS Telecom Receiver and Feedback Devices

1 Features

- 14-Bit, Dual-Channel, 3-GSPS ADC
- Noise Floor: –155 dBFS/Hz
- RF Input Supports Up to 4.0 GHz
- Aperture Jitter: 90 f_S
- Channel Isolation: 95 dB at f_{IN} = 1.8 GHz
- Spectral Performance (f_{IN} = 900 MHz, –2 dBFS):
  - SNR: 60.1 dBFS
  - SFDR: 66-dBc HD2, HD3
  - SFDR: 76-dBc Worst Spur
- Spectral Performance (f_{IN} = 1.85 GHz, –2 dBFS):
  - SNR: 58.9 dBFS
  - SFDR: 67-dBc HD2, HD3
  - SFDR: 76-dBc Worst Spur
- On-Chip Digital Down-Converters:
  - Up to 4 DDCs (Dual-Band Mode)
  - Up to 3 Independent NCOs per DDC
- On-Chip Input Clamp for Overvoltage Protection
- Programmable On-Chip Power Detectors with Alarm Pins for AGC Support
- On-Chip Dither
- On-Chip Input Termination
- Input Full-Scale: 1.35 V_{PP}
- Support for Multi-Chip Synchronization
- JESD204B Interface:
  - Subclass 1-Based Deterministic Latency
  - 4 Lanes Per Channel at 12.5 Gbps
- Power Dissipation: 3.2 W/Ch at 3.0 GSPS
- 72-Pin VQFN Package (10 mm × 10 mm)

2 Applications

- Multi-Carrier GSM Cellular Infrastructure Base Stations
- Telecommunications Receivers
- DPD Observation Receivers
- Backhaul Receivers
- RF Repeaters and Distributed Antenna Systems

3 Description

The ADC32RF8x (ADC32RF80 and ADC32RF83) is a 14-bit, 3-GSPS, dual-channel telecom receiver and feedback device family that supports RF sampling with input frequencies up to 4 GHz and beyond. Designed for high signal-to-noise ratio (SNR), the ADC32RF8x family delivers a noise spectral density of –155 dBFS/Hz as well as dynamic range and channel isolation over a large input frequency range. The buffered analog input with on-chip termination provides uniform input impedance across a wide frequency range and minimizes sample-and-hold glitch energy.

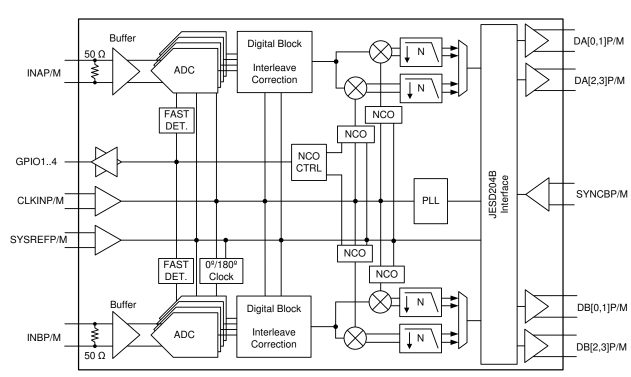
Each channel can be connected to a dual-band, digital down-converter (DDC) with up to three independent, 16-bit numerically-controlled oscillators (NCOs) per DDC for phase-coherent frequency hopping. Additionally, the ADC is equipped with front-end peak and RMS power detectors and alarm functions to support external automatic gain control (AGC) algorithms.

The ADC32RF8x supports the JESD204B serial interface with subclass 1-based deterministic latency using data rates up to 12.5 Gbps with up to four lanes per ADC. The device is offered in a 72-pin VQFN package (10 mm × 10 mm) and supports the industrial temperature range (–40°C to +85°C).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADC32RF8x	VQFN (72)	10.00 mm × 10.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Block Diagram

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4 Revision History

Changes from Revision A (December 2016) to Revision B (January 2018)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added RHH package option	1
• Changed *sync* to *SYSREF* in SYSREFM and SYSREFP pin description in *Pin Functions* table	3
• Changed *OUTSEL GPIO1* to *OUTSEL GPIO4* in register 032h, Power Detector Page	71
• Changed *OUTSEL GPIO2* to *OUTSEL GPIO1* in register 033h, Power Detector Page	71
• Changed *OUTSEL GPIO4* to *OUTSEL GPIO2* in register 035h, Power Detector Page	71
• Changed bits 3 to 0 in register 037h, Power Detector Page	71

Changes from Revision * (May 2016) to Revision A (December 2016)	Page
• Released to production	1

5 Pin Configuration and Functions

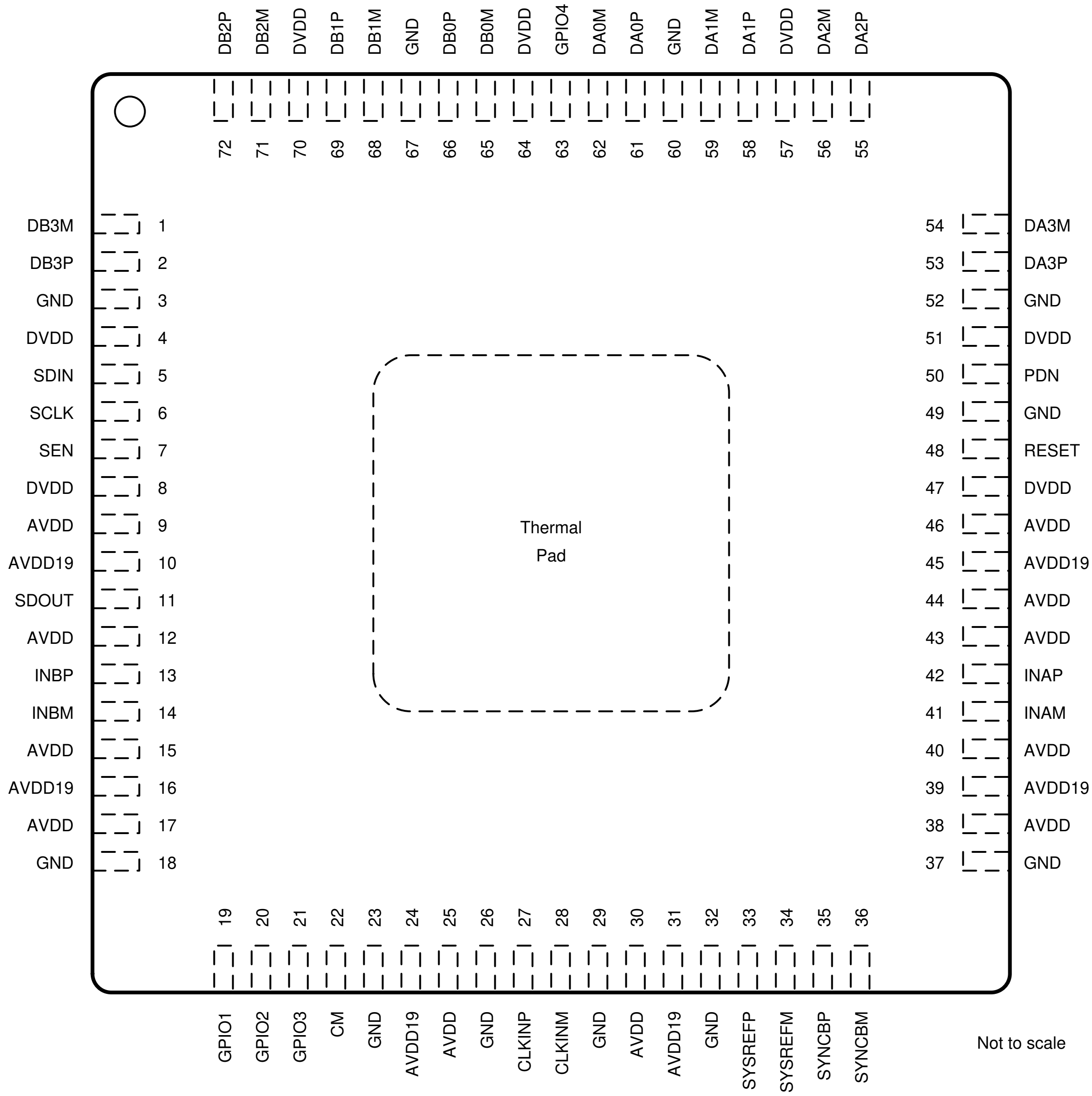


Figure 5-1. RMP or RHH Package 72-Pin VQFN Top View

Table 5-1. Pin Functions

NAME	NO.	I/O	DESCRIPTION
INPUT, REFERENCE			
INAM	41	I	Differential analog input for channel A
INAP	42		
INBM	14	I	Differential analog input for channel B
INBP	13		
CM	22	O	Common-mode voltage for analog inputs, 1.2 V

Table 5-1. Pin Functions (continued)

NAME	NO.	I/O	DESCRIPTION
CLOCK, SYNC			
CLKINM	28	I	Differential clock input for the analog-to-digital converter (ADC). This pin has an internal differential 100-Ω termination.
CLKINP	27		
SYSREFM	34	I	External SYSREF input. This pin has an internal, differential 100-Ω termination and requires external biasing.
SYSREFP	33		
GPIO1	19	I/O	GPIO control pin; configured through the SPI. This pin can be configured to be either a fast overrange output for channel A and B, a fast detect alarm signal from the peak power detect, or a numerically-controlled oscillator (NCO) control. GPIO 4 (pin 63) can also be configured as a single-ended SYNCB input.
GPIO2	20		
GPIO3	21		
GPIO4	63		
CONTROL, SERIAL			
RESET	48	I	Hardware reset; active high. This pin has an internal 20-kΩ pulldown resistor.
SCLK	6	I	Serial interface clock input. This pin has an internal 20-kΩ pulldown resistor.
SDIN	5	I/O	Serial interface data input. This pin has an internal 20-kΩ pulldown resistor. SDIN can be data input in 4-wire mode, data input and output in 3 wire-mode.
SEN	7	I	Serial interface enable. This pin has an internal 20-kΩ pullup resistor to DVDD.
SDOUT	11	O	Serial interface data output in 4-wire mode
PDN	50	I	Power down; active high. This pin can be configured through an SPI register setting and can be configured to a fast overrange output channel B through the SPI. This pin has an internal 20-kΩ pulldown resistor.
DATA INTERFACE			
DA0M	62	O	JESD204B serial data output for channel A
DA0P	61		
DA1M	59		
DA1P	58		
DA2M	56		
DA2P	55		
DA3M	54		
DA3P	53		
DB0M	65	O	JESD204B serial data output for channel B
DB0P	66		
DB1M	68		
DB1P	69		
DB2M	71		
DB2P	72		
DB3M	1		
DB3P	2		
SYNCBM	36	I	Synchronization input for the JESD204B port. This pin has an LVDS or 1.8-V logic input, an optional on-chip 100-Ω termination, and is selectable through the SPI. This pin requires external biasing.
SYNCBP	35		
POWER SUPPLY			
AVDD19	10, 16, 24, 31, 39, 45	I	Analog 1.9-V power supply
AVDD	9, 12, 15, 17, 25, 30, 38, 40, 43, 44, 46	I	Analog 1.15-V power supply
DVDD	4, 8, 47, 51, 57, 64, 70	I	Digital 1.15 V-power supply, including the JESD204B transmitter
GND	3, 18, 23, 26, 29, 32, 37, 49, 52, 60, 67	I	Ground; shorted to thermal pad inside device

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply voltage range	AVDD19	–0.3	2.1	V
	AVDD	–0.3	1.4	
	DVDD	–0.3	1.4	
Voltage applied to input pins	INAP, INAM and INBP, INBM	–0.3	AVDD19 + 0.3	V
	CLKINP, CLKINM	–0.3	AVDD + 0.6	
	SYSREFP, SYSREFM, SYNCBP, SYNCBM	–0.3	AVDD + 0.6	
	SCLK, SEN, SDIN, RESET, PDN, GPIO1, GPIO2, GPIO3, GPIO4	–0.2	AVDD19 + 0.2	
Voltage applied to output pins		–0.3	2.2	V
Temperature	Operating free-air, T_A	–40	85	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Section 6.1* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Section 6.3*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage[2]	AVDD19	1.8	1.9	2.0	V
	AVDD	1.1	1.15	1.25	
	DVDD	1.1	1.15	1.2	
Temperature	Operating free-air, T_A	–40		85	°C
	Operating junction, T_J		105[1]	125	

(1) Prolonged use above this junction temperature may increase the device failure-in-time (FIT) rate.
(2) Always power up the DVDD supply (1.15 V) before the AVDD19 (1.9 V) supply. The AVDD (1.15 V) supply can come up in any order.

6.4 Thermal Information

THERMAL METRIC[1]		ADC32RF80		UNIT
		RMP (VQFN)	RHH (VQFN)	
		72 PINS	72 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	21.8	17.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	4.4	4.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	2.0	4.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.1	0.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	2.0	3.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.2	0.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C; and chip sampling rate = 2949.12 MSPS, 50% clock duty cycle, DDC-bypassed performance, AVDD19 = 1.9 V, AVDD = 1.15 V, DVDD = 1.15 V, –2-dBFS differential input, and 0-dB digital gain (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER CONSUMPTION[4] (Dual-Channel Operation, Both Channels A and B are Active; Divide-by-4, Complex Output Mode[3])						
I_{AVDD19}	1.9-V analog supply current	f_S = 2949.12 MSPS		1777	1989	mA
I_{AVDD}	1.15-V analog supply current	f_S = 2949.12 MSPS		970	1103	mA
I_{DVDD}	1.15-V digital supply current	f_S = 2949.12 MSPS		1785	1955	mA
P_D	Power dissipation	f_S = 2949.12 MSPS		6.54	7.07	W
	Global power-down power dissipation			360		mW
ANALOG INPUTS						
	Resolution			14		Bits
	Differential input full-scale			1.35		V_{PP}
V_{IC}	Input common-mode voltage			1.2[5]		V
R_{IN}	Input resistance	Differential resistance at dc		65		Ω
C_{IN}	Input capacitance	Differential capacitance at dc		2		pF
	V_{CM} common-mode voltage output			1.2		V
	Analog input bandwidth (–3-dB point)	ADC driven with 50-Ω source		3200		MHz
ISOLATION						
	Crosstalk isolation between channel A and channel B[1]	f_{IN} = 100 MHz		100		dBc
		f_{IN} = 900 MHz		99		
		f_{IN} = 1800 MHz		95		
		f_{IN} = 2700 MHz		86		
		f_{IN} = 3500 MHz		85		
CLOCK INPUT[2]						
	Input clock frequency		1.5	3		GSPS
	Differential (peak-to-peak) input clock amplitude		0.5	1.5	2.5	V_{PP}
	Input clock duty cycle		45%	50%	55%	
	Internal clock biasing			1.0		V
	Internal clock termination (differential)			100		Ω

(1) Crosstalk is measured with a –2-dBFS input signal on aggressor channel and no input on the victim channel.
(2) See Figure 7-1.
(3) Full-scale signal is applied to the analog inputs of all active channels.
(4) See the *Section 9.1.4* section for more details.
(5) When used in dc-coupling mode, the common-mode voltage at the analog inputs should be kept within V_{CM} ±25 mV for best performance.

6.6 AC Performance Characteristics: f_S = 2949.12 MSPS

typical values specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C; and chip sampling rate = 2949.12 MSPS, 50% clock duty cycle, DDC-bypassed performance(5), AVDD19 = 1.9 V, AVDD = 1.15 V, DVDD = 1.15 V, –2-dBFS differential input, and 0-dB digital gain (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN(3)	NOM	MAX	UNIT
SNR	Signal-to-noise ratio	f_{IN} = 100 MHz, A_{OUT} = –2 dBFS		62.6		dBFS
		f_{IN} = 900 MHz, A_{OUT} = –2 dBFS		61.1		
		f_{IN} = 1850 MHz, A_{OUT} = –2 dBFS	55.4	58.9		
		f_{IN} = 2100 MHz, A_{OUT} = –2 dBFS		58.2		
		f_{IN} = 2600 MHz, A_{OUT} = –2 dBFS		56.8		
		f_{IN} = 3500 MHz, A_{OUT} (2) = –3 dBFS with 2-dB gain		54.1		
NSD	Noise spectral density averaged across the Nyquist zone	f_{IN} = 100 MHz, A_{OUT} = –2 dBFS		154.3		dBFS/Hz
		f_{IN} = 900 MHz, A_{OUT} = –2 dBFS		152.8		
		f_{IN} = 1850 MHz, A_{OUT} = –2 dBFS	147.1	150.6		
		f_{IN} = 2100 MHz, A_{OUT} = –2 dBFS		149.9		
		f_{IN} = 2600 MHz, A_{OUT} = –2 dBFS		148.5		
		f_{IN} = 3500 MHz, A_{OUT} (2) = –3 dBFS with 2-dB gain		145.8		
	Small-signal SNR	f_{IN} = 1850 MHz, A_{OUT} = –40 dBFS		63.1		dBFS
NF(1)	Noise figure	f_{IN} = 1850 MHz, A_{OUT} = –40 dBFS		24.7		dB
SINAD	Signal-to-noise and distortion ratio	f_{IN} = 100 MHz, A_{OUT} = –2 dBFS		61.7		dBFS
		f_{IN} = 900 MHz, A_{OUT} = –2 dBFS		60.2		
		f_{IN} = 1850 MHz, A_{OUT} = –2 dBFS		58.4		
		f_{IN} = 2100 MHz, A_{OUT} = –2 dBFS		57.6		
		f_{IN} = 2600 MHz, A_{OUT} = –2 dBFS		54.8		
		f_{IN} = 3500 MHz, A_{OUT} (2) = –3 dBFS with 2-dB gain		53.6		
ENOB	Effective number of bits	f_{IN} = 100 MHz, A_{OUT} = –2 dBFS		10.0		Bits
		f_{IN} = 900 MHz, A_{OUT} = –2 dBFS		9.7		
		f_{IN} = 1850 MHz, A_{OUT} = –2 dBFS		9.4		
		f_{IN} = 2100 MHz, A_{OUT} = –2 dBFS		9.3		
		f_{IN} = 2600 MHz, A_{OUT} = –2 dBFS		8.8		
		f_{IN} = 3500 MHz, A_{OUT} (2) = –3 dBFS with 2-dB gain		8.6		
SFDR	Spurious-free dynamic range	f_{IN} = 100 MHz, A_{OUT} = –2 dBFS		68.0		dBc
		f_{IN} = 900 MHz, A_{OUT} = –2 dBFS		66.0		
		f_{IN} = 1850 MHz, A_{OUT} = –2 dBFS	58	67.0		
		f_{IN} = 2100 MHz, A_{OUT} = –2 dBFS		64.0		
		f_{IN} = 2600 MHz, A_{OUT} = –2 dBFS		58.0		
		f_{IN} = 3500 MHz, A_{OUT} (2) = –3 dBFS with 2-dB gain		62.0		
HD2(4)	Second-order harmonic distortion	f_{IN} = 100 MHz, A_{OUT} = –2 dBFS		72.0		dBc
		f_{IN} = 900 MHz, A_{OUT} = –2 dBFS		73.0		
		f_{IN} = 1850 MHz, A_{OUT} = –2 dBFS	58	67.0		
		f_{IN} = 2100 MHz, A_{OUT} = –2 dBFS		64.0		
		f_{IN} = 2700 MHz, A_{OUT} = –2 dBFS		58.0		
		f_{IN} = 3500 MHz, A_{OUT} (2) = –3 dBFS with 2-dB gain		62.0		

typical values specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C; and chip sampling rate = 2949.12 MSPS, 50% clock duty cycle, DDC-bypassed performance(5), AVDD19 = 1.9 V, AVDD = 1.15 V, DVDD = 1.15 V, –2-dBFS differential input, and 0-dB digital gain (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN(3)	NOM	MAX	UNIT
HD3	Third-order harmonic distortion	f_{IN} = 100 MHz, A_{OUT} = –2 dBFS		68.0		dBc
		f_{IN} = 900 MHz, A_{OUT} = –2 dBFS		66.0		
		f_{IN} = 1850 MHz, A_{OUT} = –2 dBFS	61	73.0		
		f_{IN} = 2100 MHz, A_{OUT} = –2 dBFS		80.0		
		f_{IN} = 2600 MHz, A_{OUT} = –2 dBFS		72.0		
		f_{IN} = 3500 MHz, A_{OUT} (2) = –3 dBFS with 2-dB gain		65.0		
HD4, HD5	Fourth- and fifth-order harmonic distortion	f_{IN} = 100 MHz, A_{OUT} = –2 dBFS		85.0		dBc
		f_{IN} = 900 MHz, A_{OUT} = –2 dBFS		81.0		
		f_{IN} = 1850 MHz, A_{OUT} = –2 dBFS	61	84.0		
		f_{IN} = 2100 MHz, A_{OUT} = –2 dBFS		84.0		
		f_{IN} = 2600 MHz, A_{OUT} = –2 dBFS		80.0		
		f_{IN} = 3500 MHz, A_{OUT} (2) = –3 dBFS with 2-dB gain		87.0		
IL spur	Interleaving spurs: f_S / 2 – f_{IN}, f_S / 4 ± f_{IN}	f_{IN} = 100 MHz, A_{OUT} = –2 dBFS		90.0		dBc
		f_{IN} = 900 MHz, A_{OUT} = –2 dBFS		77.0		
		f_{IN} = 1850 MHz, A_{OUT} = –2 dBFS	69	79.0		
		f_{IN} = 2100 MHz, A_{OUT} = –2 dBFS		76.0		
		f_{IN} = 2600 MHz, A_{OUT} = –2 dBFS		77.0		
		f_{IN} = 3500 MHz, A_{OUT} (2) = –3 dBFS with 2-dB gain		77.0		
HD2 IL	Interleaving spur for HD2: f_S / 2 – HD2	f_{IN} = 100 MHz, A_{OUT} = –2 dBFS		84.0		dBc
		f_{IN} = 900 MHz, A_{OUT} = –2 dBFS		82.0		
		f_{IN} = 1850 MHz, A_{OUT} = –2 dBFS	62	80.0		
		f_{IN} = 2100 MHz, A_{OUT} = –2 dBFS		76.0		
		f_{IN} = 2600 MHz, A_{OUT} = –2 dBFS		65.0		
		f_{IN} = 3500 MHz, A_{OUT} (2) = –3 dBFS with 2-dB gain		77.0		
Worst spur	Spurious-free dynamic range (excluding HD2, HD3, HD4, HD5, and interleaving spurs IL and HD2 IL)	f_{IN} = 100 MHz, A_{OUT} = –2 dBFS		80.0		dBc
		f_{IN} = 900 MHz, A_{OUT} = –2 dBFS		76.0		
		f_{IN} = 1850 MHz, A_{OUT} = –2 dBFS	64	76.0		
		f_{IN} = 2100 MHz, A_{OUT} = –2 dBFS		75.0		
		f_{IN} = 2600 MHz, A_{OUT} = –2 dBFS		75.0		
		f_{IN} = 3500 MHz, A_{OUT} (2) = –3 dBFS with 2-dB gain		71.0		
IMD3	Two-tone, third-order intermodulation distortion	f_{IN1} = 1770 MHz, f_{IN2} = 1790 MHz, A_{OUT} = –8 dBFS (each tone)		70		dBFS
		f_{IN1} = 1800 MHz, f_{IN2} = 2600 MHz, A_{OUT} = –8 dBFS (each tone)		73		
		f_{IN1} = 3490 MHz, f_{IN2} = 3510 MHz, A_{OUT} = –8 dBFS (each tone) with 2-dB gain		67		

(1) The ADC internal resistance = 65 Ω, the driving source resistance = 50 Ω.
(2) Output amplitude, A_{OUT}, refers to the signal amplitude in the ADC digital output that is same as the analog input amplitude, A_{IN}, except when the digital gain feature is used. If digital gain is G, then A_{OUT} = G + A_{IN}.
(3) Minimum values are specified at A_{OUT} = –3 dBFS.
(4) The minimum value of HD2 is specified by bench characterization.
(5) Performance is shown with DDC bypassed. When DDC is enabled, performance improves by the decimation filtering process.

6.7 AC Performance Characteristics: f_S = 2457.6 MSPS (Performance Optimized for F + A + D Band)

typical values specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C; and chip sampling rate = 2949.12 MSPS, 50% clock duty cycle, DDC-bypassed performance, AVDD19 = 1.9 V, AVDD = 1.15 V, DVDD = 1.15 V, –2-dBFS differential input, and 0-dB digital gain (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
SNR	Signal-to-noise ratio	f_{IN} = 1850 MHz, A_{OUT} = –2 dBFS		58.5		dBFS
		f_{IN} = 2600 MHz, A_{OUT} = –2 dBFS		55.8		
SFDR	Spurious-free dynamic range	f_{IN} = 1850 MHz, A_{OUT} = –2 dBFS		60.0		dBc
		f_{IN} = 2600 MHz, A_{OUT} = –2 dBFS		57.0		
HD2	Second-order harmonic distortion	f_{IN} = 1850 MHz, A_{OUT} = –2 dBFS		59.0		dBc
		f_{IN} = 2600 MHz, A_{OUT} = –2 dBFS		57.0		
HD3	Third-order harmonic distortion	f_{IN} = 1850 MHz, A_{OUT} = –2 dBFS		75.0		dBc
		f_{IN} = 2600 MHz, A_{OUT} = –2 dBFS		65.0		
IL spur	Interleaving spurs: f_S / 2 – f_{IN}, f_S / 4 ± f_{IN}	f_{IN} = 1850 MHz, A_{OUT} = –2 dBFS		84.0		dBc
		f_{IN} = 2600 MHz, A_{OUT} = –2 dBFS		76.0		
HD2 IL	Interleaving spur for HD2: f_S / 2 – HD2	f_{IN} = 1850 MHz, A_{OUT} = –2 dBFS		76.0		dBc
		f_{IN} = 2600 MHz, A_{OUT} = –2 dBFS		67.0		
IMD3	Two-tone, third-order intermodulation distortion	f_{IN1} = 1800 MHz, f_{IN2} = 2600 MHz, A_{OUT} = –8 dBFS (each tone)		67.0		dBFS

(1) F-band = 1880 MHz to 1920 MHz, A-band = 2010 MHz to 2025 MHz, and D-band = 2570 MHz to 2620 MHz.

6.8 AC Performance Characteristics: f_S = 2457.6 MSPS (Performance Optimized for F + A Band)

typical values specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C; and chip sampling rate = 2949.12 MSPS, 50% clock duty cycle, DDC-bypassed performance, AVDD19 = 1.9 V, AVDD = 1.15 V, DVDD = 1.15 V, –2-dBFS differential input, and 0-dB digital gain (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
SNR	Signal-to-noise ratio	f_{IN} = 1850 MHz, A_{OUT} = –2 dBFS		58.7		dBFS
		f_{IN} = 2100 MHz, A_{OUT} = –2 dBFS		57.9		
SFDR	Spurious-free dynamic range	f_{IN} = 1850 MHz, A_{OUT} = –2 dBFS		71.0		dBc
		f_{IN} = 2100 MHz, A_{OUT} = –2 dBFS		69.0		
HD2	Second-order harmonic distortion	f_{IN} = 1850 MHz, A_{OUT} = –2 dBFS		71.0		dBc
		f_{IN} = 2100 MHz, A_{OUT} = –2 dBFS		69.0		
HD3	Third-order harmonic distortion	f_{IN} = 1850 MHz, A_{OUT} = –2 dBFS		75.0		dBc
		f_{IN} = 2100 MHz, A_{OUT} = –2 dBFS		76.0		
IL spur	Interleaving spurs: f_S / 2 – f_{IN}, f_S / 4 ± f_{IN}	f_{IN} = 1850 MHz, A_{OUT} = –2 dBFS		82.0		dBc
		f_{IN} = 2100 MHz, A_{OUT} = –2 dBFS		84.0		
HD2 IL	Interleaving spur for HD2: f_S / 2 – HD2	f_{IN} = 1850 MHz, A_{OUT} = –2 dBFS		80.0		dBc
		f_{IN} = 2100 MHz, A_{OUT} = –2 dBFS		80.0		

(1) F-band = 1880 MHz to 1920 MHz, A-band = 2010 MHz to 2025 MHz, and D-band = 2570 MHz to 2620 MHz.

6.9 Digital Requirements

typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C; and chip sampling rate = 2949.12 MSPS, DDC bypassed performance, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = 1.15 V, DVDD = 1.15 V, –2-dBFS differential input, and 0-dB digital gain (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
DIGITAL INPUTS (RESET, SCLK, SEN, SDIN, PDN, GPIO1, GPIO2, GPIO3, GPIO4)						
V_{IH}	High-level input voltage		0.8			V
V_{IL}	Low-level input voltage				0.4	V
I_{IH}	High-level input current			50		µA
I_{IL}	Low-level input current			–50		µA
C_i	Input capacitance			4		pF
DIGITAL OUTPUTS (SDOUT, GPIO1, GPIO2, GPIO3, GPIO4)						
V_{OH}	High-level output voltage		AVDD19–0.1	AVDD19		V
V_{OL}	Low-level output voltage				0.1	V
DIGITAL INPUTS (SYSREFP and SYSREFM; SYNCBP and SYNCBM; Requires External Biasing)						
V_{ID}	Differential input voltage		350	450	800	mV_{PP}
V_{CM}	Input common-mode voltage		1.05	1.2	1.325	V
DIGITAL OUTPUTS (JESD204B Interface: DA[3:0], DB[3:0], Meets JESD204B LV-0IF-11G-SR Standard)						
$\lvert V_{OD} \rvert$	Output differential voltage			700		mV_{PP}
$\lvert V_{OCM} \rvert$	Output common-mode voltage			450		mV
	Transmitter short-circuit current	Transmitter pins shorted to any voltage between –0.25 V and 1.45 V	–100		100	mA
z_{os}	Single-ended output impedance			50		Ω
C_o	Output capacitance	Output capacitance inside the device, from either output to ground		2		pF

6.10 Timing Requirements

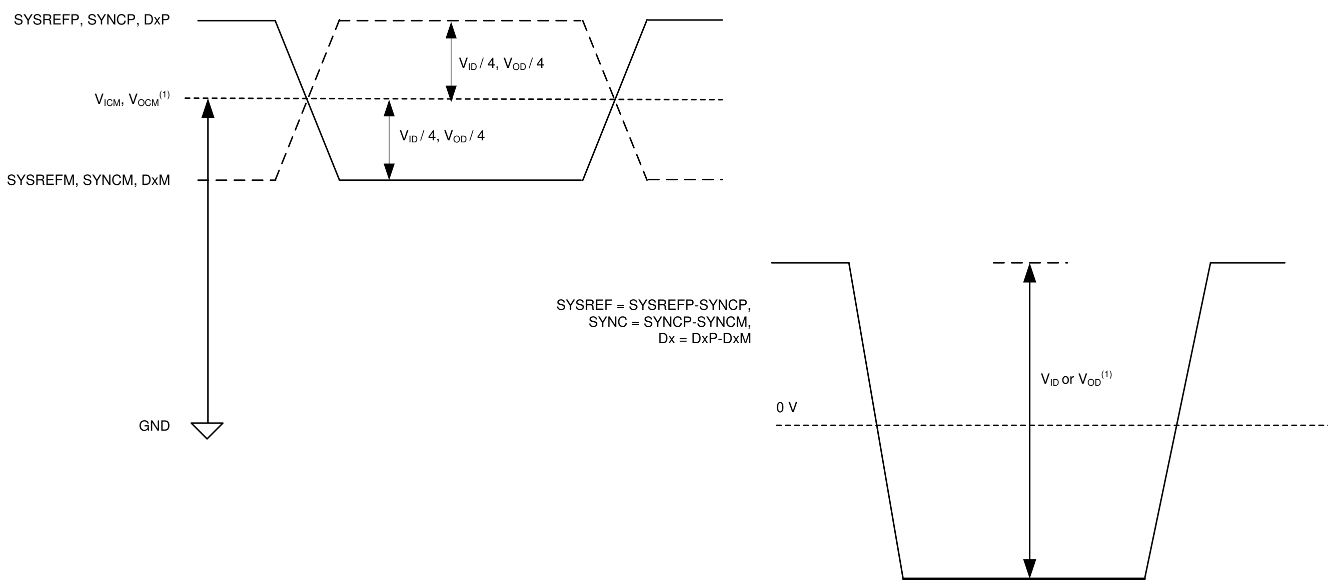
typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C; and chip sampling rate = 2949.12 MSPS, 50% clock duty cycle, DDC-bypassed performance, AVDD19 = 1.9 V, AVDD = 1.15 V, DVDD = 1.15 V, –2-dBFS differential input, and 0-dB digital gain (unless otherwise noted)

		MIN	NOM	MAX	UNIT
SAMPLE TIMING					
	Aperture delay	250		750	ps
	Aperture delay matching between two channels on the same device		±15		ps
	Aperture delay matching between two devices at the same temperature and supply voltage		±150		ps
	Aperture jitter, clock amplitude = 2 V_{PP}		90		f_S
Latency (1) (3)	Data latency, ADC sample to digital output, DDC block bypassed(4), LMFS = 8224		424		Input clock cycles
	Fast overrange latency, ADC sample to FOVR indication on GPIO pins		70		
t_{PD}	Propagation delay time: logic gates and output buffer delay (does not change with f_S)		6		ns
SYSREF TIMING(2)					
t_{SU_SYSREF}	SYSREF setup time: referenced to clock rising edge, 2949.12 MSPS	140	70		ps
t_{H_SYSREF}	SYSREF hold time: referenced to clock rising edge, 2949.12 MSPS	50	20		ps
	Valid transition window sampling period: $t_{SU\_SYSREF} – t_{H\_SYSREF}$, 2949.12 MSPS	143			ps

typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C; and chip sampling rate = 2949.12 MSPS, 50% clock duty cycle, DDC-bypassed performance, AVDD19 = 1.9 V, AVDD = 1.15 V, DVDD = 1.15 V, –2-dBFS differential input, and 0-dB digital gain (unless otherwise noted)

		MIN	NOM	MAX	UNIT
JESD OUTPUT INTERFACE TIMING					
UI	Unit interval: 12.5 Gbps	80	100	400	ps
	Serial output data rate	2.5	10.0	12.5	Gbps
	Rise, fall times: 1-pF, single-ended load capacitance to ground		60		ps
	Total jitter: BER of 1E-15 and lane rate = 12.5 Gbps		25		%UI
	Random jitter: BER of 1E-15 and lane rate = 12.5 Gbps		0.99		%UI, rms
	Deterministic jitter: BER of 1E-15 and lane rate = 12.5 Gbps		9.1		%UI, pk-pk

(1) Overall latency = latency + t_{PD}.
(2) Common-mode voltage for the SYSREF input is kept at 1.2 V.
(3) Latency increases when the DDC modes are used; see Table 8-5.
(4) For latency in different DDC options, see Table 8-5.



A. V_{OCM} is not the same as V_{ICM}. Similarly, V_{OD} is not the same as V_{ID}.

Figure 6-1. Logic Levels for Digital Inputs and Outputs

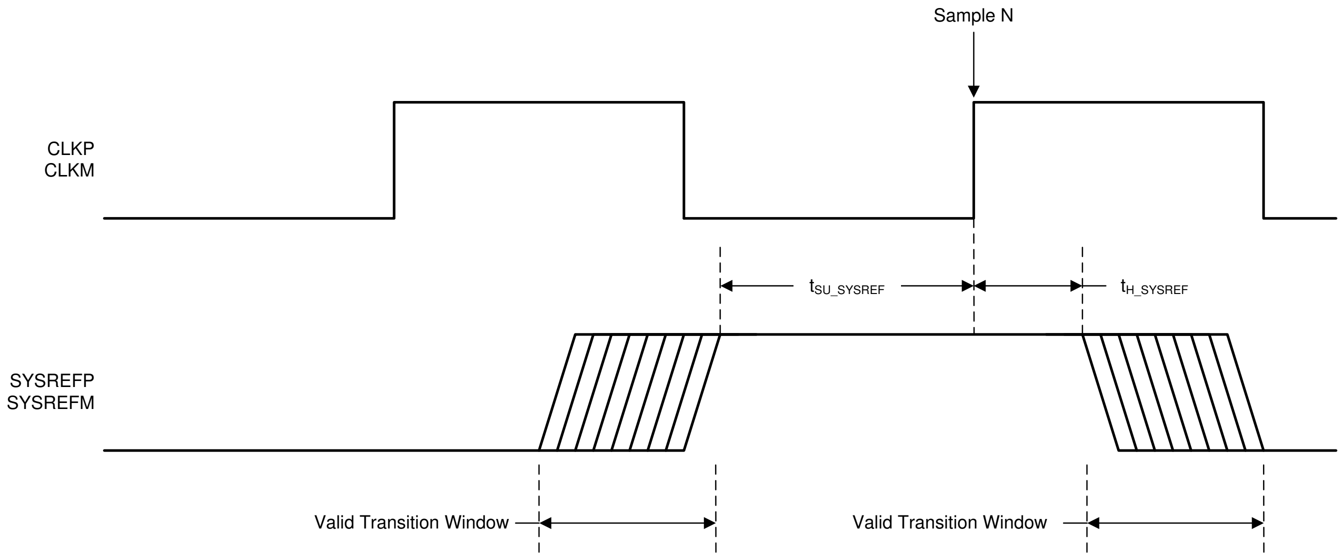
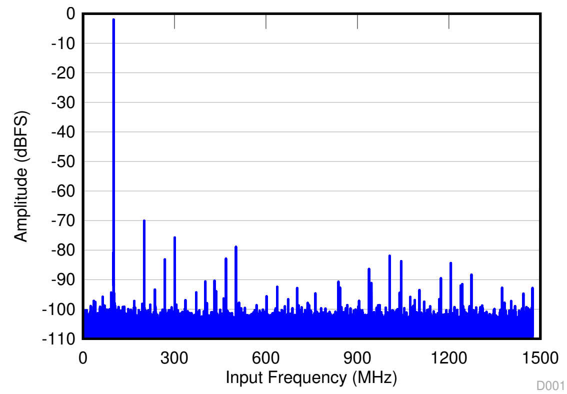


Figure 6-2. SYSREF Timing Diagram

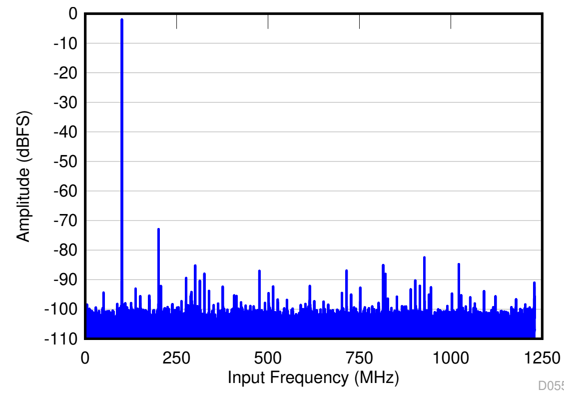
6.11 Typical Characteristics

typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C; and ADC sampling rate = 2949.12 MSPS, DDC bypassed performance, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –2-dBFS differential input, and 0-dB digital gain (unless otherwise noted)



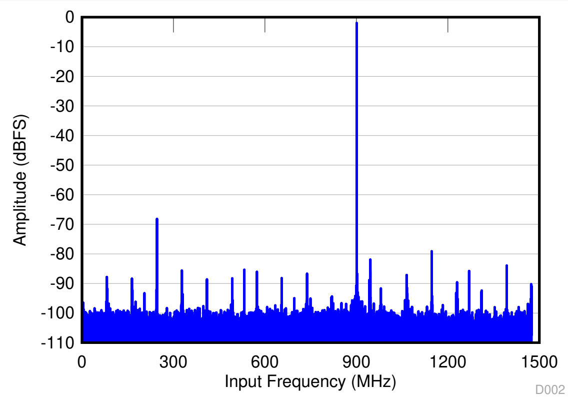
SNR = 62.2 dBFS; SFDR = 68 dBc; HD2 = –68 dBc; HD3 = –73 dBc; non HD2, HD3 = 77 dBc; IL spur = 86 dBc; f_{IN} = 100 MHz

Figure 6-3. FFT for 100-MHz Input Frequency



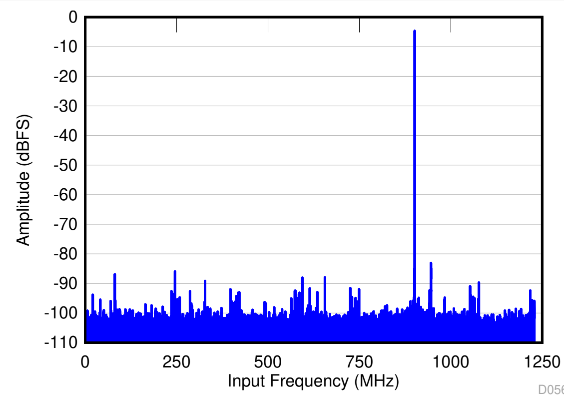
SNR = 62.4 dBFS; SFDR = 71 dBc; HD2 = –71 dBc; HD3 = –83 dBc; non HD2, HD3 = 82 dBc; IL spur = 80 dBc; f_{IN} = 100 MHz

Figure 6-4. FFT for 100-MHz Input Signal (f_S = 2457.6 MSPS)



SNR = 61.2 dBFS; SFDR = 66 dBc; HD2 = –77 dBc; HD3 = –66 dBc; non HD2, HD3 = 80 dBc; IL spur = 83 dBc; f_{IN} = 900 MHz

Figure 6-5. FFT for 900-MHz Input Signal

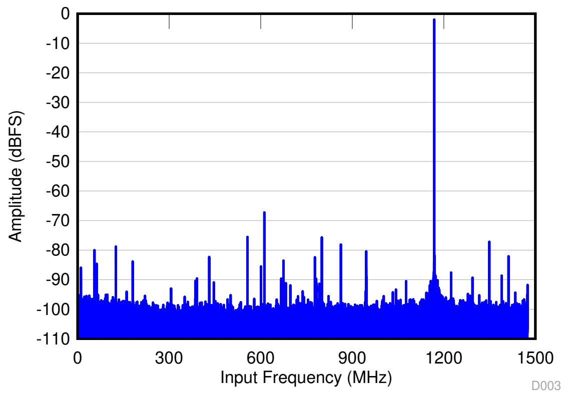


SNR = 62.1 dBFS; SFDR = 76 dBc; HD2 = –76 dBc; HD3 = –83 dBc; non HD2, HD3 = 82 dBc; IL spur = 83 dBc; f_{IN} = 900 MHz

Figure 6-6. FFT for 900-MHz Input Signal (f_S = 2457.6 MSPS)

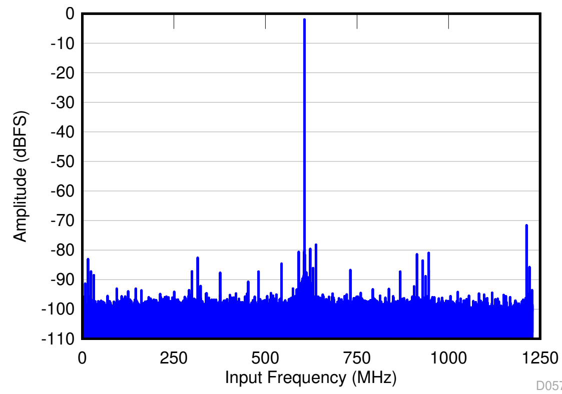
6.11 Typical Characteristics (continued)

typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C; and ADC sampling rate = 2949.12 MSPS, DDC bypassed performance, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –2-dBFS differential input, and 0-dB digital gain (unless otherwise noted)



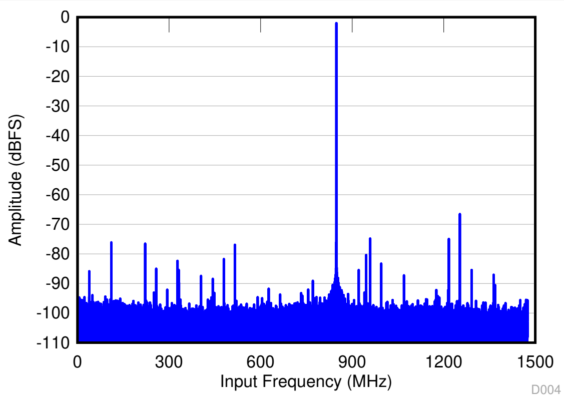
SNR = 59.1 dBFS; SFDR = 65 dBc; HD2 = –65 dBc; HD3 = –73 dBc; non HD2, HD3 = 73 dBc; IL spur = 76 dBc; f_{IN} = 1.7 GHz

Figure 6-7. FFT for 1780-MHz Input Signal



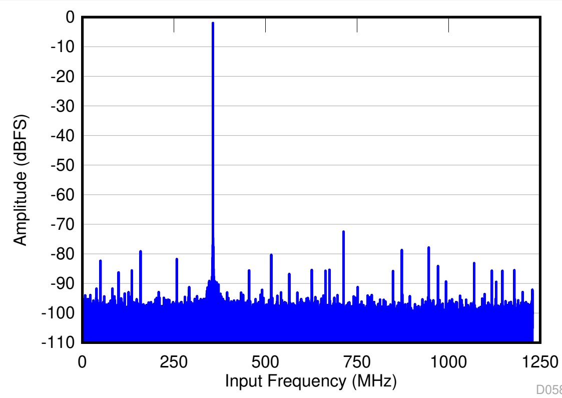
SNR = 58 dBFS; SFDR = 69 dBc; HD2 = –69 dBc; HD3 = –75 dBc; non HD2, HD3 = 74 dBc; IL spur = 78 dBc; f_{IN} = 1.85 GHz

Figure 6-8. FFT for 1850-MHz Input Signal (f_S = 2457.6 MSPS)



SNR = 58.2 dBFS; SFDR = 64 dBc; HD2 = –64 dBc; HD3 = –85 dBc; non HD2, HD3 = 73 dBc; IL spur = 74 dBc; f_{IN} = 2.1 GHz

Figure 6-9. FFT for 2100-MHz Input Signal

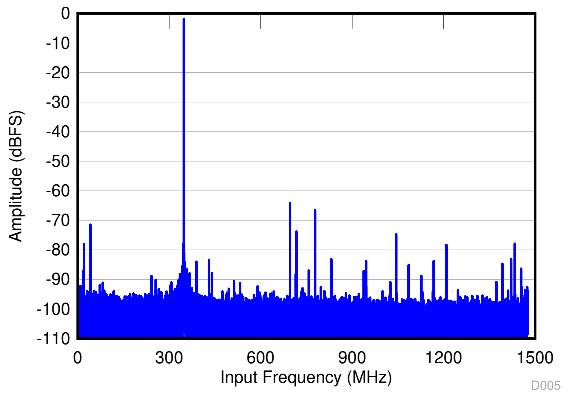


SNR = 57.5 dBFS; SFDR = 70 dBc; HD2 = –70 dBc; HD3 = –81 dBc; non HD2, HD3 = 75 dBc; IL spur = 77 dBc; f_{IN} = 2.1 GHz

Figure 6-10. FFT for 2100-MHz Input Signal (f_S = 2457.6 MSPS)

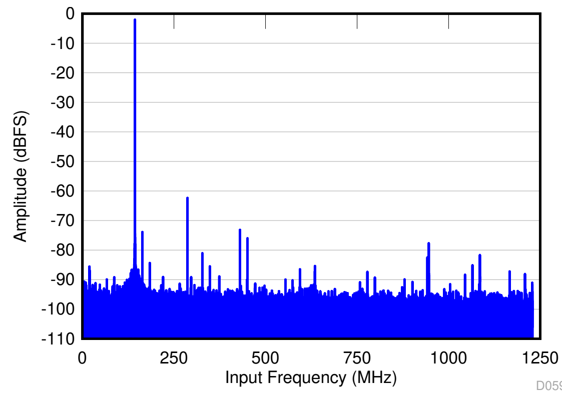
6.11 Typical Characteristics (continued)

typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C; and ADC sampling rate = 2949.12 MSPS, DDC bypassed performance, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –2-dBFS differential input, and 0-dB digital gain (unless otherwise noted)



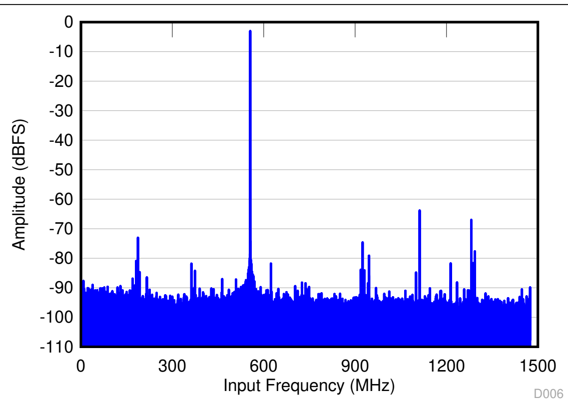
SNR = 56.9 dBFS; SFDR = 62 dBc; HD2 = –62 dBc; HD3 = –72 dBc; non HD2, HD3 = 72 dBc; IL spur = 64 dBc; f_{IN} = 2.6 GHz

Figure 6-11. FFT for 2600-MHz Input Signal



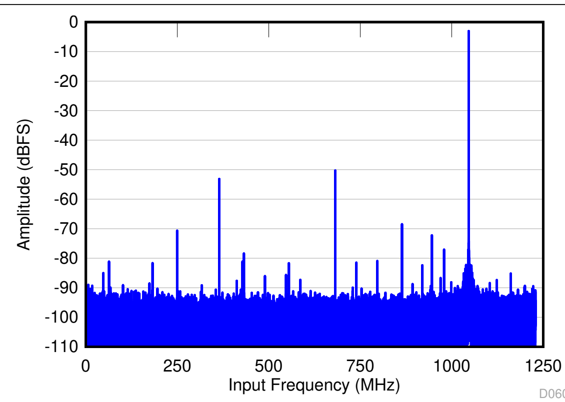
SNR = 55.4 dBFS; SFDR = 60 dBc; HD2 = –60 dBc; HD3 = –67 dBc; non HD2, HD3 = 72 dBc; IL spur = 75 dBc; f_{IN} = 2.6 GHz

Figure 6-12. FFT for 2600-MHz Input Signal (f_S = 2457.6 MSPS)



SNR = 54.2 dBFS; SFDR = 60 dBc; HD2 = –60 dBc; HD3 = –64 dBc; non HD2, HD3 = 71 dBc; IL spur = 80 dBc; f_{IN} = 3.5 GHz, A_{IN} = –3 dBFS with 2-dB gain

Figure 6-13. FFT for 3500-MHz Input Signal

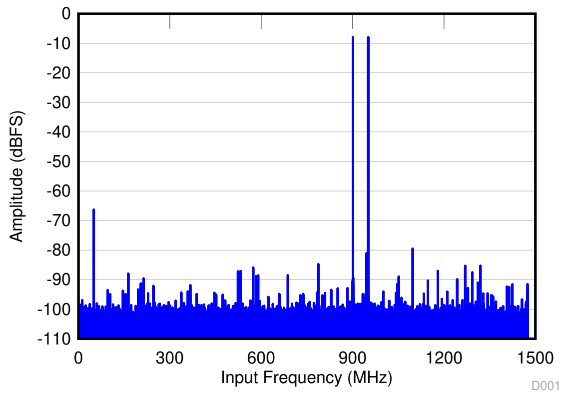


SNR = 53.6 dBFS; SFDR = 47 dBc; HD2 = –50 dBc; HD3 = –47 dBc; non HD2, HD3 = 70 dBc; IL spur = 67 dBc; f_{IN} = 3.5 GHz, A_{IN} = –3 dBFS with 2-dB gain

Figure 6-14. FFT for 3500-MHz Input Signal (f_S = 2457.6 MSPS)

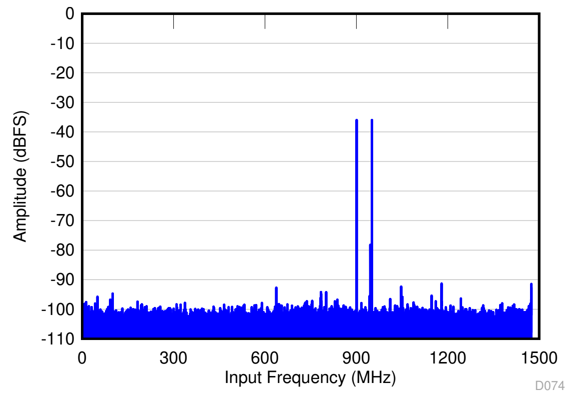
6.11 Typical Characteristics (continued)

typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C; and ADC sampling rate = 2949.12 MSPS, DDC bypassed performance, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –2-dBFS differential input, and 0-dB digital gain (unless otherwise noted)



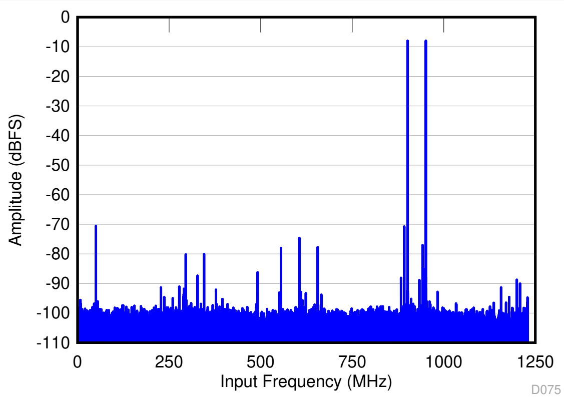
f_{IN1} = 900 MHz, f_{IN2} = 950 MHz, A_{IN} = –8 dBFS, IMD = 79 dBFS

Figure 6-15. FFT for Two-Tone Input Signal (–8 dBFS)



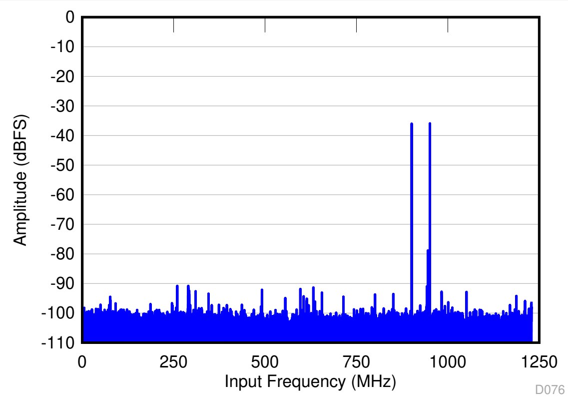
f_{IN1} = 900 MHz, f_{IN2} = 950 MHz, A_{IN} = –36 dBFS, IMD = 97 dBFS

Figure 6-16. FFT for Two-Tone Input Signal (–36 dBFS)



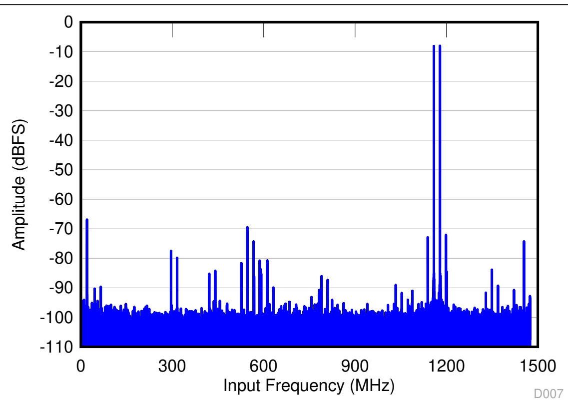
f_{IN1} = 900 MHz, f_{IN2} = 950 MHz, A_{IN} = –8 dBFS, IMD = 75 dBFS

Figure 6-17. FFT for Two-Tone Input Signal (–8 dBFS, f_S = 2457.6 MSPS)



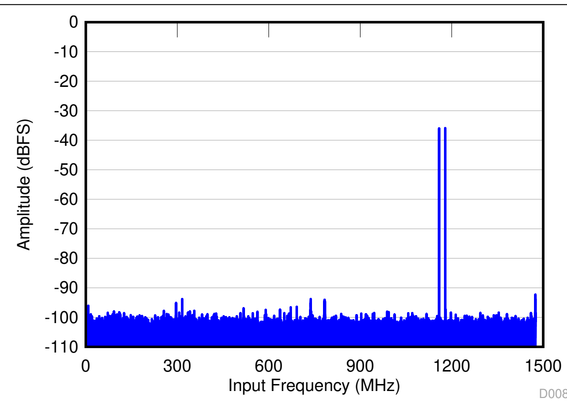
f_{IN1} = 900 MHz, f_{IN2} = 950 MHz, A_{IN} = –36 dBFS, IMD = 92 dBFS

Figure 6-18. FFT for Two-Tone Input Signal (–36 dBFS, f_S = 2457.6 MSPS)



f_{IN1} = 1.77 GHz, f_{IN2} = 1.79 GHz, A_{IN} = –8 dBFS, IMD = 70 dBFS

Figure 6-19. FFT for Two-Tone Input Signal (–8 dBFS)

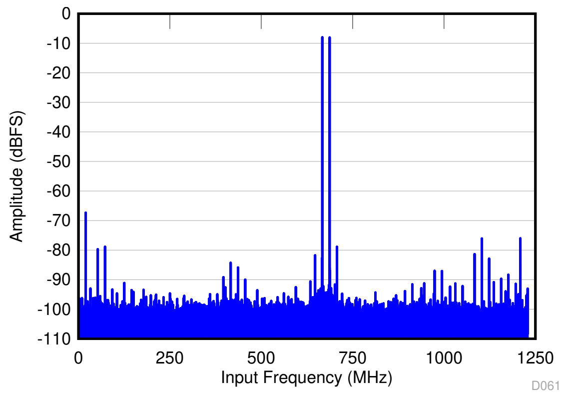


f_{IN1} = 1.77 GHz, f_{IN2} = 1.790 GHz, A_{IN} = –36 dBFS, IMD = 97 dBFS

Figure 6-20. FFT for Two-Tone Input Signal (–36 dBFS)

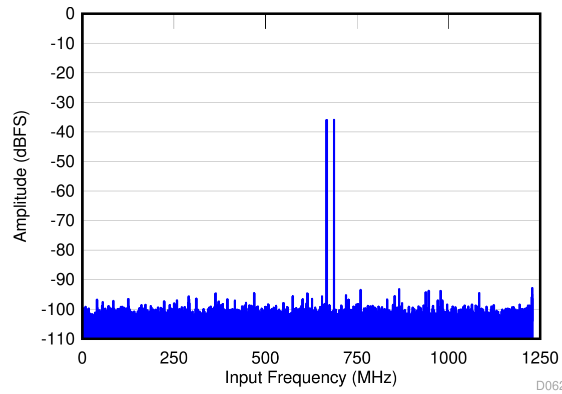
6.11 Typical Characteristics (continued)

typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C; and ADC sampling rate = 2949.12 MSPS, DDC bypassed performance, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –2-dBFS differential input, and 0-dB digital gain (unless otherwise noted)



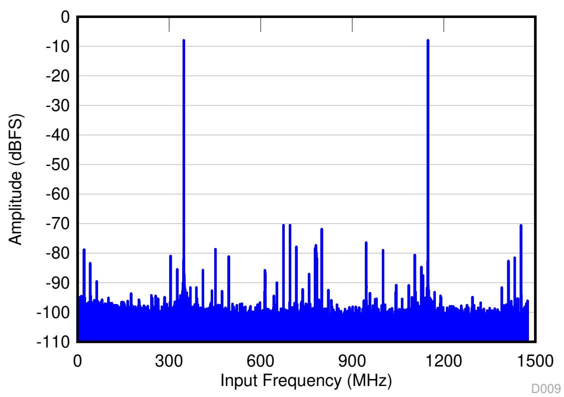
f_{IN1} = 1.77 GHz, f_{IN2} = 1.79 GHz, A_{IN} = –8 dBFS, IMD = 76 dBFS

Figure 6-21. FFT for Two-Tone Input Signal (–8 dBFS, f_S = 2457.6 MSPS)



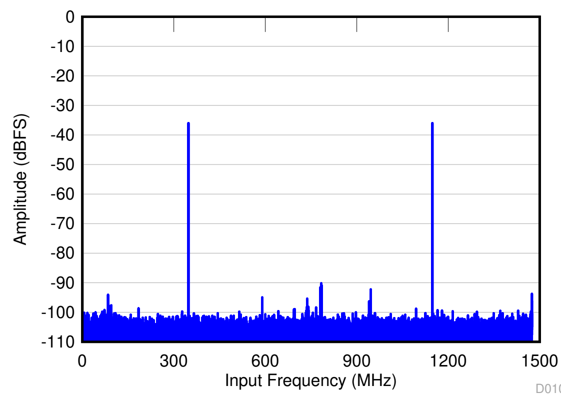
f_{IN1} = 1.77 GHz, f_{IN2} = 1.790 GHz, A_{IN} = –36 dBFS, IMD = 96 dBFS

Figure 6-22. FFT for Two-Tone Input Signal (–36 dBFS, f_S = 2457.6 MSPS)



f_{IN1} = 1.8 MHz, f_{IN2} = 2.6 GHz, A_{IN} = –8 dBFS, IMD = 71 dBFS

Figure 6-23. FFT for Two-Tone Input Signal (–8 dBFS)

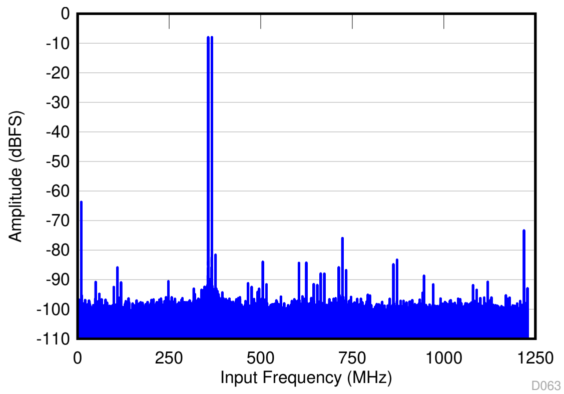


f_{IN1} = 1.8 GHz, f_{IN2} = 2.6 GHz, A_{IN} = –36 dBFS, IMD = 94 dBFS

Figure 6-24. FFT for Two-Tone Input Signal

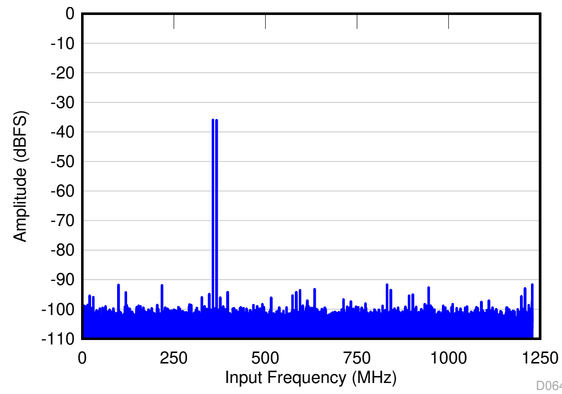
6.11 Typical Characteristics (continued)

typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C; and ADC sampling rate = 2949.12 MSPS, DDC bypassed performance, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –2-dBFS differential input, and 0-dB digital gain (unless otherwise noted)



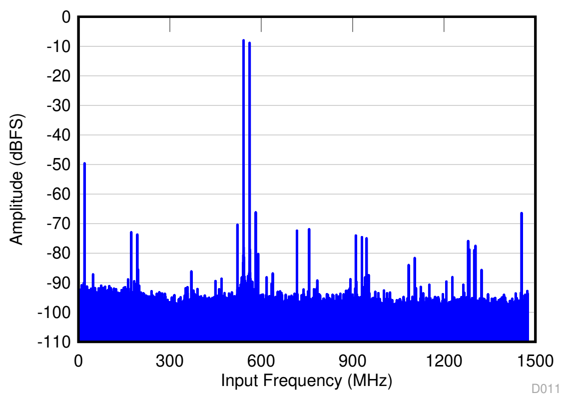
f_{IN1} = 2.09 GHz, f_{IN2} = 2.1 GHz, A_{IN} = –8 dBFS, IMD = 76 dBFS

Figure 6-25. FFT for Two-Tone Input Signal (–8 dBFS, f_S = 2457.6 MSPS)



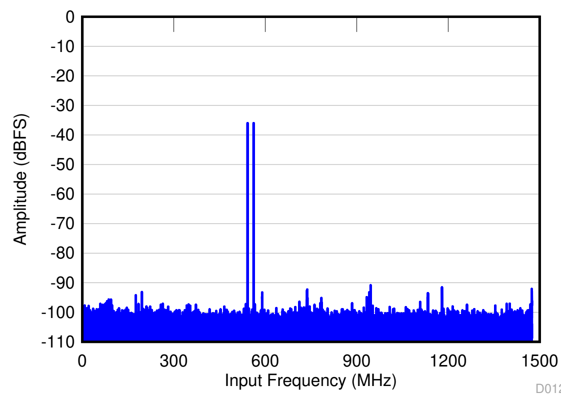
f_{IN1} = 2.09 MHz, f_{IN2} = 2.1 GHz, A_{IN} = –36 dBFS, IMD = 94 dBFS

Figure 6-26. FFT for Two-Tone Input Signal (–36 dBFS, f_S = 2457.6 MSPS)



f_{IN1} = 3.49 MHz, f_{IN2} = 3.51 GHz, IMD = 66 dBFS, A_{IN} = –3 dBFS with 2-dB gain

Figure 6-27. FFT for Two-Tone Input Signal (–8 dBFS)

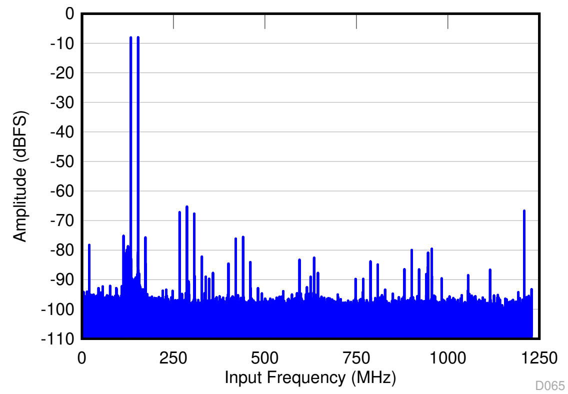


f_{IN1} = 3.49 GHz, f_{IN2} = 3.51 GHz, IMD = 92 dBFS, A_{IN} = –3 dBFS with 2-dB gain

Figure 6-28. FFT for Two-Tone Input Signal (–36 dBFS)

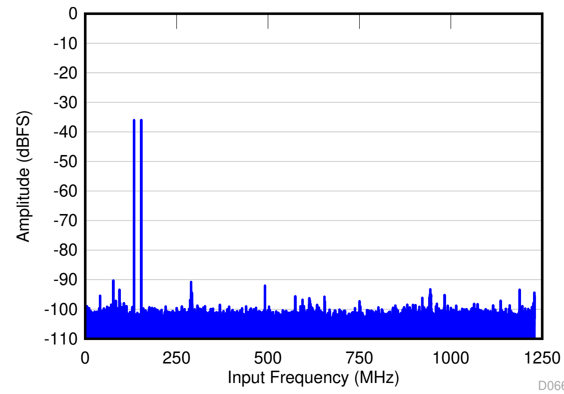
6.11 Typical Characteristics (continued)

typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C; and ADC sampling rate = 2949.12 MSPS, DDC bypassed performance, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –2-dBFS differential input, and 0-dB digital gain (unless otherwise noted)



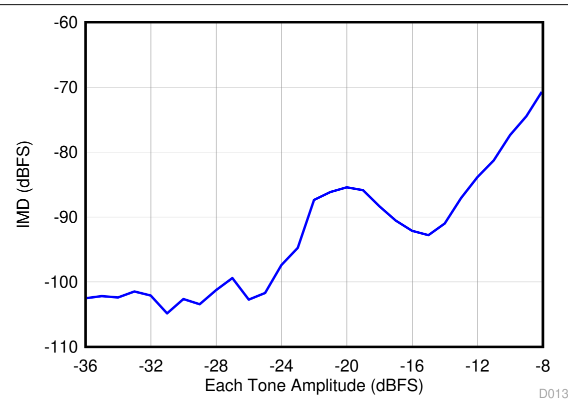
f_{IN1} = 2.59 GHz, f_{IN2} = 2.6 GHz, A_{IN} = –8 dBFS, IMD = 65 dBFS

Figure 6-29. FFT for Two-Tone Input Signal (–8 dBFS, f_S = 2457.6 MSPS)



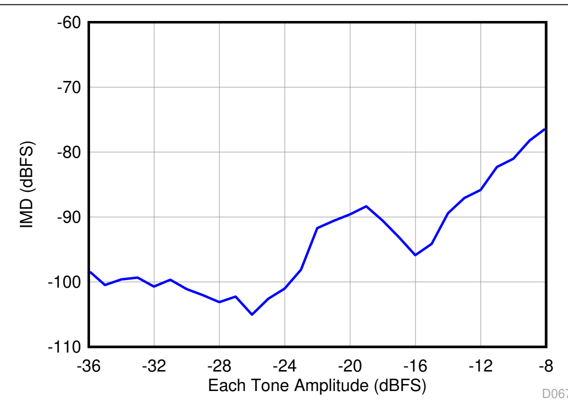
f_{IN1} = 2.59 GHz, f_{IN2} = 2.6 GHz, A_{IN} = –36 dBFS, IMD = 92 dBFS

Figure 6-30. FFT for Two-Tone Input Signal (–36 dBFS, f_S = 2457.6 MSPS)



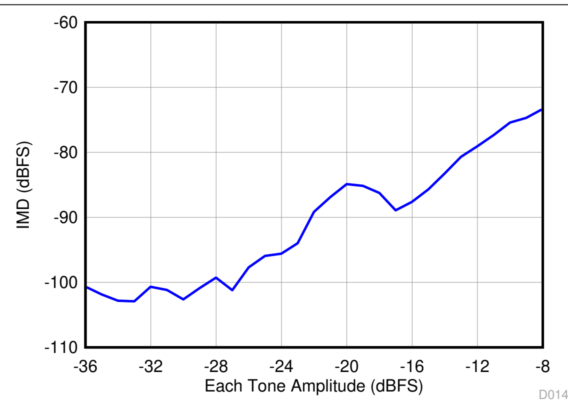
f_{IN1} = 1.77 GHz, f_{IN2} = 1.79 GHz

Figure 6-31. Intermodulation Distortion vs. Input Amplitude (1770 MHz and 1790 MHz)



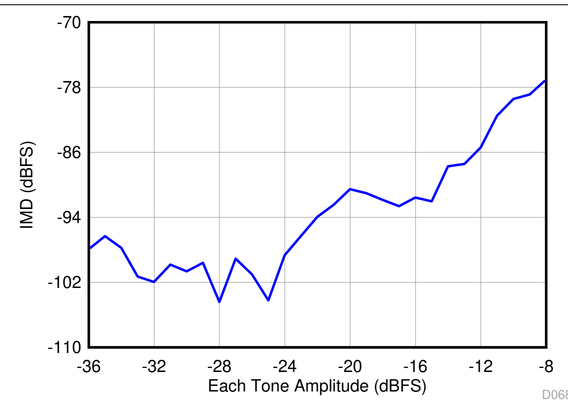
f_{IN1} = 1.77 GHz, f_{IN2} = 1.79 GHz

Figure 6-32. Intermodulation Distortion vs. Input Amplitude (1770 MHz and 1790 MHz, f_S = 2457.6 MSPS)



f_{IN1} = 1.8 GHz, f_{IN2} = 2.6 GHz, A_{IN} = –36 dBFS

Figure 6-33. Intermodulation Distortion vs. Input Amplitude (1800 MHz and 2600 MHz)

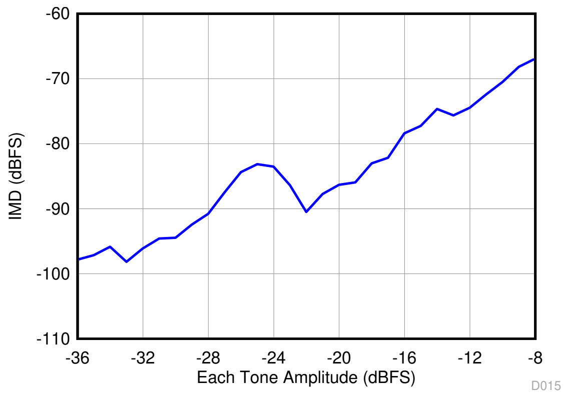


f_{IN1} = 2.09 GHz, f_{IN2} = 2.1 GHz

Figure 6-34. Intermodulation Distortion vs. Input Amplitude (1800 MHz and 2600 MHz, f_S = 2457.6 MSPS)

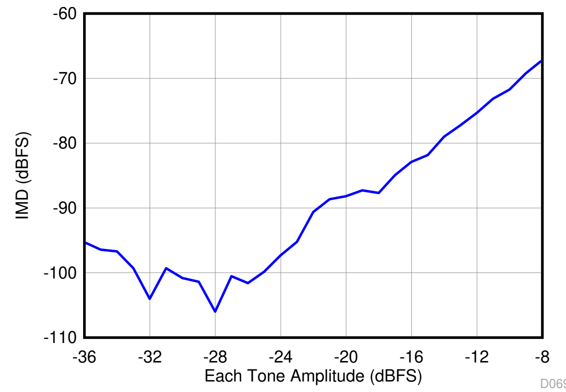
6.11 Typical Characteristics (continued)

typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C; and ADC sampling rate = 2949.12 MSPS, DDC bypassed performance, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –2-dBFS differential input, and 0-dB digital gain (unless otherwise noted)



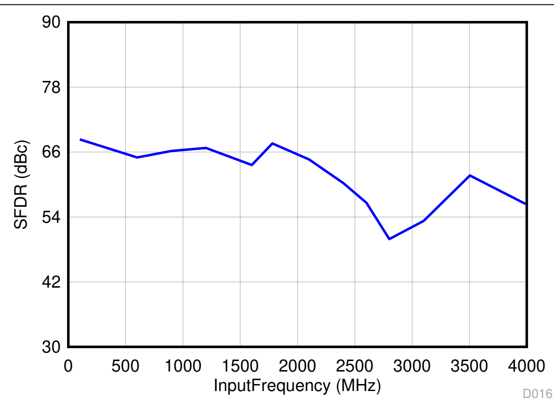
f_{IN1} = 3.49 GHz, f_{IN2} = 3.51 GHz with 2-dB digital gain

Figure 6-35. Intermodulation Distortion vs. Input Amplitude (3490 MHz and 3510 MHz)



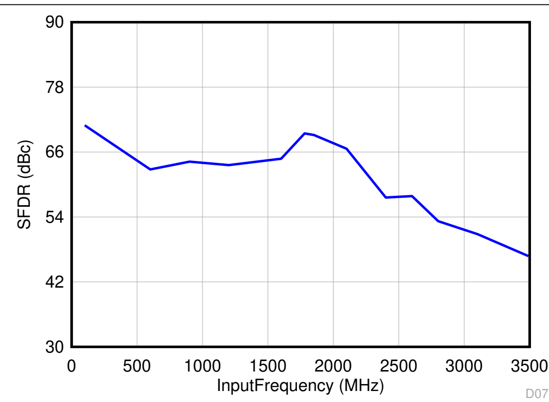
f_{IN1} = 2.59GHz, f_{IN2} = 2.6 GHz

Figure 6-36. Intermodulation Distortion vs. Input Amplitude (3490 MHz and 3510 MHz, f_S = 2457.6 MSPS)



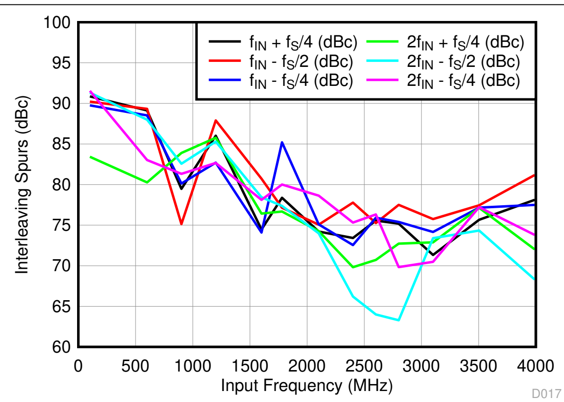
A_{OUT} = –2 dBFS with 0-dB gain for f_{IN} less than 3 GHz, A_{OUT} = –3 dBFS with 2-dB gain for f_{IN} more than 3 GHz

Figure 6-37. Spurious-Free Dynamic Range vs. Input Frequency



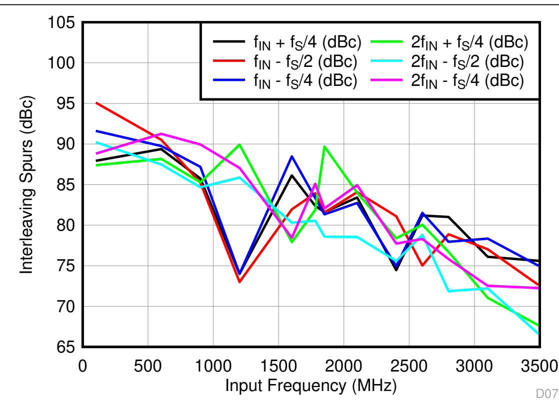
A_{OUT} = –2 dBFS with 0-dB gain for f_{IN} less than 3 GHz, A_{OUT} = –3 dBFS with 2-dB gain for f_{IN} more than 3 GHz

Figure 6-38. Spurious-Free Dynamic Range vs. Input Frequency (f_S = 2457.6 MSPS)



A_{OUT} = –2 dBFS with 0-dB gain for f_{IN} less than 3 GHz, A_{OUT} = –3 dBFS with 2-dB gain for f_{IN} more than 3 GHz

Figure 6-39. IL Spur vs. Input Frequency

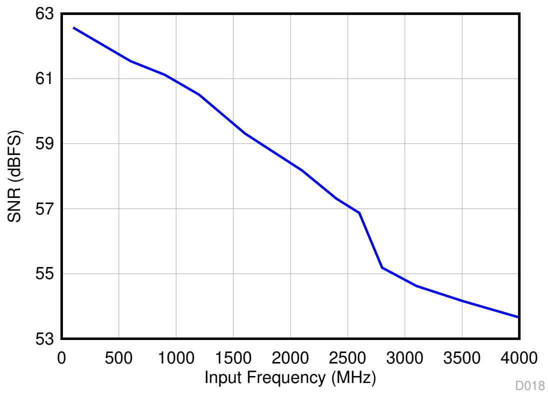


A_{OUT} = –2 dBFS with 0-dB gain for f_{IN} less than 3 GHz, A_{OUT} = –3 dBFS with 2-dB gain for f_{IN} more than 3 GHz

Figure 6-40. IL Spur vs. Input Frequency (f_S = 2457.6 MSPS)

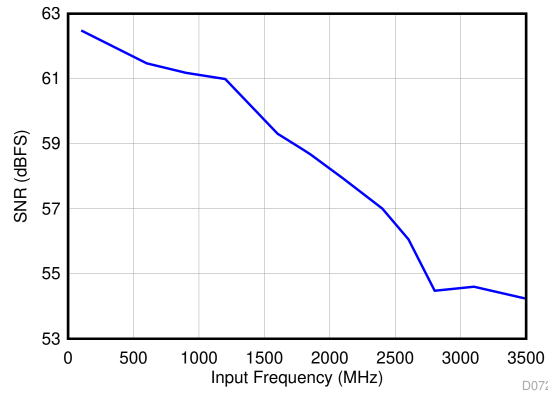
6.11 Typical Characteristics (continued)

typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C; and ADC sampling rate = 2949.12 MSPS, DDC bypassed performance, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –2-dBFS differential input, and 0-dB digital gain (unless otherwise noted)



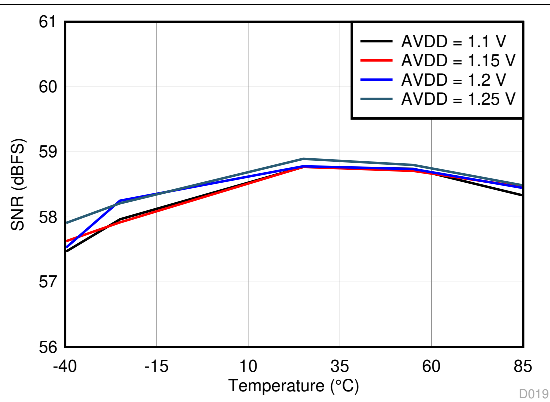
A_{OUT} = –2 dBFS with 0-dB gain for f_{IN} less than 3 GHz, A_{OUT} = –3 dBFS with 2-dB gain for f_{IN} more than 3 GHz

Figure 6-41. Signal-to-Noise Ratio vs. Input Frequency



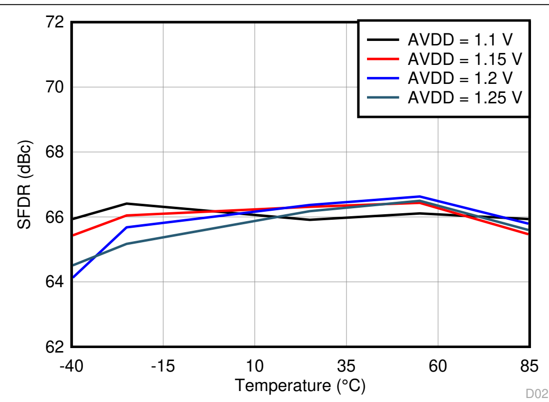
A_{OUT} = –2 dBFS with 0-dB gain for f_{IN} less than 3 GHz, A_{OUT} = –3 dBFS with 2-dB gain for f_{IN} more than 3 GHz

Figure 6-42. Signal-to-Noise Ratio vs. Input Frequency (f_S = 2457.6 MSPS)



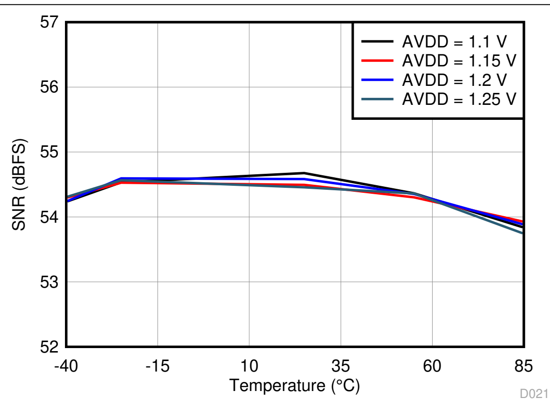
f_{IN} = 1.78 GHz, A_{IN} = –2 dBFS

Figure 6-43. Signal-to-Noise Ratio vs. AVDD Supply and Temperature



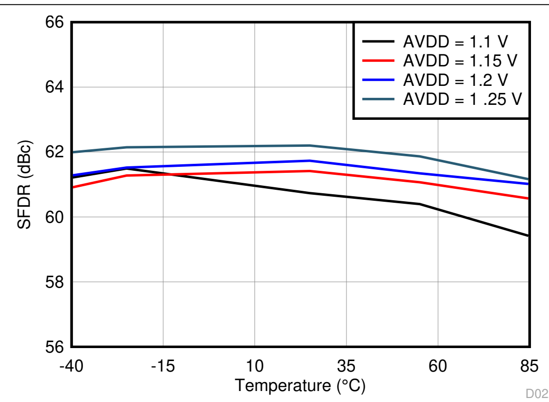
f_{IN} = 1.78 GHz, A_{IN} = –2 dBFS

Figure 6-44. Spurious-Free Dynamic Range vs. AVDD Supply and Temperature



f_{IN} = 3.5 GHz, A_{IN} = –3 dBFS with 2-dB digital gain

Figure 6-45. Signal-to-Noise Ratio vs. AVDD Supply and Temperature

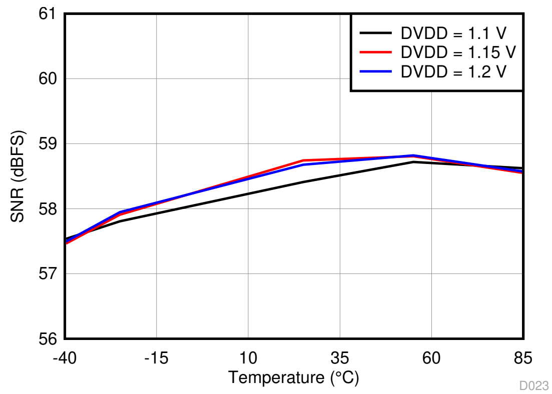


f_{IN} = 3.5GHz, A_{IN} = –3 dBFS with 2-dB digital gain

Figure 6-46. Spurious-Free Dynamic Range vs. AVDD Supply and Temperature

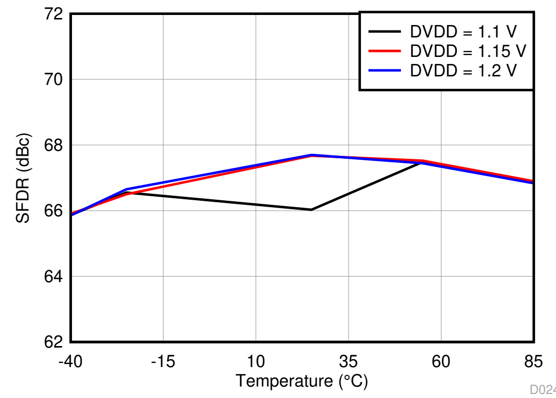
6.11 Typical Characteristics (continued)

typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C; and ADC sampling rate = 2949.12 MSPS, DDC bypassed performance, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –2-dBFS differential input, and 0-dB digital gain (unless otherwise noted)



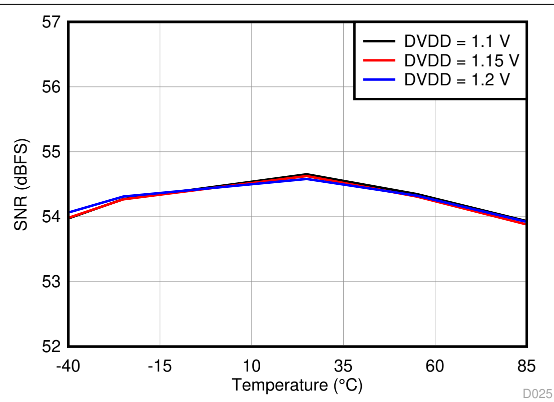
f_{IN} = 1.78 GHz, A_{IN} = –2 dBFS

Figure 6-47. Signal-to-Noise Ratio vs. DVDD Supply and Temperature



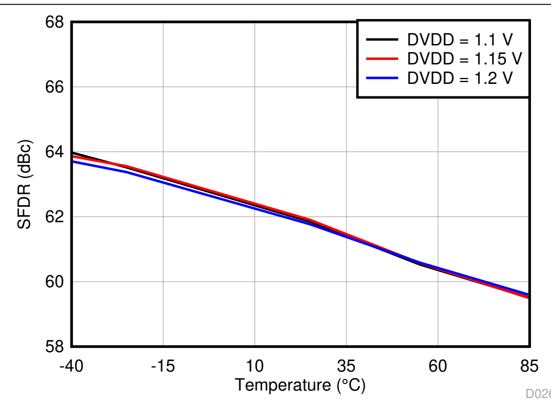
f_{IN} = 1.78 GHz, A_{IN} = –2 dBFS

Figure 6-48. Spurious-Free Dynamic Range vs. DVDD Supply and Temperature



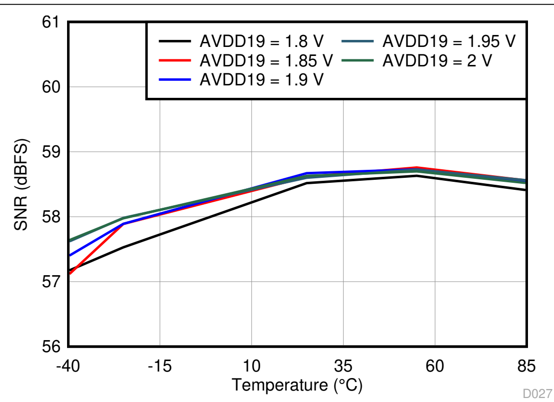
f_{IN} = 3.5 GHz, A_{IN} = –3 dBFS with 2-dB digital gain

Figure 6-49. Signal-to-Noise Ratio vs. DVDD Supply and Temperature



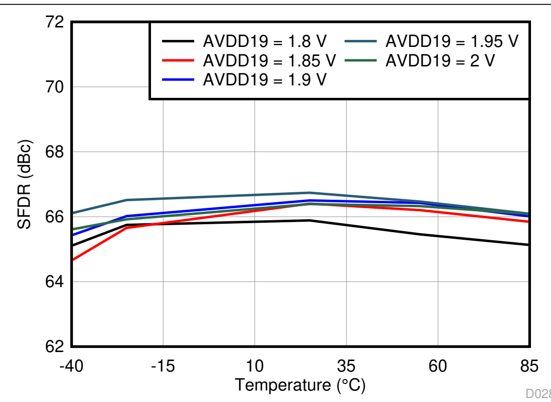
f_{IN} = 3.5 GHz, A_{IN} = –3 dBFS with 2-dB digital gain

Figure 6-50. Spurious-Free Dynamic Range vs. DVDD Supply and Temperature



f_{IN} = 1.78 GHz, A_{IN} = –2 dBFS

Figure 6-51. Signal-to-Noise Ratio vs. AVDD19 Supply and Temperature

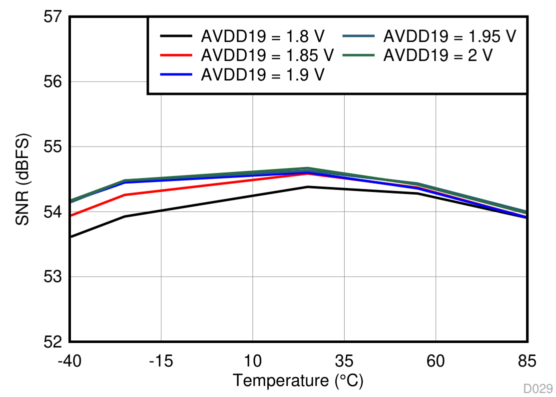


f_{IN} = 1.78 GHz, A_{IN} = –2 dBFS

Figure 6-52. Spurious-Free Dynamic Range vs. AVDD19 Supply and Temperature

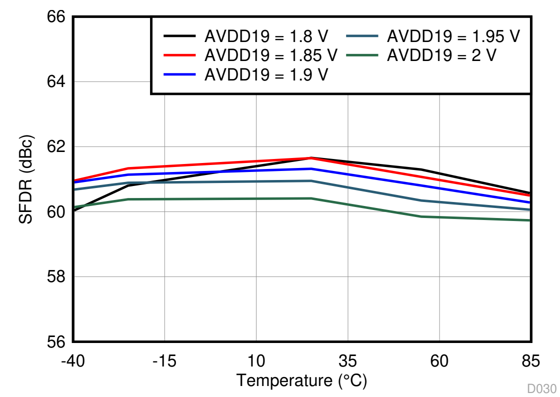
6.11 Typical Characteristics (continued)

typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C; and ADC sampling rate = 2949.12 MSPS, DDC bypassed performance, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –2-dBFS differential input, and 0-dB digital gain (unless otherwise noted)



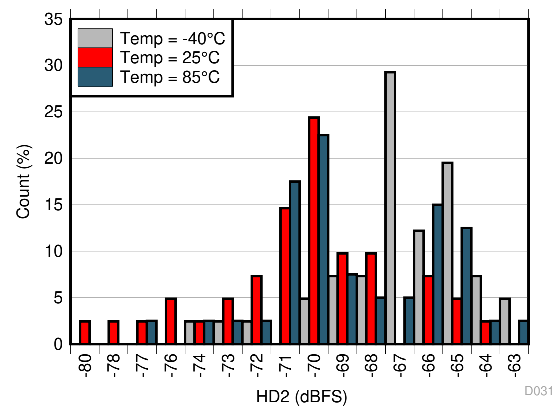
f_{IN} = 3.5 GHz, A_{IN} = –3 dBFS with 2-dB digital gain

Figure 6-53. Signal-to-Noise Ratio vs. AVDD19 Supply and Temperature



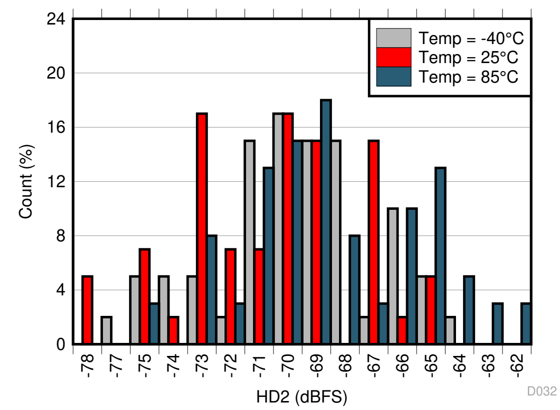
f_{IN} = 3.5 GHz, A_{IN} = –3 dBFS with 2-dB digital gain

Figure 6-54. Spurious-Free Dynamic Range vs. AVDD19 Supply and Temperature



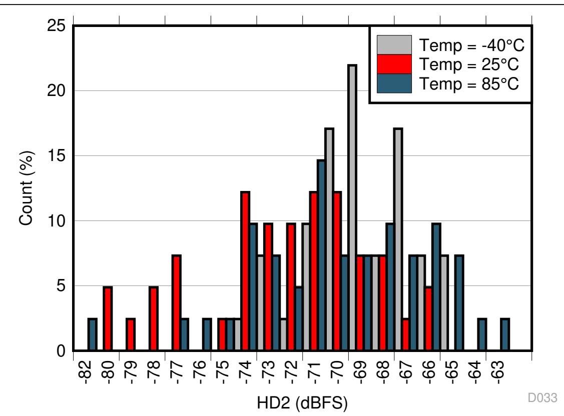
f_{IN} = 1.78 GHz

Figure 6-55. HD2 Histogram at AVDD19 = 1.8 V



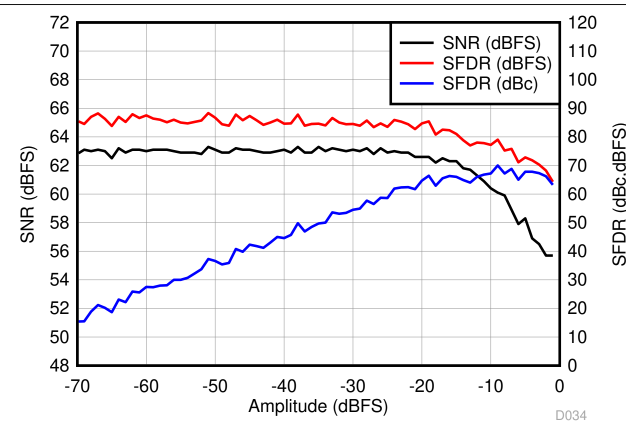
f_{IN} = 1.78 GHz

Figure 6-56. HD2 Histogram at AVDD19 = 1.9 V



f_{IN} = 1.78 GHz

Figure 6-57. HD2 Histogram at AVDD19 = 2.0 V

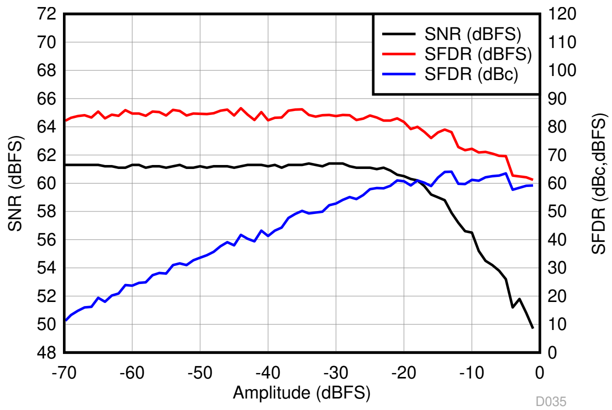


f_{IN} = 1.78 GHz, A_{IN} = –2 dBFS

Figure 6-58. Performance vs. Amplitude

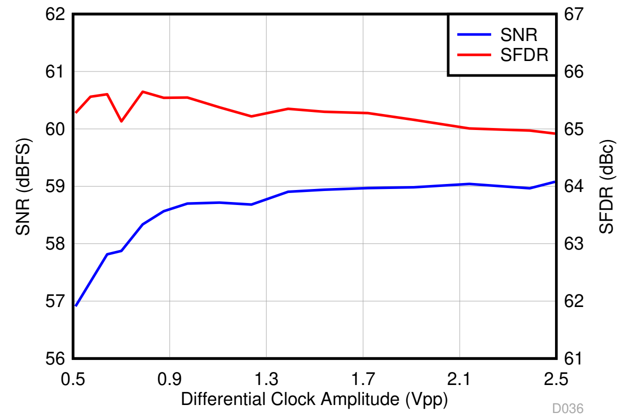
6.11 Typical Characteristics (continued)

typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C; and ADC sampling rate = 2949.12 MSPS, DDC bypassed performance, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –2-dBFS differential input, and 0-dB digital gain (unless otherwise noted)



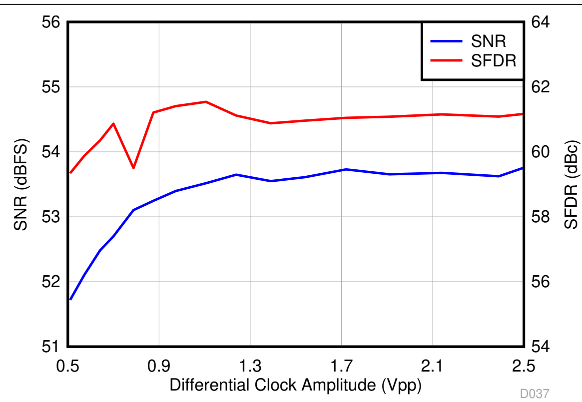
f_{IN} = 3.5 GHz, A_{IN} = –3 dBFS with 2-dB digital gain

Figure 6-59. Performance vs. Amplitude



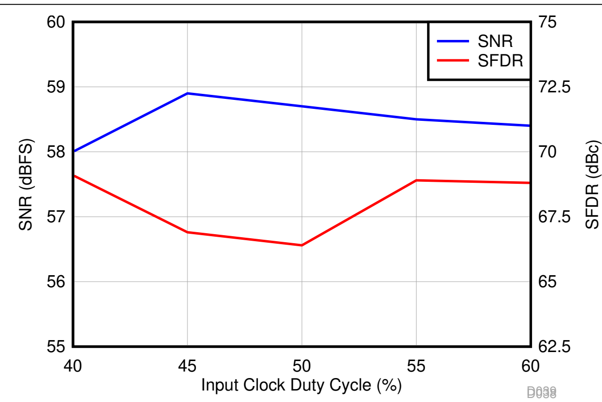
f_{IN} = 1.78 GHz, A_{IN} = –2 dBFS

Figure 6-60. Performance vs. Clock Amplitude



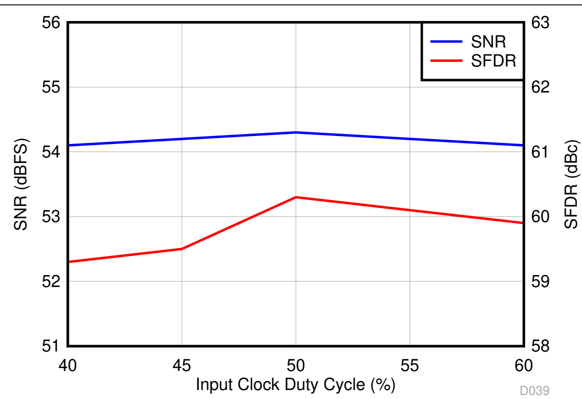
f_{IN} = 3.5 GHz, A_{IN} = –3 dBFS

Figure 6-61. Performance vs. Clock Amplitude



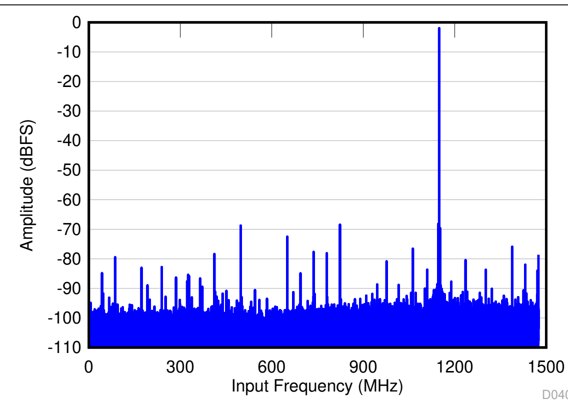
f_{IN} = 1.78 GHz, A_{IN} = –2 dBFS

Figure 6-62. Performance vs. Clock Duty Cycle



f_{IN} = 3.5 GHz, A_{IN} = –3 dBFS with 2-dB digital gain

Figure 6-63. Performance vs. Clock Duty Cycle



f_{IN} = 3.5 GHz, A_{IN} = –3 dBFS, PSRR = 37 dB, f_{PSRR} = 3 MHz, A_{PSRR} = 50 mV_{PP}, AVDD = 1.9 V

Figure 6-64. Power-Supply Rejection Ratio FFT for Test Signal on AVDD Supply

6.11 Typical Characteristics (continued)

typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C; and ADC sampling rate = 2949.12 MSPS, DDC bypassed performance, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –2-dBFS differential input, and 0-dB digital gain (unless otherwise noted)

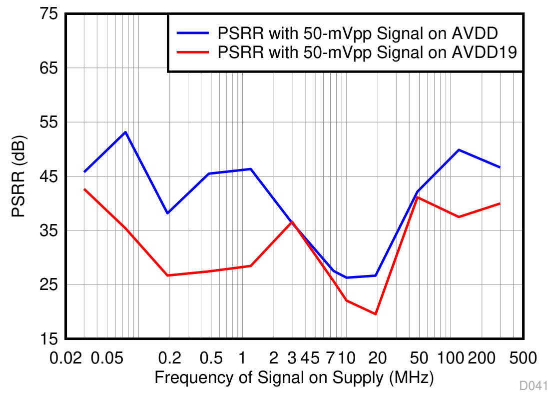
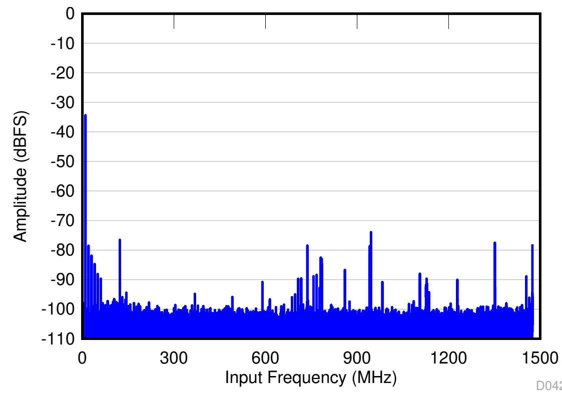
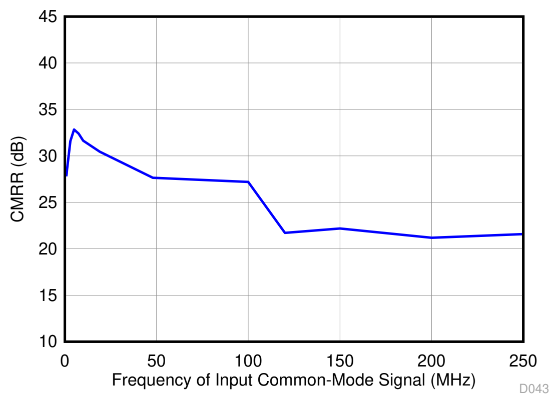


Figure 6-65. Power-Supply Rejection Ratio vs. Tone Frequency



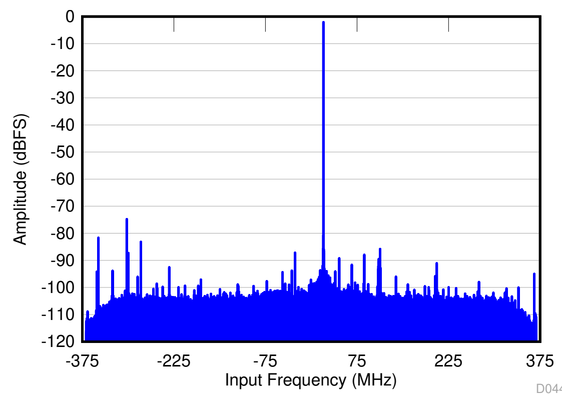
CMRR = 32 dB, f_{CMRR} = 32 dB, A_{PSRR} = 50 mVPP

Figure 6-66. Common-Mode Rejection Ratio FFT



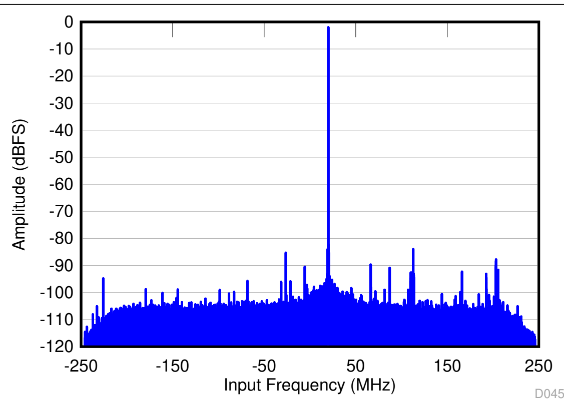
f_{IN} = 1.8 GHz, A_{OUT} = –2 dBFS

Figure 6-67. Common-Mode Rejection Ratio vs. Tone Frequency



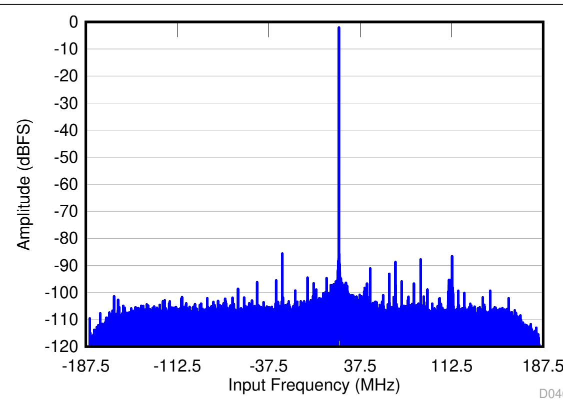
f_{IN} = 1.78 GHz, A_{IN} = –2 dBFS, f_S = 2949.12 MSPS, SNR = 60.6 dBFS, SFDR (includes IL) = 75 dBc

Figure 6-68. FFT in 4x Decimation (Complex Output)



f_{IN} = 1.78 GHz, A_{IN} = –2 dBFS, f_S = 2949.12 MSPS, SNR = 61.6 dBFS, SFDR (includes IL) = 82 dBc

Figure 6-69. FFT in 6x Decimation (Complex Output)

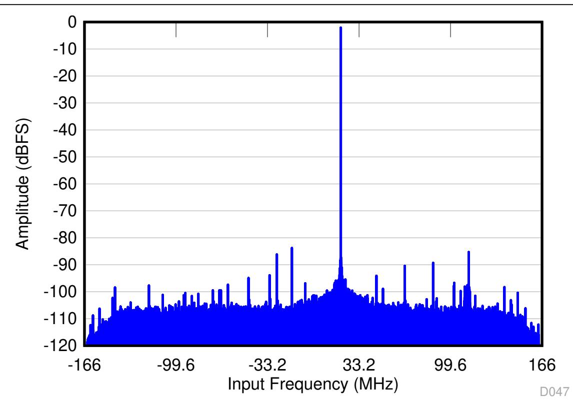


f_{IN} = 1.78 GHz, A_{IN} = –2 dBFS, f_S = 2949.12 MSPS, SNR = 62.6 dBFS, SFDR (includes IL) = 86 dBc

Figure 6-70. FFT in 8x Decimation (Complex Output)

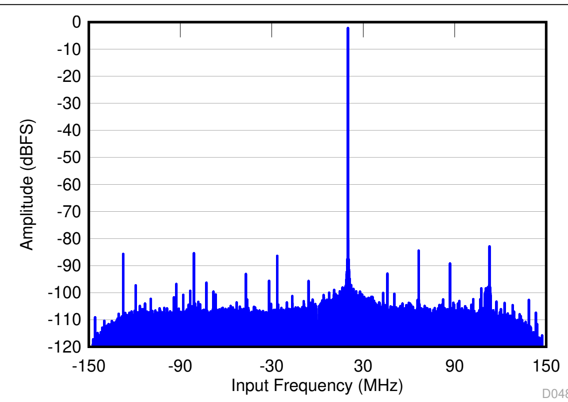
6.11 Typical Characteristics (continued)

typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C; and ADC sampling rate = 2949.12 MSPS, DDC bypassed performance, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –2-dBFS differential input, and 0-dB digital gain (unless otherwise noted)



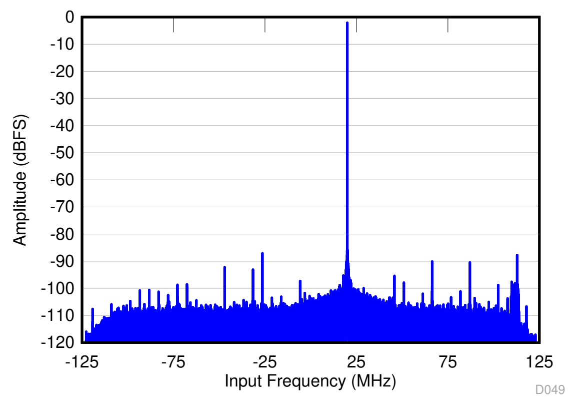
f_{IN} = 1.78 GHz, A_{IN} = –2 dBFS, f_S = 2949.12 MSPS, SNR = 63 dBFS, SFDR (includes IL) = 82 dBc

Figure 6-71. FFT in 9x Decimation (Complex Output)



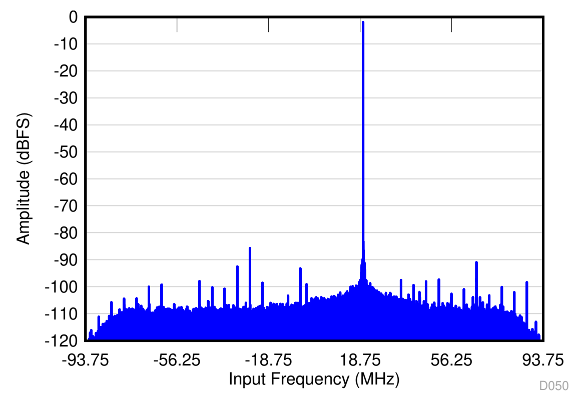
f_{IN} = 1.78 GHz, A_{IN} = –2 dBFS, f_S = 2949.12 MSPS, SNR = 63.3 dBFS, SFDR (includes IL) = 81 dBc

Figure 6-72. FFT in 10x Decimation (Complex Output)



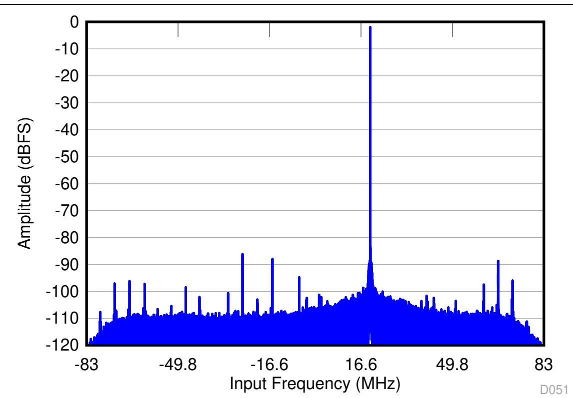
f_{IN} = 1.78 GHz, A_{IN} = –2 dBFS, f_S = 2949.12 MSPS, SNR = 63.7 dBFS, SFDR (includes IL) = 83 dBc

Figure 6-73. FFT in 12x Decimation (Complex Output)



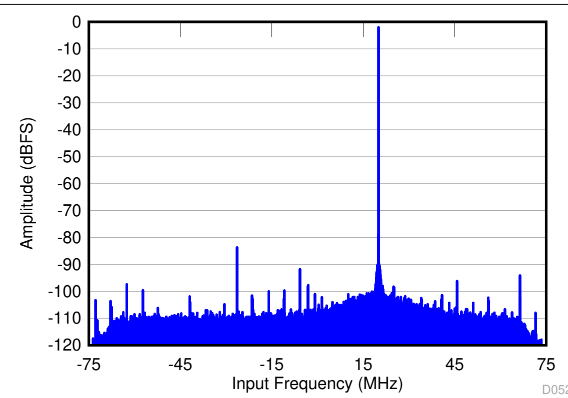
f_{IN} = 1.78 GHz, A_{IN} = –2 dBFS, f_S = 2949.12 MSPS, SNR = 63.9 dBFS, SFDR (includes IL) = 83 dBc

Figure 6-74. FFT in 16x Decimation (Complex Output)



f_{IN} = 1.78 GHz, A_{IN} = –2 dBFS, f_S = 2949.12 MSPS, SNR = 64 dBFS, SFDR (includes IL) = 83 dBc

Figure 6-75. FFT in 18x Decimation (Complex Output)

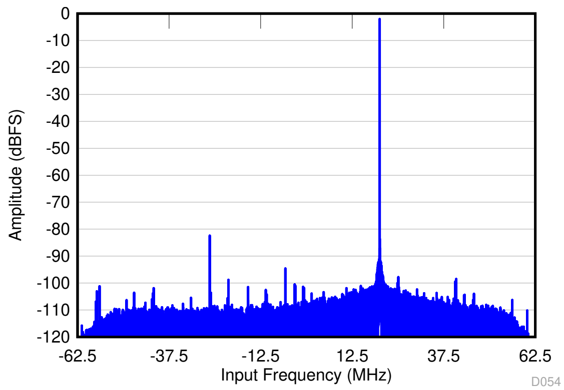


f_{IN} = 1.78 GHz, A_{IN} = –2 dBFS, f_S = 2949.12 MSPS, SNR = 64.4 dBFS, SFDR (includes IL) = 84 dBc

Figure 6-76. FFT in 20x Decimation (Complex Output)

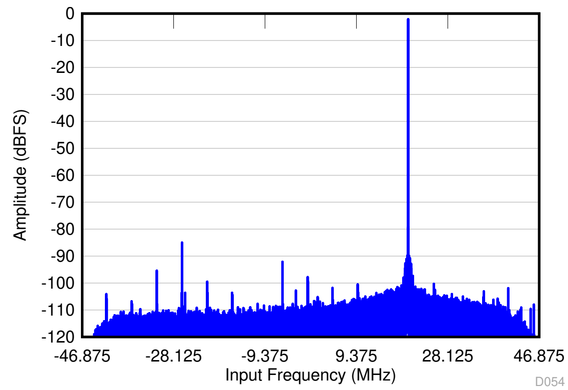
6.11 Typical Characteristics (continued)

typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C; and ADC sampling rate = 2949.12 MSPS, DDC bypassed performance, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –2-dBFS differential input, and 0-dB digital gain (unless otherwise noted)



f_{IN} = 1.78 GHz, A_{IN} = –2 dBFS, f_S = 2949.12 MSPS, SNR = 64.4 dBFS, SFDR (includes IL) = 82 dBc

Figure 6-77. FFT in 24x Decimation (Complex Output)



f_{IN} = 1.78 GHz, A_{IN} = –2 dBFS, f_S = 2949.12 MSPS, SNR = 64.5 dBFS, SFDR (includes IL) = 79 dBc

Figure 6-78. FFT in 32x Decimation (Complex Output)

7 Parameter Measurement Information

7.1 Input Clock Diagram

Figure 7-1 shows the input clock diagram.

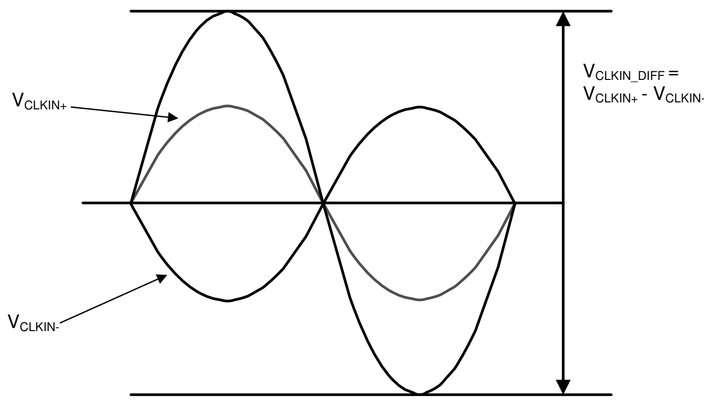


Figure 7-1. Input Clock Diagram

8 Detailed Description

8.1 Overview

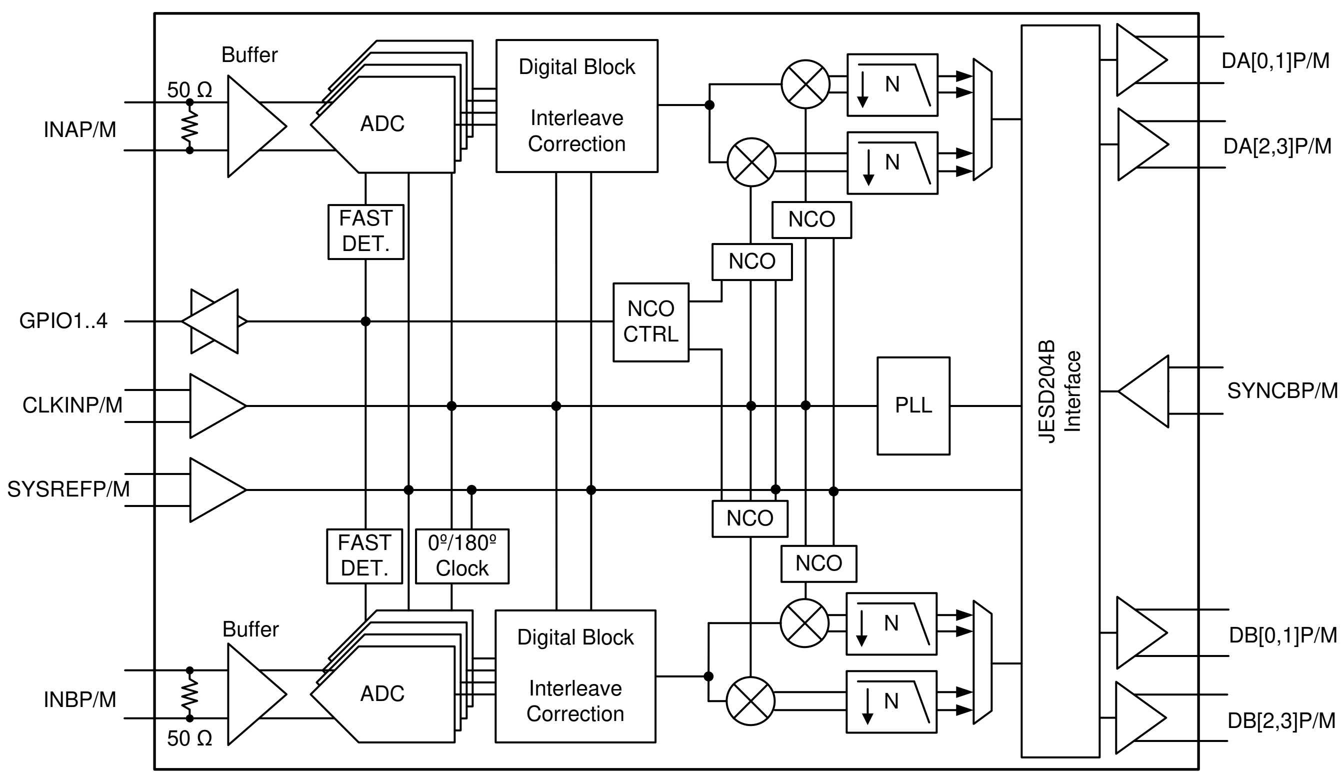
The ADC32RF8x is a dual, 14-bit, 2949.12-MSPS, telecom receiver and feedback device family containing analog-to-digital converters (ADCs) followed by multi-band digital down-converters (DDCs), and a back-end JESD204B digital interface.

The ADCs are preceded by input buffers and on-chip termination to provide a uniform input impedance over a large input frequency range. Furthermore, an internal differential clamping circuit provides first-level protection against overvoltage conditions. Each ADC channel is internally interleaved four times and equipped with background, analog and digital, and interleaving correction.

The on-chip DDC enables single- or dual-band internal processing to pre-select and filter smaller bands of interest and also reduces the digital output data traffic. Each DDC is equipped with up to three independent, 16-bit numerically-controlled oscillators (NCOs) for phase coherent frequency hopping; the NCOs can be controlled through the SPI or GPIO pins. The ADC32RF8x also provides three different power detectors on-chip with alarm outputs in order to support external automatic gain control (AGC) loops.

The processed data are passed into the JESD204B interface where the data are framed, encoded, serialized, and output on one to four lanes per channel, depending on the ADC sampling rate and decimation. The CLKIN, SYSREF, and SYNCB inputs provide the device clock and the SYSREF and SYNCB signals to the JESD204B interface that are used to derive the internal local frame and local multiframe clocks and establish the serial link. All features of the ADC32RF8x are configurable through the SPI.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Analog Inputs

The ADC32RF8x analog signal inputs are designed to be driven differentially. The analog input pins have internal analog buffers that drive the sampling circuit. The ADC32RF8x provides on-chip, differential termination to minimize reflections. The buffer also helps isolate the external driving circuit from the internal switching currents of the sampling circuit, thus resulting in a more constant SFDR performance across input frequencies.

The common-mode voltage of the signal inputs is internally biased to CM using the 32.5-Ω termination resistors that allow for ac-coupling of the input drive network. Figure 8-1 and Figure 8-2 show SDD11 at the analog inputs from dc to 5 GHz with a 100-Ω reference impedance.

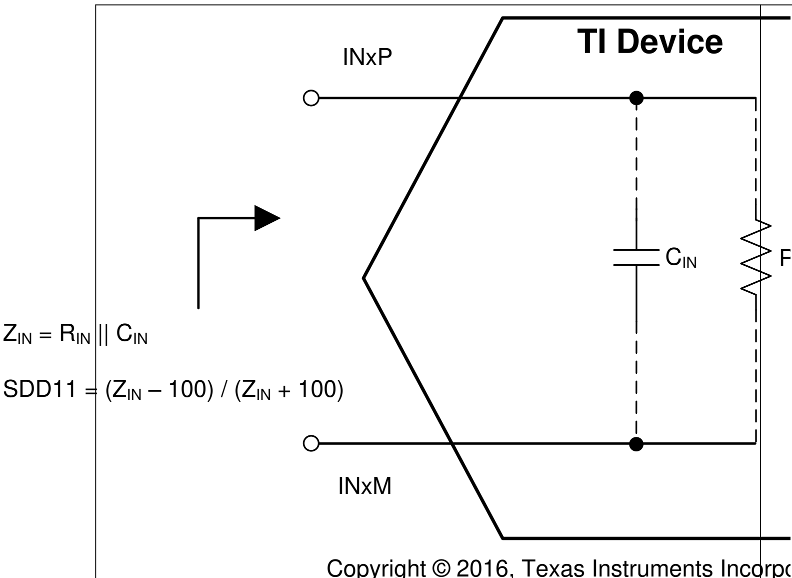


Figure 8-1. Equivalent Input Impedance

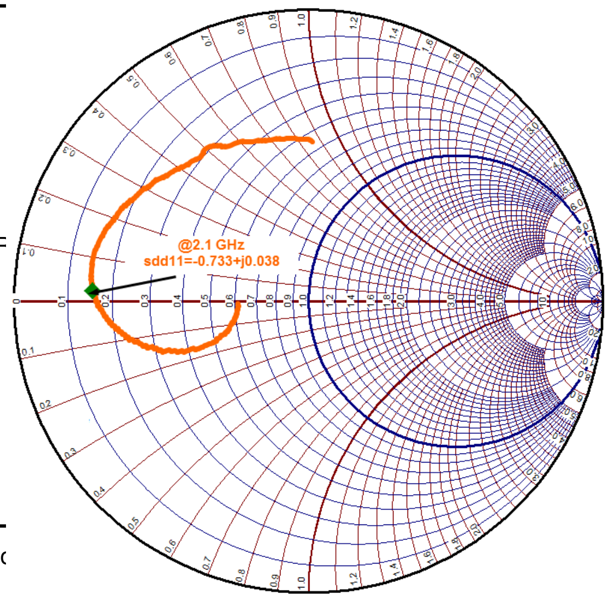


Figure 8-2. SDD11 Over the Input Frequency Range

The input impedance of analog inputs can also be modeled as parallel combination of equivalent resistance and capacitance. Figure 8-3 and Figure 8-4 show how equivalent impedance (C_{IN} and R_{IN}) vary over frequency.

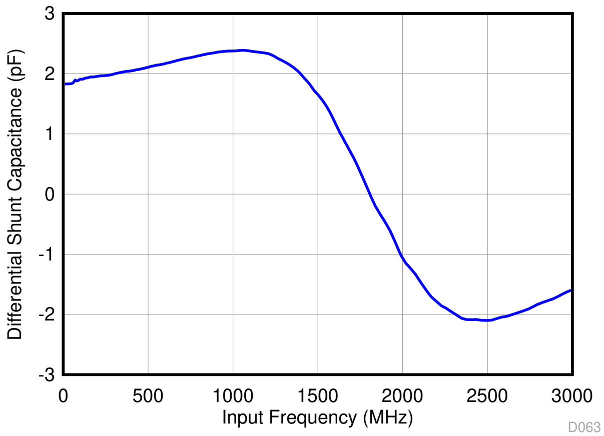


Figure 8-3. Differential Input Capacitance vs. Input Frequency

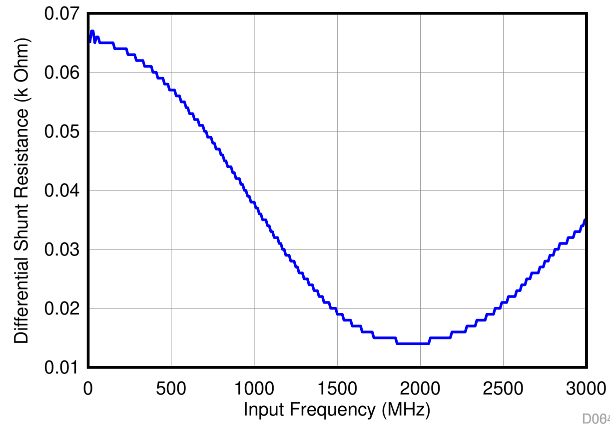


Figure 8-4. Differential Input Resistance vs. Input Frequency

Each input pin (INP, INM) must swing symmetrically between (CM + 0.3375 V) and (CM – 0.3375 V), resulting in a 1.35-V_{PP} (default) differential input swing. As shown in Figure 8-5, the input sampling circuit has a 3-dB bandwidth that extends up to approximately 3.2 GHz.

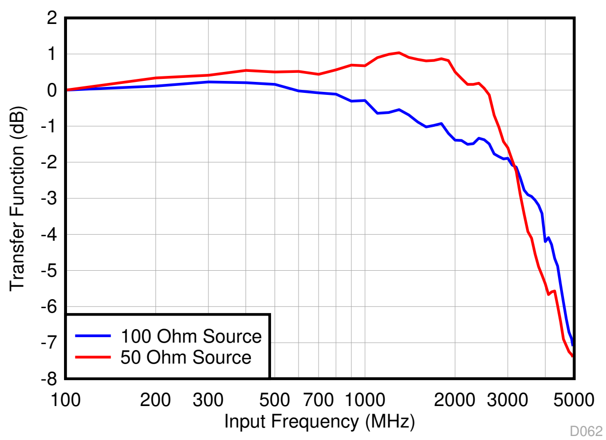


Figure 8-5. Input Bandwidth With a 100-Ω Source Resistance

8.3.1.1 Input Clamp Circuit

The ADC32RF8x analog inputs include an internal, differential clamp for overvoltage protection. As shown in Figure 8-6 and Figure 8-7, the clamp triggers for any input signals at approximately 600 mV above the input common-mode voltage, effectively limiting the maximum input signal to approximately 2.4 V_{PP}.

When the clamp circuit conducts, the maximum differential current flowing through the circuit (via input pins) must be limited to 20 mA.

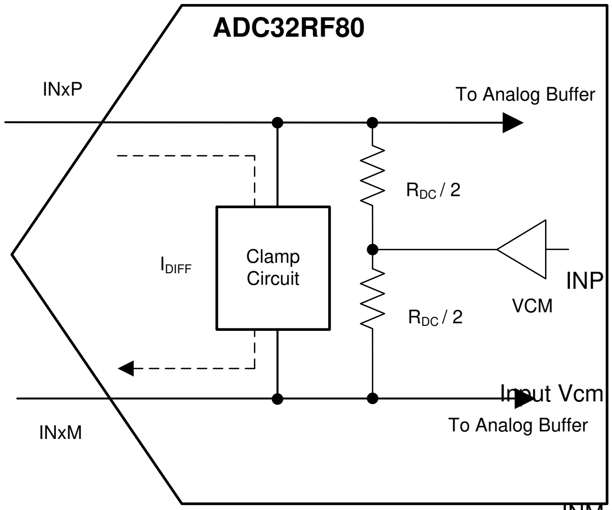


Figure 8-6. Clamp Circuit in the ADC32RF8x

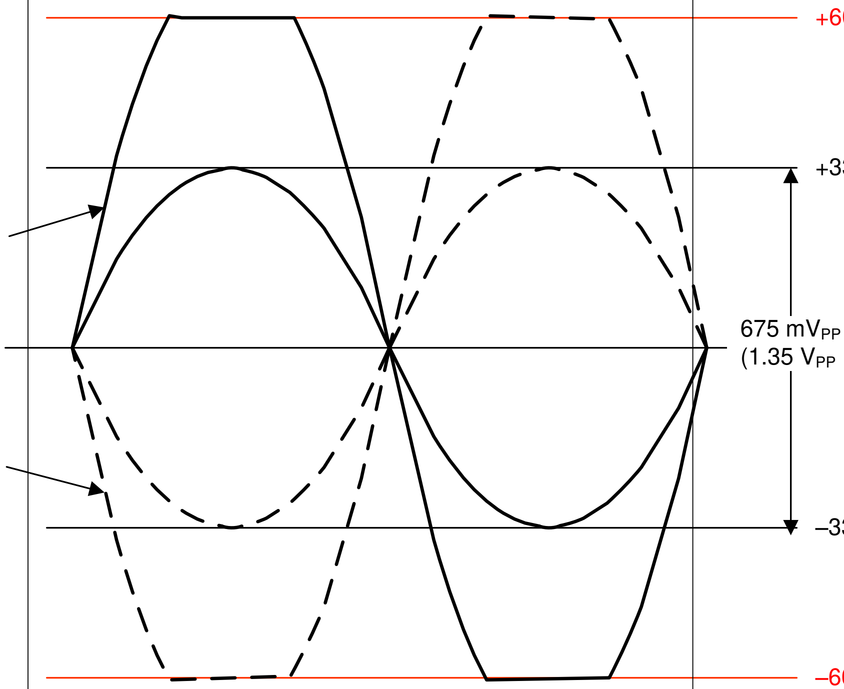


Figure 8-7. Clamp Response Timing Diagram

8.3.2 Clock Input

The ADC32RF8x sampling clock input includes internal 100-Ω differential termination along with on-chip biasing. The clock input is recommended to be ac-coupled externally. The input bandwidth of the clock input is approximately 3 GHz; the clock input impedance is shown in the smith chart of Figure 8-8 with a 100-Ω reference impedance.

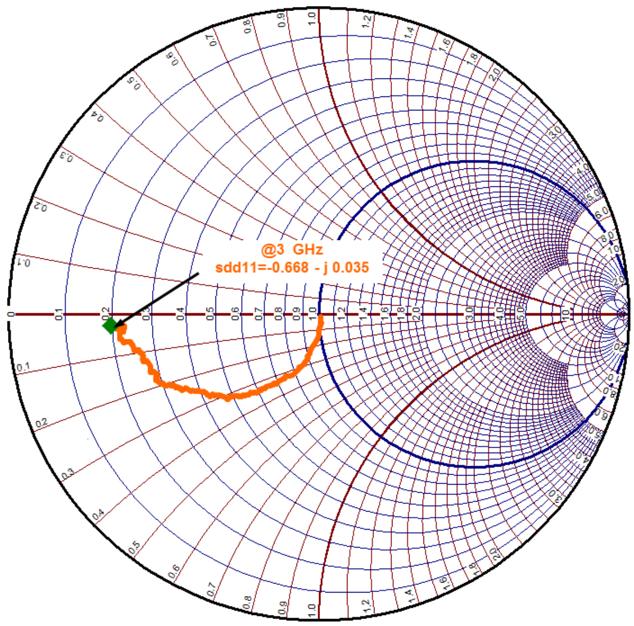


Figure 8-8. SDD11 of the Clock Input

The analog-to-digital converter (ADC) aperture jitter is a function of the clock amplitude applied to the pins. The equivalent aperture jitter is shown in Figure 8-9 for input frequencies at a 1-GHz and a 2-GHz input. Depending on the clock frequency, a matching circuit can be designed in order to maximize the clock amplitude.

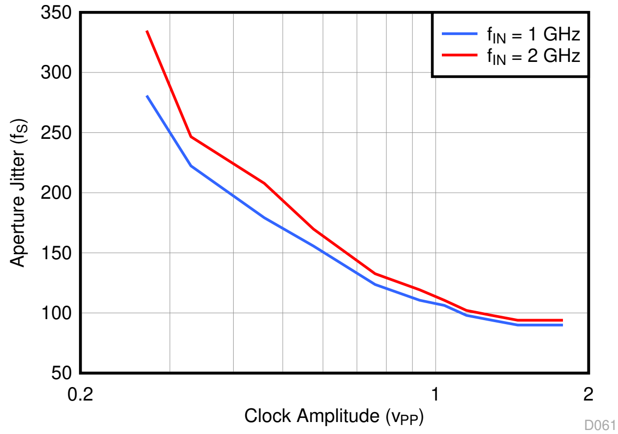


Figure 8-9. Equivalent Aperture Jitter vs. Input Clock Amplitude

8.3.3 SYSREF Input

The SYSREF signal is a periodic signal that is sampled by the ADC32RF8x device clock and is used to align the boundary of the local multiframe clock inside the data converter. SYSREF is also used to reset critical blocks [such as the clock divider for the interleaved ADCs, numerically-controlled oscillators (NCOs), decimation filters and so forth].

The SYSREF input requires external biasing. Furthermore, SYSREF must be established before the SPI registers are programmed. A programmable delay on the SYSREF input, as shown in Figure 8-10, is available to help with skew adjustment when the sampling clock and SYSREF are not provided from the same source.

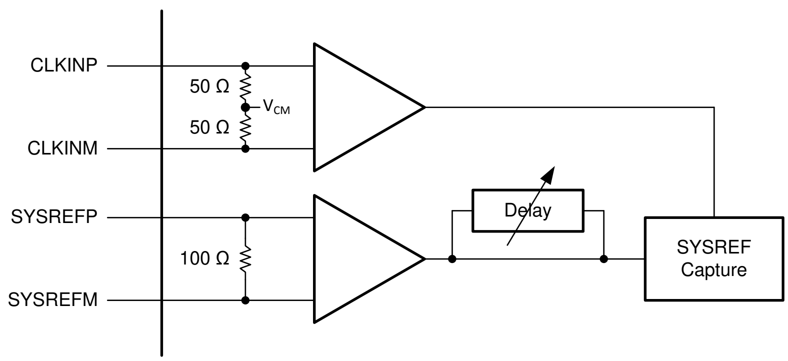


Figure 8-10. SYSREF Internal Circuit Diagram

8.3.3.1 Using SYSREF

The ADC32RF8x uses SYSREF information to reset the clock divider, the NCO phase, and the LMFC counter of the JESD interface. The device provides flexibility to provide SYSREF information either from dedicated pins or through SPI register bits. As shown in Figure 8-11, SYSREF is asserted by a low-to-high transition on the SYSREF pins or a 0-to-1 change in the ASSERT SYSREF REG bit when using SPI registers.

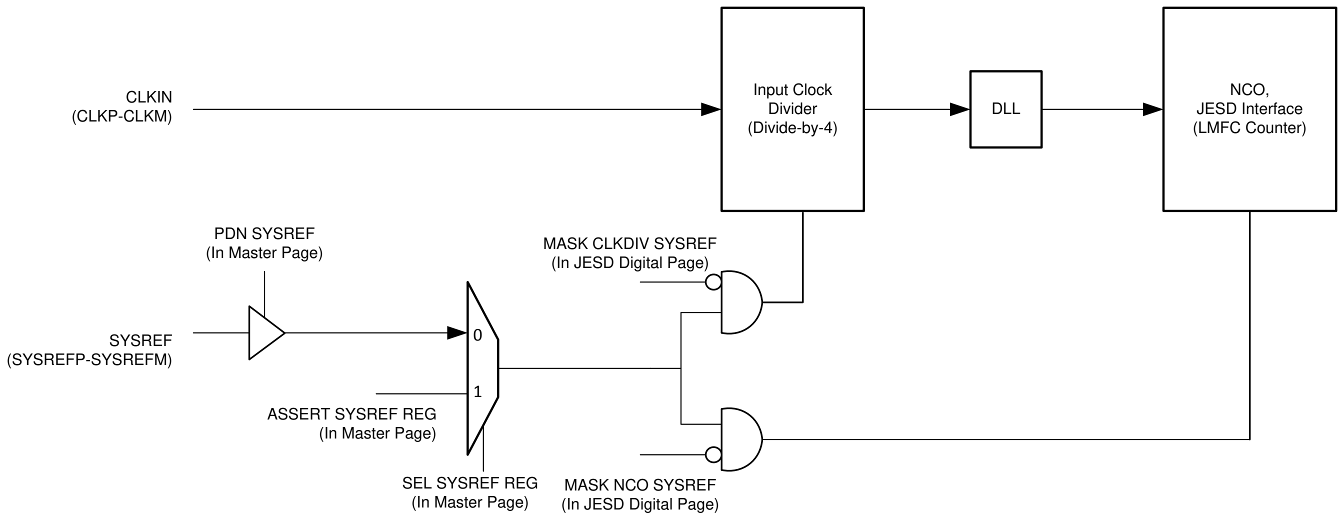


Figure 8-11. Using SYSREF to Reset the Clock Divider, the NCO, and the LMFC Counter

The ADC32RF8x samples the SYSREF signal on the input clock rising edge. Required setup and hold time are listed in the *Section 6.10* table. The input clock divider gets reset each time that SYSREF is asserted, whereas the NCO phase and the LMFC counter of the JESD interface are reset on each SYSREF assertion after disregarding the first two assertions, as shown in Table 8-1.

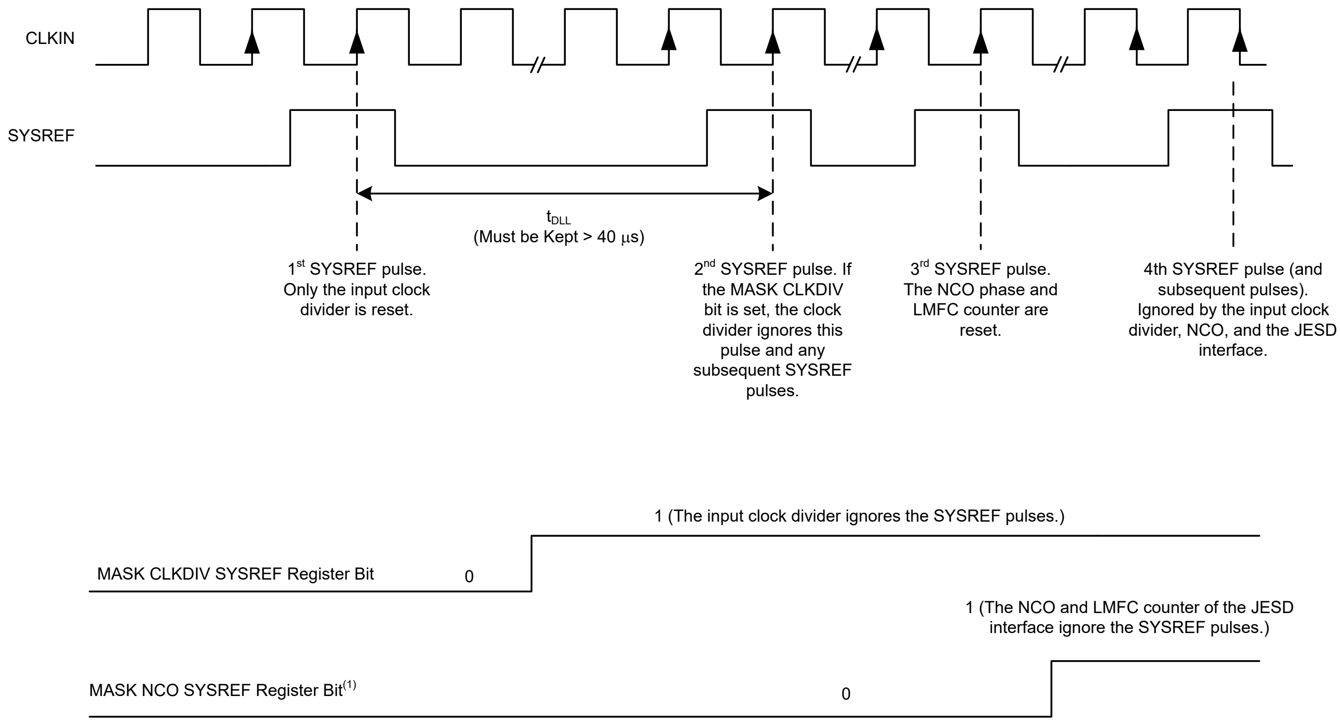
Table 8-1. Asserting SYSREF

SYSREF ASSERTION INDEX	ACTION		
	INPUT CLOCK DIVIDER	NCO PHASE	LMFC COUNTER
1	Gets reset	Does not get reset	Does not get reset
2	Gets reset	Does not get reset	Does not get reset
3	Gets reset	Gets reset	Gets reset
4 and onwards	Gets reset	Gets reset	Gets reset

The SYSREF use-cases can be classified broadly into two categories:

1. SYSREF is applied as aperiodic multi-shot pulses.

   Figure 8-12 shows a case when only a counted number of pulses are applied as SYSREF to the ADC.



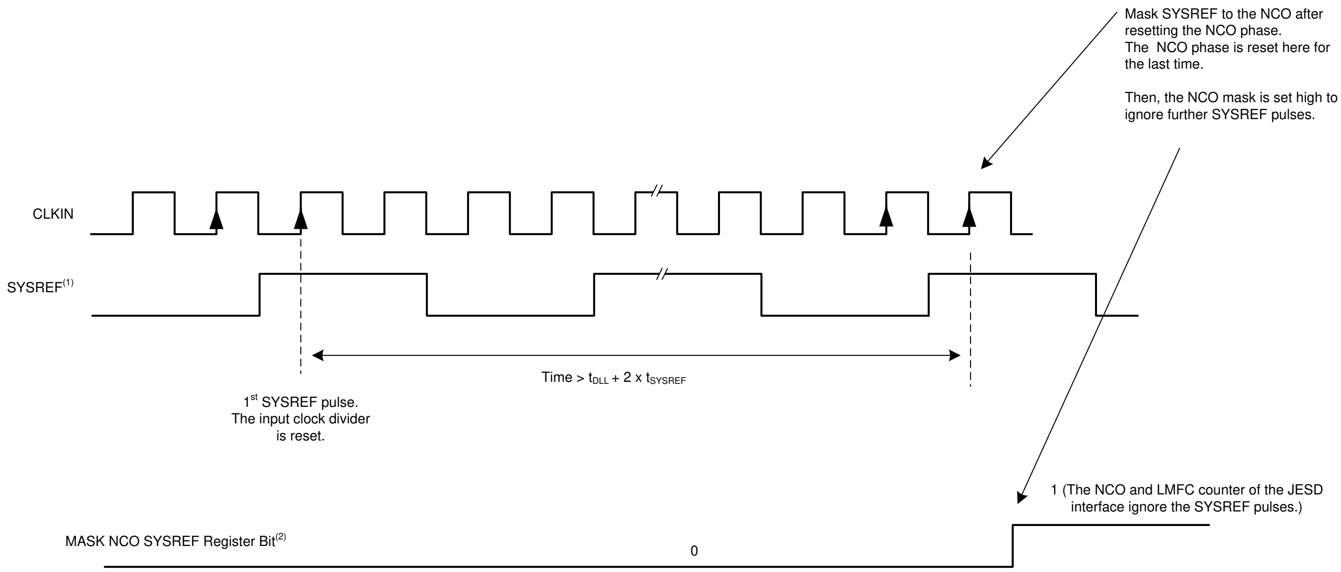
Alternatively, the SYSREF buffer can be powered down with the PDN SYSREF bit.

Figure 8-12. SYSREF Used as Aperiodic, Finite Number of Pulses

After the first SYSREF pulse is applied, allow the DLL in the clock path to settle by waiting for the t_{DLL} time (> 40 µs) before applying the second pulse. During this time, mask the SYSREF going to the input clock divider by setting the MASK CLKDIV SYSREF bit so that the divider output phase remains stable. The NCO phase and LMFC counter are reset on the third SYSREF pulse. After the third SYSREF pulse, the SYSREF going to the NCO and JESD block can be disabled by setting the MASK NCO SYSREF bit to avoid any unwanted resets.

2. SYSREF is applied as a periodic pulse.

   Figure 8-13 shows how SYSREF can be applied as a continuous periodic waveform.



A. t_{SYSREF} is a period of the SYSREF waveform.
B. Alternatively, the SYSREF buffer can be powered down using the PDN SYSREF bit.

Figure 8-13. SYSREF Used as a Periodic Waveform

After applying the SYSREF signal, DLL must be allowed to lock, and the NCO phase and LMFC counter must be allowed to reset by waiting for at least the t_{DLL} (40 µs) + 2 × t_{SYSREF} time. Then, the SYSREF going to the NCO and JESD can be masked by setting the MASK NCO SYSREF register bit.

8.3.3.2 Frequency of the SYSREF Signal

When SYSREF is a periodic signal, its frequency is required to be a sub-harmonic of the internal local multi-frame clock (LMFC) frequency, as described in Equation 1. The LMFC frequency is determined by the selected decimation, frames per multi-frame setting (K), samples per frame (S), and device input clock frequency.

$$\text{SYSREF} = \text{LMFC} / N \tag{1}$$

where

- N is an integer value (1, 2, 3, and so forth)

In order for the interleaving correction engine to synchronize properly, the SYSREF frequency must also be a multiple of f_S / 64. Table 8-2 provides a summary of the valid LMFC clock settings.

Table 8-2. . SYSREF and LMFC Clock Frequency

OPERATING MODE	LMFS SETTING	LMFC CLOCK FREQUENCY	SYSREF FRQUENCY
Decimation	Various	f_S (1) / (D × S(4) × K(3))	f_S / (N × LCM(2) (64, D(5) × S × K))

(1) f_S = sampling (device) clock frequency.
(2) LCM = least-common multiple.
(3) K = number of frames per multi-frame.
(4) S = samples per frame.
(5) D = decimation ratio.

The SYSREF signal is recommended to be a low-frequency signal less than 5 MHz in order to reduce coupling to the signal path both on the printed circuit board (PCB) as well as internal to the device.

Example: f_S = 2949.12 MSPS, Divide-by-4 (LMFS = 8411), K = 16

SYSREF = 2949.12 MSPS / LCM (4 ,64, 16) = 46.08 MHz / N

Operate SYSREF at 2.88 MHz (effectively divide-by-1024, N = 16)

For proper device operation, disable the SYSREF signal after the JESD synchronization is established.

8.3.4 DDC Block

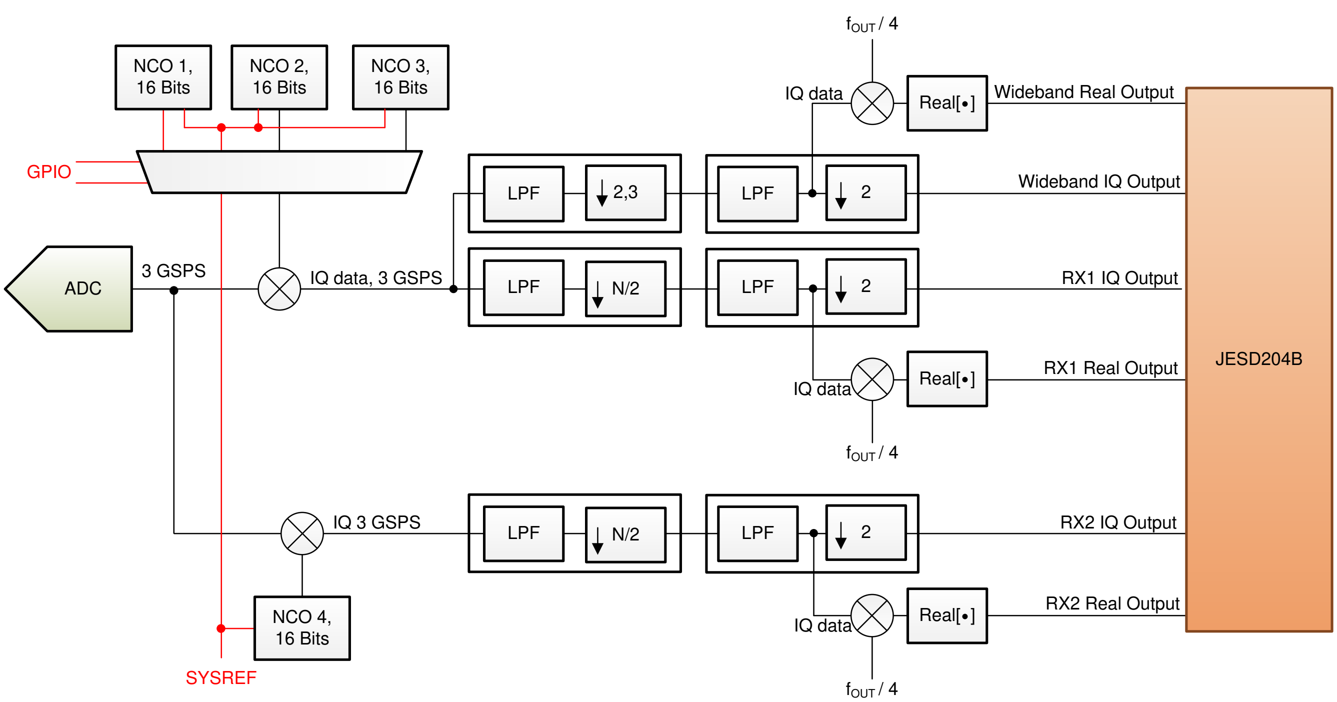
The ADC32RF8x provides a sophisticated on-chip, digital down converter (DDC) block that can be controlled through SPI register settings and the general-purpose input/output (GPIO) pins. The DDC block supports two basic operating modes: receiver (RX) mode with single- or dual-band DDC and wide-bandwidth observation receiver mode.

Note that the ADC32RF80 and ADC32RF83 are identical devices except the fact that the ADC32RF83 offers only single-band DDC option whereas the ADC32RF80 offers both single-band and dual-band DDC options, as shown in Table 8-3.

Table 8-3. DDC Option Availability

DDC OPTION	AVAILABILITY IN DEVICE
Wide-band DDC	ADC32RF80, ADC32RF83
Single-band DDC	ADC32RF80, ADC32RF83
Dual-band DDC	ADC32RF80 only

Each ADC channel is followed by two DDC chains consisting of the digital filter along with a complex digital mixer with a 16-bit numerically-controlled oscillator (NCO), as shown in Figure 8-14. The NCOs allow accurate frequency tuning within the Nyquist zone prior to the digital filtering. One DDC chain is intended for supporting a dual-band DDC configuration in receiver mode and the second DDC chain supports the wide-bandwidth output option for the observation configuration. At any given time, either the single-band DDC, the dual-band DDC, or the wideband DDC can be enabled. Furthermore, three different NCO frequencies can be selected on that path and are quickly switched using the SPI or the GPIO pins to enable wide-bandwidth observation in a multi-band application.



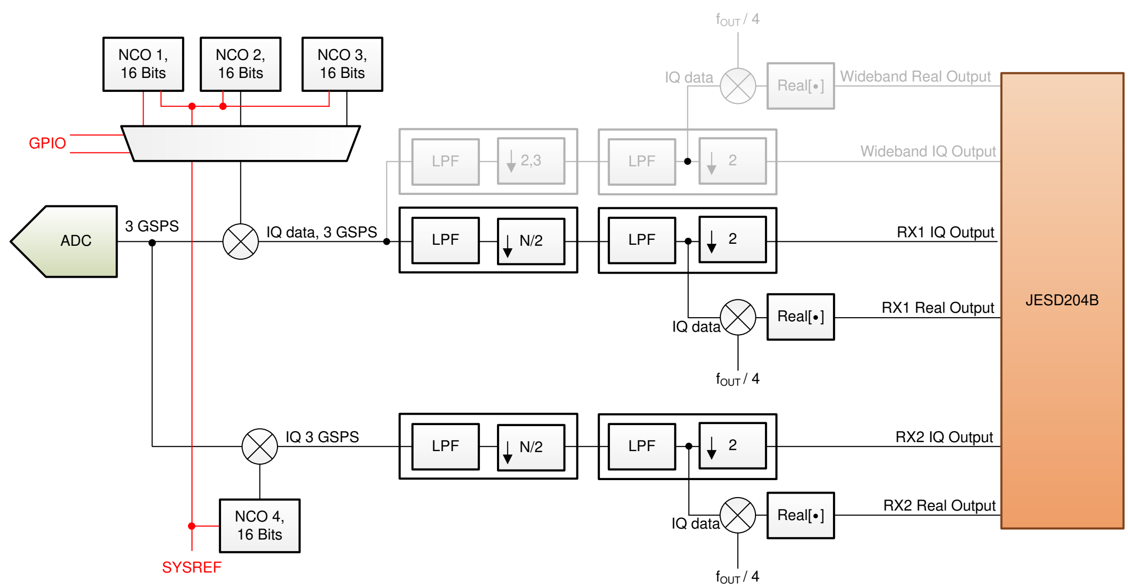
Red traces show SYSREF going to the NCO blocks.

Figure 8-14. DDC Chains Overview (One ADC Channel Shown)

Additionally, the decimation filter block provides the option to convert the complex output back to real format at twice the decimated, complex output rate. The filter response with a real output is identical to a complex output. The band is centered in the middle of the Nyquist zone (mixed with f_{OUT} / 4) based on a final output data rate of f_{OUT}.

8.3.4.1 Operating Mode: Receiver

In receiver mode, the DDC block can be configured to single- or dual-band operation, as shown in Figure 8-15. Both DDC chains use the same decimation filter setting and the available options are discussed in the *Section 8.3.4.3* section. The decimation filter setting also directly affects the interface rate and number of lanes of the JESD204B interface.

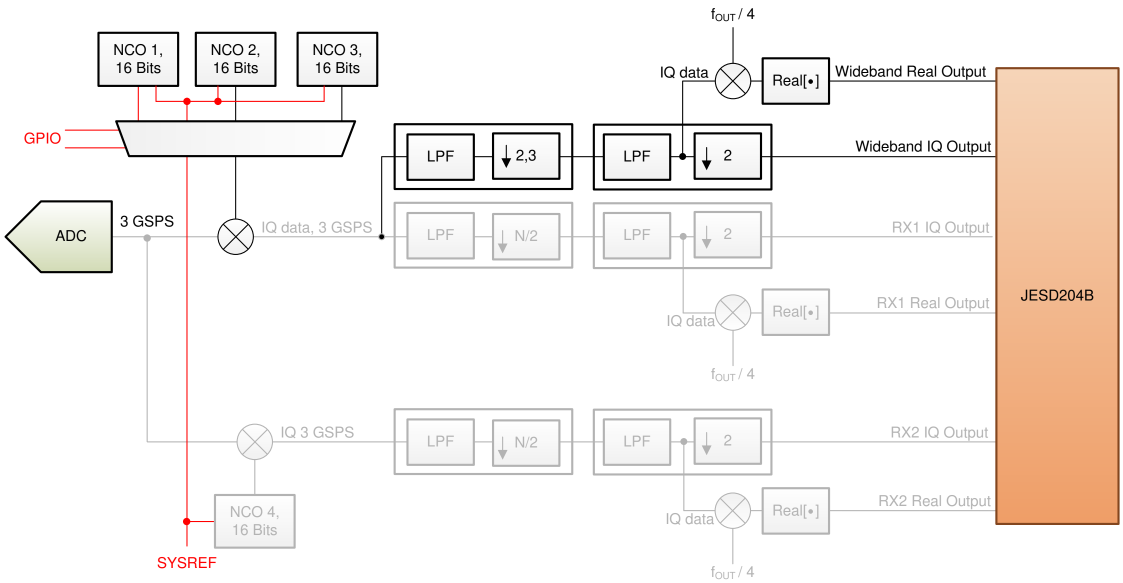


Red traces show SYSREF going to the NCO blocks.

Figure 8-15. Decimation Filter Option for Single- or Dual-Band Operation

8.3.4.2 Operating Mode: Wide-Bandwidth Observation Receiver

This mode is intended for using a DDC with a wide bandwidth output, but for multiple bands. This mode uses a single DDC chain where up to three NCOs can be used to perform wide-bandwidth observation in a multi-band environment, as shown in Figure 8-16. The three NCOs can be switched dynamically using either the GPIO pins or an SPI command. All three NCOs operate continuously to ensure phase continuity; however, when the NCO is switched, the output data are invalid until the decimation filters are completely flushed with data from the new band.



Red traces show SYSREF going to the NCO blocks.

Figure 8-16. Decimation Filter Implementation for Single-Band and Wide-Bandwidth Mode

8.3.4.3 Decimation Filters

The stop-band rejection of the decimation filters is approximately 90 dB with a pass-band bandwidth of approximately 80%. Table 8-4 gives an overview of the pass-band bandwidth depending on decimation filter setting and ADC sampling rate.

Table 8-4. Decimation Filter Summary and Maximum Available Output Bandwidth

DECIMATION SETTING	NO. OF DDCS AVAILABLE PER CHANNEL	NOMINAL PASSBAND GAIN	BANDWIDTH		ADC SAMPLE RATE = N MSPS		ADC SAMPLE RATE = 3 GSPS	
			3 dB (%)	1 dB (%)	OUTPUT RATE (MSPS) PER BAND	OUTPUT BANDWIDTH (MHz) PER BAND	COMPLEX OUTPUT RATE (MSPS) PER BAND	OUTPUT BANDWIDTH (MHz) PER BAND
Divide-by-4 complex	1	–0.4 dB	90.9	86.8	N / 4 complex	0.4 × N / 2	750	600
Divide-by-6 complex	1	–0.65 dB	90.6	86.1	N / 6 complex	0.4 × N / 3	500	400
Divide-by-8 complex	2	–0.27 dB	91.0	86.8	N / 8 complex	0.4 × N / 4	375	300
Divide-by-9 complex	2	–0.45 dB	90.7	86.3	N / 9 complex	0.4 × N / 4.5	333.3	266.6
Divide-by-10 complex	2	–0.58 dB	90.7	86.3	N / 10 complex	0.4 × N / 5	300	240
Divide-by-12 complex	2	–0.55 dB	90.7	86.4	N / 12 complex	0.4 × N / 6	250	200
Divide-by-16 complex	2	–0.42 dB	90.8	86.4	N / 16 complex	0.4 × N / 8	187.5	150

Table 8-4. Decimation Filter Summary and Maximum Available Output Bandwidth (continued)

DECIMATION SETTING	NO. OF DDCS AVAILABLE PER CHANNEL	NOMINAL PASSBAND GAIN	BANDWIDTH		ADC SAMPLE RATE = N MSPS		ADC SAMPLE RATE = 3 GSPS	
			3 dB (%)	1 dB (%)	OUTPUT RATE (MSPS) PER BAND	OUTPUT BANDWIDTH (MHz) PER BAND	COMPLEX OUTPUT RATE (MSPS) PER BAND	OUTPUT BANDWIDTH (MHz) PER BAND
Divide-by-18 complex	2	–0.83 dB	91.2	87.0	N / 18 complex	0.4 × N / 9	166.6	133
Divide-by-20 complex	2	–0.91 dB	91.2	87.0	N / 20 complex	0.4 × N / 10	150	120
Divide-by-24 complex	2	–0.95 db	91.1	86.9	N / 24 complex	0.4 × N / 12	125	100
Divide-by-32 complex	2	–0.78 dB	91.1	86.8	N / 32 complex	0.4 × N / 16	93.75	75

A dual-band example with a divide-by-8 complex is shown in Figure 8-17.

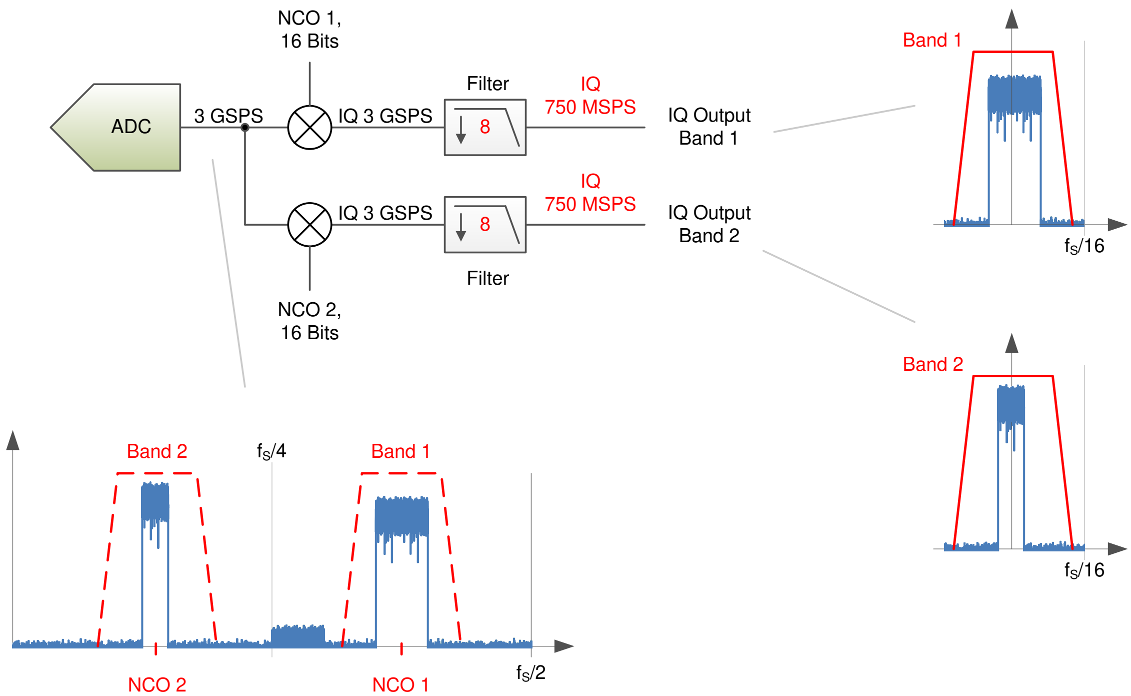


Figure 8-17. Dual-Band Example

The decimation filter responses normalized to the ADC sampling clock are illustrated in Figure 8-17 to Figure 8-40 and can be interpreted as follows:

Each figure contains the filter pass-band, transition bands, and alias bands, as shown in Figure 8-18. The x-axis in Figure 8-18 shows the offset frequency (after the NCO frequency shift) normalized to the ADC sampling clock frequency.

For example, in the divide-by-4 complex, the output data rate is an f_S / 4 complex with a Nyquist zone of f_S / 8 or 0.125 × f_S. The transition band is centered around 0.125 × f_S and the alias transition band is centered at 0.375 × f_S. The alias bands that alias on top of the wanted signal band are centered at 0.25 × f_S and 0.5 × f_S (and are colored in red).

The decimation filters of the ADC32RF8x provide greater than 90-dB attenuation for the alias bands.

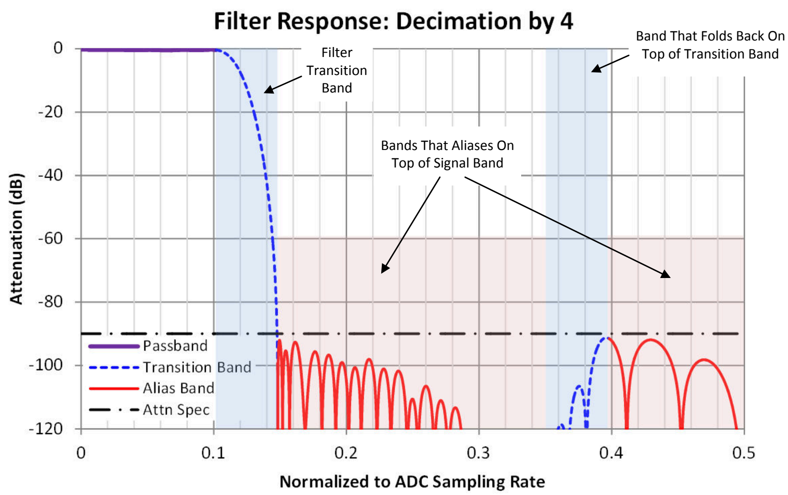


Figure 8-18. Interpretation of the Decimation Filter Plots

8.3.4.3.1 Divide-by-4

Peak-to-peak pass-band ripple: approximately 0.22 dB

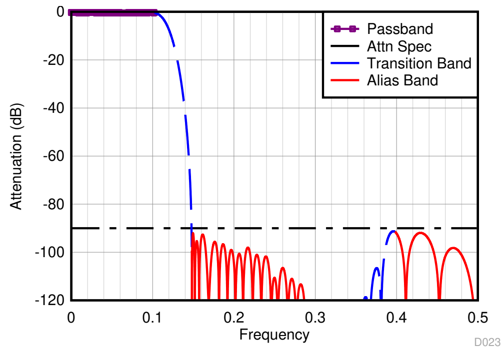


Figure 8-19. Divide-by-4 Filter Response

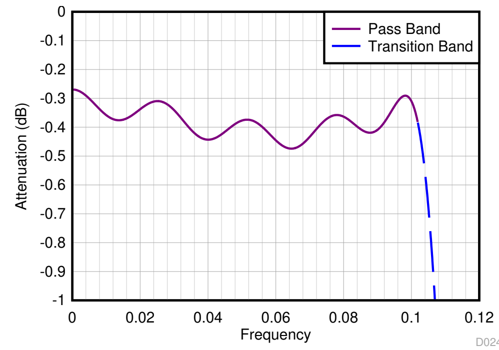


Figure 8-20. Divide-by-4 Filter Response (Zoomed)

8.3.4.3.2 Divide-by-6

Peak-to-peak pass-band ripple: approximately 0.38 dB

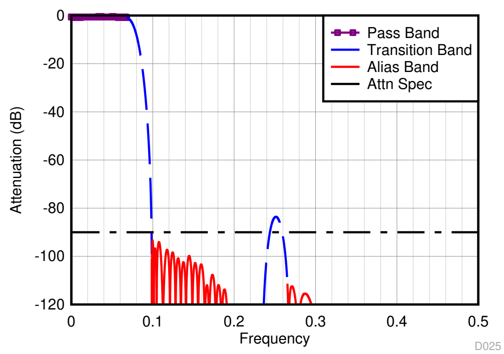


Figure 8-21. Divide-by-6 Filter Response

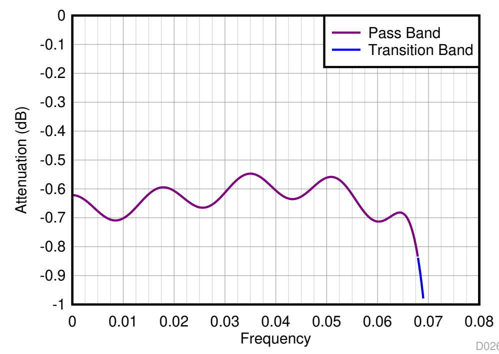


Figure 8-22. Divide-by-6 Filter Response (Zoomed)

8.3.4.3.3 Divide-by-8

Peak-to-peak pass-band ripple: approximately 0.25 dB

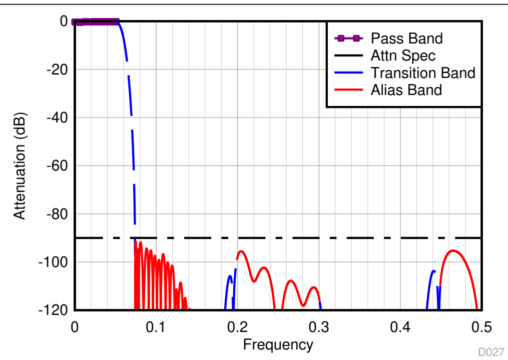


Figure 8-23. Divide-by-8 Filter Response

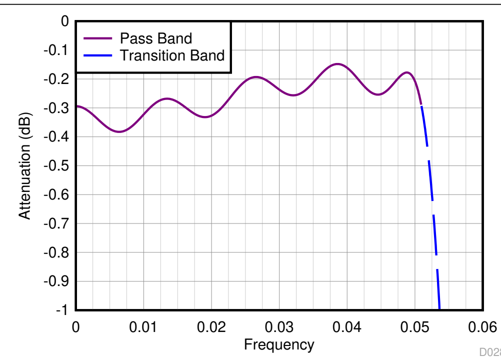


Figure 8-24. Divide-by-8 Filter Response (Zoomed)

8.3.4.3.4 Divide-by-9

Peak-to-peak pass-band ripple: approximately 0.39 dB

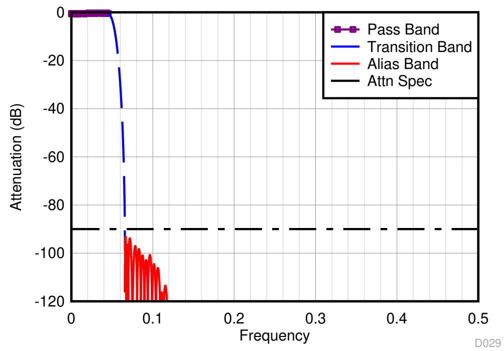


Figure 8-25. Divide-by-9 Filter Response

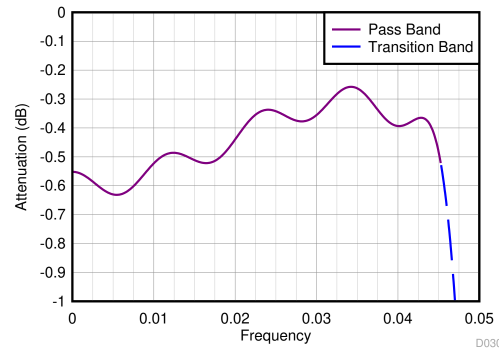


Figure 8-26. Divide-by-9 Filter Response (Zoomed)

8.3.4.3.5 Divide-by-10

Peak-to-peak pass-band ripple: approximately 0.39 dB

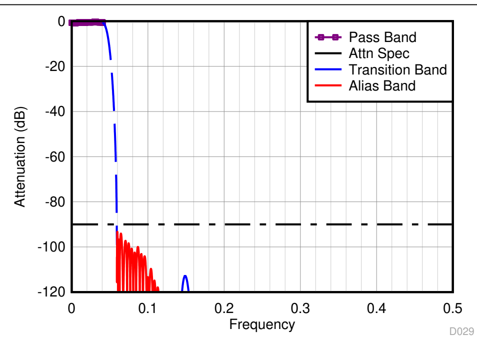


Figure 8-27. Divide-by-10 Filter Response

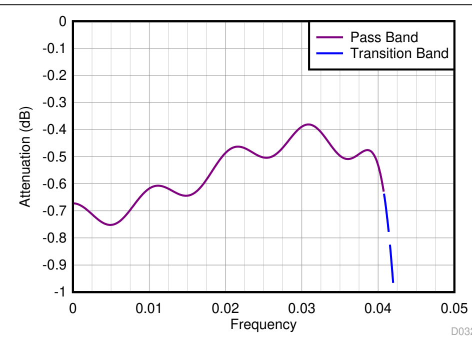


Figure 8-28. Divide-by-10 Filter Response (Zoomed)

8.3.4.3.6 Divide-by-12

Peak-to-peak pass-band ripple: approximately 0.36 dB

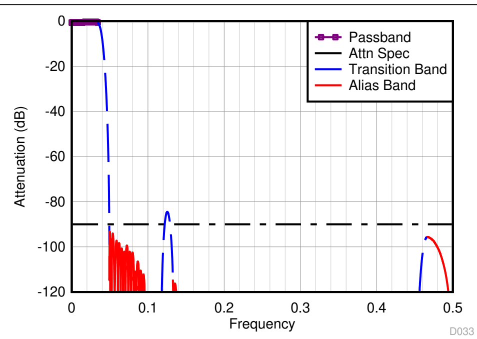


Figure 8-29. Divide-by-12 Filter Response

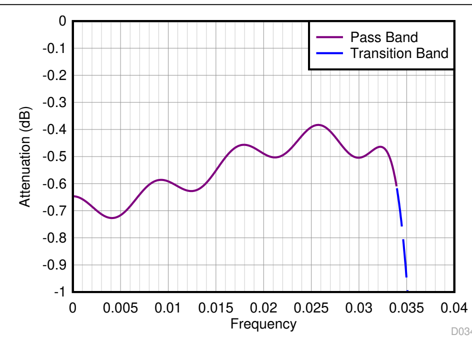


Figure 8-30. Divide-by-12 Filter Response (Zoomed)

8.3.4.3.7 Divide-by-16

Peak-to-peak pass-band ripple: approximately 0.29 dB

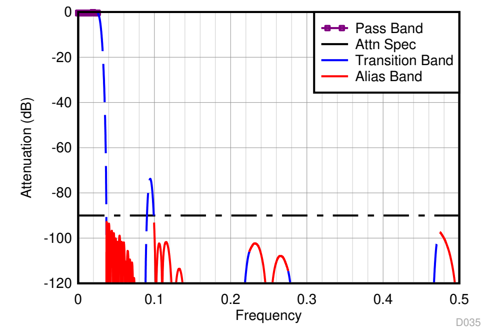


Figure 8-31. Divide-by-16 Filter Response

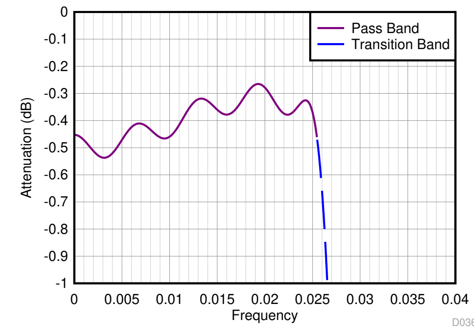


Figure 8-32. Divide-by-16 Filter Response (Zoomed)

8.3.4.3.8 Divide-by-18

Peak-to-peak pass-band ripple: approximately 0.33 dB

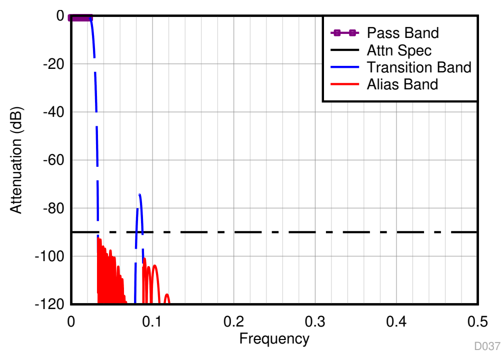


Figure 8-33. Divide-by-18 Filter Response

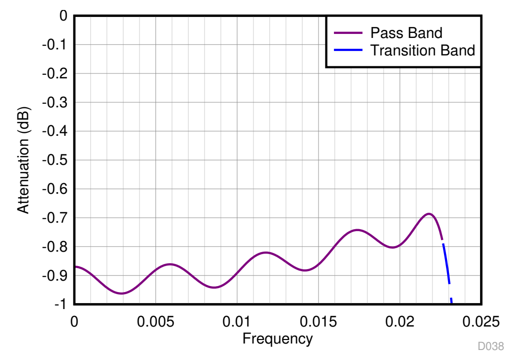


Figure 8-34. Divide-by-18 Filter Response (Zoomed)

8.3.4.3.9 Divide-by-20

Peak-to-peak pass-band ripple: approximately 0.32 dB

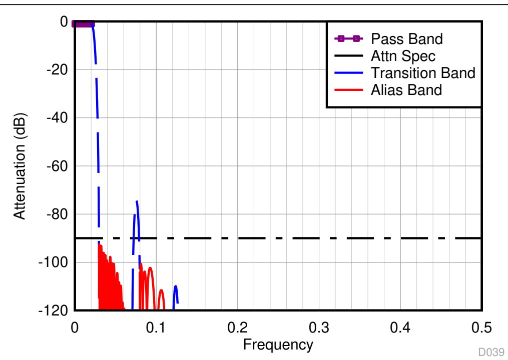


Figure 8-35. Divide-by-20 Filter Response

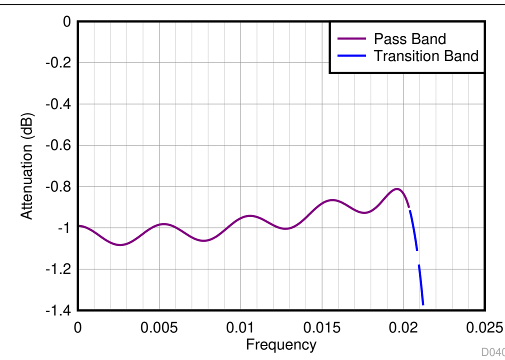


Figure 8-36. Divide-by-20 Filter Response (Zoomed)

8.3.4.3.10 Divide-by-24

Peak-to-peak pass-band ripple: approximately 0.30 dB

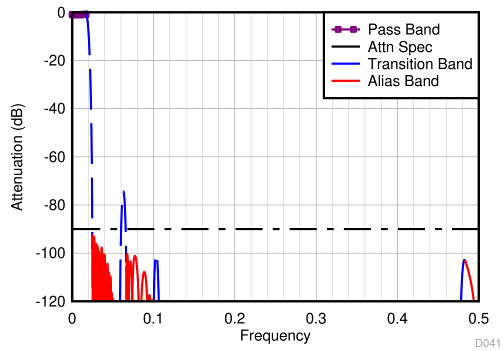


Figure 8-37. Divide-by-24 Filter Response

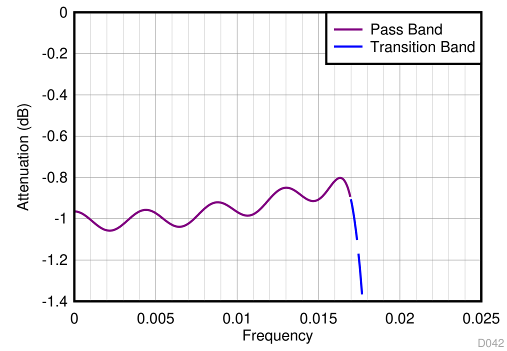


Figure 8-38. Divide-by-24 Filter Response (Zoomed)

8.3.4.3.11 Divide-by-32

Peak-to-peak pass-band ripple: approximately 0.24 dB

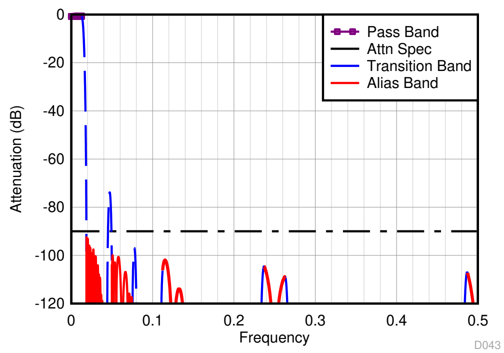


Figure 8-39. Divide-by-32 Filter Response

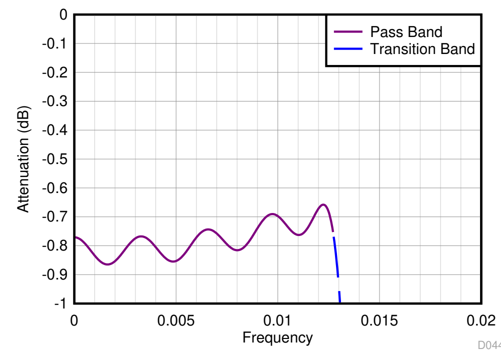


Figure 8-40. Divide-by-32 Filter Response (Zoomed)

8.3.4.3.12 Latency with Decimation Options

Device latency in 12-bit bypass mode (with LMFS = 8224) is 424 clock cycles. When the DDC option is used, latency increases as a result of decimation filters, as described in Table 8-5.

Table 8-5. Latency with different Decimation options

DECIMATION OPTION	TOTAL LATENCY, DEVICE CLOCK CYCLES
Divide-by-4	516
Divide-by-6	746
Divide-by-8	621
Divide-by-9	763.5
Divide-by-10	811
Divide-by-12	897
Divide-by-16	1045
Divide-by-18	1164
Divide-by-20	1256
Divide-by-24	1443
Divide-by-32	1773

8.3.4.4 Digital Multiplexer (MUX)

The ADC32RF8x supports a mode where the output data of the ADC channel A can be routed internally to the digital blocks of both channel A and channel B. The ADC channel B can be powered down as shown in Figure 8-41. In this manner, the ADC32RF8x can be configured as a single-channel ADC with up to four independent DDC chains or two wideband DDC chains. All decimation filters and JESD204B format configurations are identical to the two ADC channel operation.

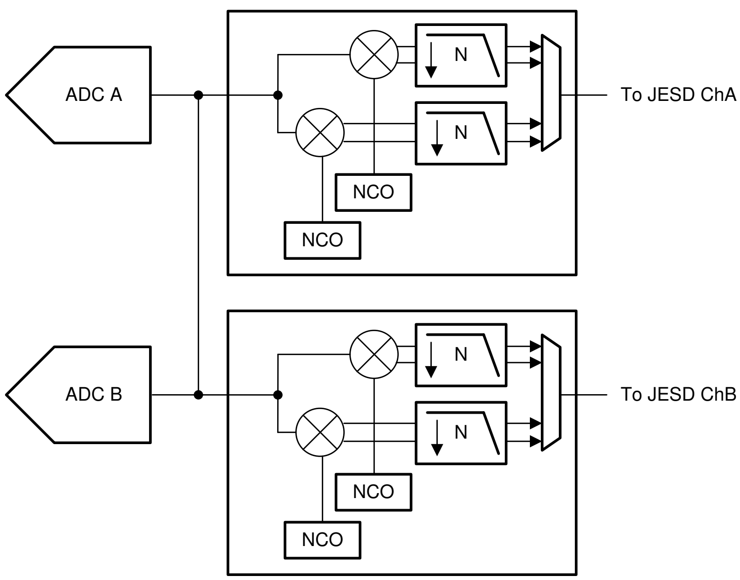


Figure 8-41. Digital Multiplexer Option

8.3.4.5 Numerically-Controlled Oscillators (NCOs) and Mixers

The ADC32RF8x is equipped with three independent, complex NCOs per ADC channel. The oscillator generates a complex exponential sequence, as shown in Equation 2.

$$x[n] = e^{-j\omega n} \quad (2)$$

where

- frequency (ω) is specified as a signed number by the 16-bit register setting

The complex exponential sequence is multiplied by the real input from the ADC to mix the desired carrier down to 0 Hz.

Each ADC channel has two DDCs. The first DDC has three NCOs and the second DDC has one NCO. The first DDC can dynamically select one of the three NCOs based on the GPIO pin or SPI selection. In wide-bandwidth mode (lower decimation factors, for example, 4 and 6), there can only be one DDC for each ADC channel. The NCO frequencies can be programmed independently through the DDCx, NCO[4:1], and the MSB and LSB register settings.

The NCO frequency setting is set by the 16-bit register value given by Equation 3:

$$f_{NCO} = \frac{DDCxNCOy \times f_S}{2^{16}} \quad (3)$$

where

- x = 0, 1
- y = 1 to 4

For example:

If f_S = 2949.12 MSPS, then the NCO register setting = 38230 (decimal).

Thus, f_{NCO} is defined by Equation 4:

$$f_{NCO} = 38230 \times \frac{2949.12\ \text{MSPS}}{2^{16}} = 1720.35\ \text{MHz} \quad (4)$$

Any register setting changes that occur after the JESD204B interface is operational results in a non-deterministic NCO phase. If a deterministic phase is required, the JESD204B interface must be reinitialized after changing the register setting.

8.3.5 NCO Switching

The first DDC (DDC0) on each ADC channel provides three different NCOs that can be used for phase-coherent frequency hopping. This feature is available in both single-band and dual-band mode, but only affects DDC0.

The NCOs can be switched through an SPI control or by using the GPIO pins with the register configurations shown in Table 8-6 for channel A (50xxh) and channel B (58xxh). The assignment of which GPIO pin to use for INSEL0 and INSEL1 is done based on Table 8-7, using registers 5438h and 5C38h. The NCO selection is done based on the logic selection on the GPIO pins; see Table 8-8 and Figure 8-42.

Table 8-6. NCO Register Configurations

REGISTER	ADDRESS	DESCRIPTION
NCO CONTROL THROUGH GPIO PINS		
NCO SEL pin	500Fh, 580Fh	Selects the NCO control through the SPI (default) or a GPIO pin.
INSEL0, INSEL1	5438h, 5C38h	Selects which two GPIO pins are used to control the NCO.
NCO CONTROL THROUGH SPI CONTROL		
NCO SEL pin	500Fh, 580Fh	Selects the NCO control through the SPI (default) or a GPIO pin.
NCO SEL	5010h, 5810h	Selects which NCO to use for DDC0.

Table 8-7. GPIO Pin Assignment

INSELx[1:0] (Where x = 0 or 1)	GPIO PIN SELECTED
00	GPIO4
01	GPIO1
10	GPIO3

Table 8-7. GPIO Pin Assignment (continued)

INSELx[1:0] (Where x = 0 or 1)	GPIO PIN SELECTED
11	GPIO2

Table 8-8. NCO Selection

NCO SEL[1]	NCO SEL[0]	NCO SELECTED
0	0	NCO1
0	1	NCO2
1	0	NCO3
1	1	n/a

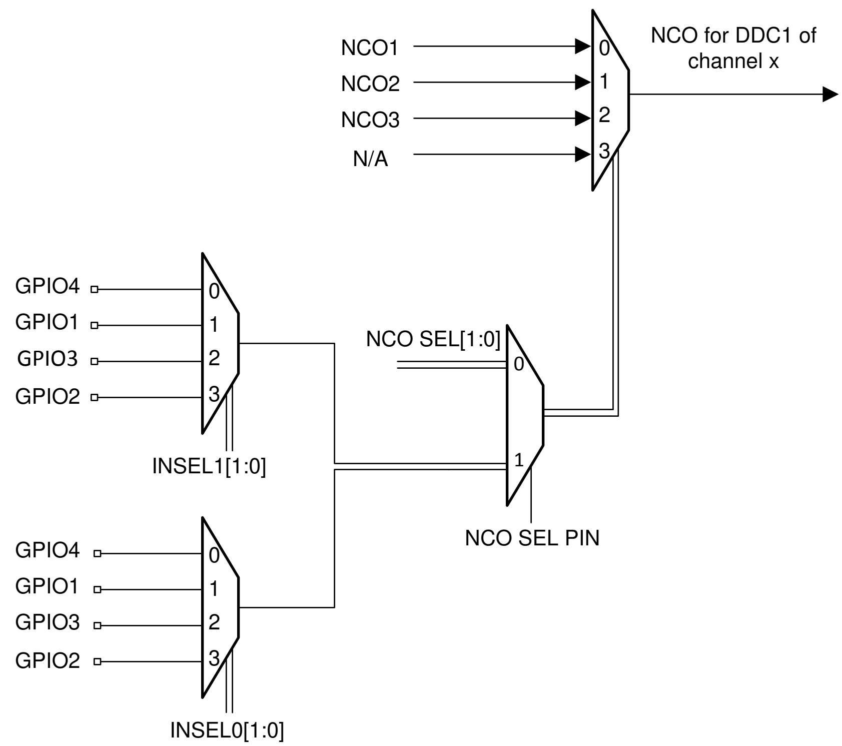


Figure 8-42. NCO Switching from GPIO and SPI

8.3.6 SerDes Transmitter Interface

Each 12.3-Gbps serializer, deserializer (SerDes) LVDS transmitter output requires ac-coupling between the transmitter and receiver. Terminate the differential pair with 100-Ω resistance (that is, two 50-Ω resistors) as close to the receiving device as possible to avoid unwanted reflections and signal degradation, as shown in Figure 8-43.

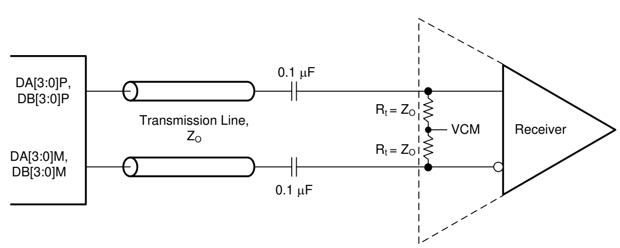


Figure 8-43. External Serial JESD204B Interface Connection

8.3.7 Eye Diagrams

Figure 8-44 and Figure 8-45 show the serial output eye diagrams of the ADC32RF8x at 5.0 Gbps and 12 Gbps against the JESD204B mask.

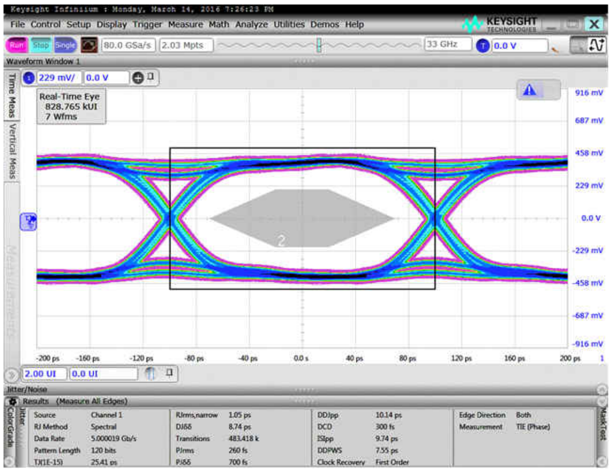


Figure 8-44. Data Eye at 5 Gbps

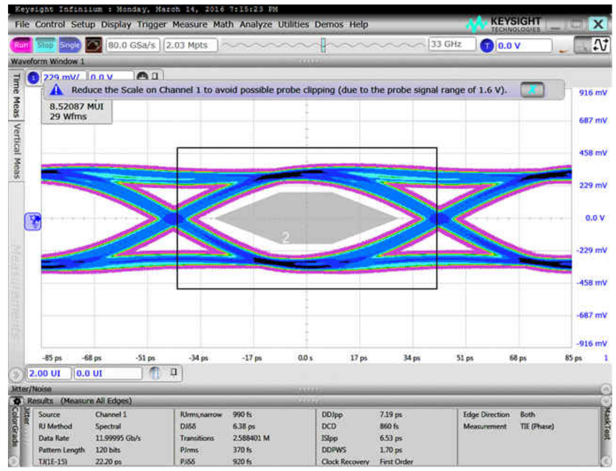


Figure 8-45. Data Eye at 12 Gbps

8.3.8 Alarm Outputs: Power Detectors for AGC Support

The GPIO pins can be configured as alarm outputs for channels A and B. The ADC32RF8x supports three different power detectors (an absolute peak power detector, crossing detector, and RMS power detector) as well as fast overrange from the ADC. The power detectors operate off the full-rate ADC output prior to the decimation filters.

8.3.8.1 Absolute Peak Power Detector

In this detector mode, the peak is computed over eight samples of the ADC output. Next, the peak for a block of N samples (N × S`) is computed over a programmable block length and then compared against a threshold to either set or reset the peak detector output (Figure 8-46 and Figure 8-47). There are two sets of thresholds and each set has two thresholds for hysteresis. The programmable DWELL-time counter is used for clearing the block detector alarm output.

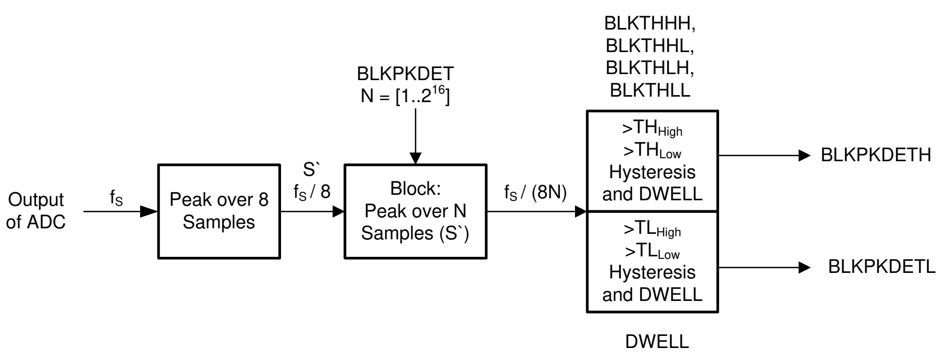


Figure 8-46. Peak Power Detector Implementation

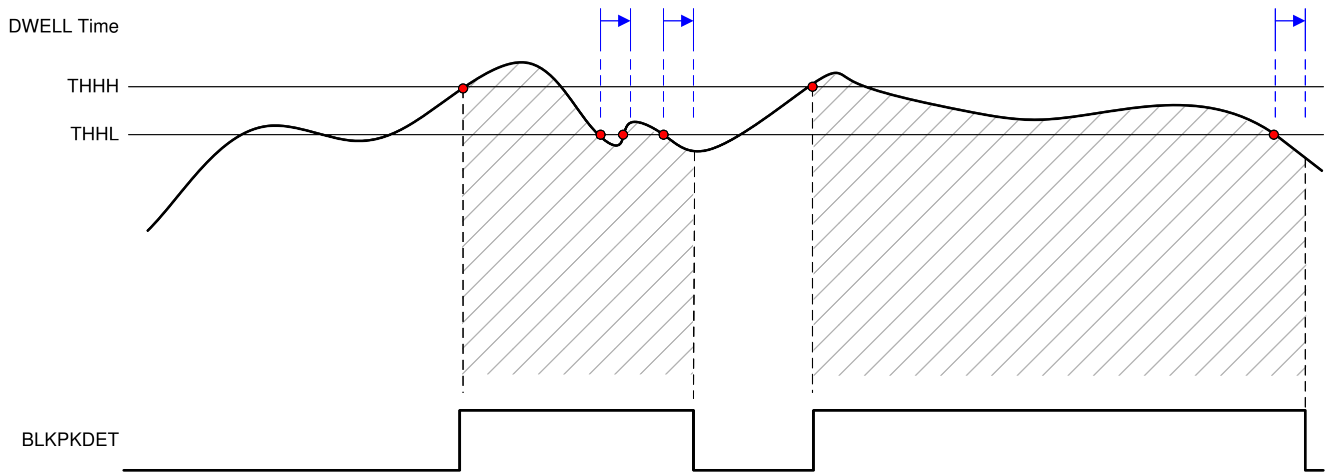


Figure 8-47. Peak Power Detector Timing Diagram

Table 8-9 shows the register configurations required to set up the absolute peak power detector. The detector operates in the f_S / 8 clock domain; one peak sample is calculated over eight actual samples.

The automatic gain control (AGC) modes can be configured separately for channel A (54xxh) and channel B (5Cxxh), although some registers are common in 54xxh (such as the GPIO pin selection).

Table 8-9. Registers Required for the Peak Power Detector

REGISTER	ADDRESS	DESCRIPTION
PKDET EN	5400, 5C00h	Enables peak detector
BLKPKDET	5401h, 5402h, 5403h, 5C01h, 5C02h, 5C03h	Sets the block length N of number of samples (S`). Number of actual ADC samples is 8x this value: N is 17 bits: 1 to 2^{16}.
BLKTHHH, BLKTHHL, BLKTHLH, BLKTHLL	5407h, 5408h, 5409h, 540Ah, 5C07h, 5C08h, 5C09h, 5C0Ah	Sets the different thresholds for the hysteresis function values from 0 to 256 (where 256 is equivalent to the peak amplitude). For example: if BLKTHHH is to –2 dBFS from peak, $10^{(-2/20)} \times 256 = 203$, then set 5407h and 5C07h = CBh.
DWELL	540Bh, 540Ch, 5C0Bh, 5C0Ch	When the computed block peak crosses the upper thresholds BLKTHHH or BLKTHLH, the peak detector output flags are set. In order to be reset, the computed block peak must remain continuously lower than the lower threshold (BLKTHHL or BLKTHLL) for the period specified by the DWELL value. This threshold is 16 bits and is specified in terms of f_S / 8 clock cycles.
OUTSEL GPIO[4:1]	5432h, 5433h, 5434h, 5435h	Connects the BLKPKDETH, BLKPKDETL alarms to the GPIO pins; common register.
IODIR	5437h	Selects the direction for the four GPIO pins; common register.
RESET AGC	542Bh, 5C2Bh	After configuration, reset the AGC module to start operation.

8.3.8.2 Crossing Detector

In this detector mode the peak is computed over eight samples of the ADC output. Next, the peak for a block of N samples (N × S`) is computed over a programmable block length and then the peak is compared against two sets of programmable thresholds (with hysteresis). The crossing detector counts how many f_S / 8 clock cycles that the block detector outputs are set high over a programmable time period and compares the counter value against the programmable thresholds. The alarm outputs are updated at the end of the time period, routed to the GPIO pins, and held in that state through the next cycle, as shown in Figure 8-48 and Figure 8-49. Alternatively, a 2-bit format can be used but (because the ADC32RF8x has four GPIO pins available) this feature uses all four pins for a single channel.

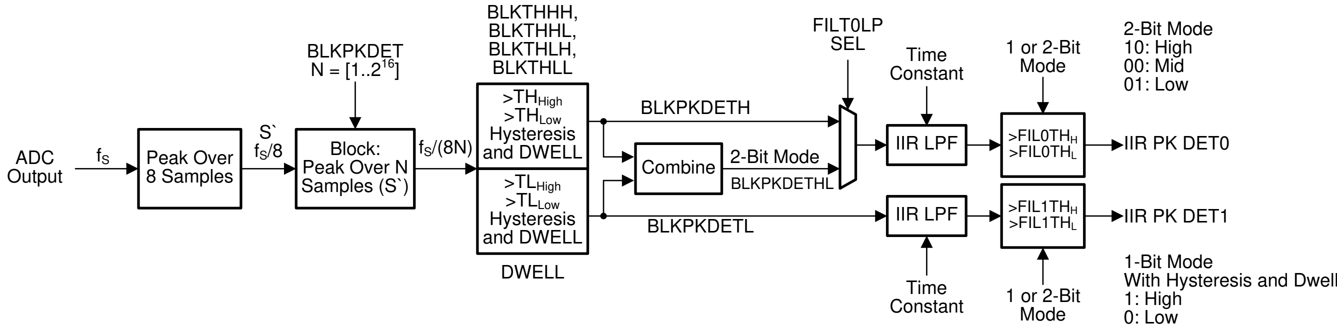


Figure 8-48. Crossing Detector Implementation

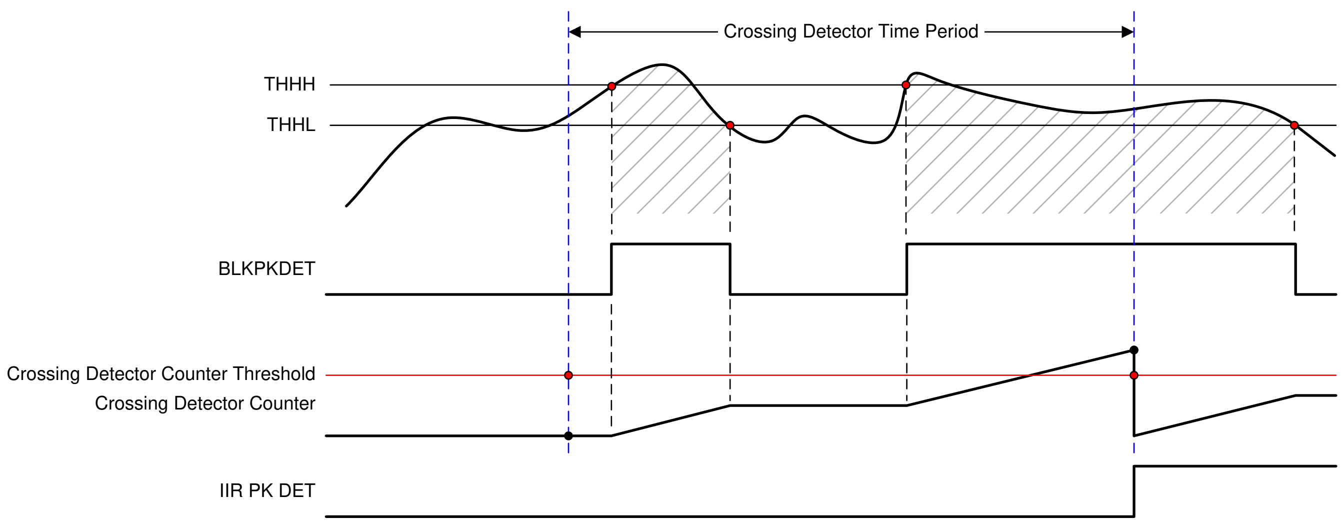


Figure 8-49. Crossing Detector Timing Diagram

Table 8-10 shows the register configurations required to set up the crossing detector. The detector operates in the
f_S / 8 clock domain. The AGC modes can be configured separately for channel A (54xxh) and channel B (5Cxxh), although some registers are common in 54xxh (such as the GPIO pin selection).

Table 8-10. Registers Required for the Crossing Detector Operation

REGISTER	ADDRESS	DESCRIPTION
PKDET EN	5400h, 5C00h	Enables peak detector
BLKPKDET	5401h, 5402h, 5403h, 5C01h, 5C02h, 5C03h	Sets the block length N of number of samples (S`). Number of actual ADC samples is 8x this value: N is 17 bits: 1 to 2^{16}.
BLKTHHH, BLKTHHL, BLKTHLH, BLKTHLL	5407h, 5408h, 5409h, 540Ah, 5C07h, 5C08h, 5C09h, 5C0Ah	Sets the different thresholds for the hysteresis function values from 0 to 256 (where 256 is equivalent to the peak amplitude). For example: if BLKTHHH is to –2 dBFS from peak, $10^{(-2 / 20)} \times 256 = 203$, then set 5407h and 5C07h = CBh.
FILT0LPSEL	540Dh, 5C0Dh	Select block detector output or 2-bit output mode as the input to the interrupt identification register (IIR) filter.
TIMECONST	540Eh, 540Fh, 5C0Eh, 5C0Fh	Sets the crossing detector time period for N = 0 to 15 as 2N × f_S / 8 clock cycles. The maximum time period is 32768 × f_S / 8 clock cycles (approximately 87 µs at 3 GSPS).
FIL0THH, FIL0THL, FIL1THH, FIL1THL	540Fh-5412h, 5C0Fh-5C12h, 5416h-5419h, 5C16h-5C19h	Comparison thresholds for the crossing detector counter. These thresholds are 16-bit thresholds in 2.14-signed notation. A value of 1 (4000h) corresponds to 100% crossings, a value of 0.125 (0800h) corresponds to 12.5% crossings.
DWELLIIR	541Dh, 541Eh, 5C1Dh, 5C1Eh	DWELL counter for the IIR filter hysteresis.
IIR0 2BIT EN, IIR1 2BIT EN	5413h, 54114h, 5C13h, 5C114h	Enables 2-bit output format for the crossing detector.
OUTSEL GPIO[4:1]	5432h, 5433h, 5434h, 5435h	Connects the IIRPKDET0, IIRPKDET1 alarms to the GPIO pins; common register.
IODIR	5437h	Selects the direction for the four GPIO pins; common register.
RESET AGC	542Bh, 5C2Bh	After configuration, reset the AGC module to start operation.

8.3.8.3 RMS Power Detector

In this detector mode the peak power is computed for a block of N samples over a programmable block length and then compared against two sets of programmable thresholds (with hysteresis).

The RMS power detector circuit provides configuration options, as shown in Figure 8-50. The RMS power value (1 or 2 bit) can be output onto the GPIO pins. In 2-bit output mode, two different thresholds are used whereas the 1-bit output provides one threshold together with hysteresis.

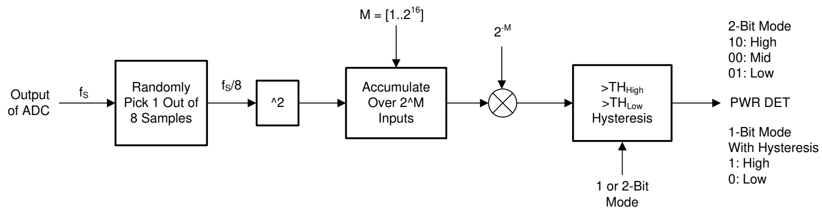


Figure 8-50. RMS Power Detector Implementation

Table 8-11 shows the register configurations required to set up the RMS power detector. The detector operates in the f_S / 8 clock domain. The AGC modes can be configured separately for channel A (54xxh) and channel B (5Cxxh), although some registers are common in 54xxh (such as the GPIO pin selection).

Table 8-11. Registers Required for Using the RMS Power Detector Feature

REGISTER	ADDRESS	DESCRIPTION
RMSDET EN	5420h, 5C20h	Enables RMS detector
PWRDETACCU	5421h, 5C21h	Programs the block length to be used for RMS power computation. The block length is defined in terms of f_S / 8 clocks. The block length can be programmed as 2^M with M = 0 to 16.
PWRDETH, PWRDETL	5422h, 5423h, 5424h, 5425h, 5C22h, 5C23h, 5C24h, 5C25h	The computed average power is compared against these high and low thresholds. One LSB of the thresholds represents 1 / 2^{16}. For example: is PWRDETH is set to –14 dBFS from peak, $[10^{(-14/20)}]^2 \times 2^{16}$ = 2609, then set 5422h, 5423h, 5C22h, 5C23h = 0A31h.
RMS2BIT EN	5427h, 5C27h	Enables 2-bit output format for the RMS detector output.
OUTSEL GPIO[4:1]	5432h, 5433h, 5434h, 5435h	Connects the PWRDET alarms to the GPIO pins; common register.
IODIR	5437h	Selects the direction for the four GPIO pins; common register.
RESET AGC	542Bh, 5C2Bh	After configuration, reset the AGC module to start operation.

8.3.8.4 GPIO AGC MUX

The GPIO pins can be used to control the NCO in wideband DDC mode or as alarm outputs for channel A and B. The GPIO pins can be configured through the SPI control to output the alarm from the peak power (1 bit), crossing detector (1 or 2 bit), faster overrange, or the RMS power output, as shown in Figure 8-51.

The programmable output MUX allows connecting any signal (including the NCO control) to any of the four GPIO pins. These pins can be configured as outputs (AGC alarm) or inputs (NCO control) through SPI programming.

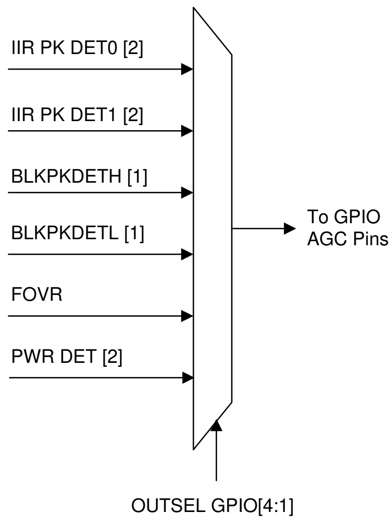


Figure 8-51. GPIO Output MUX Implementation

8.3.9 Power-Down Mode

The ADC32RF8x provides a lot of configurability for the power-down mode. Power-down can be enabled using the PDN pin or the SPI register writes.

8.3.10 ADC Test Pattern

The ADC32RF8x provides several different options to output test patterns instead of the actual output data of the ADC in order to simplify the serial interface and system debug of the JESD204B digital interface link. The output data path is shown in Figure 8-52.

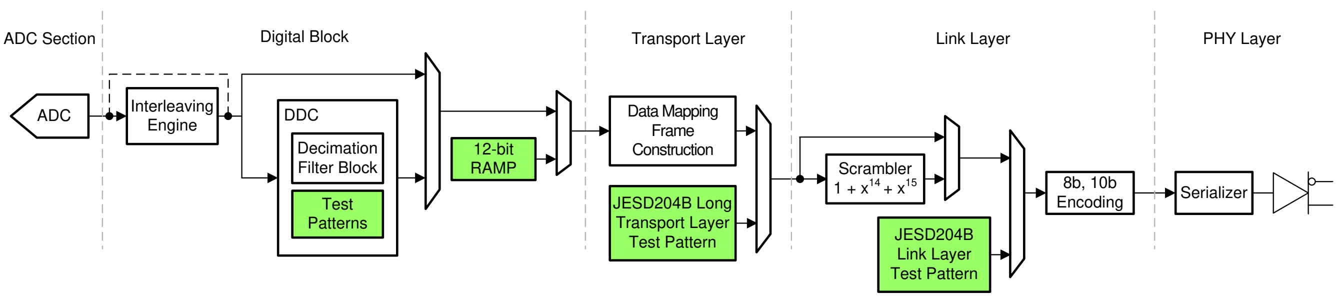


Figure 8-52. Test Pattern Generator Implementation

8.3.10.1 Digital Block

The ADC test pattern replaces the actual output data of the ADC. The test patterns listed in Table 8-12 are available when the DDC is enabled and located in register 37h of the decimation filter page. When programmed, the test patterns are output for each converter (M) stream. The number of converter streams per channel increases by 2 when complex (I, Q) output or dual-band DDC is selected. The test patterns can be synchronized for both ADC channels using the SYSREF signal.

Additionally, a 12-bit test pattern is also available.

Note

The number of converters increases in dual-band DDC mode and with a complex output.

Table 8-12. Test Pattern Options (Register 37h and 38h in Decimation Filter Page)

BIT	NAME	DEFAULT	DESCRIPTION
Address 37h, 38h (bits 7-0)	TEST PATTERN DDC1 I-DATA, TEST PATTERN DDC1 Q-DATA, TEST PATTERN DDC2 I-DATA, TEST PATTERN DDC2 Q-DATA,	0000	Test pattern outputs onI and Q stream of channel A and B when DDC option is chosen. 0000 = Normal operation using ADC output data 0001 = Outputs all 0s 0010 = Outputs all 1s 0011 = Outputs toggle pattern: output data are an alternating sequence of 10101010101010 and 01010101010101 0100 = Output digital ramp: output data increment by one LSB every clock cycle from code 0 to 65535 0110 = Single pattern: output data are a custom pattern 1 (75h and 76h) 0111 Double pattern: output data alternate between custom pattern 1 and custom pattern 2 1000 = Deskew pattern: output data are AAAAh 1001 = SYNC pattern: output data are FFFFh

8.3.10.2 Transport Layer

The transport layer maps the ADC output data into 8-bit octets and constructs the JESD204B frames using the LMFS parameters. Tail bits or 0's are added when needed. Alternatively, the JESD204B long transport layer test pattern can be substituted instead of the ADC data with the JESD frame, as shown in Table 8-13.

Table 8-13. Transport Layer Test Mode EN (Register 01h)

BIT	NAME	DEFAULT	DESCRIPTION
4	TESTMODE EN	0	Generates long transport layer test pattern mode according to section 5.1.6.3 of the JESD204B specification. 0 = Test mode disabled 1 = Test mode disabled

8.3.10.3 Link Layer

The link layer contains the scrambler and the 8b, 10b encoding of any data passed on from the transport layer. Additionally, the link layer also handles the initial lane alignment sequence that can be manually restarted.

The link layer test patterns are intended for testing the quality of the link (jitter testing and so forth). The test patterns do not pass through the 8b, 10b encoder and contain the options listed in Table 8-14.

Table 8-14. Link Layer Test Mode (Register 03h)

BIT	NAME	DEFAULT	DESCRIPTION
7-5	LINK LAYER TESTMODE	000	Generates a pattern according to section 5.3.3.8.2 of the JESD204B document. 000 = Normal ADC data 001 = D21.5 (high-frequency jitter pattern) 010 = K28.5 (mixed-frequency jitter pattern) 011 = Repeat the initial lane alignment (generates a K28.5 character and repeats lane alignment sequences continuously) 100 = 12-octet random pattern (RPAT) jitter pattern

Furthermore, a 2^{15} pseudo-random binary sequence (PRBS) can be enabled by setting up a custom test pattern (AAAAh) in the ADC section and running AAAAh through the 8b, 10b encoder with scrambling enabled.

8.4 Device Functional Modes

8.4.1 Device Configuration

The ADC32RF8x can be configured using a serial programming interface, as described in the *Section 8.4.3* section. In addition, the device has one dedicated parallel pin (PDN) for controlling the power-down modes.

8.4.2 JESD204B Interface

The ADC32RF8x supports device subclass 1 with a maximum output data rate of 12.5 Gbps for each serial transmitter.

An external SYSREF signal is used to align all internal clock phases and the local multiframe clock to a specific sampling clock edge. This alignment allows synchronization of multiple devices in a system and minimizes timing and alignment uncertainty. The SYNCB input is used to control the JESD204B SerDes blocks, as shown in Figure 8-53.

Depending on the ADC sampling rate, the JESD204B output interface can be operated with one, two, or four lanes per ADC channel. The JESD204B setup and configuration of the frame assembly parameters is controlled through the SPI interface.

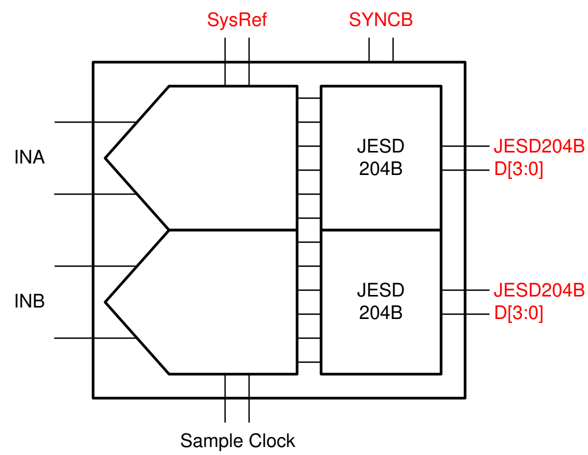


Figure 8-53. JESD Signal Overview

The JESD204B transmitter block consists of the transport layer, the data scrambler, and the link layer, as shown in Figure 8-54. The transport layer maps the ADC output data into the selected JESD204B frame data format and manages if the ADC output data or test patterns are transmitted. The link layer performs the 8b, 10b data encoding as well as the synchronization and initial lane alignment using the SYNC input signal. Optionally, data from the transport layer can be scrambled.

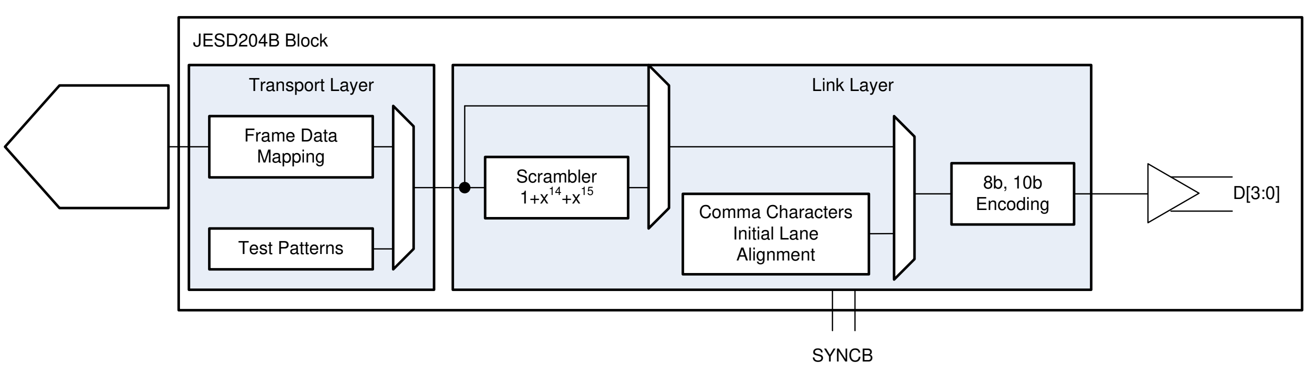


Figure 8-54. JESD Digital Block Implementation

8.4.2.1 JESD204B Initial Lane Alignment (ILA)

The receiving device starts the initial lane alignment process by deasserting the SYNCB signal. The SYNCB signal can be issued using the SYNCB input pins or by setting the proper SPI bits. When a logic low is detected on the SYNCB input, the ADC32RF8x starts transmitting comma (K28.5) characters to establish the code group synchronization, as shown in Figure 8-55.

When synchronization completes, the receiving device reasserts the SYNCB signal and the ADC32RF8x starts the initial lane alignment sequence with the next local multiframe clock boundary. The ADC32RF8x transmits four multiframes, each containing K frames (K is SPI programmable). Each of the multiframes contains the frame start and end symbols. The second multiframe also contains the JESD204 link configuration data.

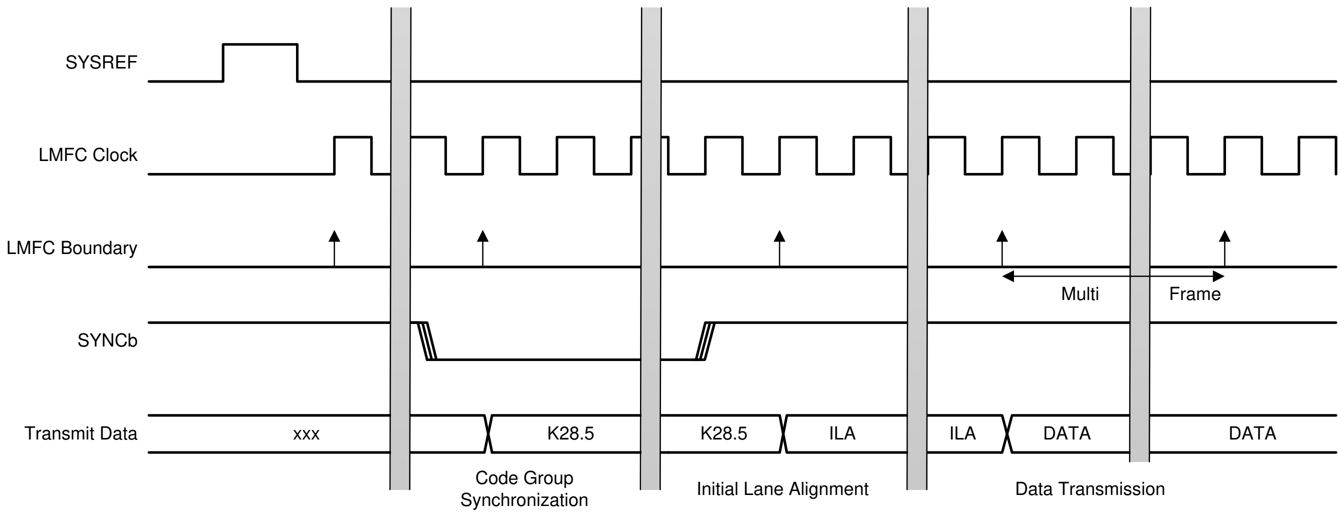


Figure 8-55. JESD Internal Timing Information

8.4.2.2 JESD204B Frame Assembly

The JESD204B standard defines the following parameters:

- F is the number of octets per frame clock period
- L is the number of lanes per link
- M is the number of converters for the device
- S is the number of samples per frame

8.4.2.3 JESD204B Frame Assembly with Decimation (Single-Band DDC): Complex Output

Table 8-15 lists the available JESD204B interface formats and valid ranges for the ADC32RF8x with decimation (single-band DDC) when using a complex output format. The ranges are limited by the SerDes line rate and the maximum ADC sample frequency. The sample alignment on the different lanes is shown in Table 8-16.

Table 8-15. JESD Mode Options: Single-Band Complex Output

DECIMATION SETTING (Complex)	NUMBER OF ACTIVE DDCS	L	M	F	S	PLL MODE	JESD MODE0	JESD MODE1	JESD MODE2	RATIO [fSerDes / f CLK (Gbps/ GSPS)]
Divide-by-4	1per channel	8	4	1	1	20X	1	1	0	2.5
		8	4	2	2	20X	1	0	0	
		4	4	2	1	40X	0	0	1	5
		4	4	4	2	40X	2	0	0	
Divide-by-6	1per channel	8	4	1	1	20X	1	1	0	1.67
		8	4	2	2	20X	1	0	0	
		4	4	2	1	40X	0	0	1	3.33
		4	4	4	2	40X	2	0	0	
Divide-by-8	1per channel	4	4	2	1	20X	1	0	0	2.5
		2	4	4	1	40X	2	0	0	5
Divide-by-9	1per channel	4	4	2	1	20X	1	0	0	2.22
		2	4	4	1	40X	2	0	0	4.44
Divide-by-10	1per channel	4	4	2	1	20X	1	0	0	2
		2	4	4	1	40X	2	0	0	4
Divide-by-12	1per channel	4	4	2	1	20X	1	0	0	1.67
		2	4	4	1	40X	2	0	0	3.33
Divide-by-16	1per channel	4	4	2	1	20X	1	0	0	1.25
		2	4	4	1	40X	2	0	0	2.5
Divide-by-18	1per channel	4	4	2	1	20X	1	0	0	1.11
		2	4	4	1	40X	2	0	0	2.22
Divide-by-20	1per channel	4	4	2	1	20X	1	0	0	1
		2	4	4	1	40X	2	0	0	2
Divide-by-24	1per channel	2	4	4	1	20X	1	0	0	1.67
Divide-by-32	1per channel	2	4	4	1	40X	2	0	0	1.25

Table 8-16. JESD Sample Lane Alignments: Single-Band Complex Output

OUTPUT LANE	LMFS = 8411	LMFS = 8422		LMFS = 4421 20x		LMFS = 4421 40x		LMFS = 4442				LMFS = 2441			
DA0	AI_0 [15:8]	AI_0 [15:8]	AI_0 [7:0]	AI_0 [15:8]	AI_0 [7:0]										
DA1	AI_0 [7:0]	AI_1 [15:8]	AI_1 [7:0]	AQ_0 [15:8]	AQ_0 [7:0]	AI_0 [15:8]	AI_0 [7:0]	AI_0 [15:8]	AI_0 [7:0]	AI_1 [15:8]	AI_1 [7:0]	AI_0 [15:8]	AI_0 [7:0]	AQ_0 [15:8]	AQ_0 [7:0]
DA2	AQ_0 [15:8]	AQ_0 [15:8]	AQ_0 [7:0]			AQ_0 [15:8]	AQ_0 [7:0]	AQ_0 [15:8]	AQ_0 [7:0]	AQ_1 [15:8]	AQ_1 [7:0]				
DA3	AQ_0 [7:0]	AQ_1 [15:8]	AQ_1 [7:0]												
DB0	BI_0 [15:8]	BI_0 [15:8]	BI_0 [7:0]	BI_0 [15:8]	BI_0 [7:0]										
DB1	BI_0 [7:0]	BI_1 [15:8]	BI_1 [7:0]	BQ_0 [15:8]	BQ_0 [7:0]	BI_0 [15:8]	BI_0 [7:0]	BI_0 [15:8]	BI_0 [7:0]	BI_1 [15:8]	BI_1 [7:0]	BI_0 [15:8]	BI_0 [7:0]	BQ_0 [15:8]	BQ_0 [7:0]
DB2	BQ_0 [15:8]	BQ_0 [15:8	BQ_0 [7:0]			BQ_0 [15:8]	BQ_0 [7:0]	BQ_0 [15:8]	BQ_0 [7:0]	BQ_1 [15:8]	BQ_1 [7:0]				
DB3	BQ_0 [7:0]	BQ_1 [15:8]	BQ_1 [7:0]												

8.4.2.4 JESD204B Frame Assembly with Decimation (Single-Band DDC): Real Output

Table 8-17 lists the available JESD204B formats and valid ranges for the ADC32RF8x with decimation (single-band DDC) when using real output format. The ranges are limited by the SerDes line rate and the maximum ADC sample frequency. The sample alignment on the different lanes is shown in Table 8-18.

Table 8-17. JESD Mode Options: Single-Band Real Output (Wide Bandwidth)

DECIMATION SETTING (Complex)	NUMBER OF ACTIVE DDCS	L	M	F	S	PLL MODE	JESD MODE0	JESD MODE1	JESD MODE2	RATIO [f_{SerDes} / f_{CLK} (Gbps / GSPS)]
Divide-by-4 (Divide-by-2 real)	1 per channel	8	2	2	4	20x	1	0	0	2.5
		4	2	4	4	40x	2	0	0	5
		4	2	1	1	40x	0	0	1	
Divide-by-6 (Divide-by-3 real)	1 per channel	8	2	2	4	20x	1	0	0	1.67
		4	2	4	4	40x	2	0	0	3.33
		4	2	1	1	40x	0	0	1	

Table 8-18. JESD Sample Lane Alignment: Single-Band Real Output (Wide Bandwidth)

OUTPUT LANE	LMFS = 8224		LMFS = 4244				LMFS = 4211
DA0	A_0[15:8]	A_0[7:0]					
DA1	A_1[15:8]	A_1[7:0]	A_0[15:8]	A_0[7:0]	A_1[15:8]	A_1[7:0]	A_0[15:8]
DA2	A_2[15:8]	A_2[7:0]	A_2[15:8]	A_2[7:0]	A_3[15:8]	A_3[7:0]	A_0[7:0]
DA3	A_3[15:8]	A_3[7:0]					
DB0	B_0[15:8]	B_0[7:0]					
DB1	B_1[15:8]	B_1[7:0]	B_0[15:8]	B_0[7:0]	B_1[15:8]	B_1[7:0]	B_0[15:8]
DB2	B_2[15:8]	B_2[7:0]	B_0[15:8]	B_2[7:0]	B_3[15:8]	B_3[7:0]	B_0[7:0]
DB3	B_3[15:8]	B_3[7:0]					

8.4.2.5 JESD204B Frame Assembly with Decimation (Single-Band DDC): Real Output

Table 8-19 lists the available JESD204B formats and valid ranges for the ADC32RF8x with decimation (dual-band DDC) when using a complex output format. The sample alignment on the different lanes is shown in Table 8-20.

Table 8-19. JESD Mode Options: Single-Band Real Output

DECIMATION SETTING (Complex)	NUMBER OF ACTIVE DDCS	L	M	F	S	PLL MODE	JESD MODE0	JESD MODE1	JESD MODE2	RATIO [f_{SerDes} / f_{CLK} (Gbps / GSPS)]
Divide-by-8 (Divide-by-4 real)	1 per channel	4	2	1	1	20x	1	1	0	2.5
		4	2	2	2	20x	1	0	0	
		2	2	2	1	40x	0	0	1	5
		2	2	4	2	40x	2	0	0	
Divide-by-9 (Divide-by-4.5 real)	1 per channel	4	2	1	1	20x	1	1	0	2.22
		4	2	2	2	20x	1	0	0	
		2	2	2	1	40x	0	0	1	4.44
		2	2	4	2	40x	2	0	0	
Divide-by-10 (Divide-by-5 real)	1 per channel	4	2	1	1	20x	1	1	0	2
		4	2	2	2	20x	1	0	0	
		2	2	2	1	40x	0	0	1	4
		2	2	4	2	40x	2	0	0	
Divide-by-12 (Divide-by-6 real)	1 per channel	4	2	1	1	20x	1	1	0	1.67
		4	2	2	2	20x	1	0	0	
		2	2	2	1	40x	0	0	1	3.33
		2	2	4	2	40x	2	0	0	
Divide-by-16 (Divide-by-8 real)	1 per channel	4	2	1	1	20x	1	1	0	1.25
		4	2	2	2	20x	1	0	0	
		2	2	2	1	40x	0	0	1	2.5
		2	2	4	2	40x	2	0	0	
Divide-by-18 (Divide-by-9 real)	1 per channel	4	2	1	1	20x	1	1	0	1.11
		4	2	2	2	20x	1	0	0	
		2	2	2	1	40x	0	0	1	2.22
		2	2	4	2	40x	2	0	0	
Divide-by-20 (Divide-by-10 real)	1 per channel	4	2	1	1	20x	1	1	0	1
		4	2	2	2	20x	1	0	0	
		2	2	2	1	40x	0	0	1	2
		2	2	4	2	40x	2	0	0	
Divide-by-24 (Divide-by-12 real)	1 per channel	2	2	2	1	40x	0	0	1	1.67
		2	2	4	2	40x	2	0	0	
Divide-by-32 (Divide-by-16 real)	1 per channel	2	2	2	1	40x	0	0	1	1.25
		2	2	4	2	40x	2	0	0	

Table 8-20. JESD Sample Lane Assignment: Single-Band Real Output

OUTPUT LANE	LMFS = 4211	LMFS = 4222		LMFS = 2221		LMFS = 2242			
DA0	A_0[15:8]	A_0[15:8]	A_0[7:0]						
DA1	A_0[7:0]	A_1[15:8]	A_1[7:0]	A_0 [15:8]	A_0[7:0]	A_0[15:8]	A_0[7:0]	A_1[15:8]	A_1[7:0]
DB0	B_0[15:8]	B_0[15:8]	B_0[7:0]						
DB1	B_0[7:0]	B_1[15:8]	B_1[7:0]	B_0[15:8]	B_0[7:0]	B_0[15:8]	B_0[7:0]	B_1[15:8]	B_1[7:0]

8.4.2.6 JESD204B Frame Assembly with Decimation (Dual-Band DDC): Complex Output

Table 8-21 lists the available JESD204B formats and valid ranges for the ADC32RF8x with decimation (dual-band DDC) when using a complex output format. The ranges are limited by the SerDes line rate and the maximum ADC sample frequency. The sample alignment on the different lanes is shown in Table 8-22.

Table 8-21. JESD Mode Options: Dual-Band Complex Output

DECIMATION SETTING (Complex)	NUMBER OF ACTIVE DDCS	L	M	F	S	PLL MODE	JESD MODE0	JESD MODE1	JESD MODE2	RATIO [f_{SerDes} / f_{CLK} (Gbps / GSPS)]
Divide-by-8	2 per channel	8	8	2	1	20x	1	0	0	2.5
		4	8	4	1	40x	2	0	0	5
Divide-by-9	2 per channel	8	8	2	1	20x	1	0	0	2.22
		4	8	4	1	40x	2	0	0	4.44
Divide-by-10	2 per channel	8	8	2	1	20x	1	0	0	2
		4	8	4	1	40x	2	0	0	4
Divide-by-12	2 per channel	8	8	2	1	20x	1	0	0	1.67
		4	8	4	1	40x	2	0	0	3.33
Divide-by-16	2 per channel	8	8	2	1	20x	1	0	0	1.25
		4	8	4	1	40x	2	0	0	2.5
Divide-by-18	2 per channel	8	8	2	1	20x	1	0	0	1.11
		4	8	4	1	40x	2	0	0	2.22
Divide-by-20	2 per channel	8	8	2	1	20x	1	0	0	1
		4	8	4	1	40x	2	0	0	2
Divide-by-24	2 per channel	4	8	4	1	40x	2	0	0	1.67
Divide-by-32	2 per channel	4	8	4	1	40x	2	0	0	1.25

Table 8-22. JESD Sample Lane Assignment: Dual-Band Complex Output(1)

OUTPUT LANE	LMFS = 8821		LMFS = 4841			
DA0	$A1_0$[15:8]	$A1_0$[7:0]				
DA1	$A1Q_0$[15:8]	$A1Q_0$[7:0]	$A1I_0$[15:8]	$A1I_0$[7:0]	$A1Q_0$[15:8]	$A1Q_0$[7:0]
DA2	$A2I_0$[15:8]	$A2I_0$[7:0]	$A2I_0$[15:8]	$A2I_0$[7:0]	$A2Q_0$[15:8]	$A2Q_0$[7:0]
DA3	$A2Q_0$[15:8]	$A2Q_0$[7:0]				
DB0	$B1I_0$[15:8]	$B1I_0$[7:0]				
DB1	$B1Q_0$[15:8]	$B1Q_0$[7:0]	$B1I_0$[15:8]	$B1I_0$[7:0]	$B1Q_0$[15:8]	$B1Q_0$[7:0]
DB2	$B2I_0$[15:8]	$B2I_0$[7:0]	$B2I_0$[15:8]	$B2I_0$[7:0]	$B2Q_0$[15:8]	$B2Q_0$[7:0]
DB3	$B2Q_0$[15:8]	$B2Q_0$[7:0]				

(1) Blue and green shading indicates the two bands for channel A; yellow and orange shading indicates the two bands for channel B.

8.4.2.7 JESD204B Frame Assembly with Decimation (Dual-Band DDC): Real Output

Table 8-23 lists the available JESD204B formats and valid ranges for the ADC32RF8x with decimation (dual-band DDC) when using real output format. The ranges are limited by the SerDes line rate and the maximum ADC sample frequency. The sample alignment on the different lanes is shown in Table 8-24.

Table 8-23. JESD Mode Options: Dual-Band Real Output

DECIMATION SETTING (Complex)	NUMBER OF ACTIVE DDCS	L	M	F	S	PLL MODE	JESD MODE0	JESD MODE1	JESD MODE2	RATIO [f_{SerDes} / f_{CLK} (Gbps / GSPS)]
Divide-by-8 (Divide-by-4 real)	2 per channel	8	4	1	1	20x	1	1	0	2.5
		8	4	2	2	20x	1	0	0	
		4	4	2	1	40x	0	0	1	5
		4	4	4	2	40x	2	0	0	
Divide-by-9 (Divide-by-4.5 real)	2 per channel	8	4	1	1	20x	1	1	0	2.22
		8	4	2	2	20x	1	0	0	
		4	4	2	1	40x	0	0	1	4.44
		4	4	4	2	40x	2	0	0	
Divide-by-10 (Divide-by-5 real)	2 per channel	8	4	1	1	20x	1	1	0	2
		8	4	2	2	20x	1	0	0	
		4	4	2	1	40x	0	0	1	4
		4	4	4	2	40x	2	0	0	
Divide-by-12 (Divide-by-6 real)	2 per channel	8	4	1	1	20x	1	1	0	1.67
		8	4	2	2	20x	1	0	0	
		4	4	2	1	40x	0	0	1	3.33
		4	4	4	2	40x	2	0	0	
Divide-by-16 (Divide-by-8 real)	2 per channel	8	4	1	1	20x	1	1	0	1.25
		8	4	2	2	20x	1	0	0	
		4	4	2	1	40x	0	0	1	2.5
		4	4	4	2	40x	2	0	0	
Divide-by-18 (Divide-by-9 real)	2 per channel	8	4	1	1	20x	1	1	0	1.11
		8	4	2	2	20x	1	0	0	
		4	4	2	1	40x	0	0	1	2.22
		4	4	4	2	40x	2	0	0	
Divide-by-20 (Divide-by-10 real)	2 per channel	8	4	1	1	20x	1	1	0	1
		8	4	2	2	20x	1	0	0	
		4	4	2	1	40x	0	0	1	2
		4	4	4	2	40x	2	0	0	
Divide-by-24 (Divide-by-12 real)	2 per channel	4	4	2	1	40x	0	0	1	1.67
		4	4	4	2	40x	2	0	0	
Divide-by-32 (Divide-by-16 real)	2 per channel	4	4	2	1	40x	0	0	1	1.25
		4	4	4	2	40x	2	0	0	

Table 8-24. JESD Sample Lane Assignment: Dual-Band Complex Output

OUTPUT LANE	LMFS = 8411	LMFS = 8422		LMFS = 4421		LMFS = 4442			
DA0	$A1_0$[15:8]	$A1_0$[15:8]	$A1_0$[7:0]						
DA1	$A1_0$[7:0]	$A1_1$[15:8]	$A1_1$[7:0]	$A1_0$[15:8]	$A1_0$[7:0]	$A1_0$[15:8]	$A1_0$[7:0]	$A1_1$[15:8]	$A1_1$[7:0]
DA2	$A2_0$[15:8]	$A2_0$[15:8]	$A2_0$[7:0]	$A2_0$[15:8]	$A2_0$[7:0]	$A2_0$[15:8]	$A2_0$[7:0]	$A2_1$[15:8]	$A2_1$[7:0]
DA3	$A2_0$[7:0]	$A2_1$[15:8]	$A2_1$[7:0]						
DB0	$B1_0$[15:8]	$B1_0$[15:8]	$B1_0$[7:0]						
DB1	$B1_0$[7:0]	$B1_1$[15:8]	$B1_1$[7:0]	$B1_0$[15:8]	$B1_0$[7:0]	$B1_0$[15:8]	$B1_0$[7:0]	$B1_1$[15:8]	$B1_1$[7:0]
DB2	$B2_0$[15:8]	$B2_0$[15:8]	$B2_0$[7:0]	$B2_0$[15:8]	$B2_0$[7:0]	$B2_0$[15:8]	$B2_0$[7:0]	$B2_1$[15:8]	$B2_1$[7:0]
DB3	$B2_0$[7:0]	$B2_1$[15:8]	$B2_1$[7:0]						

8.4.3 Serial Interface

The ADC has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), and SDIN (serial interface data) pins. Serially shifting bits into the device is enabled when SEN is low. SDIN serial data are latched at every SCLK rising edge when SEN is active (low), as shown in Figure 8-56. The interface can function with SCLK frequencies from 20 MHz down to low speeds (of a few hertz) and also with a non-50% SCLK duty cycle, as shown in Table 8-25.

The SPI access uses 24 bits consisting of eight register data bits, 12 register address bits, and four special bits to distinguish between read/write, page and register, and individual channel access, as described in Table 8-26.

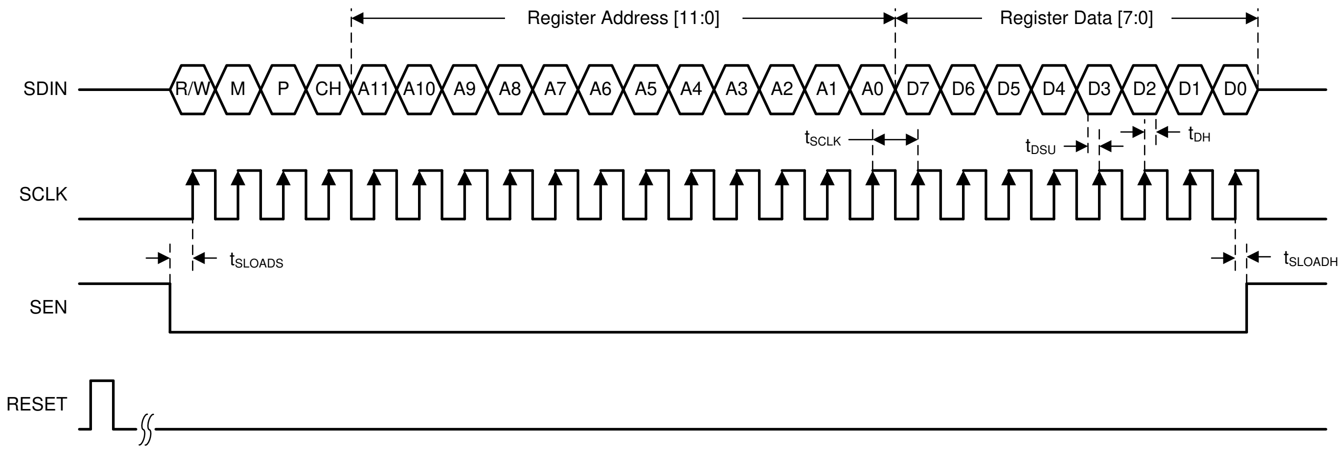


Figure 8-56. SPI Timing Diagram

Table 8-25. SPI Timing Information

		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency (equal to 1 / t_{SCLK})	1		20	MHz
t_{SLOADS}	SEN to SCLK setup time	50			ns
t_{SLOADH}	SCLK to SEN hold time	50			ns
t_{DSU}	SDIN setup time	10			ns
t_{DH}	SDIN hold time	10			ns
t_{SDOUT}	Delay between SCLK falling edge to SDOUT		10		ns

Table 8-26. SPI Input Description

SPI BIT	DESCRIPTION	OPTIONS
R/W bit	Read/write bit	0 = SPI write 1 = SPI read back
M bit	SPI bank access	0 = Analog SPI bank (master) 1 = All digital SPI banks (main digital, interleaving, decimation filter, JESD digital, and so forth)
P bit	JESD page selection bit	0 = Page access 1 = Register access
CH bit	SPI access for a specific channel of the JESD SPI bank	0 = Channel A 1 = Channel B
ADDR[11:0]	SPI address bits	—
DATA[7:0]	SPI data bits	—

Figure 8-57 shows the SDOUT timing when data are read back from a register. Data are placed on the SDOUT bus at the SCLK falling edge so that the data can be latched at the SCLK rising edge by the external receiver.

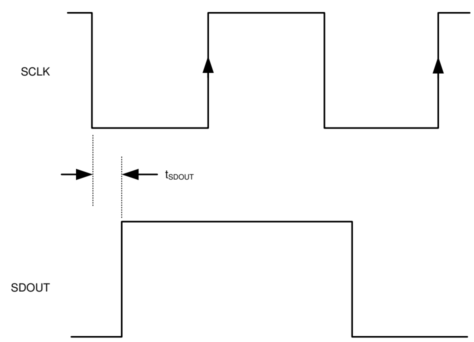


Figure 8-57. SDOUT Timing

8.4.3.1 Serial Register Write: Analog Bank

The internal register of the ADC32RF8x analog bank (Figure 8-58) can be programmed by:

1. Driving the SEN pin low.
2. Initiating a serial interface cycle selecting the page address of the register whose content must be written. To select the master page: write address 0012h with 04h. To select the ADC page: write address 0011h with FFh.
3. Writing the register content. When a page is selected, multiple registers located in the same page can be programmed.

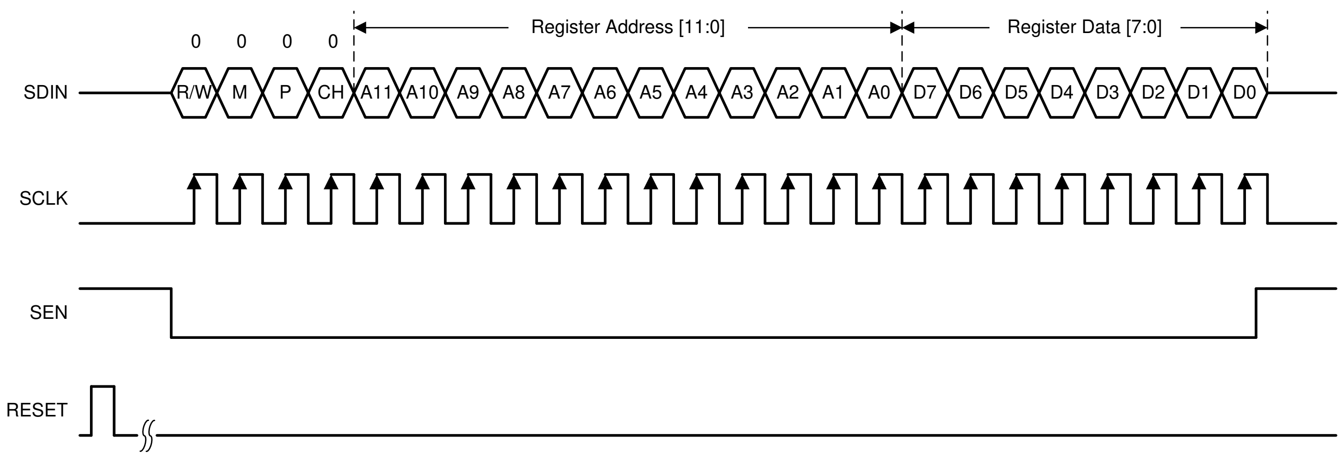


Figure 8-58. SPI Write Timing Diagram for the Analog Bank

8.4.3.2 Serial Register Readout: Analog Bank

Contents of the registers located in the two pages of the analog bank (Figure 8-59) can be readback by:

1. Driving the SEN pin low.
2. Selecting the page address of the register whose content must be read. Master page: write address 0012h with 04h. ADC page: write address 0011h with FFh.
3. Setting the R/W bit to 1 and writing the address to be read back.
4. Reading back the register content on the SDOUT pin. When a page is selected, the contents of multiple registers located in same page can be readback.

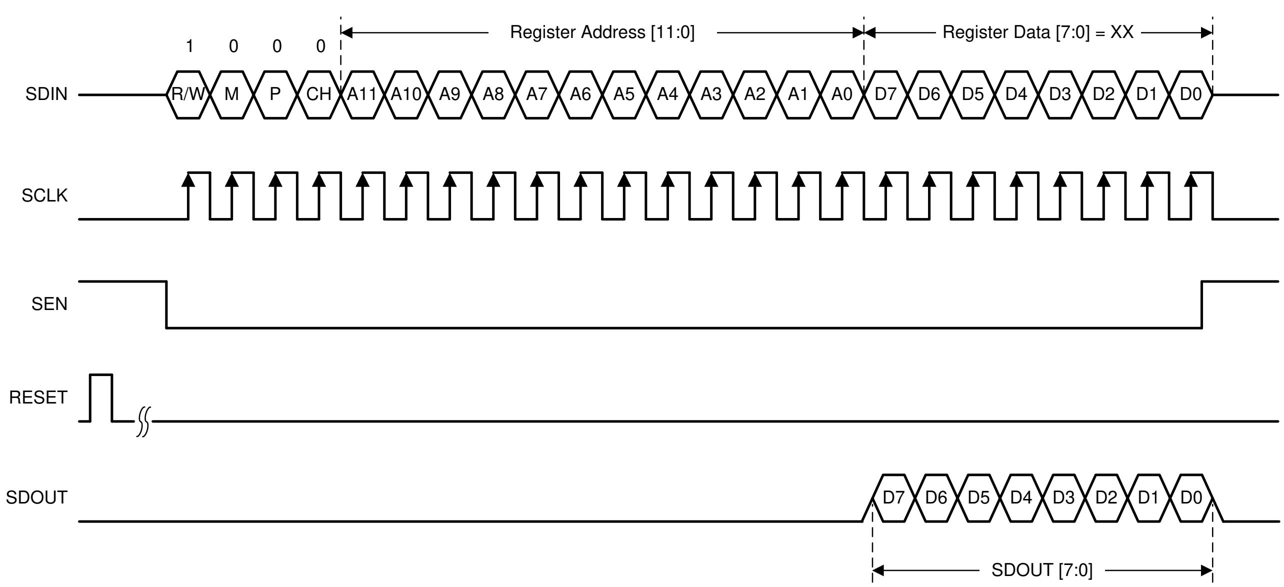


Figure 8-59. SPI Read Timing Diagram for the Analog Bank

8.4.3.3 Serial Register Write: Digital Bank

The digital bank contains seven pages (Offset Corrector Page for channel A and B; Digital Gain Page for channel A and B; Main digital Page for channel A and B; and JESD Digital Page). The timing for the individual page selection is shown in Figure 8-60. The registers located in the pages of the digital bank can be programmed by:

1. Driving the SEN pin low.
2. Setting the M bit to 1 and specifying the page with the desired register. There are seven pages in Digital Bank. These pages can be selected by appropriately programming register bits DIGITAL BANK PAGE SEL, located in addresses 002h, 003h, and 004h, using three consecutive SPI cycles. Addressing in a SPI cycle begins with 4xxx when selecting a page from digital bank because the M bit must be set to 1.
   - To select the offset corrector page channel A: write address 4004h with 61h, 4003h with 00h, and 4002h with 00h.
   - To select the offset corrector page channel B: write address 4004h with 61h, 4003h with 01h, and 4002h with 00h.
   - To select the digital gain page channel A: write address 4004h with 61h, 4003h with 00h, and 4002h with 05h.
   - To select the digital gain page channel B: write address 4004h with 61h, 4003h with 01h, and 4002h with 05h.
   - To select the main digital page channel A: write address 4004h with 68h, 4003h with 00h, and 4002h with 00h.
   - To select the main digital page channel B: write address 4004h with 68h, 4003h with 01h, and 4002h with 00h.
   - To select the JESD digital page: write address 4004h with 69h, 4003h with 00h, and 4002h with 00h.

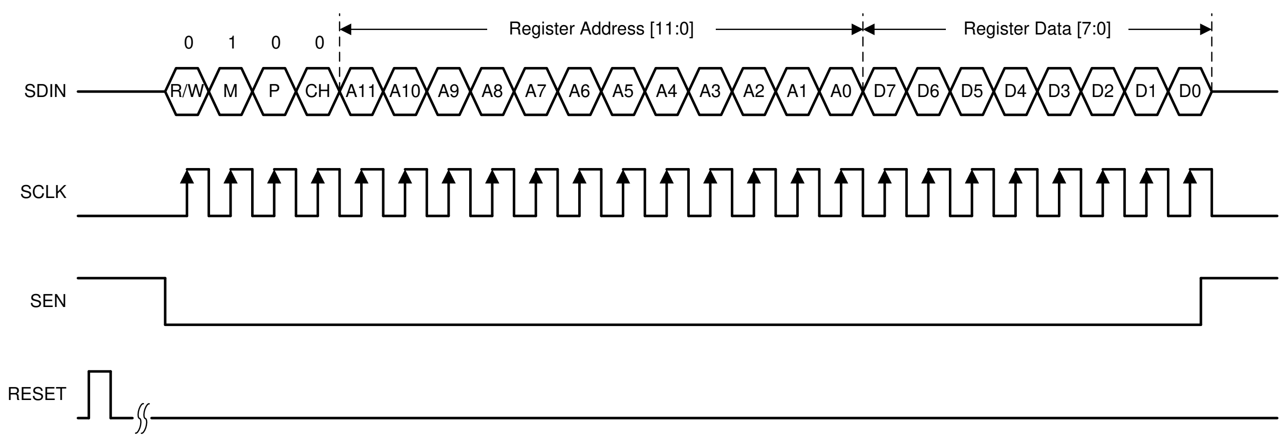


Figure 8-60. SPI Write Timing Diagram for Digital Bank Page Selection

3. Writing into the desired register by setting both the M bit and P bit to 1. Write register content. When a page is selected, multiple writes into the same page can be done. Addressing in an SPI cycle begins with 6xxx when selecting a page from the digital bank because the M bit must be set to 1, as shown in Figure 8-61.

   Note that the JESD digital page is common for both channels. The CH bit can be used to distinguish between two channels when programming registers in the JESD digital page. When CH = 0, registers are programmed for channel B; when CH = 1, registers are programmed for channel A. Thus, an SPI cycle to program registers for channel B begins with 6xxx and channel A begins with 7xxx.

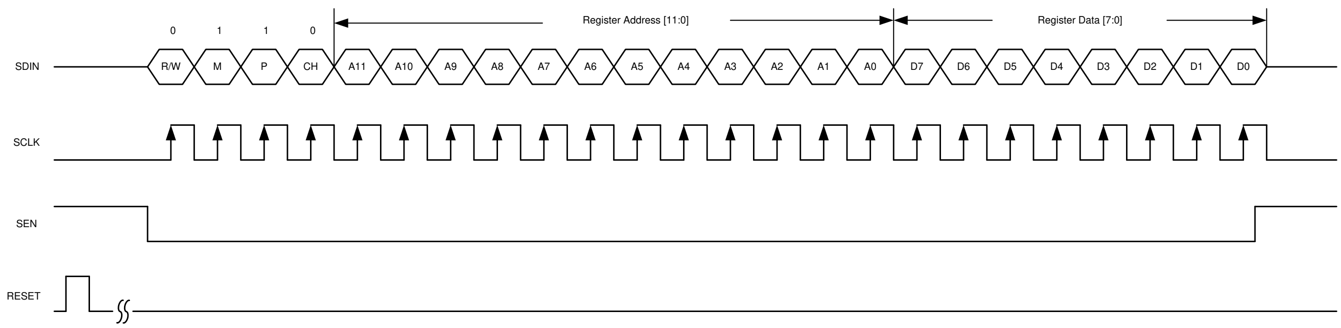


Figure 8-61. SPI Write Timing Diagram for Digital Bank Register Write

8.4.3.4 Serial Register Readout: Digital Bank

Readback of the register in one of the digital banks (as shown in Figure 8-62) can be accomplished by:

1. Driving the SEN pin low.
2. Selecting the page in the digital page: follow step 2 in the *Section 8.4.3.3* section.
3. Set the R/W, M, and P bits to 1, select channel A or channel B, and write the address to be read back.
   - JESD digital page: use the CH bit to select channel B (CH = 0) or channel A (CH = 1).
4. Read back the register content on the SDOUT pin. When a page is selected, multiple read backs from the same page can be done.

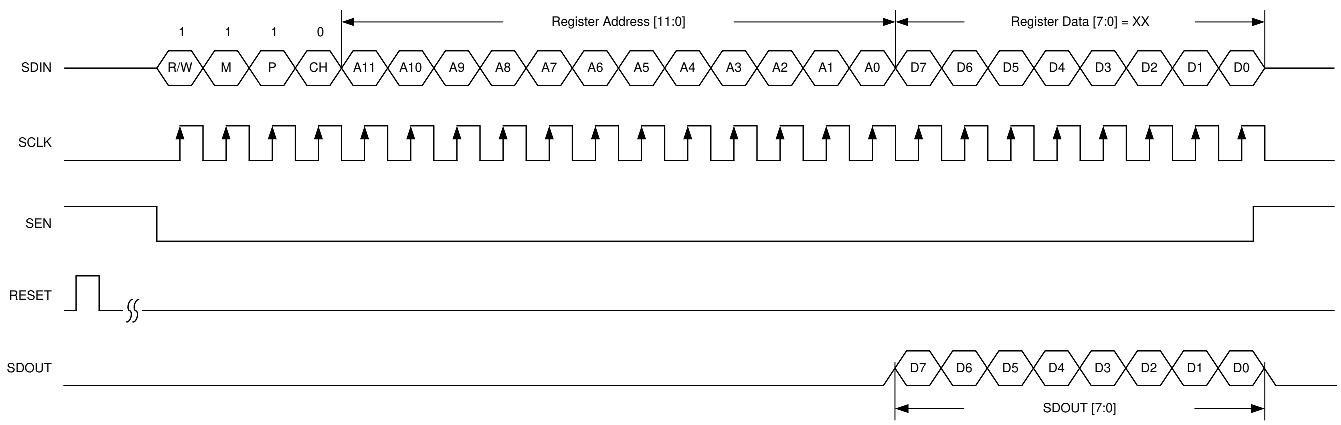


Figure 8-62. SPI Read Timing Diagram for the Digital Bank

8.4.3.5 Serial Register Write: Decimation Filter and Power Detector Pages

The decimation filter and power detector pages are special pages that accept direct addressing. The sampling clock and SYSREF signal are required to properly configure the decimation settings. Registers located in these pages can be programmed in one SPI cycle (Figure 8-63).

1. Drive the SEN pin low.
2. Directly write to the decimation filter or power detector pages. To program registers in these pages, set M = 1 and CH = 1. Additionally, address bit A[10] selects the decimation filter page (A[10] = 0) or the power detector page (A[10] = 1). Address bit A[11] selects channel A (A[11] = 0) or channel B (A[11] = 1).
   - Decimation filter page: write address 50xxh for channel A or 58xxh for channel B.
   - Power detector page: write address 54xxh for channel A or 5Cxxh for channel B.

Example: Writing address 5001h with 02h selects the decimation filter page for channel A and programs decimation factor of divide-by-8 (complex output).

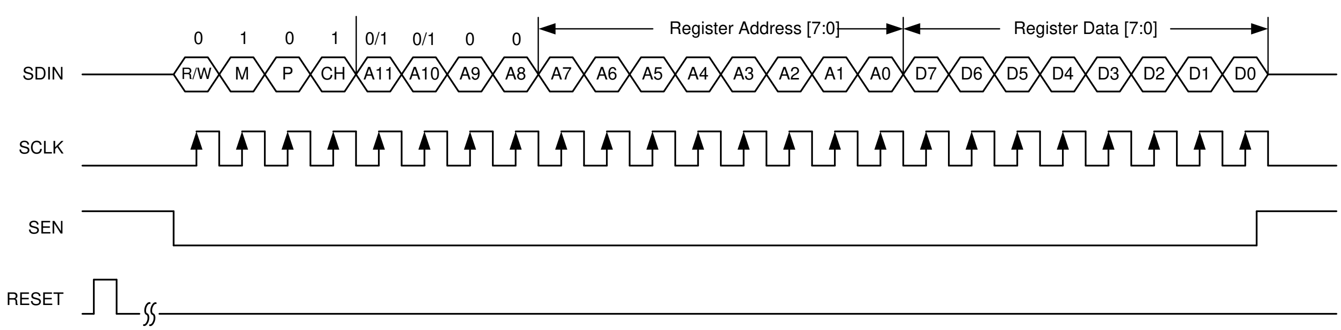
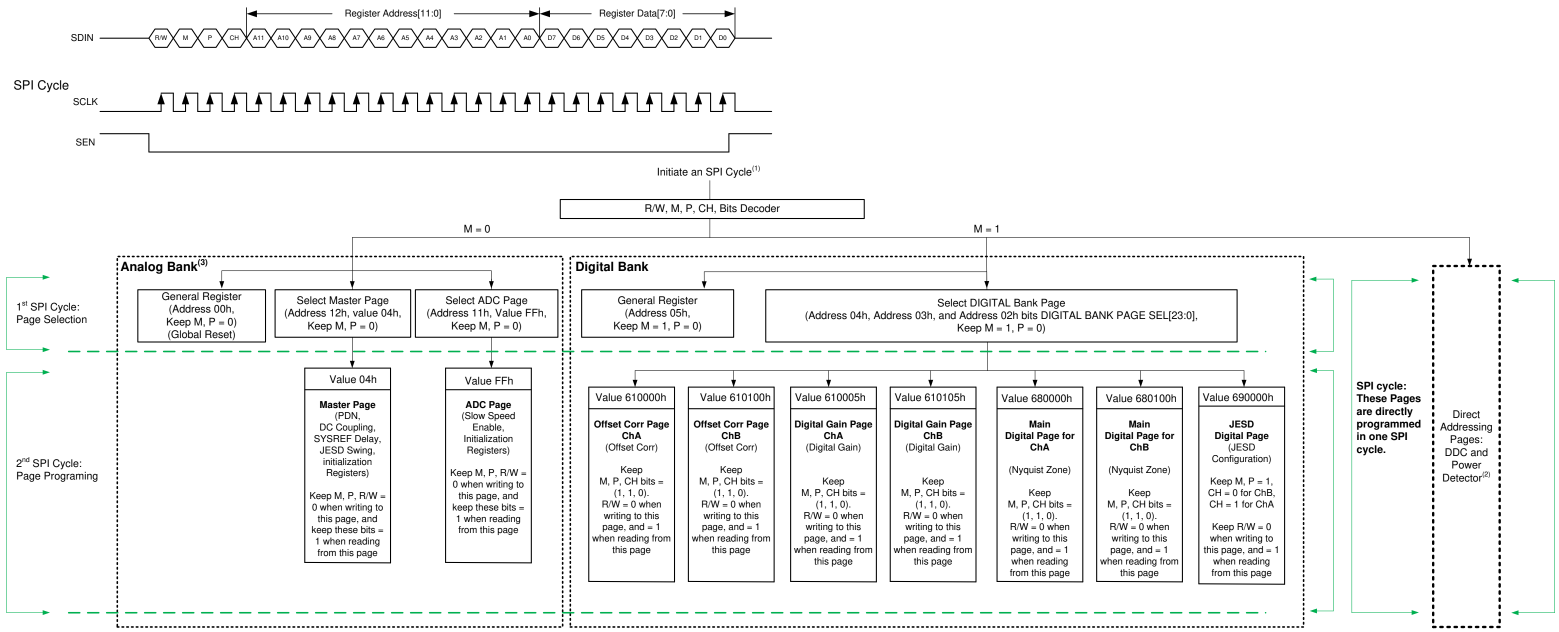


Figure 8-63. SPI Write Timing Diagram for the Decimation and Power Detector Pages

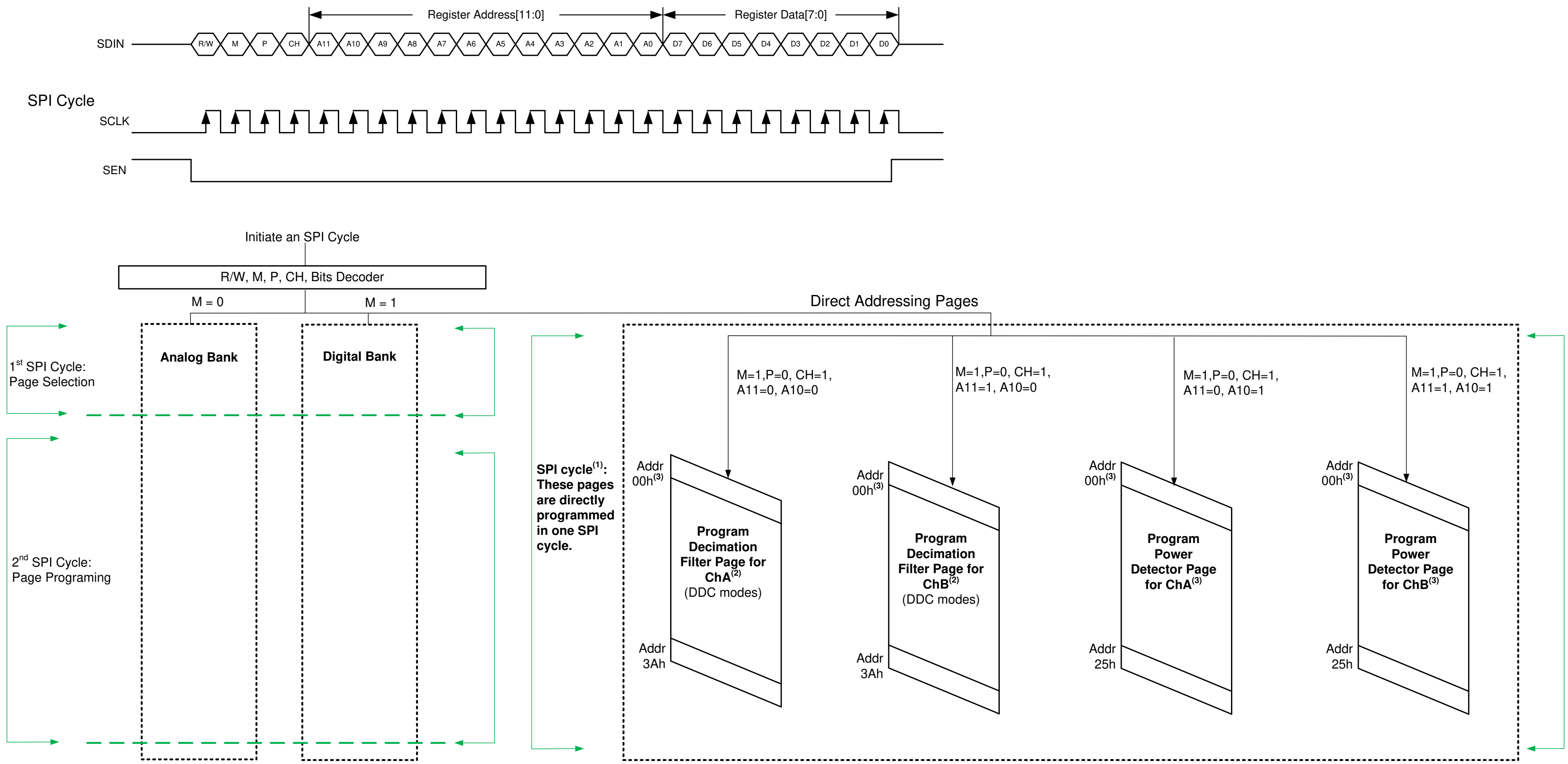
8.5 Register Maps

The ADC32RF8x contains two main SPI banks. The analog SPI bank provides access to the ADC core and the digital SPI bank controls the digital blocks (including the serial JESD interface). Figure 8-64 and Figure 8-65 provide a conceptual view of the SPI registers inside the ADC32RF8x. The analog SPI bank contains the master and ADC pages. The digital SPI bank is divided into multiple pages (the main digital, digital gain, decimation filter, JESD digital, and power detector pages).



A. In general, SPI writes are completed in two steps. The first step is to access the necessary page. The second step is to program the desired register in that page. When a page is accessed, the registers in that page can be programmed multiple times.
B. Registers in the decimation filter page and the power detector page can be directly programmed in one SPI cycle.
C. The CH bit is a *don't care* bit and is recommended to be kept at 0.

Figure 8-64. SPI Registers, Two-Step Addressing



A. Registers in the decimation filter page and the power detector page can be directly programmed in one SPI cycle.
B. To program registers in the decimation filter page, set M = 1, CH = 1, A[10] = 0, and A[11] = 0 or 1 for channel A or B. Addressing begins at 50xx for channel A and 58xx for channel B.
C. To program registers in power detector page, set M = 1, CH = 1, A[10] = 1, and A[11] = 0 or 1 for channel A or B. Addressing begins at 54xx for channel A and 5Cxx for channel B.

Figure 8-65. SPI Registers: Direct Addressing

Table 8-27 lists the register map for the ADC32RF8x.

Table 8-27. Register Map

REGISTER ADDRESS A[11:0] (Hex)	REGISTER DATA							
	7	6	5	4	3	2	1	0
GENERAL REGISTERS								
000	RESET	0	0	0	0	0	0	RESET
002	DIGITAL BANK PAGE SEL[7:0]							
003	DIGITAL BANK PAGE SEL[15:8]							
004	DIGITAL BANK PAGE SEL[23:16]							
010	0	0	0	0	0	0	0	3 or 4 WIRE
011	ADC PAGE SEL							
012	0	0	0	0	0	MASTER PAGE SEL	0	0
MASTER PAGE (M = 0)								
020	0	0	0	PDN SYSREF	0	0	PDN CHB	GLOBAL PDN
032	0	0	INCR CM IMPEDANCE	0	0	0	0	0
039	0	ALWAYS WRITE 1	0	ALWAYS WRITE 1	0	0	PDN CHB EN	SYNC TERM DIS
03C	0	SYSREF DEL EN	0	0	0	0	SYSREF DEL[4:3]	
03D	0	0	0	0	0	JESD OUTPUT SWING		
05A	SYSREF DEL[2:0]			0	0	0	0	0
057	0	0	0	SEL SYSREF REG	ASSERT SYSREF REG	0	0	0
058	0	0	SYNCB POL	0	0	0	0	0
ADC PAGE (FFh, M = 0)								
03F	0	0	0	0	0	SLOW SP EN1	0	0
042	0	0	0	SLOW SP EN2	0	0	1	1
Offset Corr Page Channel A (610000h, M = 1)								
68	FREEZE OFFSET CORR	ALWAYS WRITE 1	0	0	0	DIS OFFSET CORR	ALWAYS WRITE 1	0
Offset Corr Page Channel B (610100h, M = 1)								
68	FREEZE OFFSET CORR	ALWAYS WRITE 1	0	0	0	DIS OFFSET CORR	ALWAYS WRITE 1	0
Digital Gain Page Channel A (610005, M = 1)								
0A6	0	0	0	0	DIGITAL GAIN			

Table 8-27. Register Map (continued)

REGISTER ADDRESS A[11:0] (Hex)	REGISTER DATA							
	7	6	5	4	3	2	1	0
Digital Gain Page Channel B (610105, M = 1)								
0A6	0	0	0	0	DIGITAL GAIN			
Main Digital Page Channel A (680000h, M = 1)								
000	0	0	0	0	0	0	0	DIG CORE RESET GBL
0A2	0	0	0	0	NQ ZONE EN	NYQUIST ZONE		
Main Digital Page Channel B (680001h, M = 1)								
000	0	0	0	0	0	0	0	0
0A2	0	0	0	0	NQ ZONE EN	NYQUIST ZONE		
JESD DIGITAL PAGE (690000h, M = 1)								
001	CTRL K	0	0	TESTMODE EN	0	LANE ALIGN	FRAME ALIGN	TX LINK DIS
002	SYNC REG	SYNC REG EN	0	0	12BIT MODE		JESD MODE0	
003	LINK LAYER TESTMODE			LINK LAY RPAT	LMFC MASK RESET	JESD MODE1	JESD MODE2	RAMP 12BIT
004	0	0	0	0	0	0	REL ILA SEQ	
006	SCRAMBLE EN	0	0	0	0	0	0	0
007	0	0	0	FRAMES PER MULTIFRAME (K)				
016	0	40X MODE			0	0	0	0
017	0	0	0	0	LANE0 POL	LANE1 POL	LANE2 POL	LANE3 POL
032	SEL EMP LANE 0						0	0
033	SEL EMP LANE 1						0	0
034	SEL EMP LANE 2						0	0
035	SEL EMP LANE 3						0	0
036	0	CMOS SYNCB	0	0	0	0	0	0
037	0	0	0	0	0	0	PLL MODE	
03C	0	0	0	0	0	0	0	EN CMOS SYNCB
03E	0	MASK CLKDIV SYSREF	MASK NCO SYSREF	0	0	0	0	0

Table 8-27. Register Map (continued)

REGISTER ADDRESS A[11:0] (Hex)	REGISTER DATA							
	7	6	5	4	3	2	1	0
DECIMATION FILTER PAGE (Direct Addressing, 16-Bit Address, 5000h for Channel A and 5800h for Channel B)								
000	0	0	0	0	0	0	0	DDC EN
001	0	0	0	0	DECIM FACTOR			
002	0	0	0	0	0	0	0	DUAL BAND EN
005	0	0	0	0	0	0	0	REAL OUT EN
006	0	0	0	0	0	0	0	DDC MUX
007	DDC0 NCO1 LSB							
008	DDC0 NCO1 MSB							
009	DDC0 NCO2 LSB							
00A	DDC0 NCO2 MSB							
00B	DDC0 NCO3 LSB							
00C	DDC0 NCO3 MSB							
00D	DDC1 NCO4 LSB							
00E	DDC1 NCO4 MSB							
00F	0	0	0	0	0	0	0	NCO SEL PIN
010	0	0	0	0	0	0	NCO SEL	
011	0	0	0	0	0	0	LMFC RESET MODE	
014	0	0	0	0	0	0	0	DDC0 6DB GAIN
016	0	0	0	0	0	0	0	DDC1 6DB GAIN
01E	0	DDC DET LAT			0	0	0	0
01F	0	0	0	0	0	0	0	WBF 6DB GAIN
033	CUSTOM PATTERN1[7:0]							
034	CUSTOM PATTERN1[15:8]							
035	CUSTOM PATTERN2[7:0]							
036	CUSTOM PATTERN2[15:8]							
037	TEST PATTERN DDC1 Q-DATA				TEST PATTERN DDC1 I-DATA			
038	TEST PATTERN DDC2 Q-DATA				TEST PATTERN DDC2 I -DATA			
039	0	0	0	0	0	0	0	USE COMMON TEST PATTERN
03A	0	0	0	0	0	0	TEST PAT RES	TP RES EN

Table 8-27. Register Map (continued)

REGISTER ADDRESS A[11:0] (Hex)	REGISTER DATA							
	7	6	5	4	3	2	1	0
POWER DETECTOR PAGE (Direct Addressing, 16-Bit Address, 5400h for Channel A and 5C00h for Channel B)								
000	0	0	0	0	0	0	0	PKDET EN
001	BLKPKDET [7:0]							
002	BLKPKDET [15:8]							
003	0	0	0	0	0	0	0	BLKPKDET [16]
007	BLKTHHH							
008	BLKTHHL							
009	BLKTHLH							
00A	BLKTHLL							
00B	DWELL[7:0]							
00C	DWELL[15:8]							
00D	0	0	0	0	0	0	0	FILT0LPSEL
00E	0	0	0	0	TIMECONST			
00F	FIL0THH[7:0]							
010	FIL0THH[15:8]							
011	FIL0THL[7:0]							
012	FIL0THL[15:8]							
013	0	0	0	0	0	0	0	IIR0 2BIT EN
016	FIL1THH[7:0]							
017	FIL1THH[15:8]							
018	FIL1THL[7:0]							
019	FIL1THL[15:8]							
01A	0	0	0	0	0	0	0	IIR1 2BIT EN
01D	DWELLIIR[7:0]							
01E	DWELLIIR[15:8]							
020	0	0	0	0	0	0	0	IIR0 2BIT EN
021	0	0	0	PWRDETACCU				
022	PWRDETH[7:0]							
023	PWRDETH[15:8]							
024	PWRDETL[7:0]							
025	PWRDETL[15:8]							

Table 8-27. Register Map (continued)

REGISTER ADDRESS A[11:0] (Hex)	REGISTER DATA							
	7	6	5	4	3	2	1	0
POWER DETECTOR PAGE (continued)								
027	0	0	0	0	0	0	0	RMS 2BIT EN
02B	0	0	0	RESET AGC	0	0	0	0
032	OUTSEL GPIO4							
033	OUTSEL GPIO1							
034	OUTSEL GPIO3							
035	OUTSEL GPIO2							
037	0	0	0	0	IODIR GPIO2	IODIR GPIO3	IODIR GPIO1	IODIR GPIO4
038	0	0	INSEL1		0	0	INSEL0	

8.5.1 Example Register Writes

This section provides three different example register writes. Table 8-28 describes a global power-down register write, Table 8-29 describes the register writes when the scrambler is enabled, and Table 8-30 describes the register writes for 8x decimation for channels A and B (complex output, 1 DDC mode) with the NCO set to 1.8 GHz (f_S = 3 GSPS) and the JESD format configured to LMFS = 4421.

Table 8-28. Global Power-Down

ADDRESS	DATA	COMMENT
12h	04h	Set the master page
20h	01h	Set the global power-down

Table 8-29. Scrambler Enable

ADDRESS	DATA	COMMENT
4004h	69h	Select the digital JESD page
4003h	00h	
6006h	80h	Scrambler enable, channel A
7006h	80h	Scrambler enable, channel B

Table 8-30. 8x Decimation for Channel A and B

ADDRESS	DATA	COMMENT
4004h	68h	Select the main digital page for channel A
4003h	00h	
6000h	01h	Issue a digital reset for channel A
6000h	00h	Clear the digital for reset channel A
4003h	01h	Select the main digital page for channel B
6000h	01h	Issue a digital reset for channel B
6000h	00h	Clear the digital reset for channel B
4004h	69h	Select the digital JESD page
4003h	00h	
6002h	01h	Set JESD MODE0 = 1, channel A
7002h	01h	Set JESD MODE0 = 1, channel B
5000h	01h	Enable the DDC, channel A
5001h	02h	Set decimation to 8x complex
5007h	9Ah	Set the LSB of DDC0, NCO1 to 9Ah (f_{NCO} = 1.8 GHz, f_S = 3 GSPS)
5008h	99h	Set the MSB of DDC0, NCO1 to 99h (f_{NCO} = 1.8 GHz, f_S = 3 GSPS)
5014h	01h	Enable the 6-dB digital gain of DDC0
5801h	02h	Set decimation to 8x complex
5807h	9Ah	Set the LSB of DDC0, NCO1 to 9Ah (f_{NCO} = 1.8 GHz, f_S = 3 GSPS)
5808h	99h	Set the MSB of DDC0, NCO1 to 99h (f_{NCO} = 1.8 GHz, f_S = 3 GSPS)
5814h	01h	Enable the 6-dB digital gain of DDC0

8.5.2 Register Descriptions

8.5.2.1 General Registers

8.5.2.1.1 Register 000h (address = 000h), General Registers

Figure 8-36. Register 000h

7	6	5	4	3	2	1	0
RESET	0	0	0	0	0	0	RESET
R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

Table 8-31. Register 000h Field Descriptions

Bit	Field	Type	Reset	Description
7	RESET	R/W	0h	0 = Normal operation 1 = Internal software reset, clears back to 0
6-1	0	W	0h	Must write 0
0	RESET	R/W	0h	0 = Normal operation(1) 1 = Internal software reset, clears back to 0

(1) Both bits (7, 0) must be set simultaneously to perform a reset.

8.5.2.1.2 Register 002h (address = 002h), General Registers

Figure 8-37. Register 002h

7	6	5	4	3	2	1	0
DIGITAL BANK PAGE SEL[7:0]							
R/W-0h							

Table 8-32. Register 002h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIGITAL BANK PAGE SEL[7:0]	R/W	0h	Program the JESD BANK PAGE SEL[23:0] bits to access the desired page in the JESD bank. 680000h = Main digital page CHA selected 680100h = Main digital page CHB selected 610000h = Digital function page CHA selected 610100h = Digital function page CHB selected 690000h = JESD digital page selected

8.5.2.1.3 Register 003h (address = 003h), General Registers

Figure 8-38. Register 003h

7	6	5	4	3	2	1	0
DIGITAL BANK PAGE SEL[15:8]							
R/W-0h							

Table 8-33. Register 003h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIGITAL BANK PAGE SEL[15:8]	R/W	0h	Program the JESD BANK PAGE SEL[23:0] bits to access the desired page in the JESD bank. 680000h = Main digital page CHA selected 680100h = Main digital page CHB selected 610000h = Digital function page CHA selected 610100h = Digital function page CHB selected 690000h = JESD digital page selected

8.5.2.1.4 Register 004h (address = 004h), General Registers

Figure 8-39. Register 004h

7	6	5	4	3	2	1	0
DIGITAL BANK PAGE SEL[23:16]							
R/W-0h							

Table 8-34. Register 004h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIGITAL BANK PAGE SEL[23:16]	R/W	0h	Program the JESD BANK PAGE SEL[23:0] bits to access the desired page in the JESD bank. 680000h = Main digital page CHA selected 680100h = Main digital page CHB selected 610000h = Digital function page CHA selected 610100h = Digital function page CHB selected 690000h = JESD digital page selected

8.5.2.1.5 Register 010h (address = 010h), General Registers

Figure 8-40. Register 010h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	3 or 4 WIRE
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

Table 8-35. Register 010h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	3 or 4 WIRE	R/W	0h	0 = 4-wire SPI (default) 1 = 3-wire SPI where SDIN become input or output

8.5.2.1.6 Register 011h (address = 011h), General Registers

Figure 8-41. Register 011h

7	6	5	4	3	2	1	0
ADC PAGE SEL							
R/W-0h							

Table 8-36. Register 011h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ADC PAGE SEL	R/W	0h	00000000 = Normal operation, ADC page is not selected 11111111 = ADC page is selected; MASTER PAGE SEL must be set to 0

8.5.2.1.7 Register 012h (address = 012h), General Registers

Figure 8-42. Register 012h

7	6	5	4	3	2	1	0
0	0	0	0	0	MASTER PAGE SEL	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h

Table 8-37. Register 012h Field Descriptions

Bit	Field	Type	Reset	Description
7-3	0	W	0h	Must write 0
2	MASTER PAGE SEL	R/W	0h	0 = Normal operation 1 = Selects the master page address; ADC PAGE must be set to 0
1-0	0	W	0h	Must write 0

8.5.3 Master Page (M = 0)

8.5.3.1 Register 020h (address = 020h), Master Page

Figure 8-43. Register 020h

7	6	5	4	3	2	1	0
0	0	0	PDN SYSREF	0	0	PDN CHB	GLOBAL PDN
W-0h	W-0h	W-0h	R/W-0h	W-0h	R/W-0h	R/W-0h	R/W-0h

Table 8-38. Register 020h Field Descriptions

Bit	Field	Type	Reset	Description
7-5	0	W	0h	Must write 0
4	PDN SYSREF	R/W	0h	This bit powers down the SYSREF input buffer. 0 = Normal operation 1 = SYSREF input capture buffer is powered down and further SYSREF input pulses are ignored
3-2	0	W	0h	Must write 0
1	PDN CHB	R/W	0h	This bit powers down channel B. 0 = Normal operation 1 = Channel B is powered down
0	GLOBAL PDN	R/W	0h	This bit enables the global power-down. 0 = Normal operation 1 = Global power-down enabled

8.5.3.2 Register 032h (address = 032h), Master Page

Figure 8-44. Register 032h

7	6	5	4	3	2	1	0
0	0	INCR CM IMPEDANCE	0	0	0	0	0
W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 8-39. Register 032h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	W	0h	Must write 0
5	INCR CM IMPEDANCE	R/W	0h	Only use this bit when analog inputs are dc-coupled to the driver. 0 = VCM buffer directly drives the common point of biasing resistors. 1 = VCM buffer drives the common point of biasing resistors with > 5 kΩ
4-0	0	W	0h	Must write 0

8.5.3.3 Register 039h (address = 039h), Master Page

Figure 8-45. Register 039h

7	6	5	4	3	2	1	0
0	ALWAYS WRITE 1	0	ALWAYS WRITE 1	0	0	PDN CHB EN	SYNC TERM DIS
W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	R/W-0h	R/W-0h

Table 8-40. Register 039h Field Descriptions

Bit	Field	Type	Reset	Description
7	0	W	0h	Must write 0
6	ALWAYS WRITE 1	W	0h	Always set this bit to 1
5	0	W	0h	Must write 0
4	ALWAYS WRITE 1	W	0h	Always set this bit to 1
3-2	0	W	0h	Must write 0
1	PDN CHB EN	R/W	0h	This bit enables the power-down control of channel B through the SPI in register 20h. 0 = PDN control disabled 1 = PDN control enabled
0	SYNC TERM DIS	R/W	0h	This bit disables the on-chip, 100-Ω termination resistors on the SYNCB input. 0 = On-chip, 100-Ω termination enabled 1 = On-chip, 100-Ω termination disabled

8.5.3.4 Register 03Ch (address = 03Ch), Master Page

Figure 8-46. Register 03Ch

7	6	5	4	3	2	1	0
0	SYSREF DEL EN	0	0	0	0	SYSREF DEL[4:3]	
W-0h	R/W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	

Table 8-41. Register 03Ch Field Descriptions

Bit	Field	Type	Reset	Description
7	0	W	0h	Must write 0
6	SYSREF DEL EN	R/W	0h	This bit allows an internal delay to be added to the SYSREF input. 0 = SYSREF delay disabled 1 = SYSREF delay enabled through register settings [3Ch (bits 1-0), 5Ah (bits 7-5)]
5-2	0	W	0h	Must write 0
1-0	SYSREF DEL[4:3]	R/W	0h	When the SYSREF delay feature is enabled (3Ch, bit 6) the delay can be adjusted in 25-ps steps; the first step is 175 ps. The PVT variation of each 25-ps step is ±10 ps. The 175-ps step is ±50 ps; see Table 8-43.

8.5.3.5 Register 05Ah (address = 05Ah), Master Page

Figure 8-47. Register 05Ah

7	6	5	4	3	2	1	0
SYSREF DEL[2:0]			0	0	0	0	0
W-0h	R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 8-42. Register 05Ah Field Descriptions

Bit	Field	Type	Reset	Description
7	SYSREF DEL2	W	0h	When the SYSREF delay feature is enabled (3Ch, bit 6) the delay can be adjusted in 25-ps steps; the first step is 175 ps. The PVT variation of each 25-ps step is ±10 ps. The 175-ps step is ±50 ps; see Table 8-43.
6	SYSREF DEL1	R/W		
5	SYSREF DEL0	W		
4-0	0	W	0h	Must write 0

Table 8-43. SYSREF DEL[2:0] Bit Settings

STEP	SETTING	STEP (NOM)	TOTAL DELAY (NOM)
1	01000	175 ps	175 ps
2	00111	25 ps	200 ps
3	00110	25 ps	225 ps
4	00101	25 ps	250 ps
5	00100	25 ps	275 ps
6	00011	25 ps	300 ps

8.5.3.6 Register 03Dh (address = 3Dh), Master Page

Figure 8-48. Register 03Dh

7	6	5	4	3	2	1	0
0	0	0	0	0	JESD OUTPUT SWING		
W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h		

Table 8-44. Register 03Dh Field Descriptions

Bit	Field	Type	Reset	Description
7-3	0	W	0h	Must write 0
2-0	JESD OUTPUT SWING	R/W	0h	These bits select the output amplitude, V_{OD} (mV_{PP}), of the JESD transmitter for all lanes. 0 = 860 mV_{PP} 1= 810 mV_{PP} 2 = 770 mV_{PP} 3 = 745 mV_{PP} 4 = 960 mV_{PP} 5 = 930 mV_{PP} 6 = 905 mV_{PP} 7 = 880 mV_{PP}

8.5.3.7 Register 057h (address = 057h), Master Page

Figure 8-49. Register 057h

7	6	5	4	3	2	1	0
0	0	0	SEL SYSREF REG	ASSERT SYSREF REG	0	0	0
W-0h	W-0h	W-0h	R/W-0h	R/W-0h	W-0h	W-0h	W-0h

Table 8-45. Register 057h Field Descriptions

Bit	Field	Type	Reset	Description
7-5	0	W	0h	Must write 0
4	SEL SYSREF REG	R/W	0h	SYSREF can be asserted using this bit. Ensure that the SEL SYSREF REG register bit is set high before using this bit; see the *Section 8.3.3.1* section. 0 = SYSREF is logic low 1 = SYSREF is logic high
3	ASSERT SYSREF REG	R/W	0h	Set this bit to use the SPI register to assert SYSREF. 0 = SYSREF is asserted by device pins 1 = SYSREF can be asserted by the ASSERT SYSREF REG register bit Other bits = 0
2-0	0	W	0h	Must write 0

8.5.3.8 Register 058h (address = 058h), Master Page

Figure 8-50. Register 058h

7	6	5	4	3	2	1	0
0	0	SYNCB POL	0	0	0	0	0
W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 8-46. Register 058h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	W	0h	Must write 0
5	SYNCB POL	R/W	0h	This bit inverts the SYNCB polarity. 0 = Polarity is not inverted; this setting matches the timing diagrams in this document and is the proper setting to use 1 = Polarity is inverted
4-0	0	W	0h	Must write 0

8.5.4 ADC Page (FFh, M = 0)

8.5.4.1 Register 03Fh (address = 03Fh), ADC Page

Figure 8-51. Register 03Fh

7	6	5	4	3	2	1	0
0	0	0	0	0	SLOW SP EN1	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h

Table 8-47. Register 03Fh Field Descriptions

Bit	Field	Type	Reset	Description
7-3	0	W	0h	Must write 0
2	SLOW SP EN1	R/W	0h	This bit must be enabled for clock rates below 2.5 GSPS. 0 = ADC sampling rates are faster than 2.5 GSPS 1 = ADC sampling rates are slower than 2.5 GSPS
1-0	0	W	0h	Must write 0

8.5.4.2 Register 042h (address = 042h), ADC Page

Figure 8-52. Register 042h

7	6	5	4	3	2	1	0
0	0	0	SLOW SP EN2	0	0	0	0
W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h	W-0h

Table 8-48. Register 042h Field Descriptions

Bit	Field	Type	Reset	Description
7-5	0	W	0h	Must write 0
4	SLOW SP EN2	R/W	0h	This bit must be enabled for clock rates below 2.5 GSPS. 0 = ADC sampling rates are faster than 2.5 GSPS 1 = ADC sampling rates are slower than 2.5 GSPS
3-0	0	W	0h	Must write 0

8.5.5 Digital Function Page (610000h, M = 1 for Channel A and 610100h, M = 1 for Channel B)

8.5.5.1 Register A6h (address = 0A6h), Digital Function Page

Figure 8-53. Register 0A6h

7	6	5	4	3	2	1	0
0	0	0	0	DIG GAIN			
W-0h	W-0h	W-0h	W-0h	R/W-0h			

Table 8-49. Register 0A6h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	W	0h	Must write 0
3-0	DIG GAIN	R/W	0h	These bits set the digital gain of the ADC output data prior to decimation up to 11 dB; see Table 8-50.

Table 8-50. DIG GAIN Bit Settings

SETTING	DIGITAL GAIN
0000	0 dB
0001	1 dB
0010	2 dB
…	…
1010	10 dB
1011	11 dB

8.5.6 Offset Corr Page Channel A (610000h, M = 1)

8.5.6.1 Register 034h (address = 034h), Offset Corr Page Channel A

Figure 8-54. Register 034h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	SEL EXT EST
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

Table 8-51. Register 034h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	SEL EXT EST	R/W	0h	This bit selects the external estimate for the offset correction block; see the *Section 9.1.5* section.

8.5.6.2 Register 068h (address = 068h), Offset Corr Page Channel A

Figure 8-55. Register 068h

7	6	5	4	3	2	1	0
FREEZE OFFSET CORR	ALWAYS WRITE 1	0	0	0	DIS OFFSET CORR	ALWAYS WRITE 1	0
R/W-0h	R/W-0h	W-0h	W-0h	W-0h	R/W-0h	R/W-0h	R/W-0h

Table 8-52. Register 068h Field Descriptions

Bit	Field	Type	Reset	Description
7	FREEZE OFFSET CORR	R/W	0h	Use this bit and bits 5 and 1 to freeze the offset estimation process of the offset corrector; see the *Section 9.1.5* section. 011 = Apply this setting after powering up the device 111 = Offset corrector is frozen, does not estimate offset anymore, and applies the last computed value. Others = Do not use
6	ALWAYS WRITE 1	R/W	0h	Always write this bit as 1 for the offset correction block to work properly.
5	0	W	0h	Must write 0
4-3	0	W	0h	Must write 0
2	DIS OFFSET CORR	R/W	0h	0 = Offset correction block works and removes f_S / 8, f_S / 4, 3f_S / 8, and f_S / 2 spurs 1 = Offset correction block is disabled
1	ALWAYS WRITE 1	R/W	0h	Always write this bit as 1 for the offset correction block to work properly.
0	0	W	0h	Must write 0

8.5.7 Offset Corr Page Channel B (610000h, M = 1)

8.5.7.1 Register 068h (address = 068h), Offset Corr Page Channel B

Figure 8-56. Register 068h

7	6	5	4	3	2	1	0
FREEZE OFFSET CORR	ALWAYS WRITE 1	0	0	0	DIS OFFSET CORR	ALWAYS WRITE 1	0
R/W-0h	R/W-0h	W-0h	W-0h	W-0h	R/W-0h	R/W-0h	R/W-0h

Table 8-53. Register 068h Field Descriptions

Bit	Field	Type	Reset	Description
7	FREEZE OFFSET CORR	R/W	0h	Use this bit and bits 5 and 1 to freeze the offset estimation process of the offset corrector; see the *Section 9.1.5* section. 011 = Apply this setting after powering up the device 111 = Offset corrector is frozen, does not estimate offset anymore, and applies the last computed value. Others = Do not use
6	ALWAYS WRITE 1	R/W	0h	Always write this bit as 1 for the offset correction block to work properly.
5	0	W	0h	Must write 0
4-3	0	W	0h	Must write 0
2	DIS OFFSET CORR	R/W	0h	0 = Offset correction block works and removes f_S / 8, f_S / 4, 3f_S / 8, and f_S / 2 spurs 1 = Offset correction block is disabled
1	ALWAYS WRITE 1	R/W	0h	Always write this bit as 1 for the offset correction block to work properly.
0	0	W	0h	Must write 0

8.5.8 Digital Gain Page (610005h, M = 1 for Channel A and 610105h, M = 1 for Channel B)

8.5.8.1 Register 0A6h (address = 0A6h), Digital Gain Page

Figure 8-57. Register 0A6h

7	6	5	4	3	2	1	0
0	0	0	0	DIGITAL GAIN			
W-0h	W-0h	W-0h	W-0h	R/W-0h			

Table 8-54. Register 0A6h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	W	0h	Must write 0
3-0	DIGITAL GAIN	R/W	0h	These bits apply a digital gain to the ADC data (before the DDC) up to 11 dB. 0000 = Default 0001 = 1 dB 1011 = 11 dB Others = Do not use

8.5.9 Main Digital Page Channel A (680000h, M = 1)

8.5.9.1 Register 000h (address = 000h), Main Digital Page Channel A

Figure 8-58. Register 000h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	DIG CORE RESET GBL
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

Table 8-55. Register 000h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	DIG CORE RESET GBL	R/W	0h	Pulse this bit (0 →1 →0) to reset the digital core (applies to both channel A and B). All Nyquist zone settings take effect when this bit is pulsed.

8.5.9.2 Register 0A2h (address = 0A2h), Main Digital Page Channel A

Figure 8-59. Register 0A2h

7	6	5	4	3	2	1	0
0	0	0	0	NQ ZONE EN	NYQUIST ZONE		
W-0h	W-0h	W-0h	W-0h	R/W-0h	R/W-0h		

Table 8-56. Register 0A2h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	W	0h	Must write 0
3	NQ ZONE EN	R/W	0h	This bit allows for specification of the operating Nyquist zone. 0 = Nyquist zone specification disabled 1 = Nyquist zone specification enabled
2-0	NYQUIST ZONE	R/W	0h	These bits specify the Nyquist band for the portion of aliased spectrum that is not spanned by the frequencies specified in the Band-Freq. registers (register addresses B0-BB). If the Band-Freq registers are not enabled, this setting specifies the common Nyquist band information for the entire aliased spectrum. Set the NQ ZONE EN bit before programming these bits. For example, at s 3-GSPS chip clock, the first Nyquist zone is from dc to 1.5 GHz, the second Nyquist zone is from 1.5 GHz to 3 GHz, and so on. 000 = First Nyquist zone (dc – f_S / 2) 001 = Second Nyquist zone (f_S / 2 – f_S) 010 = Third Nyquist zone 011 = Fourth Nyquist zone

8.5.10 Main Digital Page Channel B (680001h, M = 1)

8.5.10.1 Register 000h (address = 000h), Main Digital Page Channel B

Figure 8-60. Register 000h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	DIG CORE RESET GBL
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

Table 8-57. Register 000h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	DIG CORE RESET GBL	R/W	0h	Pulse this bit (0 →1 →0) to reset the digital core (applies to both channel A and B). All Nyquist zone settings take effect when this bit is pulsed.

8.5.10.2 Register 0A2h (address = 0A2h), Main Digital Page Channel B

Figure 8-61. Register 0A2h

7	6	5	4	3	2	1	0
0	0	0	0	NQ ZONE EN	NYQUIST ZONE		
W-0h	W-0h	W-0h	W-0h	R/W-0h	R/W-0h		

Table 8-58. Register 0A2h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	W	0h	Must write 0
3	NQ ZONE EN	R/W	0h	This bit allows for specification of the operating Nyquist zone. 0 = Nyquist zone specification disabled 1 = Nyquist zone specification enabled
2-0	NYQUIST ZONE	R/W	0h	These bits specify the Nyquist band for the portion of aliased spectrum that is not spanned by the frequencies specified in the Band-Freq. registers (register addresses B0-BB). If the Band-Freq registers are not enabled, this setting specifies the common Nyquist band information for the entire aliased spectrum. Set the NQ ZONE EN bit before programming these bits. For example, at a 3-GSPS chip clock, first Nyquist zone is from dc to 1.5 GHz, the second Nyquist zone is from 1.5 GHz to 3 GHz, and so on. 000 = First Nyquist zone (dc – f_S / 2) 001 = Second Nyquist zone (f_S / 2 – f_S) 010 = Third Nyquist zone 011 = Fourth Nyquist zone

8.5.11 JESD Digital Page (6900h, M = 1)

8.5.11.1 Register 001h (address = 001h), JESD Digital Page

Figure 8-62. Register 001h

7	6	5	4	3	2	1	0
CTRL K	0	0	TESTMODE EN	0	LANE ALIGN	FRAME ALIGN	TX LINK DIS
R/W-0h	W-0h	W-0h	R/W-0h	W-0h	R/W-0h	R/W-0h	R/W-0h

Table 8-59. Register 001h Field Descriptions

Bit	Field	Type	Reset	Description
7	CTRL K	R/W	0h	This bit is the enable bit for the number of frames per multiframe. 0= Default is five frames per multiframe 1= Frames per multiframe can be set in register 06h
6-5	0	R/W	0h	Must write 0
4	TESTMODE EN		0	This bit generates a long transport layer test pattern mode according to section 5.1.6.3 of the JESD204B specification. 0 = Test mode disabled 1 = Test mode enabled
3	0	W	0h	Must write 0
2	LANE ALIGN	R/W	0h	This bit inserts a lane alignment character (K28.3) for the receiver to align to the lane boundary per section 5.3.3.5 of the JESD204B specification. 0 = Normal operation 1 = Inserts lane alignment characters
1	FRAME ALIGN	R/W	0h	This bit inserts a frame alignment character (K28.7) for the receiver to align to the frame boundary per section 5.3.35 of the JESD204B specification. 0 = Normal operation 1 = Inserts frame alignment characters
0	TX LINK DIS	R/W	0h	This bit disables sending the initial link alignment (ILA) sequence when SYNC is deasserted. 0 = Normal operation 1 = ILA disabled

8.5.11.2 Register 002h (address = 002h), JESD Digital Page

Figure 8-63. Register 002h

7	6	5	4	3	2	1	0
SYNC REG	SYNC REG EN	0	0	12BIT MODE		JESD MODE0	
R/W-0h	R/W-0h	W-0h	W-0h	R/W-0h		R/W-0h	

Table 8-60. Register 002h Field Descriptions

Bit	Field	Type	Reset	Description
7	SYNC REG	R/W	0h	This bit provides SYNC control through the SPI. 0 = Normal operation 1 = ADC output data are replaced with K28.5 characters
6	SYNC REG EN	R/W	0h	This bit is the enable bit for SYNC control through the SPI. 0 = Normal operation 1 = SYNC control through the SPI is enabled (ignores the SYNCB input pins)
5-4	0	W	0h	Must write 0
3-2	12BIT MODE	R/W	0h	This bit enables the 12-bit output mode for more efficient data packing. 00 = Normal operation, 14-bit output 01, 10 = Unused 11 = High-efficient data packing enabled
1-0	JESD MODE0	R/W	0h	These bits select the configuration register to configure the correct LMFS frame assemblies for different decimation settings; see the JESD frame assembly tables in the *Section 8.4.2.2* section. 00 = 0 01 = 1 10 = 2 11 = 3

8.5.11.3 Register 003h (address = 003h), JESD Digital Page

Figure 8-64. Register 003h

7	6	5	4	3	2	1	0
LINK LAYER TESTMODE			LINKLAY RPAT	LMFC MASKRESET	JESDMODE1	JESDMODE2	RAMP12BIT
R/W-0h			R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h

Table 8-61. Register 003h Field Descriptions

Bit	Field	Type	Reset	Description
7-5	LINK LAYER TESTMODE	R/W	0h	These bits generate a pattern according to section 5.3.3.8.2 of the JESD204B document. 000= Normal ADC data 001= D21.5 (high-frequency jitter pattern) 010 = K28.5 (mixed-frequency jitter pattern) 011= Repeat initial lane alignment (generates a K28.5 character and repeats lane alignment sequences continuously) 100= 12-octet RPAT jitter pattern
4	LINKLAY RPAT	R/W	0h	This bit changes the running disparity in a modified RPAT pattern test mode (only when link layer test mode = 100). 0 = Normal operation 1= Changes disparity
3	LMFCMASK RESET	R/W	0h	0= Normal operation
2	JESDMODE1	R/W	1h	These bits select the configuration register to configure the correct LMFS frame assemblies for different decimation settings; see the JESD frame assembly tables in the *Section 8.4.2.2* section
1	JESDMODE2	R/W	0h	These bits select the configuration register to configure the correct LMFS frame assemblies for different decimation settings; see the JESD frame assembly tables in the *Section 8.4.2.2* section
0	RAMP12BIT	R/W	0h	12-bit RAMP test pattern.0 = Normal data output 1= Digital output is the RAMP pattern

8.5.11.4 Register 004h (address = 004h), JESD Digital Page

Figure 8-65. Register 004h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	REL ILA SEQ	
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	

Table 8-62. Register 004h Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0
1-0	REL ILA SEQ	R/W	0h	These bits delay the generation of the lane alignment sequence by 0, 1, 2, or 3 multiframes after the code group synchronization. 00 = 0 multiframe delays 01 = 1 multiframe delay 10 = 2 multiframe delays 11 = 3 multiframe delays

8.5.11.5 Register 006h (address = 006h), JESD Digital Page

Figure 8-66. Register 006h

7	6	5	4	3	2	1	0
SCRAMBLE EN	0	0	0	0	0	0	0
R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 8-63. Register 006h Field Descriptions

Bit	Field	Type	Reset	Description
7	SCRAMBLE EN	R/W	0h	This bit is the scramble enable bit in the JESD204B interface. 0 = Scrambling disabled 1 = Scrambling enabled
6-0	0	W	0h	Must write 0

8.5.11.6 Register 007h (address = 007h), JESD Digital Page

Figure 8-67. Register 007h

7	6	5	4	3	2	1	0
0	0	0	FRAMES PER MULTIFRAME (K)				
W-0h	W-0h	W-0h	R/W-0h				

Table 8-64. Register 007h Field Descriptions

Bit	Field	Type	Reset	Description
7-5	0	W	0h	Must write 0
4-0	FRAMES PER MULTIFRAME (K)	R/W	0h	These bits set the number of multiframes. Actual K is the value in hex + 1 (that is, 0Fh is K = 16).

8.5.11.7 Register 016h (address = 016h), JESD Digital Page

Figure 8-68. Register 016h

7	6	5	4	3	2	1	0
0	40x MODE			0	0	0	0
W-0h	R/W-0h			W-0h	W-0h	W-0h	W-0h

Table 8-65. Register 016h Field Descriptions

Bit	Field	Type	Reset	Description
7	0	W	0h	Must write 0
6-4	40X MODE	R/W	0h	This register must be set for 40x mode operation. 000 = Register is set for 20x and 80x mode 111 = Register must be set for 40x mode
3-0	0	W	0h	Must write 0

8.5.11.8 Register 017h (address = 017h), JESD Digital Page

Figure 8-69. Register 017h

7	6	5	4	3	2	1	0
0	0	0	0	Lane0 POL	Lane1 POL	Lane2 POL	Lane3 POL
W-0h	R/W-0h	R/W-0h	R/W-0h	W-0h	W-0h	W-0h	W-0h

Table 8-66. Register 017h Field Descriptions

Bit	Field	Type	Reset	Description
7	0	W	0h	Must write 0
6-4	0	R/W	0h	Must write 0
3-0	Lane[3:0] POL	W	0h	These bits set the polarity of the individual JESD output lanes. 0 = Polarity as given in the pinout (noninverted) 1 = Inverts polarity (positive, P, or negative, M)

8.5.11.9 Register 032h-035h (address = 032h-035h), JESD Digital Page

Figure 8-70. Register 032h

7	6	5	4	3	2	1	0
SEL EMP LANE 0						0	0
R/W-0h						W-0h	W-0h

Figure 8-71. Register 033h

7	6	5	4	3	2	1	0
SEL EMP LANE 1						0	0
R/W-0h						W-0h	W-0h

Figure 8-72. Register 034h

7	6	5	4	3	2	1	0
SEL EMP LANE 2						0	0
R/W-0h						W-0h	W-0h

Figure 8-73. Register 035h

7	6	5	4	3	2	1	0
SEL EMP LANE 3						0	0
R/W-0h						W-0h	W-0h

Table 8-67. Register 032h-035h Field Descriptions

Bit	Field	Type	Reset	Description
7-2	SEL EMP LANE	R/W	0h	These bits select the amount of de-emphasis for the JESD output transmitter. The de-emphasis value in dB is measured as the ratio between the peak value after the signal transition to the settled value of the voltage in one bit period. 0 = 0 dB 1 = –1 dB 3 = –2 dB 7 = –4.1 dB 15 = –6.2 dB 31 = –8.2 dB 63 = –11.5 dB
1-0	0	W	0h	Must write 0

8.5.11.10 Register 036h (address = 036h), JESD Digital Page

Figure 8-74. Register 036h

7	6	5	4	3	2	1	0

Figure 8-74. Register 036h (continued)

0	CMOS SYNCB	0	0	0	0	0	0
W-0h	R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 8-68. Register 036h Field Descriptions

Bit	Field	Type	Reset	Description
7	0	W	0h	Must write 0
6	CMOS SYNCB	R/W	0h	This bit enables single-ended control of SYNCB using the GPIO4 pin (pin 63). The differential SYNCB input is ignored. Set the EN CMOS SYNCB bit and keep the CH bit high to make this bit effective. 0 = Differential SYNCB input 1 = Single-ended SYNCB input using pin 63
5-0	0	W	0h	Must write 0

8.5.11.11 Register 037h (address = 037h), JESD Digital Page

Figure 8-75. Register 037h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	PLL MODE	
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	

Table 8-69. Register 037h Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0
1-0	PLL MODE	R/W	0h	These bits select the PLL multiplication factor; see the JESD tables in the *Section 8.4.2.2* section for settings. 00 = 20x mode 01 = 16x mode 10 = 40x mode (the 40x MODE bit in register 16h must also be set) 11 = 80x mode

8.5.11.12 Register 03Ch (address = 03Ch), JESD Digital Page

Figure 8-76. Register 03Ch

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	EN CMOS SYNCB
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

Table 8-70. Register 03Ch Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	EN CMOS SYNCB	R/W	0h	Set this bit and the CMOS SYNCB bit high to provide a single-ended SYNC input to the device instead of differential. Also, keep the CH bit high. Thus: 1. Select the JESD digital page. 2. Write address 7036h with value 40h. 3. Write address 703Ch with value 01h.

8.5.11.13 Register 03Eh (address = 03Eh), JESD Digital Page

Figure 8-77. Register 03Eh

7	6	5	4	3	2	1	0
0	MASK CLKDIV SYSREF	MASK NCO SYSREF	0	0	0	0	0
W-0h	R/W-0h	R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 8-71. Register 03Eh Field Descriptions

Bit	Field	Type	Reset	Description
7	0	W	0h	Must write 0
6	MASK CLKDIV SYSREF	R/W	0h	Use this bit to mask the SYSREF going to the input clock divider. 0 = Input clock divider is reset when SYSREF is asserted (that is, when SYSREF transitions from low to high) 1 = Input clock divider ignores SYSREF assertions
5	MASK NCO SYSREF	R/W	0h	Use this bit to mask the SYSREF going to the NCO in the DDC block and LMFC counter of the JESD interface. 0 = NCO phase and LMFC counter are reset when SYSREF is asserted (that is, when SYSREF transitions from low to high) 1 = NCO and LMFC counter ignore SYSREF assertions
4-0	0	W	0h	Must write 0

8.5.12 Decimation Filter Page

Direct Addressing, 16-Bit Address, 5000h for Channel A, 5800h for Channel B

8.5.12.1 Register 000h (address = 000h), Decimation Filter Page

Figure 8-78. Register 000h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	DDC EN
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

Table 8-72. Register 000h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	DDC EN	R/W	0h	This bit enables the decimation filter and disables the bypass mode. 0 = Do not use 1 = Decimation filter enabled

8.5.12.2 Register 001h (address = 001h), Decimation Filter Page

Figure 8-79. Register 001h

7	6	5	4	3	2	1	0
0	0	0	0	DECIM FACTOR			
W-0h	W-0h	W-0h	W-0h	R/W-0h			

Table 8-73. Register 001h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	W	0h	Must write 0
3-0	DECIM FACTOR	R/W	0h	These bits configure the decimation filter setting. 0000 = Divide-by-4 complex 0001 = Divide-by-6 complex 0010 = Divide-by-8 complex 0011 = Divide-by-9 complex 0100 = Divide-by-10 complex 0101 = Divide-by-12 complex 0110 = Not used 0111 = Divide-by-16 complex 1000 = Divide-by-18 complex 1001 = Divide-by-20 complex 1010 = Divide-by-24 complex 1011 = Not used 1100 = Divide-by-32 complex

8.5.12.3 Register 002h (address = 2h), Decimation Filter Page

Figure 8-80. Register 002h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	DUAL BAND EN
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

Table 8-74. Register 002h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	DUAL BAND EN	R/W	0h	This bit enables the dual-band DDC filter for the corresponding channel. 0 = Single-band DDC; available in both ADC32RF80 and ADC32RF83 1 = Dual-band DDC; available in ADC32RF80 only

8.5.12.4 Register 005h (address = 005h), Decimation Filter Page

Figure 8-81. Register 005h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	REAL OUT EN
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

Table 8-75. Register 005h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	REAL OUT EN	R/W	0h	This bit converts the complex output to real output at 2x the output rate. 0 = Complex output format 1 = Real output format

8.5.12.5 Register 006h (address = 006h), Decimation Filter Page

Figure 8-82. Register 006h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	DDC MUX
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

Table 8-76. Register 006h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	DDC MUX	R/W	0h	This bit connects the DDC to the alternate channel ADC to enable up to four DDCs with one ADC and completely turn off the other ADC channel. 0 = Normal operation 1 = DDC block takes input from the alternate ADC

8.5.12.6 Register 007h (address = 007h), Decimation Filter Page

Figure 8-83. Register 007h

7	6	5	4	3	2	1	0
DDC0 NCO1 LSB							
R/W-0h							

Table 8-77. Register 007h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DDC0 NCO1 LSB	R/W	0h	These bits are the LSB of the NCO frequency word for NCO1 of DDC0 (band 1). The LSB represents f_S / (2^{16}), where f_S is the ADC sampling frequency.

8.5.12.7 Register 008h (address = 008h), Decimation Filter Page

Figure 8-84. Register 008h

7	6	5	4	3	2	1	0
DDC0 NCO1 MSB							
R/W-0h							

Table 8-78. Register 008h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DDC0 NCO1 MSB	R/W	0h	These bits are the MSB of the NCO frequency word for NCO1 of DDC0 (band 1). The LSB represents f_S / (2^{16}), where f_S is the ADC sampling frequency.

8.5.12.8 Register 009h (address = 009h), Decimation Filter Page

Figure 8-85. Register 009h

7	6	5	4	3	2	1	0
DDC0 NCO2 LSB							
R/W-0h							

Table 8-79. Register 009h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DDC0 NCO2 MSB	R/W	0h	These bits are the LSB of the NCO frequency word for NCO2 of DDC0 (band 1). The LSB represents f_S / (2^{16}), where f_S is the ADC sampling frequency.

8.5.12.9 Register 00Ah (address = 00Ah), Decimation Filter Page

Figure 8-86. Register 00Ah

7	6	5	4	3	2	1	0
DDC0 NCO2 MSB							
R/W-0h							

Table 8-80. Register 00Ah Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DDC0 NCO2 MSB	R/W	0h	These bits are the MSB of the NCO frequency word for NCO2 of DDC0 (band 1). The LSB represents f_S / (2^{16}), where f_S is the ADC sampling frequency.

8.5.12.10 Register 00Bh (address = 00Bh), Decimation Filter Page

Figure 8-87. Register 00Bh

7	6	5	4	3	2	1	0
DDC0 NCO3 LSB							
R/W-0h							

Table 8-81. Register 00Bh Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DDC0 NCO3 LSB	R/W	0h	These bits are the LSB of the NCO frequency word for NCO3 of DDC0 (band 1). The LSB represents f_S / (2^{16}), where f_S is the ADC sampling frequency.

8.5.12.11 Register 00Ch (address = 00Ch), Decimation Filter Page

Figure 8-88. Register 00Ch

7	6	5	4	3	2	1	0
DDC0 NCO3 MSB							
R/W-0h							

Table 8-82. Register 00Ch Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DDC0 NCO3 MSB	R/W	0h	These bits are the MSB of the NCO frequency word for NCO3 of DDC0 (band 1). The LSB represents f_S / (2^{16}), where f_S is the ADC sampling frequency.

8.5.12.12 Register 00Dh (address = 00Dh), Decimation Filter Page

Figure 8-89. Register 00Dh

7	6	5	4	3	2	1	0
DDC1 NCO4 LSB							
R/W-0h							

Table 8-83. Register 00Dh Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DDC1 NCO4 LSB	R/W	0h	These bits are the LSB of the NCO frequency word for NCO4 of DDC1 (band 2, only when dual-band mode is enabled). The LSB represents f_S / (2^{16}), where f_S is the ADC sampling frequency.

8.5.12.13 Register 00Eh (address = 00Eh), Decimation Filter Page

Figure 8-90. Register 00Eh

7	6	5	4	3	2	1	0
DDC1 NCO4 MSB							
R/W-0h							

Table 8-84. Register 00Eh Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DDC1 NCO4 MSB	R/W	0h	These bits are the MSB of the NCO frequency word for NCO4 of DDC1 (band 2, only when dual-band mode is enabled). The LSB represents f_S / (2^{16}), where f_S is the ADC sampling frequency.

8.5.12.14 Register 00Fh (address = 00Fh), Decimation Filter Page

Figure 8-91. Register 00Fh

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	NCO SEL PIN
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

Table 8-85. Register 00Fh Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	NCO SEL PIN	R/W	0h	This bit enables NCO selection through the GPIO pins. 0 = NCO selection through SPI (see address 0h10) 1 = NCO selection through GPIO pins

8.5.12.15 Register 010h (address = 010h), Decimation Filter Page

Figure 8-92. Register 010h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	NCO SEL	
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	

Table 8-86. Register 010h Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0
1-0	NCO SEL	R/W	0h	These bits enable NCO selection through register setting. 00 = NCO1 selected for DDC 1 01 = NCO2 selected for DDC 1 10 = NCO3 selected for DDC 1

8.5.12.16 Register 011h (address = 011h), Decimation Filter Page

Figure 8-93. Register 011h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	LMFC RESET MODE	
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	

Table 8-87. Register 011h Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0
1-0	LMFC RESET MODE	R/W	0h	These bits reset the configuration for all DDCs and NCOs. 00 = All DDCs and NCOs are reset with every LMFC RESET 01 = Reset with first LMFC RESET after DDC start. Afterwards, reset only when analog clock dividers are resynchronized. 10 = Reset with first LMFC RESET after DDC start. Afterwards, whenever analog clock dividers are resynchronized, use two LMFC resets. 11 = Do not use an LMFC reset at all. Reset the DDCs only when a DDC start is asserted and afterwards continue normal operation. Deterministic latency is not ensured.

8.5.12.17 Register 014h (address = 014h), Decimation Filter Page

Figure 8-94. Register 014h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	DDC0 6DB GAIN
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

Table 8-88. Register 014h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	DDC0 6DB GAIN	R/W	0h	This bit scales the output of DDC0 by 2 (6 dB) to compensate for real-to-complex conversion and image suppression. This scaling does not apply to the high-bandwidth filter path (divide-by-4 and -6); see register 1Fh. 0 = Normal operation 1 = 6-dB digital gain is added

8.5.12.18 Register 016h (address = 016h), Decimation Filter Page

Figure 8-95. Register 016h

7	6	5	4	3	2	1	0

Figure 8-95. Register 016h (continued)

0	0	0	0	0	0	0	DDC1 6DB GAIN
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

Table 8-89. Register 016h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	DDC1 6DB GAIN	R/W	0h	This bit scales the output of DDC1 by 2 (6 dB) to compensate for real-to-complex conversion and image suppression. This scaling does not apply to the high-bandwidth filter path (divide-by-4 and -6); see register 1Fh. 0 = Normal operation 1 = 6-dB digital gain is added

8.5.12.19 Register 01Eh (address = 01Eh), Decimation Filter Page

Figure 8-96. Register 01Eh

7	6	5	4	3	2	1	0
0	DDC DET LAT			0	0	0	0
W-0h	R/W-5h			W-1h	W-1h	W-1h	W-1h

Table 8-90. Register 01Eh Field Descriptions

Bit	Field	Type	Reset	Description
7	0	W	0h	Must write 0
6-4	DDC DET LAT	R/W	5h	These bits ensure deterministic latency depending on the decimation setting used; see Table 8-91.
3-0	0	W	1h	Must write 0

Table 8-91. DDC DET LAT Bit Settings

SETTING	COMPLEX DECIMATION SETTING
10h	Divide-by-24, -32 complex
20h	Divide-by-16, -18, -20 complex
40h	Divide-by-by 6, -12 complex
50h	Divide-by-4, -8, -9, -10 complex

8.5.12.20 Register 01Fh (address = 01Fh), Decimation Filter Page

Figure 8-97. Register 01Fh

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	WBF 6DB GAIN
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

Table 8-92. Register 01Fh Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	WBF 6DB GAIN	R/W	0h	This bit scales the output of the wide bandwidth DDC filter by 2 (6 dB) to compensate for real-to-complex conversion and image suppression. This setting only applies to the high-bandwidth filter path (divide-by-4 and -6). 0 = Normal operation 1 = 6-dB digital gain is added

8.5.12.21 Register 033h-036h (address = 033h-036h), Decimation Filter Page

Figure 8-98. Register 033h

7	6	5	4	3	2	1	0
CUSTOM PATTERN1[7:0]							
R/W-0h							

Figure 8-99. Register 034h

7	6	5	4	3	2	1	0
CUSTOM PATTERN1[15:8]							
R/W-0h							

Figure 8-100. Register 035h

7	6	5	4	3	2	1	0
CUSTOM PATTERN2[7:0]							
R/W-0h							

Figure 8-101. Register 036h

7	6	5	4	3	2	1	0
CUSTOM PATTERN2[15:8]							
R/W-0h							

Table 8-93. Register 033h-036h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CUSTOM PATTERN	R/W	0h	These bits set the custom test pattern in address 33h, 34h, 35h, or 36h.

8.5.12.22 Register 037h (address = 037h), Decimation Filter Page

Figure 8-102. Register 037h

7	6	5	4	3	2	1	0
TEST PATTERN DDC1 Q-DATA				TEST PATTERN DDC1 I-DATA			
W-0h	W-0h	W-0h	W-0h	R/W-0h			

Table 8-94. Register 037h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	TEST PATTERN DDC1 Q-DATA	W	0h	These bits select the test patten for the Q stream of the DDC1. 0000 = Normal operation using ADC output data 0001 = Outputs all 0s 0010 = Outputs all 1s 0011 = Outputs toggle pattern: output data are an alternating sequence of 10101010101010 and 01010101010101 0100 = Output digital ramp: output data increment by one LSB every clock cycle from code 0 to 65535 0110 = Single pattern: output data are a custom pattern 1 (75h and 76h) 0111 Double pattern: output data alternate between custom pattern 1 and custom pattern 2 1000 = Deskew pattern: output data are AAAAh 1001 = SYNC pattern: output data are FFFFh
3-0	TEST PATTERN DDC1 I-DATA	R/W	0h	These bits select the test patten for the I stream of the DDC1. 0000 = Normal operation using ADC output data 0001 = Outputs all 0s 0010 = Outputs all 1s 0011 = Outputs toggle pattern: output data are an alternating sequence of 10101010101010 and 01010101010101 0100 = Output digital ramp: output data increment by one LSB every clock cycle from code 0 to 65535 0110 = Single pattern: output data are a custom pattern 1 (75h and 76h) 0111 Double pattern: output data alternate between custom pattern 1 and custom pattern 2 1000 = Deskew pattern: output data are AAAAh 1001 = SYNC pattern: output data are FFFFh

8.5.12.22.1 Register 038h (address = 038h), Decimation Filter Page

Figure 8-103. Register 038h

7	6	5	4	3	2	1	0
TEST PATTERN DDC2 Q-DATA				TEST PATTERN DDC2 I -DATA			
R/W-0h				R/W-0h			

Table 8-95. Register 038h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	TEST PATTERN DDC2 Q-DATA	W	0h	These bits select the test patten for the Q stream of the DDC2. 0000 = Normal operation using ADC output data 0001 = Outputs all 0s 0010 = Outputs all 1s 0011 = Outputs toggle pattern: output data are an alternating sequence of 10101010101010 and 01010101010101 0100 = Output digital ramp: output data increment by one LSB every clock cycle from code 0 to 65535 0110 = Single pattern: output data are a custom pattern 1 (75h and 76h) 0111 Double pattern: output data alternate between custom pattern 1 and custom pattern 2 1000 = Deskew pattern: output data are AAAAh 1001 = SYNC pattern: output data are FFFFh
3-0	TEST PATTERN DDC2 I -DATA	R/W	0h	These bits select the test patten for the I stream of the DDC2. 0000 = Normal operation using ADC output data 0001 = Outputs all 0s 0010 = Outputs all 1s 0011 = Outputs toggle pattern: output data are an alternating sequence of 10101010101010 and 01010101010101 0100 = Output digital ramp: output data increment by one LSB every clock cycle from code 0 to 65535 0110 = Single pattern: output data are a custom pattern 1 (75h and 76h) 0111 Double pattern: output data alternate between custom pattern 1 and custom pattern 2 1000 = Deskew pattern: output data are AAAAh 1001 = SYNC pattern: output data are FFFFh

8.5.12.22.2 Register 039h (address = 039h), Decimation Filter Page

Figure 8-104. Register 039h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	USE COMMON TEST PATTERN
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

Table 8-96. Register 039h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	USE COMMON TEST PATTERN	R/W	0h	0 = Each data stream sends test patterns programmed by bits[3:0] of register 37h. 1 = Test patterns are individually programmed for the I and Q stream of each DDC using the TEST PATTERN DDCx y-DATA register bits (where x = 1 or 2 and y = I or Q).

8.5.12.23 Register 03Ah (address = 03Ah), Decimation Filter Page

Figure 8-105. Register 03Ah

7	6	5	4	3	2	1	0
0	0	0	0	0	0	TEST PAT RES	TP RES EN
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	R/W-0h

Table 8-97. Register 03Ah Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0
1	TEST PAT RES	R/W	0h	Pulsing this bit resets the test pattern. The test pattern reset must be enabled first (bit D0). 0 = Normal operation 1 = Reset the test pattern
0	TP RES EN	R/W	0h	This bit enables the test pattern reset. 0 = Reset disabled 1 = Reset enabled

8.5.13 Power Detector Page

8.5.13.1 Register 000h (address = 000h), Power Detector Page

Figure 8-106. Register 000h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	PKDET EN
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

Table 8-98. Register 000h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	PKDET EN	R/W	0h	This bit enables the peak power and crossing detector. 0 = Power detector disabled 1 = Power detector enabled

8.5.13.2 Register 001h-002h (address = 001h-002h), Power Detector Page

Figure 8-107. Register 001h

7	6	5	4	3	2	1	0
BLKPKDET [7:0]							
R/W-0h							

Figure 8-108. Register 002h

7	6	5	4	3	2	1	0
BLKPKDET [15:8]							
R/W-0h							

Table 8-99. Register 001h-002h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BLKPKDET	R/W	0h	This register specifies the block length in terms of number of samples (S`) used for peak power computation. Each sample S` is a peak of 8 actual ADC samples. This parameter is a 17-bit value directly in linear scale. In decimation mode, the block length must be a multiple of a divide-by-4 or -6 complex: length = 5 × decimation factor. The divide-by-8 to -32 complex: length = 10 × decimation factor.

8.5.13.3 Register 003h (address = 003h), Power Detector Page

Figure 8-109. Register 003h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	BLKPKDET[16]
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

Table 8-100. Register 003h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	BLKPKDET[16]	R/W	0h	This register specifies the block length in terms of number of samples (S`) used for peak power computation. Each sample S` is a peak of 8 actual ADC samples. This parameter is a 17-bit value directly in linear scale. In decimation mode, the block length must be a multiple of a divide-by-4 or -6 complex: length = 5 × decimation factor. The divide-by-8 to -32 complex: length = 10 × decimation factor.

8.5.13.4 Register 007h-00Ah (address = 007h-00Ah), Power Detector Page

Figure 8-110. Register 007h

7	6	5	4	3	2	1	0
BLKTHHH							
R/W-0h							

Figure 8-111. Register 008h

7	6	5	4	3	2	1	0
BLKTHHL							
R/W-0h							

Figure 8-112. Register 009h

7	6	5	4	3	2	1	0
BLKTHLH							
R/W-0h							

Figure 8-113. Register 00Ah

7	6	5	4	3	2	1	0
BLKTHLL							
R/W-0h							

Table 8-101. Register 007h-00Ah Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BLKTHHH BLKTHHL BLKTHLH BLKTHLL	R/W	0h	These registers set the four different thresholds for the hysteresis function threshold values from 0 to 256 (2TH), where 256 is equivalent to the peak amplitude. Example: BLKTHHH is set to –2 dBFS from peak: $10^{(-2 / 20) \times 256}$ = 203, then set 5407h, 5C07h = CBh.

8.5.13.5 Register 00Bh-00Ch (address = 00Bh-00Ch), Power Detector Page

Figure 8-114. Register 00Bh

7	6	5	4	3	2	1	0
DWELL[7:0]							
R/W-0h							

Figure 8-115. Register 00Ch

7	6	5	4	3	2	1	0
DWELL[15:8]							
R/W-0h							

Table 8-102. Register 00Bh-00Ch Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DWELL	R/W	0h	DWELL time counter. When the computed block peak crosses the upper thresholds BLKTHHH or BLKTHLH, the peak detector output flags are set. In order to be reset, the computed block peak must remain continuously lower than the lower threshold (BLKTHHL or BLKTHLL) for the period specified by the DWELL value. This threshold is 16 bits, is specified in terms of f_S / 8 clock cycles, and must be set to 0 for the crossing detector. Example: if f_S = 3 GSPS, f_S / 8 = 375 MHz, and DWELL = 0100h then the DWELL time = 2^9 / 375 MHz = 1.36 µs.

8.5.13.6 Register 00Dh (address = 00Dh), Power Detector Page

Figure 8-116. Register 00Dh

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	FILT0LPSEL
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

Table 8-103. Register 00Dh Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	FILT0LPSEL	R/W	0h	This bit selects either the block detector output or 2-bit output as the input to the IIR filter. 0 = Use the output of the high comparators (HH and HL) as the input of the IIR filter 1 = Combine the output of the high (HH and HL) and low (LH and LL) comparators to generate a 3-level input to the IIR filter (–1, 0, 1)

8.5.13.7 Register 00Eh (address = 00Eh), Power Detector Page

Figure 8-117. Register 00Eh

7	6	5	4	3	2	1	0
0	0	0	0	TIMECONST			
W-0h	W-0h	W-0h	W-0h	R/W-0h			

Table 8-104. Register 00Eh Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	W	0h	Must write 0
3-0	TIMECONST	R/W	0h	These bits set the crossing detector time period for N = 0 to 15 as $2^N \times f_S$ / 8 clock cycles. The maximum time period is 32768 × f_S / 8 clock cycles (approximately 87 µs at 3 GSPS).

8.5.13.8 Register 00Fh, 010h-012h, and 016h-019h (address = 00Fh, 010h-012h, and 016h-019h), Power Detector Page

Figure 8-118. Register 00Fh

7	6	5	4	3	2	1	0
FIL0THH[7:0]							
R/W-0h							

Figure 8-119. Register 010h

7	6	5	4	3	2	1	0
FIL0THH[15:8]							
R/W-0h							

Figure 8-120. Register 011h

7	6	5	4	3	2	1	0
FIL0THL[7:0]							
R/W-0h							

Figure 8-121. Register 012h

7	6	5	4	3	2	1	0
FIL0THL[15:8]							
R/W-0h							

Figure 8-122. Register 016h

7	6	5	4	3	2	1	0
FIL1THH[7:0]							
R/W-0h							

Figure 8-123. Register 017h

7	6	5	4	3	2	1	0
FIL1THH[15:8]							
R/W-0h							

Figure 8-124. Register 018h

7	6	5	4	3	2	1	0
FIL1THL[7:0]							
R/W-0h							

Figure 8-125. Register 019h

7	6	5	4	3	2	1	0
FIL1THL[15:8]							
R/W-0h							

Table 8-105. Register 00Fh, 010h, 011h, 012h, 016h, 017h, 018h, and 019h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FIL0THH FIL0THL FIL1THH FIL1THL	R/W	0h	Comparison thresholds for the crossing detector counter. This threshold is 16 bits in 2.14 signed notation. A value of 1 (4000h) corresponds to 100% crossings, a value of 0.125 (0800h) corresponds to 12.5% crossings.

8.5.13.9 Register 013h-01Ah (address = 013h-01Ah), Power Detector Page

Figure 8-126. Register 013h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	IIR0 2BIT EN
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

Figure 8-127. Register 01Ah

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	IIR1 2BIT EN
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

Table 8-106. Register 013h and 01Ah Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	IIR0 2BIT EN IIR1 2BIT EN	R/W	0h	This bit enables 2-bit output format of the IIR0 and IIR1 output comparators. 0 = Selects 1-bit output format 1 = Selects 2-bit output format

8.5.13.10 Register 01Dh-01Eh (address = 01Dh-01Eh), Power Detector Page

Figure 8-128. Register 01Dh

7	6	5	4	3	2	1	0
DWELLIIR[7:0]							
R/W-0h							

Figure 8-129. Register 01Eh

7	6	5	4	3	2	1	0
DWELLIIR[15:8]							
R/W-0h							

Table 8-107. Register 01Dh-01Eh Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DWELLIIR	R/W	0h	DWELL time counter for the IIR output comparators. When the IIR filter output crosses the upper thresholds FIL0THH or FIL1THH, the IIR peak detector output flags are set. In order to be reset, the output of the IIR filter must remain continuously lower than the lower threshold (FIL0THL or FIL1THL) for the period specified by the DWELLIIR value. This threshold is 16 bits and is specified in terms of f_S / 8 clock cycles. Example: if f_S = 3 GSPS, f_S / 8 = 375 MHz, and DWELLIIR = 0100h, then the DWELL time = 29 / 375 MHz = 1.36 µs.

8.5.13.11 Register 020h (address = 020h), Power Detector Page

Figure 8-130. Register 020h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	RMSDET EN
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

Table 8-108. Register 020h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	RMSDET EN	R/W	0h	This bit enables the RMS power detector. 0 = Power detector disabled 1 = Power detector enabled

8.5.13.12 Register 021h (address = 021h), Power Detector Page

Figure 8-131. Register 021h

7	6	5	4	3	2	1	0
0	0	0	PWRDETACCU				
W-0h	W-0h	W-0h	R/W-0h				

Table 8-109. Register 021h Field Descriptions

Bit	Field	Type	Reset	Description
7-5	0	W	0h	Must write 0
4-0	PWRDETACCU	R/W	0h	These bits program the block length to be used for RMS power computation. The block length is defined in terms of f_S / 8 clocks and can be programmed as 2M, where M = 0 to 16.

8.5.13.13 Register 022h-025h (address = 022h-025h), Power Detector Page

Figure 8-132. Register 022h

7	6	5	4	3	2	1	0
PWRDETH[7:0]							
R/W-0h							

Figure 8-133. Register 023h

7	6	5	4	3	2	1	0
PWRDETH[15:8]							
R/W-0h							

Figure 8-134. Register 024h

7	6	5	4	3	2	1	0
PWRDETL[7:0]							
R/W-0h							

Figure 8-135. Register 025h

7	6	5	4	3	2	1	0
PWRDETL[15:8]							
R/W-0h							

Table 8-110. Register 022h-025h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PWRDETH[15:0] PWRDETL[15:0]	R/W	0h	The computed average power is compared against these high and low thresholds. One LSB of the thresholds represents 1 / 2^{16}. Example: if PWRDETH is set to –14 dBFS from peak, $(10^{(-14 / 20)})^2 \times 2^{16}$ = 2609, then set 5422h, 5423h, 5C22h, 5C23h = 0A31h.

8.5.13.14 Register 027h (address = 027h), Power Detector Page

Figure 8-136. Register 027h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	RMS 2BIT EN
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

Table 8-111. Register 027h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	RMS 2BIT EN	R/W	0h	This bit enables 2-bit output format on the RMS output comparators. 0 = Selects 1-bit output format 1 = Selects 2-bit output format

8.5.13.15 Register 02Bh (address = 02Bh), Power Detector Page

Figure 8-137. Register 02Bh

7	6	5	4	3	2	1	0
0	0	0	RESET AGC	0	0	0	0
W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h	W-0h

Table 8-112. Register 02Bh Field Descriptions

Bit	Field	Type	Reset	Description
7-5	0	W	0h	Must write 0
4	RESET AGC	R/W	0h	After configuration, the AGC module must be reset and then brought out of reset to start operation. 0 = Clear AGC reset 1 = Set AGC reset Example: set 542Bh to 10h and then to 00h.
3-0	0	W	0h	Must write 0

8.5.13.16 Register 032h-035h (address = 032h-035h), Power Detector Page

Figure 8-138. Register 032h

7	6	5	4	3	2	1	0
OUTSEL GPIO4							
R/W-0h							

Figure 8-139. Register 033h

7	6	5	4	3	2	1	0
OUTSEL GPIO1							
R/W-0h							

Figure 8-140. Register 034h

7	6	5	4	3	2	1	0
OUTSEL GPIO3							
R/W-0h							

Figure 8-141. Register 035h

7	6	5	4	3	2	1	0
OUTSEL GPIO2							
R/W-0h							

Table 8-113. Register 032h-035h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUTSEL GPIO1 OUTSEL GPIO2 OUTSEL GPIO3 OUTSEL GPIO4	R/W	0h	These bits set the function or signal for each GPIO pin. 0 = IIR PK DET0[0] of channel A 1 = IIR PK DET0[1] of channel A (2-bit mode) 2 = IIR PK DET1[0] of channel A 3 = IIR PK DET1[1] of channel A (2-bit mode) 4 = BLKPKDETH of channel A 5 = BLKPKDETL of channel A 6 = PWR Det[0] of channel A 7 = PWR Det[1] of channel A (2-bit mode) 8 = FOVR of channel A 9-17 = Repeat outputs 0-8 but for channel B instead

8.5.13.17 Register 037h (address = 037h), Power Detector Page

Figure 8-142. Register 037h

7	6	5	4	3	2	1	0
0	0	0	0	IODIR GPIO2	IODIR GPIO3	IODIR GPIO1	IODIR GPIO4
W-0h	W-0h	W-0h	W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 8-114. Register 037h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	W	0h	Must write 0
3-0	IODIRGPIO[4:1]	R/W	0h	These bits select the output direction for the GPIO[4:1] pins. 0 = Input (for the NCO control) 1 = Output (for the AGC alarm function)

8.5.13.18 Register 038h (address = 038h), Power Detector Page

Figure 8-143. Register 038h

7	6	5	4	3	2	1	0
0	0	INSEL1		0	0	INSEL0	
W-0h	W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-0h	

Table 8-115. Register 038h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	W	0h	Must write 0
5-4	INSEL1	R/W	0h	These bits select which GPIO pin is used for the INSEL1 bit. 00 = GPIO4 01 = GPIO1 10 = GPIO3 11 = GPIO2 Table 8-116 lists the NCO selection, based on the bit settings of the INSEL pins.
3-2	0	W	0h	Must write 0
1-0	INSEL0	R/W	0h	These bits select which GPIO pin is used for the INSEL0 bit. 00 = GPIO4 01 = GPIO1 10 = GPIO3 11 = GPIO2 Table 8-116 lists the NCO selection, based on the bit settings of the INSEL pins.

Table 8-116. INSEL Bit Settings

INSEL1	INSEL2	NCO SELECTED
0	0	NCO1
0	1	NCO2
1	0	NCO3
1	1	n/a

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Start-Up Sequence

The steps in Table 9-1 are recommended as the power-up sequence when the ADC32RF8x is in the decimation-by-4 complex output mode.

Table 9-1. Initialization Sequence

STEP	DESCRIPTION	PAGE,REGISTER ADDRESS AND DATA	COMMENT
1	Supply all supply voltages. There is no required power-supply sequence for the 1.15 V, 1.2 V, and 1.9 V supplies, and can be supplied in any order.	—	—
2	Provide the SYSREF signal.	—	—
3	Pulse a hardware reset (low-to-high-to-low) on pins 33 and 34.	—	—
4	Write the register addresses described in the *PowerUpConfig*file.	Seethe files located in SBAA226	The*Power-up config* file contains analog trim registers that are required for best performance of the ADC. Write these registers every time after power up.
5	Write the register addresses mentioned in the ILConfigNyqX_ChA file, where X is the Nyquist zone.	Seethe files located in SBAA226	Based on the signal band of interest, provide the Nyquist zone information to the device.
6	Write the register addresses mentioned in the ILConfigNyqX_ChB file, where X is the Nyquist zone.	Seethe files located in SBAA226	This step optimizes device' performance by reducing interleaving mismatch errors.
6.1	Wait for 50 ms for the device to estimate the interleaving errors.	—	—
7	Depending upon the Nyquist band of operation, choose and write the registers from the appropriate file, *NLConfigNyqX_ChA*, where X is the Nyquist zone.	Seethe files located in SBAA226	Third-order nonlinearity of the device is optimized by this step for channel A.
7.1	Depending upon the Nyquist band of operation, choose and write the registers from the appropriate file, *NLConfigNyqX_ChB*, where X is the Nyquist zone.	Seethe files located in SBAA226	Third-order nonlinearity of the device is optimized by this step for channel B.
8	Configure the JESD interface and DDC block by writing the registers mentioned in the *DDCConfig* file.	Seethe files located in SBAA226	Determine the DDC and JESD interface LMFS options. Program these options in this step.

9.1.2 Hardware Reset

Timing information for the hardware reset is shown in Figure 9-1 and Table 9-2.

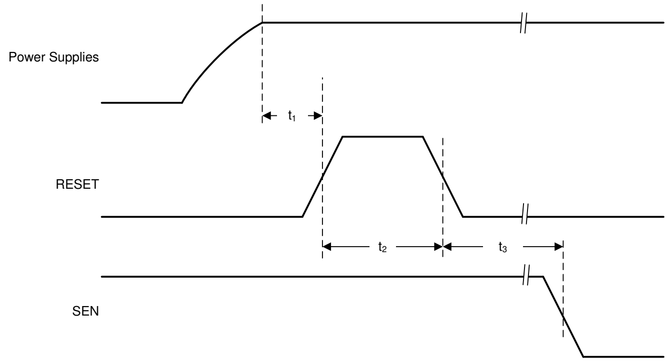


Figure 9-1. Hardware Reset Timing Diagram

Table 9-2. Hardware Reset Timing Information

		MIN	TYP	MAX	UNIT
t_1	Power-on delay from power-up to active high RESET pulse	1			ms
t_2	Reset pulse duration: active high RESET pulse duration	1			μs
t_3	Register write delay from RESET disable to SEN active	100			ns

9.1.3 SNR and Clock Jitter

The signal-to-noise ratio (SNR) of the ADC is limited by three different factors: quantization noise, thermal noise, and jitter, as shown in Equation 5. The quantization noise is typically not noticeable in pipeline converters and is 84 dB for a 14-bit ADC. The thermal noise limits the SNR at low input frequencies and the clock jitter sets the SNR for higher input frequencies.

$$\mathrm{SNRADC}\left[\mathrm{dBc}\right] = -20\log\sqrt{\left(10^{-\frac{\mathrm{SNR}_{\mathrm{Quantization\ Noise}}}{20}}\right)^2 + \left(10^{-\frac{\mathrm{SNR}_{\mathrm{Thermal\ Noise}}}{20}}\right)^2 + \left(10^{-\frac{\mathrm{SNR}_{\mathrm{Jitter}}}{20}}\right)^2} \quad (5)$$

The SNR limitation resulting from sample clock jitter can be calculated by Equation 6:

$$\mathrm{SNR}_{\mathrm{Jitter}}\left[\mathrm{dBc}\right] = -20\log\left(2\pi \times f_{\mathrm{IN}} \times t_{\mathrm{Jitter}}\right) \quad (6)$$

The total clock jitter (T_{Jitter}) has two components: the internal aperture jitter (90 f_S) is set by the noise of the clock input buffer and the external clock jitter. T_{Jitter} can be calculated by Equation 7:

$$t_{\mathrm{Jitter}} = \sqrt{\left(t_{\mathrm{Jitter,\ Ext\_Clock\_Input}}\right)^2 + \left(t_{\mathrm{Aperture\_ADC}}\right)^2} \quad (7)$$

External clock jitter can be minimized by using high-quality clock sources and jitter cleaners as well as band-pass filters at the clock input. A faster clock slew rate also improves the ADC aperture jitter.

The ADC32RF8x has a thermal noise of approximately 63 dBFS and an internal aperture jitter of 90 f_S. The SNR, depending on the amount of external jitter for different input frequencies, is shown in Figure 9-2.

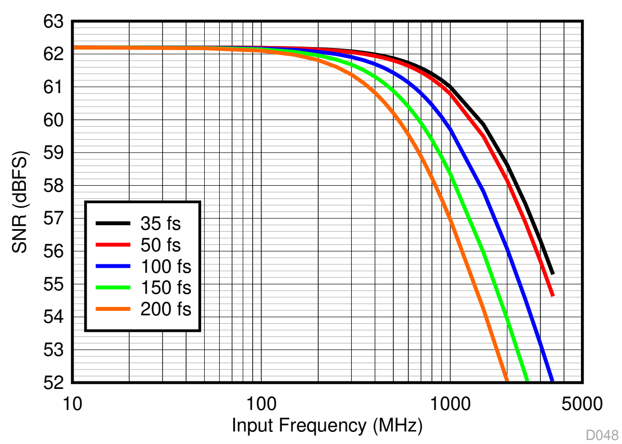


Figure 9-2. ADC SNR vs. Input Frequency and External Clock Jitter

9.1.3.1 External Clock Phase Noise Consideration

External clock jitter can be calculated by integrating the phase noise of the clock source out to approximately two times of the ADC sampling rate (2 × f_S), as shown in Figure 9-3. In order to maximize the ADC SNR, an external band-pass filter is recommended to be used on the clock input. This filter reduces the jitter contribution from the broadband clock phase noise floor by effectively reducing the integration bandwidth to the pass band of the band-pass filter. This method is suitable when estimating the overall ADC SNR resulting from clock jitter at a certain input frequency.

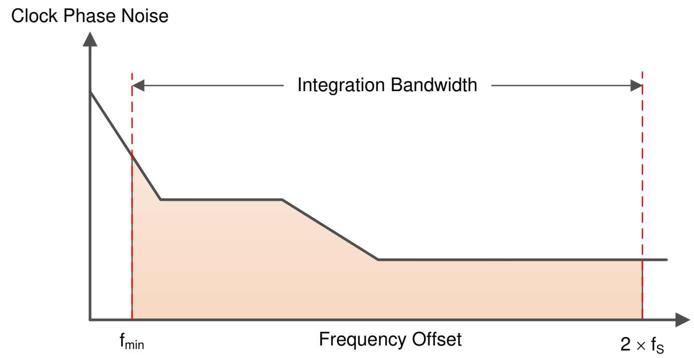


Figure 9-3. Integration Bandwidth for Extracting Jitter from Clock Phase Noise

However, when estimating the affect of a nearby blocker (such as a strong in-band interferer to the sensitivity, the phase noise information can be used directly to estimate the noise budget contribution at a certain offset frequency, as shown in Figure 9-4.

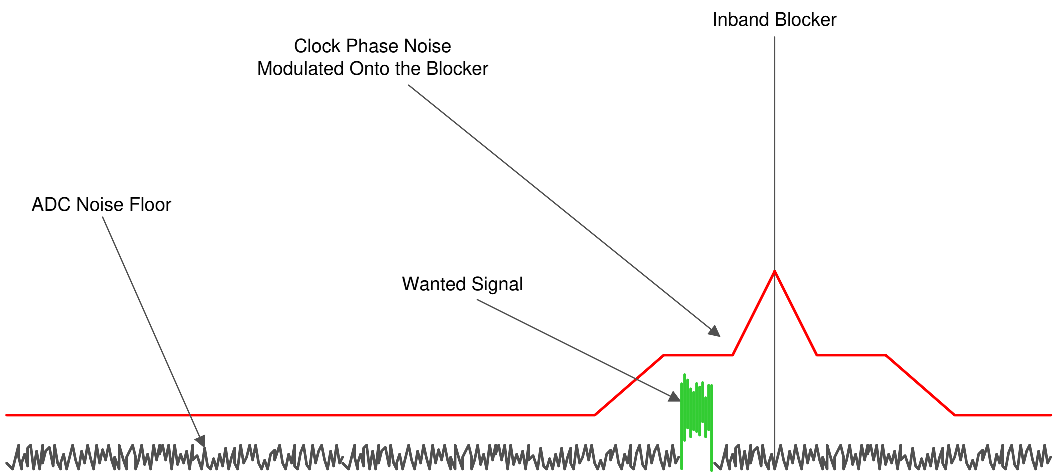


Figure 9-4. Small Wanted Signal in Presence of Interferer

At the sampling instant, the phase noise profile of the clock source convolves with the input signal (for example, the small wanted signal and the strong interferer merge together). If the power of the clock phase noise in the signal band of interest is too large, the wanted signal cannot not be recovered.

The resulting equivalent phase noise at the ADC input is also dependent on the sampling rate of the ADC and frequency of the input signal. The ADC sampling rate scales the clock phase noise, as shown in Equation 8.

$$ADC_{NSD}\left(dBc / Hz\right) = PN_{CLK}\left(dBc / Hz\right) - 20 \times \log\left(\frac{f_S}{f_{IN}}\right) \quad (8)$$

Using this information, the noise contribution resulting from the phase noise profile of the ADC sampling clock can be calculated.

9.1.4 Power Consumption in Different Modes

The ADC32RF8x consumes approximately 6.6 W of power when both channels are active with a divide-by-4 complex output. When different DDC options are used, the power consumption on the DVDD supply changes by a small amount but remains unaffected on other supplies. In the applications requiring just one channel to be active, channel A must be chosen as the active channel and channel B can be powered down. Power consumption reduces to approximately 4 W in single-channel operation with a divide-by-4 option at a 2949.12-MSPS device clock rate.

Table 9-3 shows power consumption in different DDC modes for dual-channel and single-channel operation.

Table 9-3. Power Consumption in Different DDC Modes (Sampling Clock Frequency, f_S = 3 GSPS)

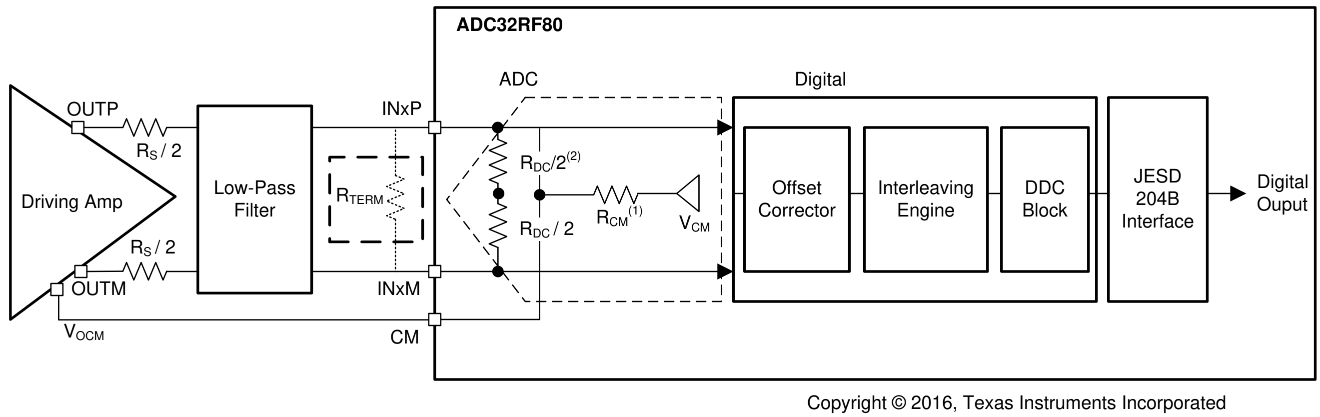
DECIMATION OPTION	ACTIVE CHANNEL	ACTIVE DDC	AVDD19 (mA)	AVDD (mA)	DVDD (mA)	TOTAL POWER (mW)
Divide-by-4	Channels A, B	Single	1777	970	1785	6545
Divide-by-8	Channels A, B	Dual	1777	973	1960	6749
Divide-by-8	Channels A, B	Single	1777	973	1730	6485
Divide-by-16	Channels A, B	Dual	1777	972	1971	6761
Divide-by-16	Channels A, B	Single	1777	972	1705	6455
Divide-by-24	Channels A, B	Dual	1771	975	1938	6715
Divide-by-24	Channels A, B	Single	1771	972	1667	6400
Divide-by-32	Channels A, B	Dual	1768	972	1835	6587
Divide-by-32	Channels A, B	Single	1768	970	1574	6285
Divide-by-4	Channel A	Single	961	796	1096	4002
Divide-by-8	Channel A	Dual	961	790	1168	4078
Divide-by-8	Channel A	Single	961	786	1047	3934
Divide-by-16	Channel A	Dual	961	789	1172	4081
Divide-by-16	Channel A	Single	961	786	1045	3932
Divide-by-24	Channel A	Dual	958	785	1155	4051
Divide-by-24	Channel A	Single	958	787	1016	3894
Divide-by-32	Channel A	Dual	956	788	1104	3992
Divide-by-32	Channel A	Single	956	786	978	3845

9.1.5 Using DC Coupling in the ADC32RF8x

The ADC32RF8x can be used in dc-coupling applications. However, the following points must be considered when designing the system:

1. Ensure that the correct common-mode voltage is used at the ADC analog inputs.

   The analog inputs are internally self-biased to V_{CM} through approximately a 33-Ω resistor. The internal biasing resistors also function as a termination resistor. However, if a different termination is required, the external resistor R_{TERM} can be differentially placed between the analog inputs, as shown in Figure 9-5. The amplifier V_{OCM} pin is recommended to be driven from the CM pin of the ADC to help the amplifier output common-mode voltage track the required common-mode voltage of the ADC.



A. Set the INCR CM IMPEDANCE bit to increase the RCM from 0 Ω to > 5000 Ω.

B. R_{DC} is approximately 65 Ω.

Figure 9-5. The ADC32RF8x in a DC-Coupling Application

2. Ensure that the correct SPI settings are written to the ADC.

   As shown in Figure 9-6, the ADC32RF8x has a digital block that estimates and corrects the offset mismatch among four interleaving ADC cores for a given channel.

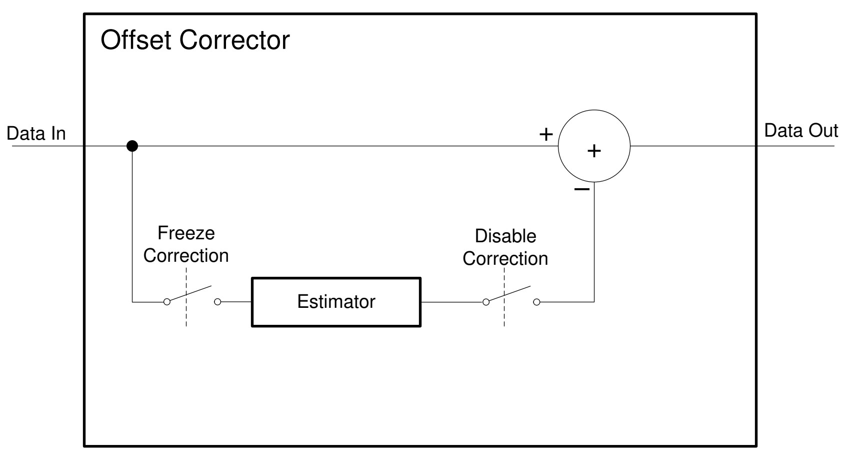


Figure 9-6. Offset Corrector in the ADC32RF8x

The offset corrector block nullifies dc, f_S / 8, f_S / 4, 3 f_S / 8, and f_S / 2. The resulting spectrum becomes free from static spurs at these frequencies. The corrector continuously processes the data coming from the interleaving ADC cores and cannot distinguish if the tone at these frequencies is part of signal or if the tone originated from a mismatch among the interleaving ADC cores. Thus, in applications where the signal is present at these frequencies, the offset corrector block can be bypassed.

9.1.5.1 Bypassing the Offset Corrector Block

When the offset corrector is bypassed, offset mismatch among interleaving ADC cores appears in the ADC output spectrum. To correct the effects of mismatch, place the ADC in an idle channel state (no signal at the ADC inputs) and the corrector must be allowed to run for some time to estimate the mismatch, then the corrector is frozen so that the last estimated value is held. Required register writes are provided in Table 9-4.

Table 9-4. Freezing and Bypassing the Offset Corrector Block

STEP	REGISTER WRITE	COMMENT
STEPS FOR FREEZING THE CORRECTOR BLOCK		
1	—	Signal source is turned off. The device detects an idle channel at its input.
2	—	Wait for at least 0.4 ms for the corrector to estimate the internal offset
3	Address 4001h, value 00h	Select Offset Corr Page Channel A
	Address 4002h, value 00h	
	Address 4003h, value 00h	
	Address 4004h, value 61h	
	Address 6068h, value C2h	Freeze the corrector for channel A
	Address 4003h, value 01h	Select Offset Corr Page Channel B
	Address 6068h, value C2h	Freeze the corrector for channel B
4	—	Signal source can now be turned on
STEPS FOR BYPASSING THE CORRECTOR BLOCK		
1	Address 4001h, value 00h	—
	Address 4002h, value 00h	
	Address 4003h, value 00h	
	Address 4004h, value 61h	Select Offset Corr Page Channel A
	Address 6068h, value 46h	Disable the corrector for channel A
	Address 4003h, value 01h	Select Offset Corr Page Channel B
	Address 6068h, value 46h	Disable the corrector for channel B

9.1.5.1.1 Effect of Temperature

Figure 9-7 and Figure 9-8 show the behavior of nf_S / 8 tones with respect to temperature when the offset corrector block is frozen or disabled.

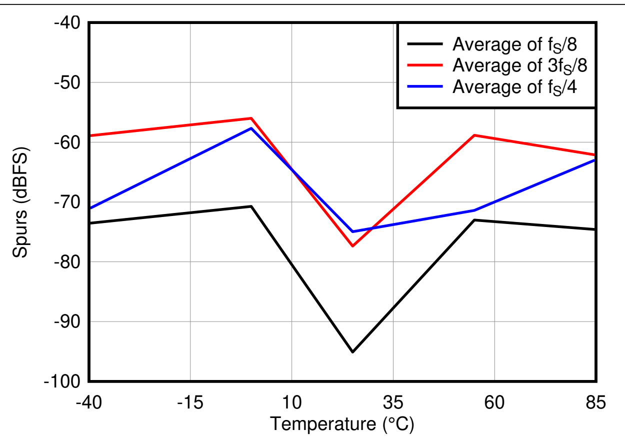


Figure 9-7. Offset Corrector Block Frozen at Room Temperature

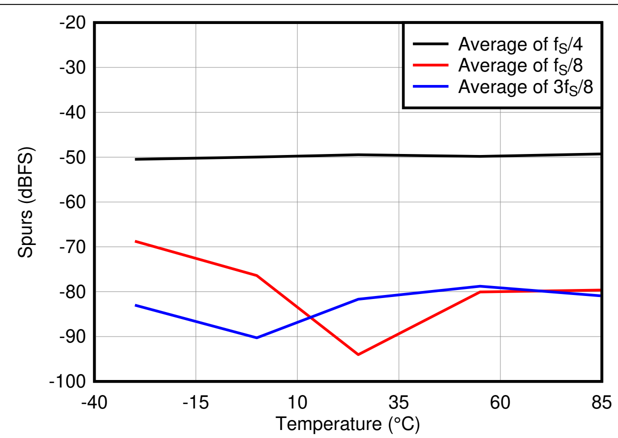


Figure 9-8. Offset Corrector Block Disabled

9.2 Typical Application

The ADC32RF8x is designed for wideband receiver applications demanding high dynamic range over a large input frequency range. A typical schematic for an ac-coupled receiver is shown in Figure 9-9.

Decoupling capacitors with low ESL are recommended to be placed as close as possible at the pins indicated in Figure 9-9. Additional capacitors can be placed on the remaining power pins.

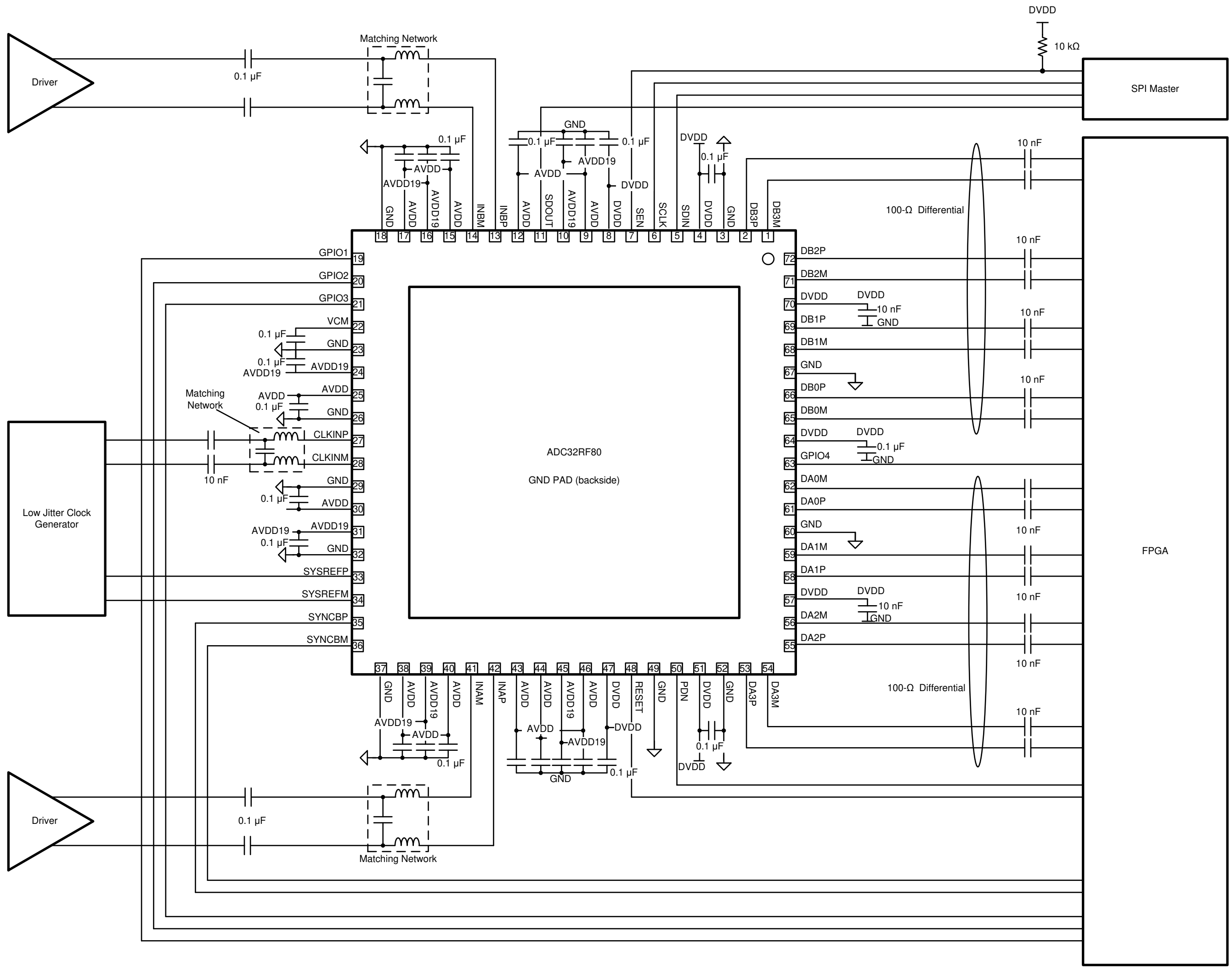


Figure 9-9. Typical Application Implementation Diagram

9.2.1 Design Requirements

9.2.1.1 Transformer-Coupled Circuits

Typical applications involving transformer-coupled circuits are discussed in this section. To ensure good amplitude and phase balance at the analog inputs, transformers (such as TC1-1-13 and TC1-1-43) can be used from the dc to 1000-MHz range and from the 1000-MHz to 4-GHz range of input frequencies, respectively. When designing the driving circuits, the ADC input impedance (or SDD11) must be considered.

By using the simple drive circuit of Figure 9-10, uniform performance can be obtained over a wide frequency range. The buffers present at the analog inputs of the device help isolate the external drive source from the switching currents of the sampling circuit.

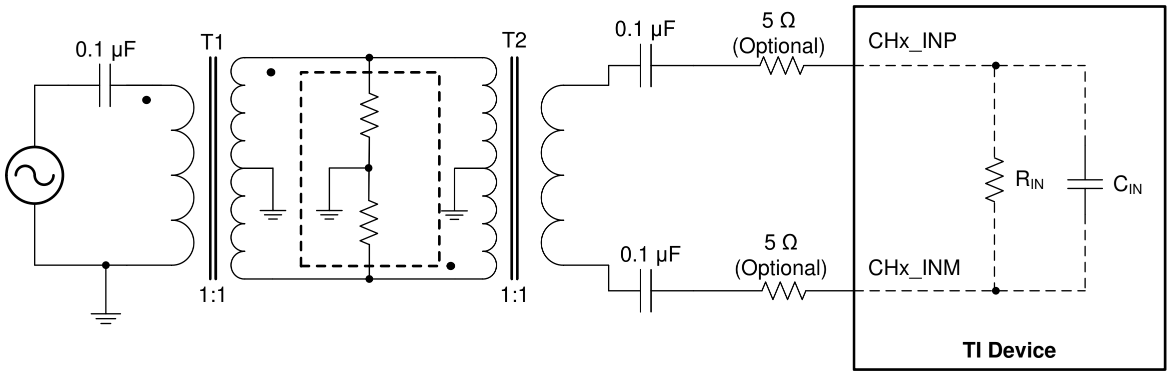


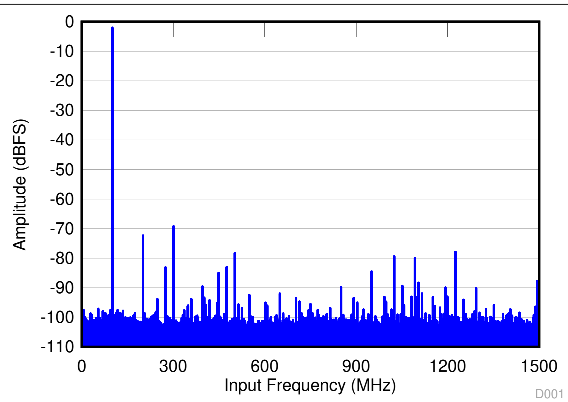
Figure 9-10. Input Drive Circuit

9.2.2 Detailed Design Procedure

For optimum performance, the analog inputs must be driven differentially. This architecture improves common-mode noise immunity and even-order harmonic rejection. A small resistor (5 Ω to 10 Ω) in series with each input pin is recommended to damp out ringing caused by package parasitics, as shown in Figure 9-10.

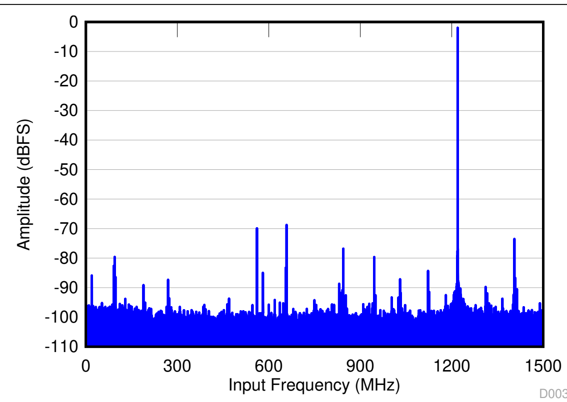
9.2.3 Application Curves

Figure 9-11 and Figure 9-12 show the typical performance at 100 MHz and 1780 MHz, respectively.



SNR = 61.8 dBFS, SINAD = 61.2 dBFS, HD2 = 71 dBc, HD3 = 75 dBc, SFDR = 71 dBc, THD = 68 dBc, IL spur = 77 dBc, worst spur = 73 dBc

Figure 9-11. FFT for 100-MHz Input Frequency



SNR = 57.9 dBFS, SINAD = 57.1 dBFS, HD2 = 63 dBc, HD3 = 66 dBc, SFDR = 63 dBc, THD = 60 dBc, IL spur = 79 dBc, worst spur = 77 dBc

Figure 9-12. FFT for 1780-MHz Input Frequency

10 Power Supply Recommendations

The DVDD power supply (1.15 V) must be stable before ramping up the AVDD19 supply (1.9 V), as shown in Figure 10-1. The AVDD supply (1.15 V) can come up in any order during the power sequence. The power supplies can ramp up at any rate and there is no hard requirement for the time delay between DVDD (1.15 V) ramping up to AVDD (1.9 V) ramping up (which can be in orders of microseconds but is recommended to be a few milliseconds).

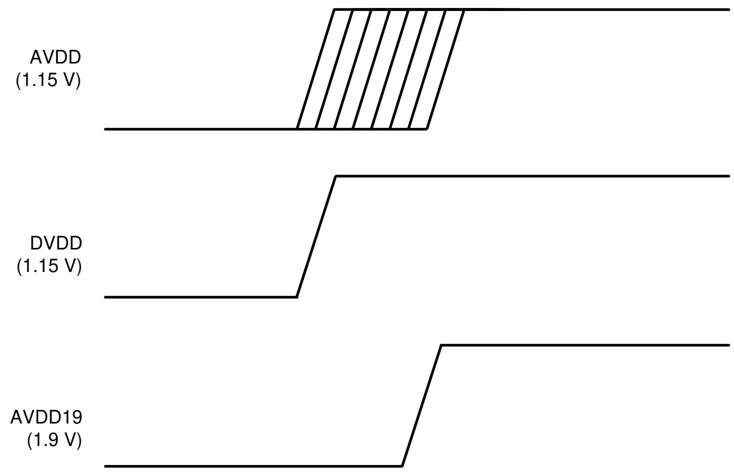


Figure 10-1. Power Sequencing for the ADC32RF8x Family of Devices

11 Layout

11.1 Layout Guidelines

The device evaluation module (EVM) layout can be used as a reference layout to obtain the best performance. A layout diagram of the EVM top layer is provided in Figure 11-1. The *ADC32RF45/RF80 EVM Quick Startup Guide* provides a complete layout of the EVM. Some important points to remember during board layout are:

- Analog inputs are located on opposite sides of the device pinout to ensure minimum crosstalk on the package level. To minimize crosstalk onboard, the analog inputs must exit the pinout in opposite directions, as shown in the reference layout of Figure 11-1 as much as possible.
- In the device pinout, the sampling clock is located on a side perpendicular to the analog inputs in order to minimize coupling. This configuration is also maintained on the reference layout of Figure 11-1 as much as possible.
- Keep digital outputs away from the analog inputs. When these digital outputs exit the pinout, the digital output traces must not be kept parallel to the analog input traces because this configuration can result in coupling from the digital outputs to the analog inputs and degrade performance. All digital output traces to the receiver [such as field-programmable gate arrays (FPGAs) or application-specific integrated circuits (ASICs)] must be matched in length to avoid skew among outputs.
- At each power-supply pin (AVDD, DVDD, or AVDD19), keep a 0.1-µF decoupling capacitor close to the device. A separate decoupling capacitor group consisting of a parallel combination of 10-µF, 1-µF, and 0.1-µF capacitors can be kept close to the supply source.

11.2 Layout Example

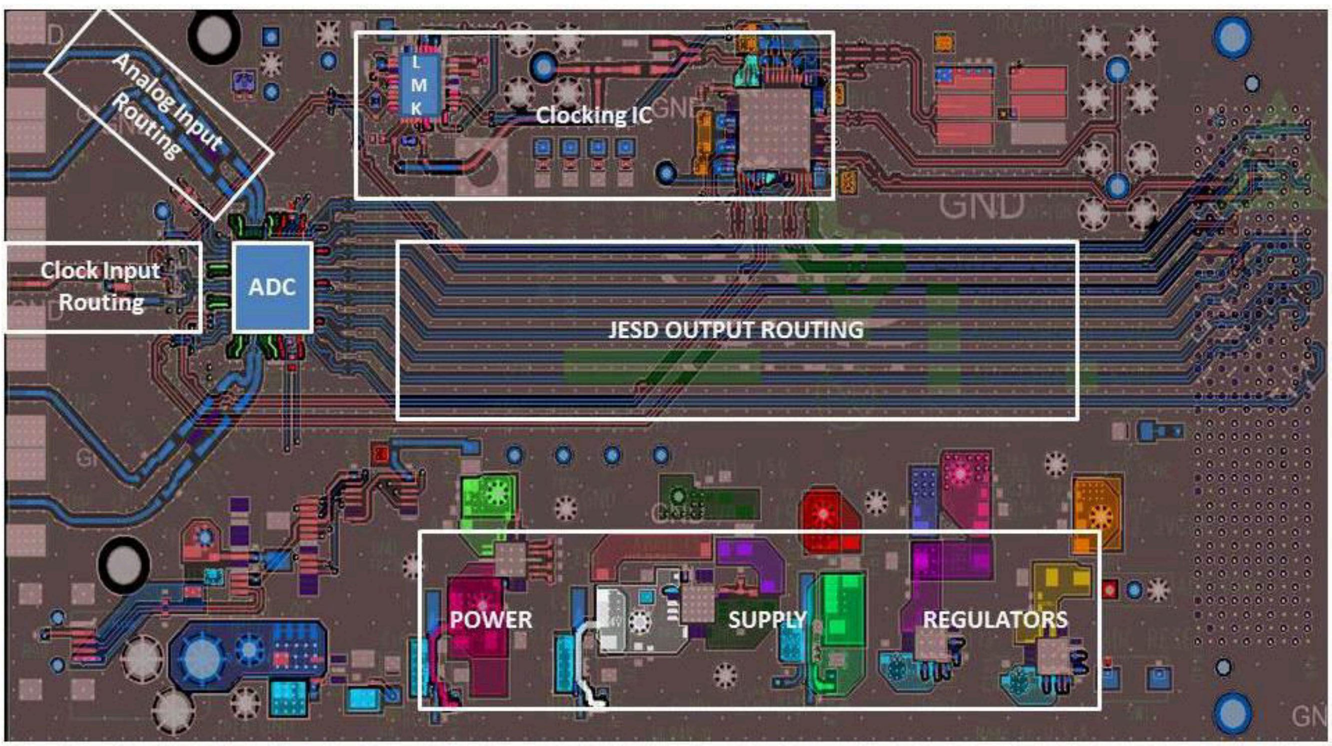


Figure 11-1. ADC32RF8xEVM Layout

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *ADC32RF45/RF80 EVM Quick Startup Guide*
- *Configuration Files for the ADC32RF45*

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADC32RF80IRMPR	ACTIVE	VQFN	RMP	72	1500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ32RF80	Samples
ADC32RF80IRMPT	ACTIVE	VQFN	RMP	72	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ32RF80	Samples
ADC32RF80IRRHR	ACTIVE	VQFN	RRH	72	1500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ32RF80	Samples
ADC32RF80IRRHT	ACTIVE	VQFN	RRH	72	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ32RF80	Samples
ADC32RF83IRMPR	ACTIVE	VQFN	RMP	72	1500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ32RF83	Samples
ADC32RF83IRMPT	ACTIVE	VQFN	RMP	72	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ32RF83	Samples
ADC32RF83IRRHR	ACTIVE	VQFN	RRH	72	1500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ32RF83	Samples
ADC32RF83IRRHT	ACTIVE	VQFN	RRH	72	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ32RF83	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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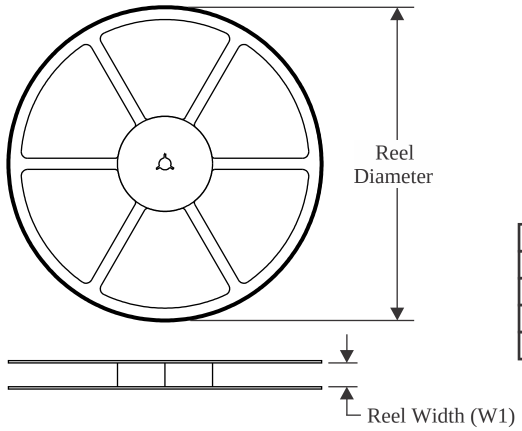
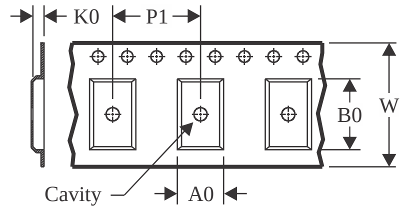
TAPE AND REEL INFORMATION

REEL DIMENSIONS

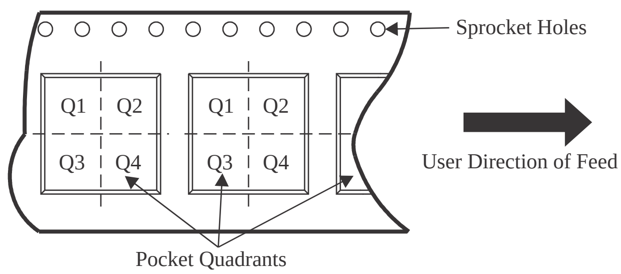


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

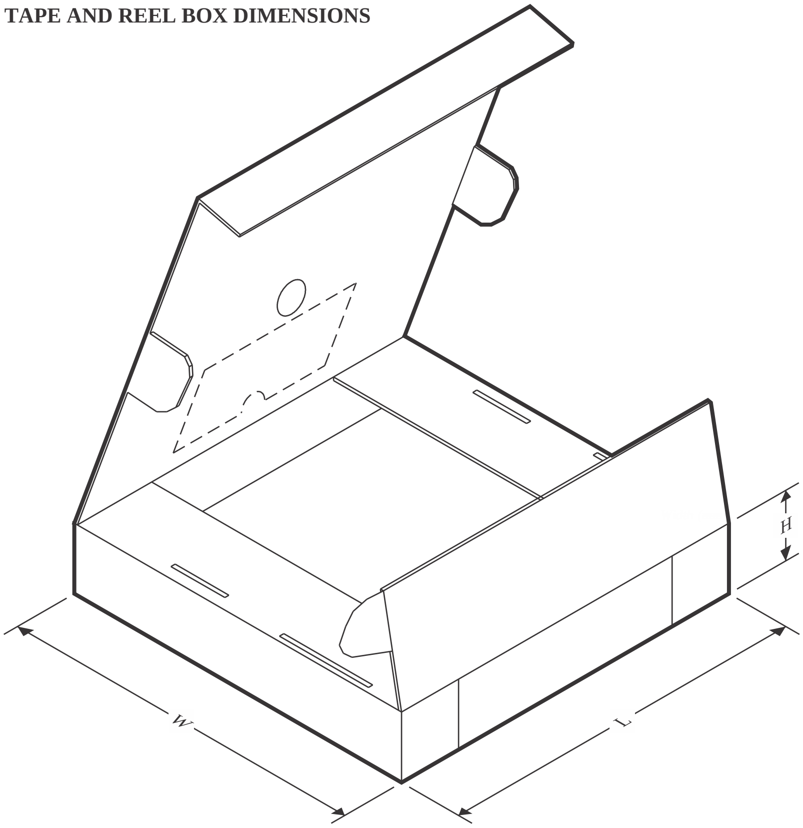
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

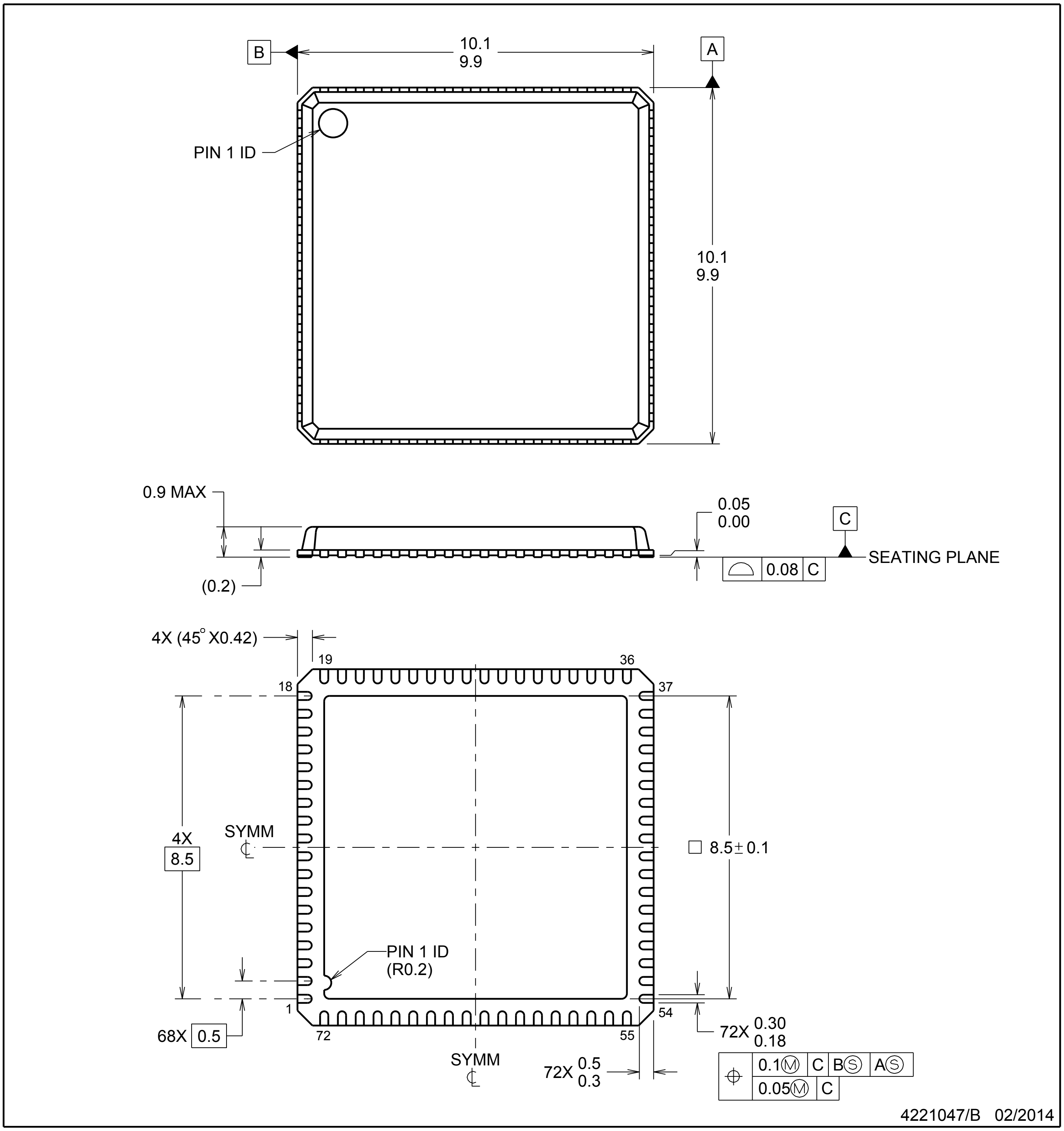
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC32RF80IRMPR	VQFN	RMP	72	1500	330.0	24.4	10.25	10.25	2.25	16.0	24.0	Q2
ADC32RF80IRRHR	VQFN	RRH	72	1500	330.0	24.4	10.25	10.25	2.25	16.0	24.0	Q2
ADC32RF83IRMPR	VQFN	RMP	72	1500	330.0	24.4	10.25	10.25	2.25	16.0	24.0	Q2
ADC32RF83IRRHR	VQFN	RRH	72	1500	330.0	24.4	10.25	10.25	2.25	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



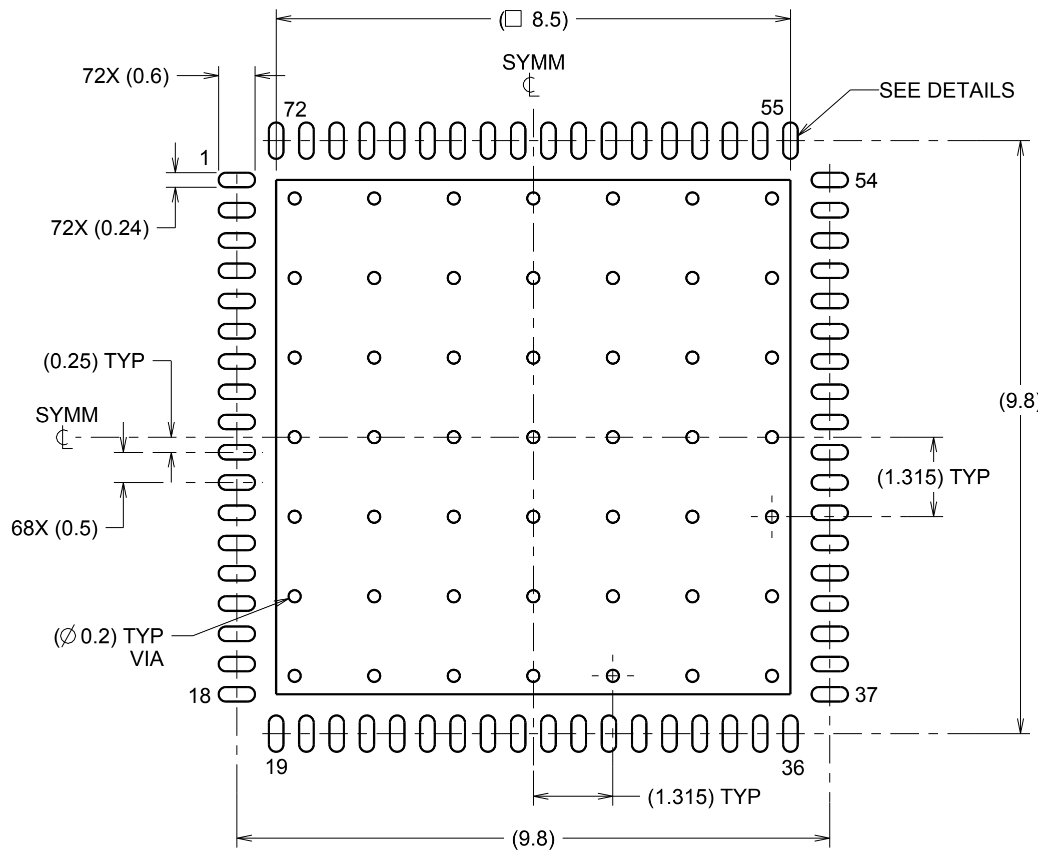
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC32RF80IRMPR	VQFN	RMP	72	1500	350.0	350.0	43.0
ADC32RF80IRRHR	VQFN	RRH	72	1500	350.0	350.0	43.0
ADC32RF83IRMPR	VQFN	RMP	72	1500	350.0	350.0	43.0
ADC32RF83IRRHR	VQFN	RRH	72	1500	350.0	350.0	43.0

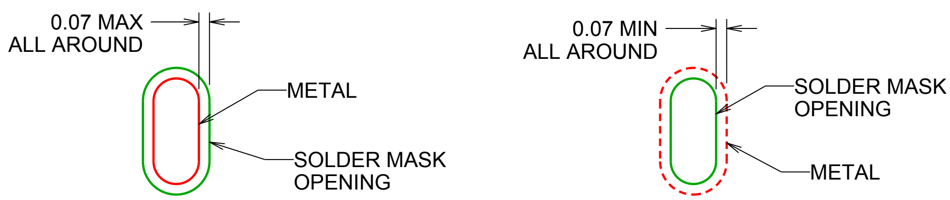


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:8X



NON SOLDER MASK DEFINED (PREFERRED)

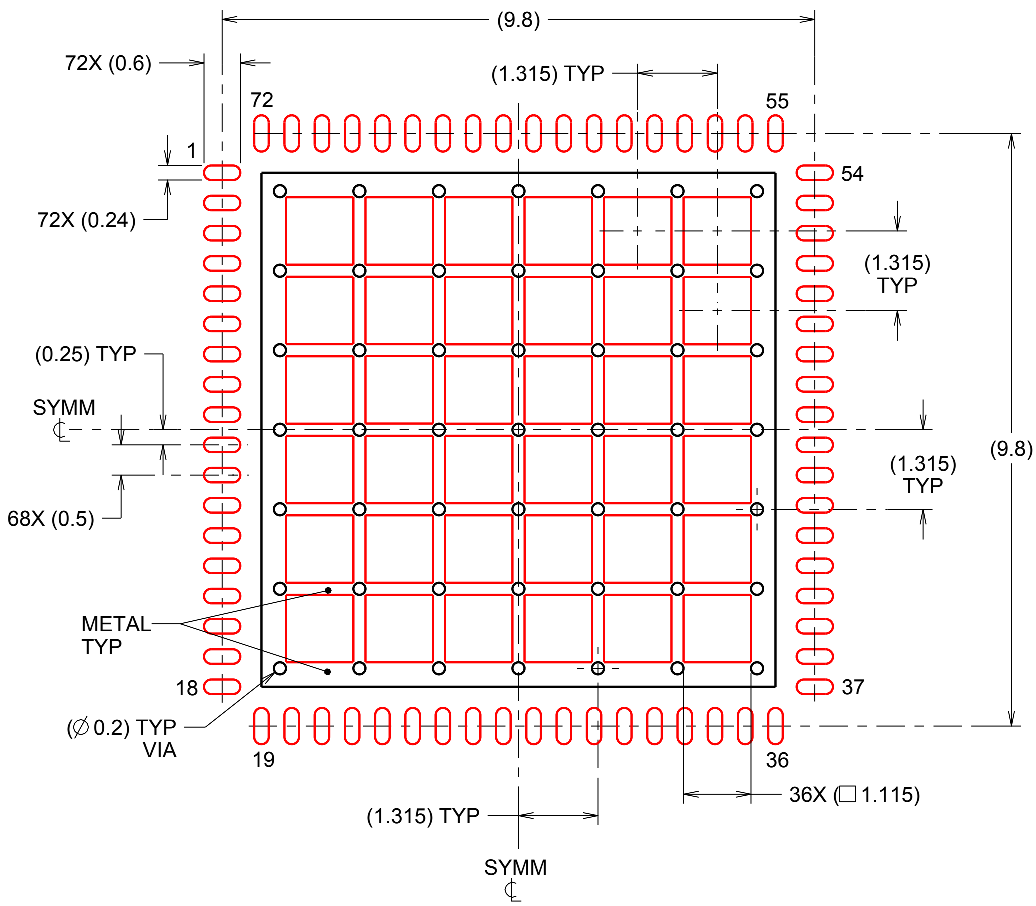
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221047/B 02/2014

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

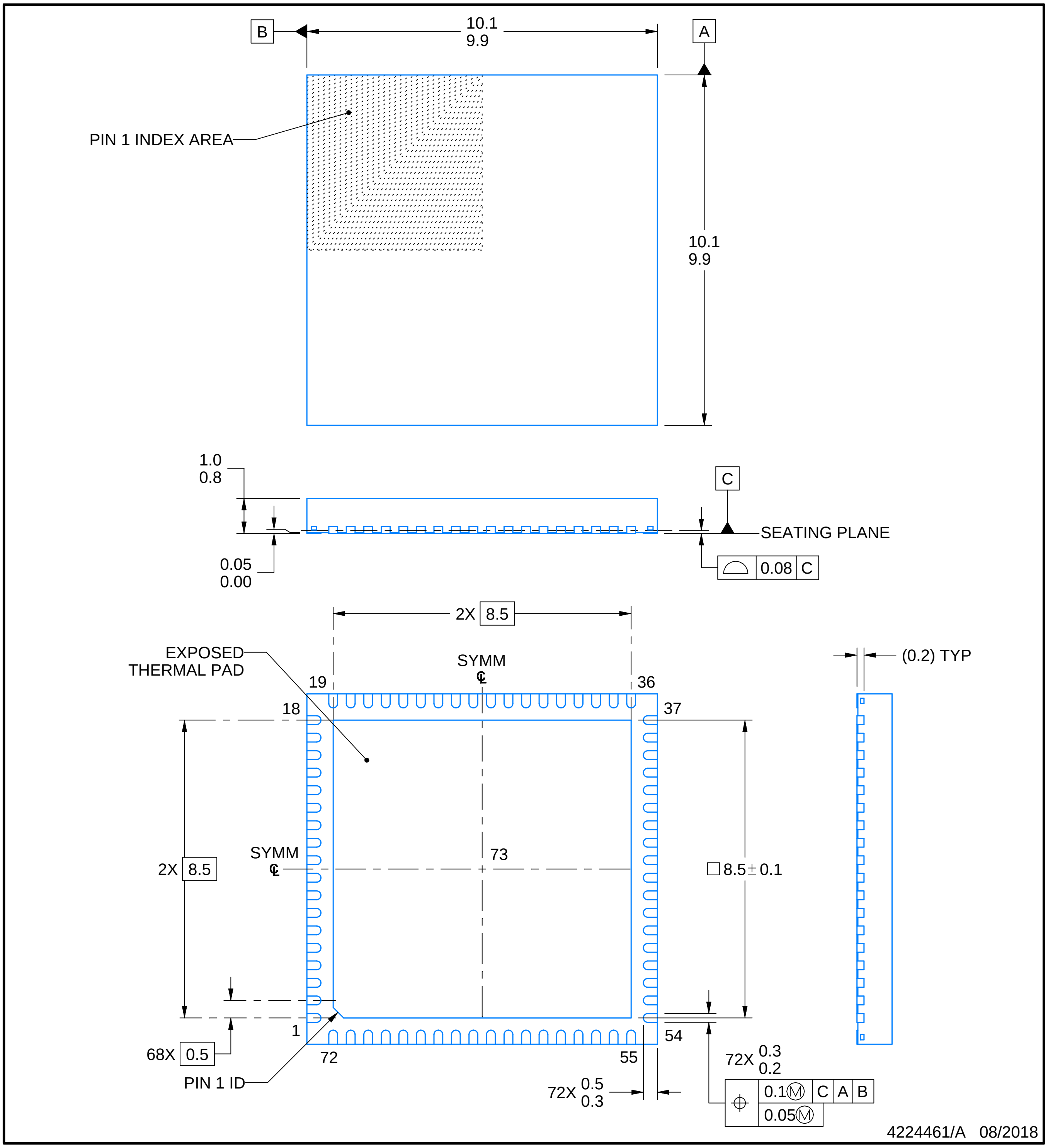


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
62% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

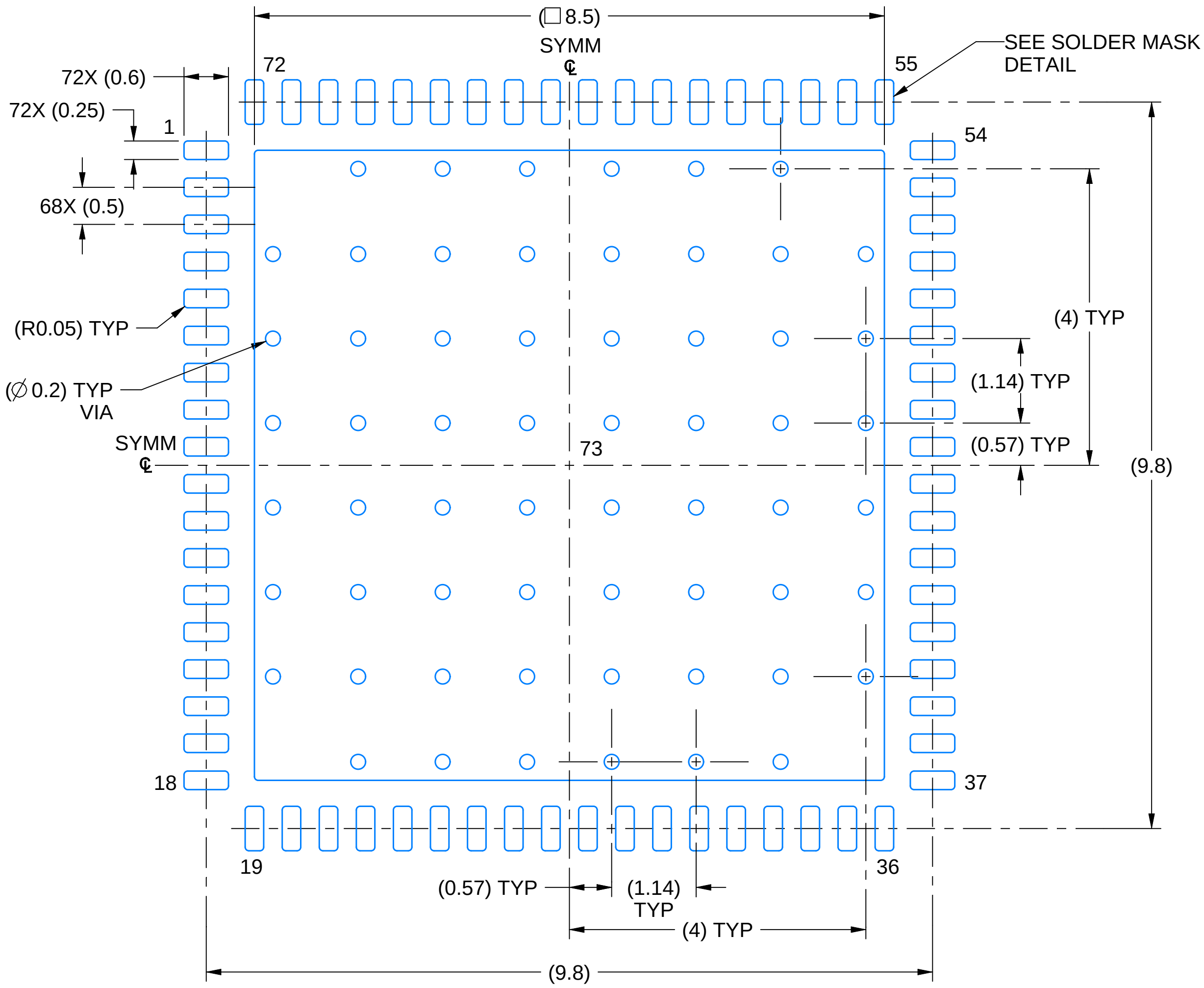
NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

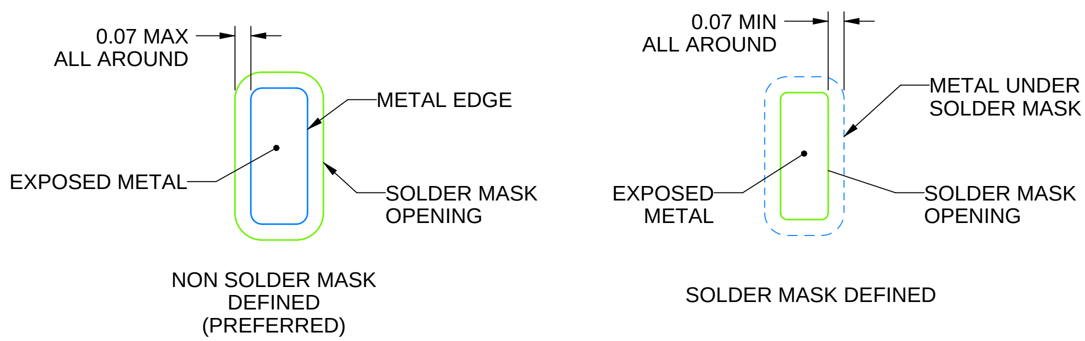


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

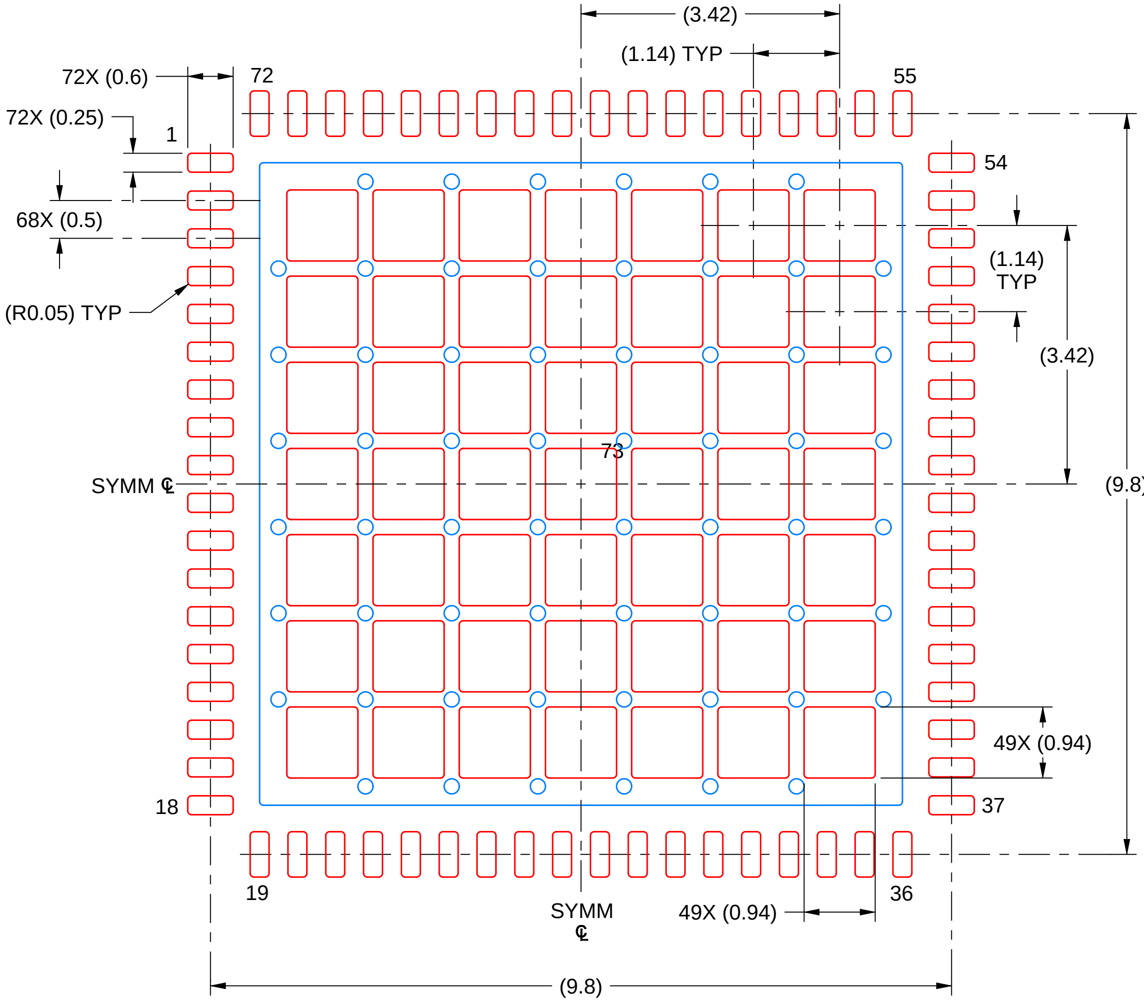


SOLDER MASK DETAILS

4224461/A 08/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 73
60% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4224461/A 08/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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