

XS5A1T4157

Low-ohmic single-pole double-throw analog switch

Rev. 2 — 9 February 2022

Product data sheet

1. General description

The XS5A1T4157 is a low-ohmic single-pole double-throw analog switch suitable for use as an analog or digital 2:1 multiplexer/demultiplexer. It has a digital select input (S), two inputs/outputs (Y0 and Y1) and a common input/output (Z).

The XS5A1T4157 passes analog and digital voltages that may vary across the full voltage supply range (GND to V_{CC}).

2. Features and benefits

- Supply voltage range from $V_{CC} = 4.5\text{ V}$ to 5.5 V
- Very low ON resistance: $4\ \Omega$ (typical) at $V_{CC} = 5\text{ V}$
- Switch inputs voltage range: $V_{SW} = \text{GND to } V_{CC}$
- Control input voltage range: $V_{I(S)} = \text{GND to } V_{CC}$
- Latch-up performance exceeds 200 mA per JESD 78 Class II level A
- ESD protection:
 - HBM: ANSI/ESDA/Jedec JS-001 Class 2 exceeds 2 kV
 - CDM: ANSI/ESDA/Jedec JS-002 Class C3 exceeds 1 kV
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
XS5A1T4157GW	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	TSSOP6	plastic thin shrink small outline package; 6 leads; body width 1.25 mm	SOT363-2

4. Marking

Table 2. Marking codes

Type number	Marking code ^[1]
XS5A1T4157GW	zb

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

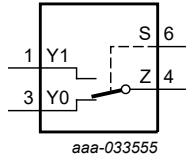


Fig. 1. Logic symbol

6. Pinning information

6.1. Pinning

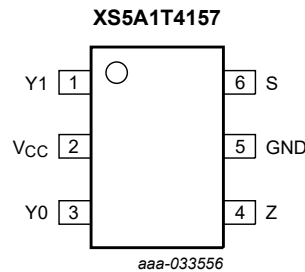


Fig. 2. Pin configuration SOT363-2 (TSSOP6)

6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
Y1	1	independent input or output
V _{CC}	2	supply voltage
Y0	3	independent input or output
Z	4	common output or input
GND	5	ground (0 V)
S	6	select input

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level.

Input	Channel on
S	
L	Y0
H	Y1

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
V_I	input voltage	S input [1]	-0.5	+6.5	V
I_{IK}	input clamping current	S input; $V_I < -0.5$ V	-50	-	mA
I_{SK}	switch clamping current	Z, Y0 and Y1 inputs/outputs; $V_{SW} < -0.5$ V or $V_{SW} > V_{CC} + 0.5$ V	-	± 50	mA
V_{SW}	switch voltage	Z, Y0 and Y1 inputs/outputs [2]	-0.5	$V_{CC} + 0.5$	V
I_{SW}	switch current	Z, Y0 and Y1 inputs/outputs; -0.5 V $< V_{SW} < V_{CC} + 0.5$ V [3]	-	± 128	mA
$T_{J(max)}$	maximum junction temperature		-	+150	°C
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C [4]	-	250	mW

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.

[2] The minimum and maximum switch voltage ratings may be exceeded if the switch clamping current rating is observed.

[3] Continuous current sustained maximum of 2 years.

[4] For SOT363-2 (TSSOP6) package: P_{tot} derates linearly with 3.7 mW/K above 83 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		4.5	5.5	V
V_I	input voltage	S input	0	5.5	V
V_{SW}	switch voltage	Z, Y0 and Y1 inputs/outputs	0	V_{CC}	V
I_{SW}	switch current	Z, Y0 and Y1 inputs/outputs; -0.5 V $< V_{SW} < V_{CC} + 0.5$ V	-	± 64	mA
T_{amb}	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	S input	-	100	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground 0 V).

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +125 °C			Unit
			Min	Typ[1]	Max	
V _{IH}	HIGH-level input voltage	S input; V _{CC} = 4.5 V to 5.5 V	1.4	-	-	V
V _{IL}	LOW-level input voltage	S input; V _{CC} = 4.5 V to 5.5 V	-	-	0.3	V
I _I	input leakage current	S input; V _{I(S)} = 5.5 V	-50	0.2	50	nA
I _{S(OFF)}	OFF-state leakage current	V _{I(S)} = V _{IL} or V _{IH} ; V _I = 1.5 V or 4.5 V; V _O = 4.5 V or 1.5 V; V _{CC} = 5.0 V; see Fig. 3	-320	±0.02	320	nA
I _{S(ON)}	ON-state leakage current	V _{I(S)} = V _{IL} or V _{IH} ; V _I = V _O = 1 V or 4.5 V; V _{CC} = 5.0 V; see Fig. 4	-320	±0.02	320	nA
I _{CC}	supply current	V _{I(S)} = GND or V _{CC} ; V _{SW} = GND or V _{CC} ; V _{CC} = 5.0 V	-	0.6	8000	nA
		V _{I(S)} = 1.8 V; V _{SW} = GND or V _{CC} ; V _{CC} = 5.0 V; see Fig. 5	-	90	-	µA
C _I	input capacitance	S input; V _{CC} = 5.0 V	-	2	-	pF
C _{S(OFF)}	OFF-state capacitance	Y0, Y1 input/output; V _{CC} = 5.0 V; see Fig. 6	-	11	-	pF
C _{S(ON)}	ON-state capacitance	Z input/output; V _{CC} = 5.0 V; see Fig. 7	-	35	-	pF

[1] Typical values are measured at T_{amb} = 25 °C.

10.1. Test circuits and graphs

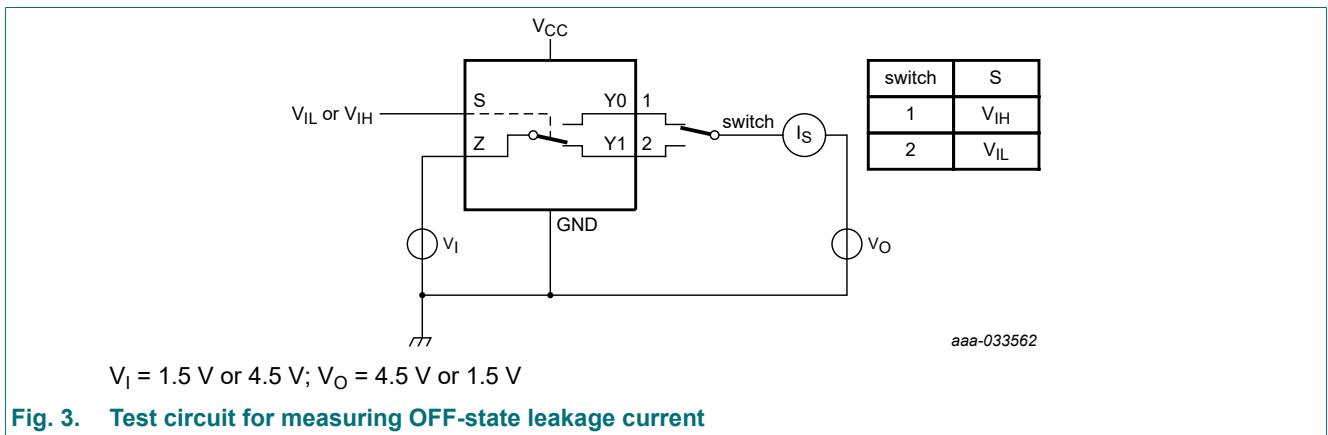
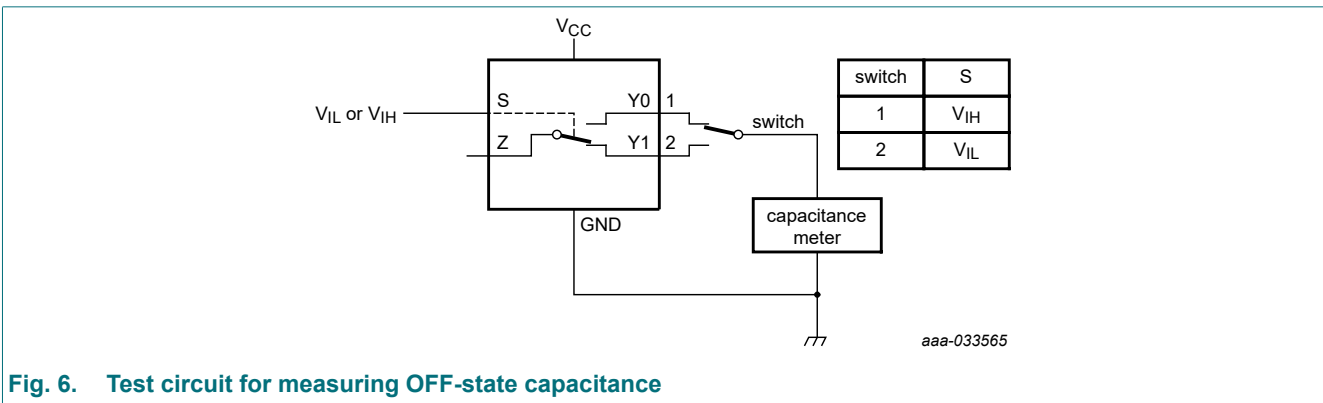
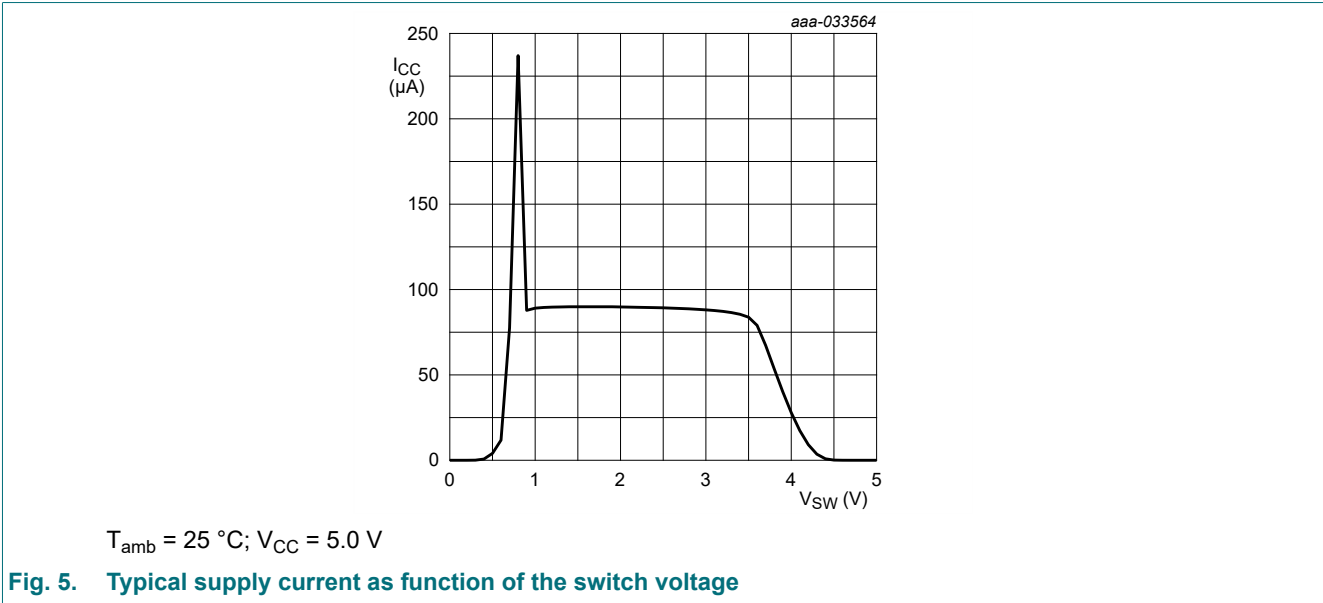
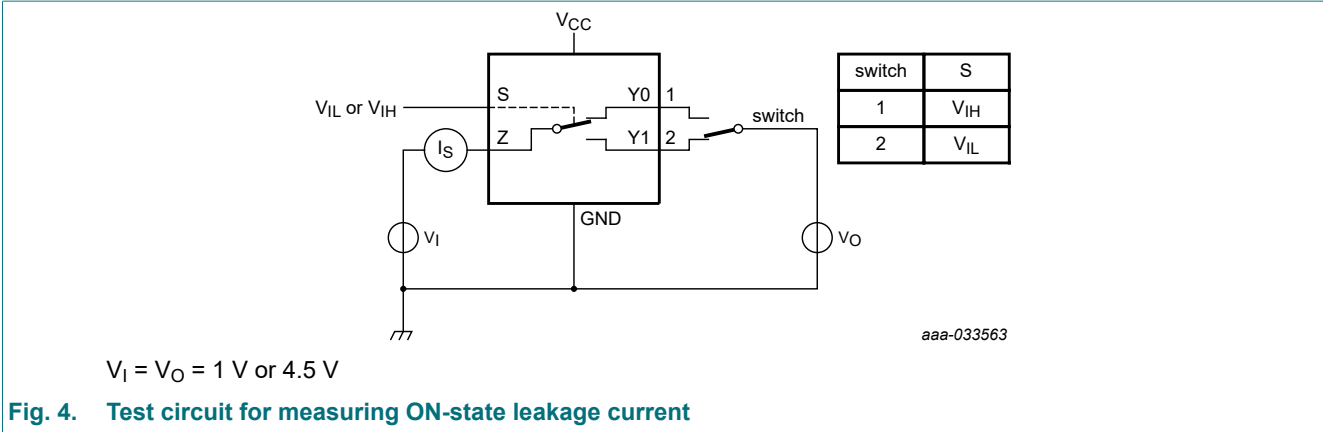


Fig. 3. Test circuit for measuring OFF-state leakage current



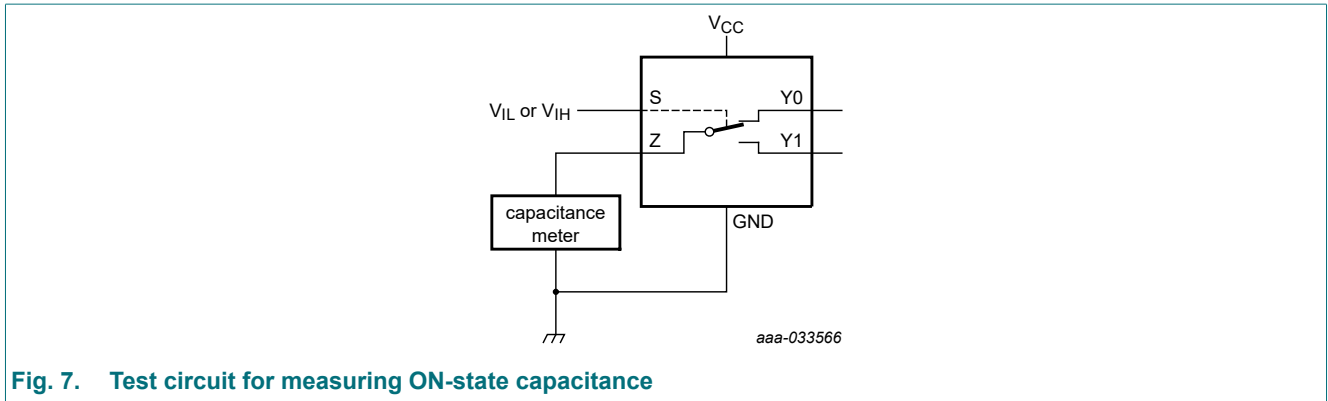


Fig. 7. Test circuit for measuring ON-state capacitance

10.2. ON resistance

Table 8. ON resistance

At recommended operating conditions; voltages are referenced to GND (ground 0 V);
For test circuit see Fig. 8; for graphs see Fig. 9 and Fig. 10.

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +125 °C			Unit
			Min	Typ[1]	Max	
R _{ON(peak)}	ON resistance (peak)	V _{I(S)} = V _{IL} or V _{IH} ; V _{I(Z)} = GND to V _{CC} ; V _{CC} = 4.5 V to 5.5 V [2]				
		I _{SW} = 10 mA	2.2	4.0	7.5	Ω
		I _{SW} = 32 mA	2.2	4.0	7.7	Ω
		I _{SW} = 64 mA	2.2	4.0	7.7	Ω
ΔR _{ON}	ON resistance mismatch between channels	I _{SW} = 64 mA; V _{I(Z)} = GND to V _{CC} ; V _{CC} = 4.5 V to 5.0 V [2]	-	90	-	mΩ
R _{ON(flat)}	ON resistance (flatness)	V _{I(S)} = V _{IL} or V _{IH} ; V _{I(Z)} = GND to V _{CC} ; V _{CC} = 4.5 V to 5.0 V [2] [3]				
		I _{SW} = 10 mA	0.2	0.8	3	Ω
		I _{SW} = 32 mA	0.2	0.8	3	Ω
		I _{SW} = 64 mA	0.2	0.9	3	Ω

- [1] Typical values are measured at T_{amb} = 25 °C.
- [2] Measured by the voltage drop between Z and Yn pins at the indicated current through the switch. ON resistance is determined by the lower of the voltages on the two (Z or Yn pins).
- [3] Flatness is defined as the difference between the maximum and minimum value of ON resistance over the specified range of conditions.

10.3. ON resistance test circuit and graphs

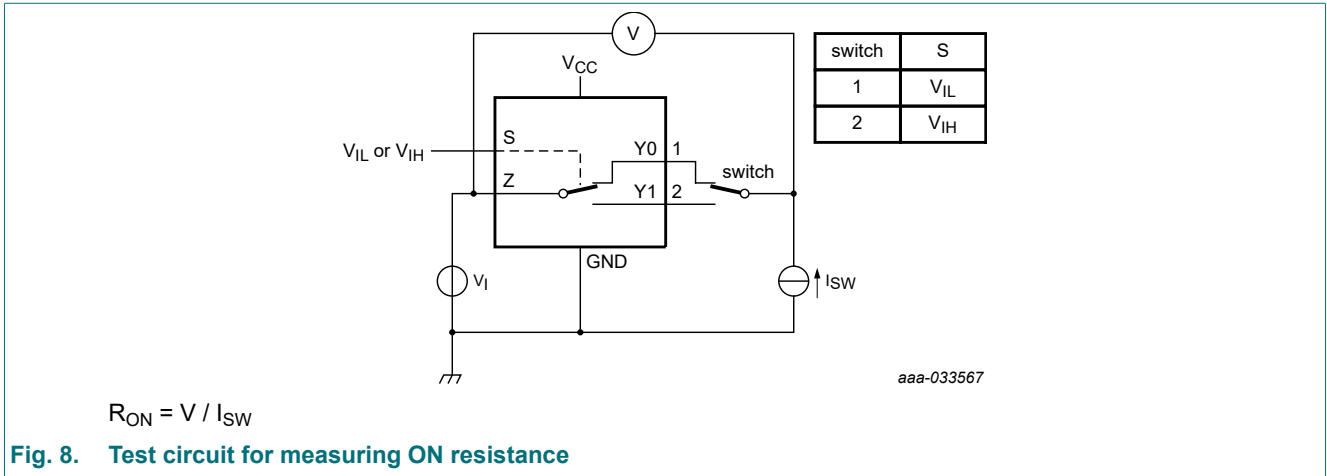


Fig. 8. Test circuit for measuring ON resistance

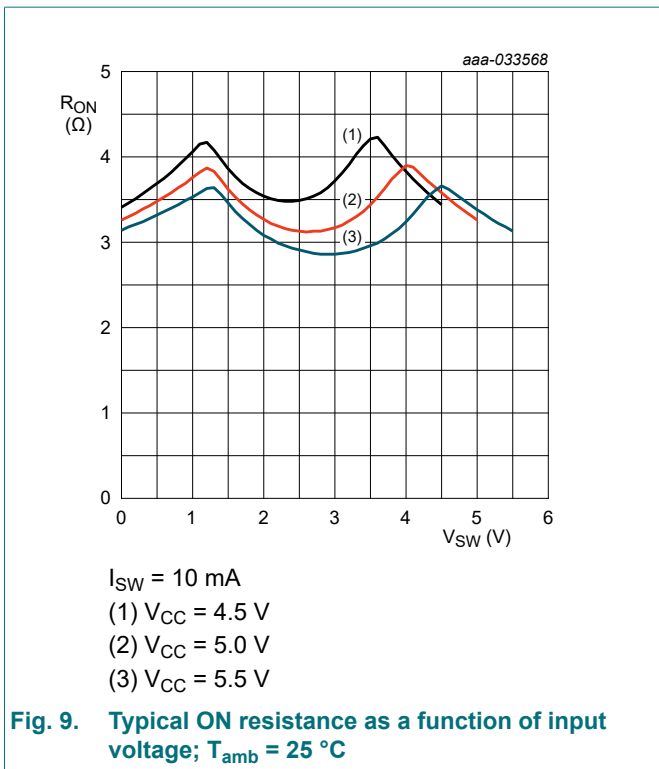


Fig. 9. Typical ON resistance as a function of input voltage; $T_{amb} = 25 \text{ }^\circ\text{C}$

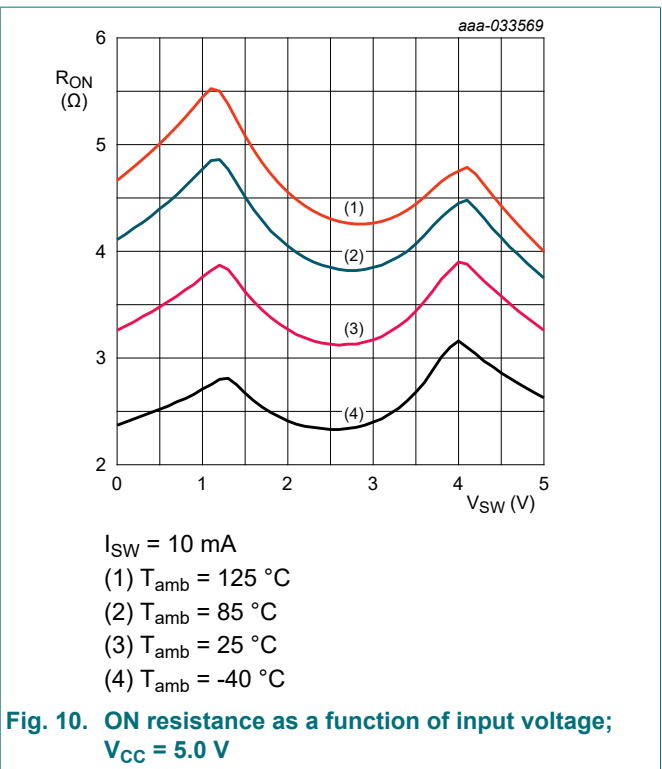


Fig. 10. ON resistance as a function of input voltage; $V_{CC} = 5.0 \text{ V}$

11. Dynamic characteristics

Table 9. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +125 °C			Unit
			Min	Typ[1]	Max	
t _{pd}	propagation delay	Z to Y _n or Y _n to Z; see Fig. 11 and Fig. 13; V _{CC} = 4.5 V to 5.5 V	-	0.4	1.0	ns
t _{TRAN}	transition time between channels	S to Z or Y _n ; see Fig. 12 and Fig. 14; V _{CC} = 4.5 V to 5.5 V	10	23	40	ns
t _{b-m}	break-before-make time	C _L = 15 pF; R _L = 200 Ω; see Fig. 15; V _{CC} = 4.5 V to 5.5 V	1	7.5	17	ns

[1] Typical values are measured at T_{amb} = 25 °C.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

11.1. Waveforms and test circuits

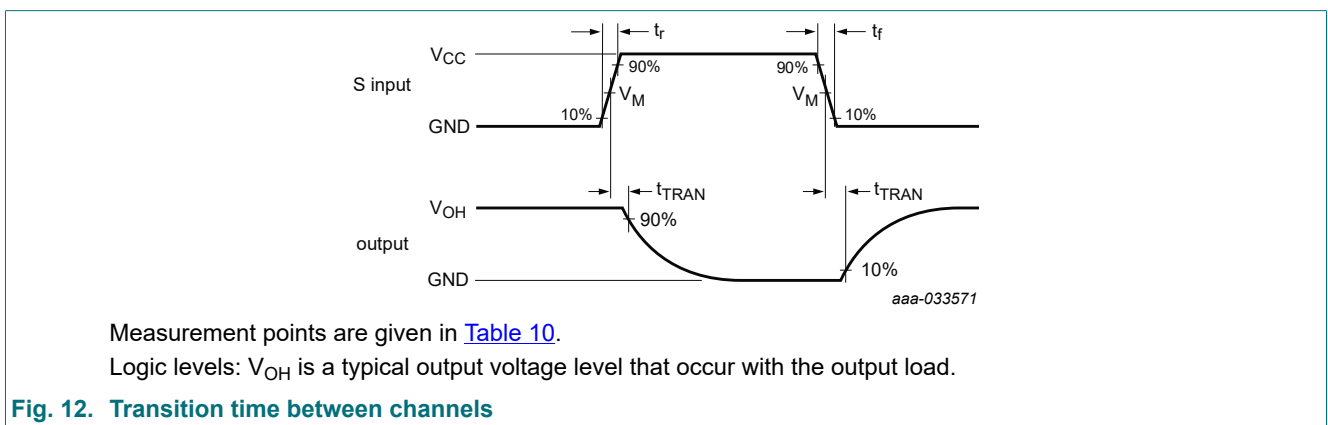
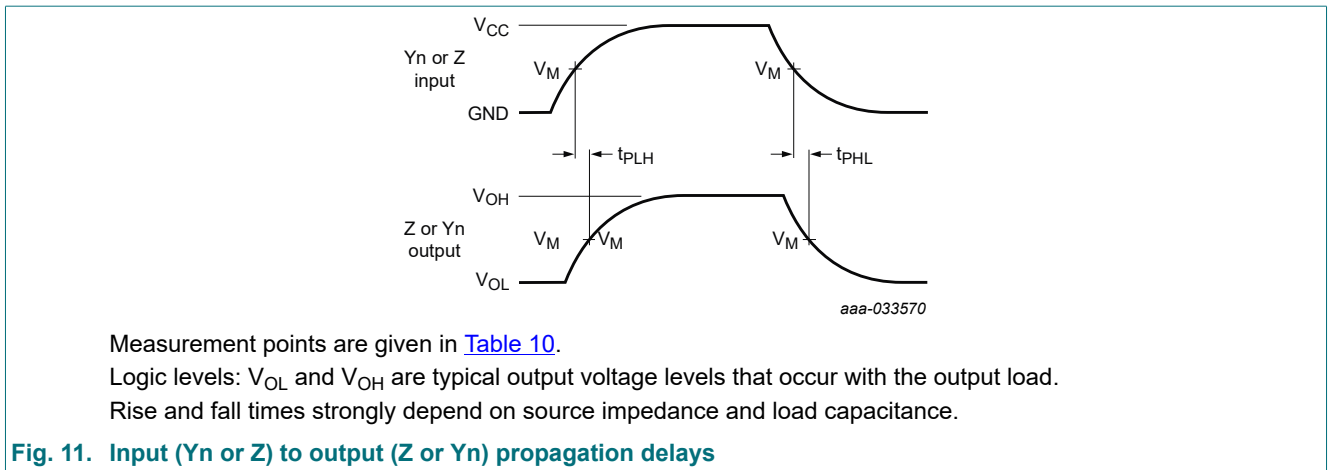
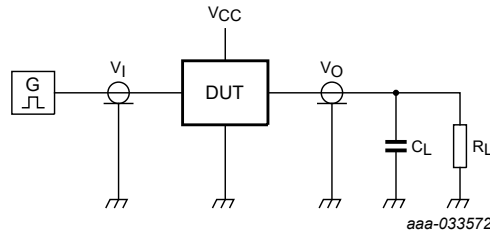


Table 10. Measurement points

Supply voltage	Input	Output
V _{CC}	V _M	V _M
GND to V _{CC}	50%	50%



Test data is given in [Table 11](#).

All input pulses are supplied by generators having the following characteristics:

PRR ≤ 10 MHz; Z_O = 50 Ω; t_r, t_f = 2 ns.

Definitions test circuit:

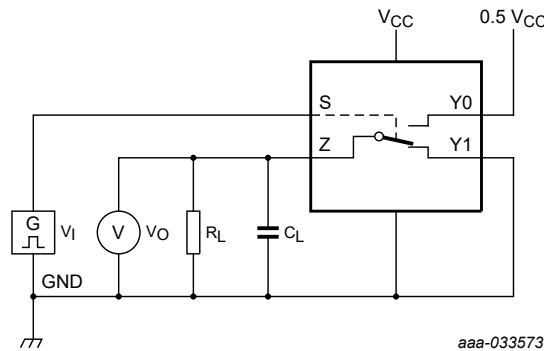
C_L = Load capacitance (including jig and probe capacitance).

R_L = Load resistance.

Fig. 13. Test circuit for measuring propagation delay times

Table 11. Test data

Load	
C _L	R _L
100 pF	1 MΩ



Test data is given in [Table 12](#).

All input pulses are supplied by generators having the following characteristics:

PRR ≤ 10 MHz; Z_O = 50 Ω.

Definitions test circuit:

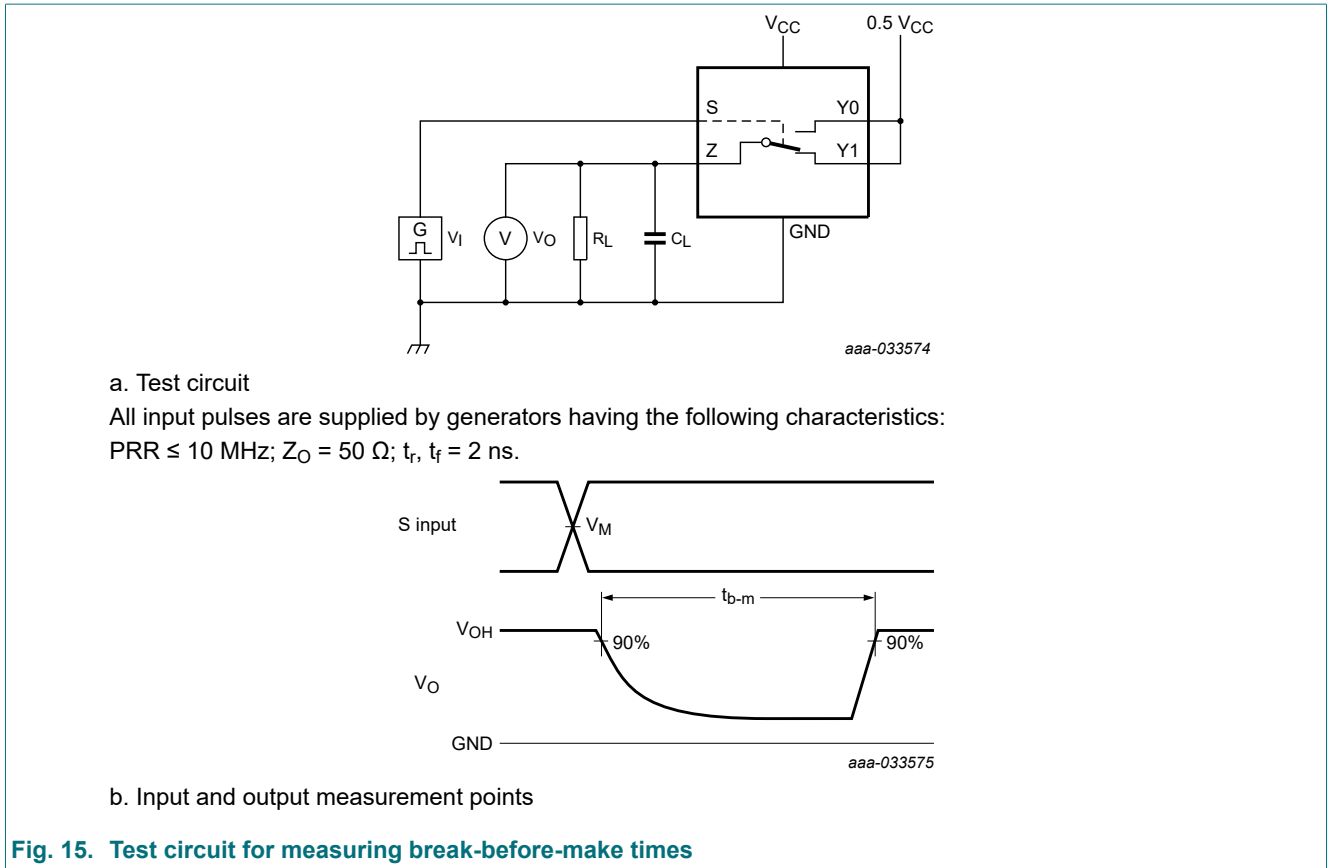
C_L = Load capacitance (including jig and probe capacitance).

R_L = Load resistance.

Fig. 14. Test circuit for measuring transition times between channels

Table 12. Test data

Input S	Load	
t _r , t _f	C _L	R _L
≤ 2 ns	15 pF	1 MΩ



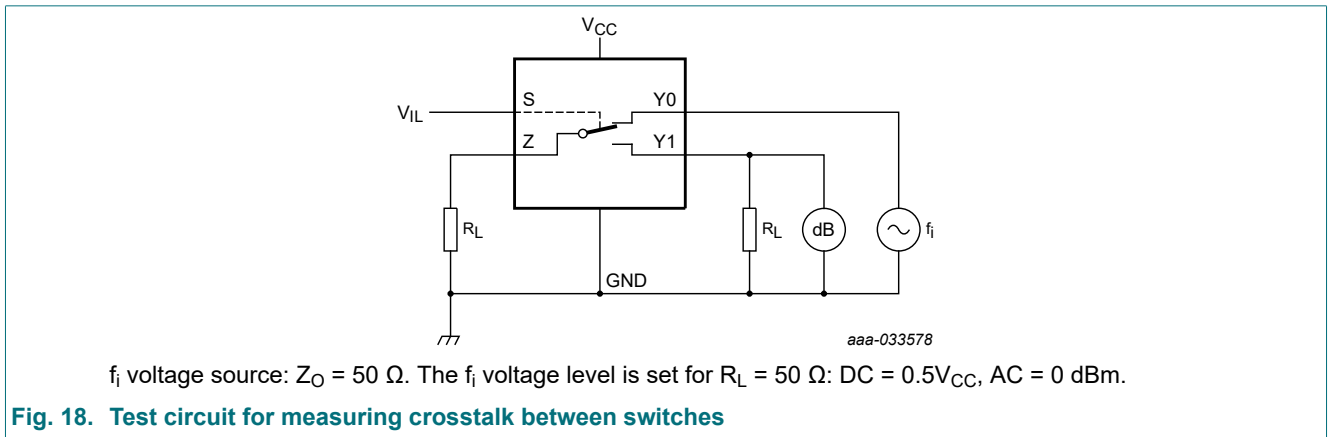
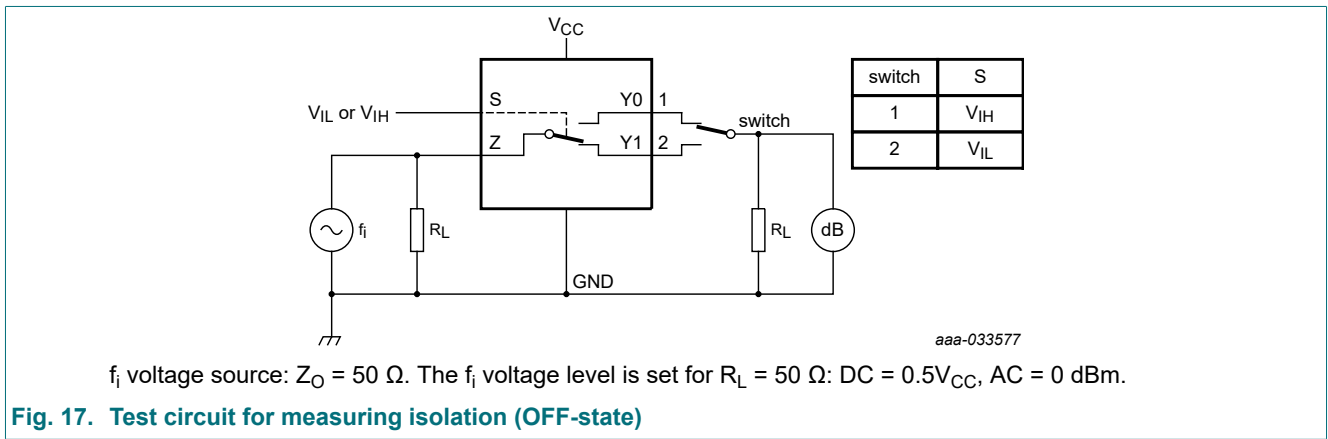
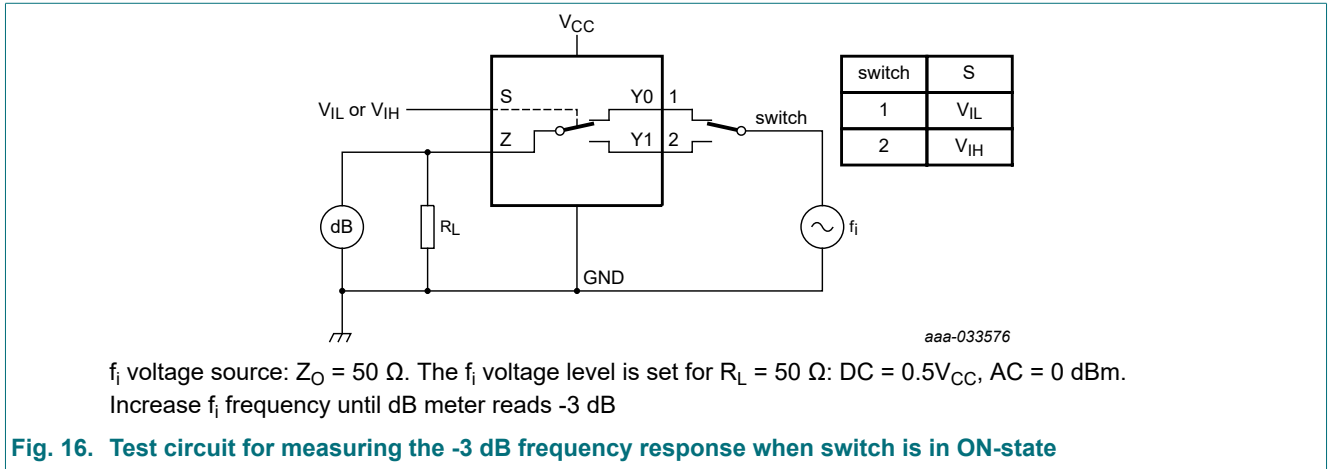
11.2. Additional dynamic characteristics

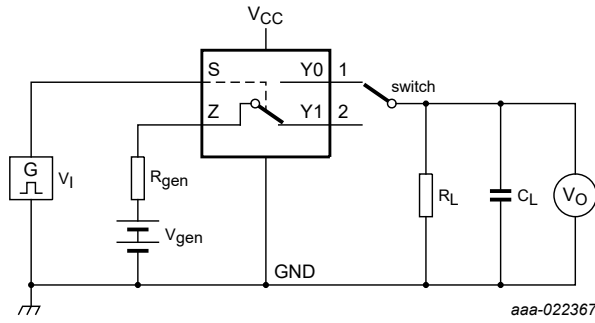
Table 13. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

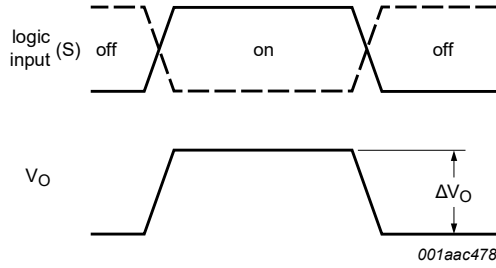
Symbol	Parameter	Conditions	$T_{amb} = 25 \text{ }^\circ\text{C}$			
			Min	Typ	Max	Unit
$f_{(-3\text{dB})}$	-3 dB frequency response	$R_L = 50 \Omega$; see Fig. 16; $V_{CC} = 5.0 \text{ V}$	-	190	-	MHz
α_{iso}	isolation (OFF-state)	$R_L = 50 \Omega$; $f_i = 10 \text{ MHz}$; see Fig. 17; $V_{CC} = 5.0 \text{ V}$	-	-56	-	dB
Xtalk	crosstalk	between switches; $R_L = 50 \Omega$; $f_i = 1 \text{ MHz}$; $V_{CC} = 5.0 \text{ V}$; see Fig. 18	-	-76	-	dB
Q_{inj}	charge injection	$C_L = 1 \text{ nF}$; $V_{gen} = 0.5V_{CC}$; $R_{gen} = 0 \Omega$; $f_i = 1 \text{ MHz}$; $R_L = 1 \text{ M}\Omega$; $V_{CC} = 5.0 \text{ V}$; see Fig. 19	-	4.5	-	pC

11.3. Test circuits





a. Test circuit



b. Input and output pulse definitions

Definitions for test circuit:

$$Q_{inj} = \Delta V_O \times C_L;$$

ΔV_O = output voltage variation;

R_{gen} = generator resistance;

V_{gen} = generator voltage.

Fig. 19. Test circuit for measuring charge injection

12. Package outline

TSSOP6: plastic thin shrink small outline package; 6 leads; body width 1.25 mm

SOT363-2

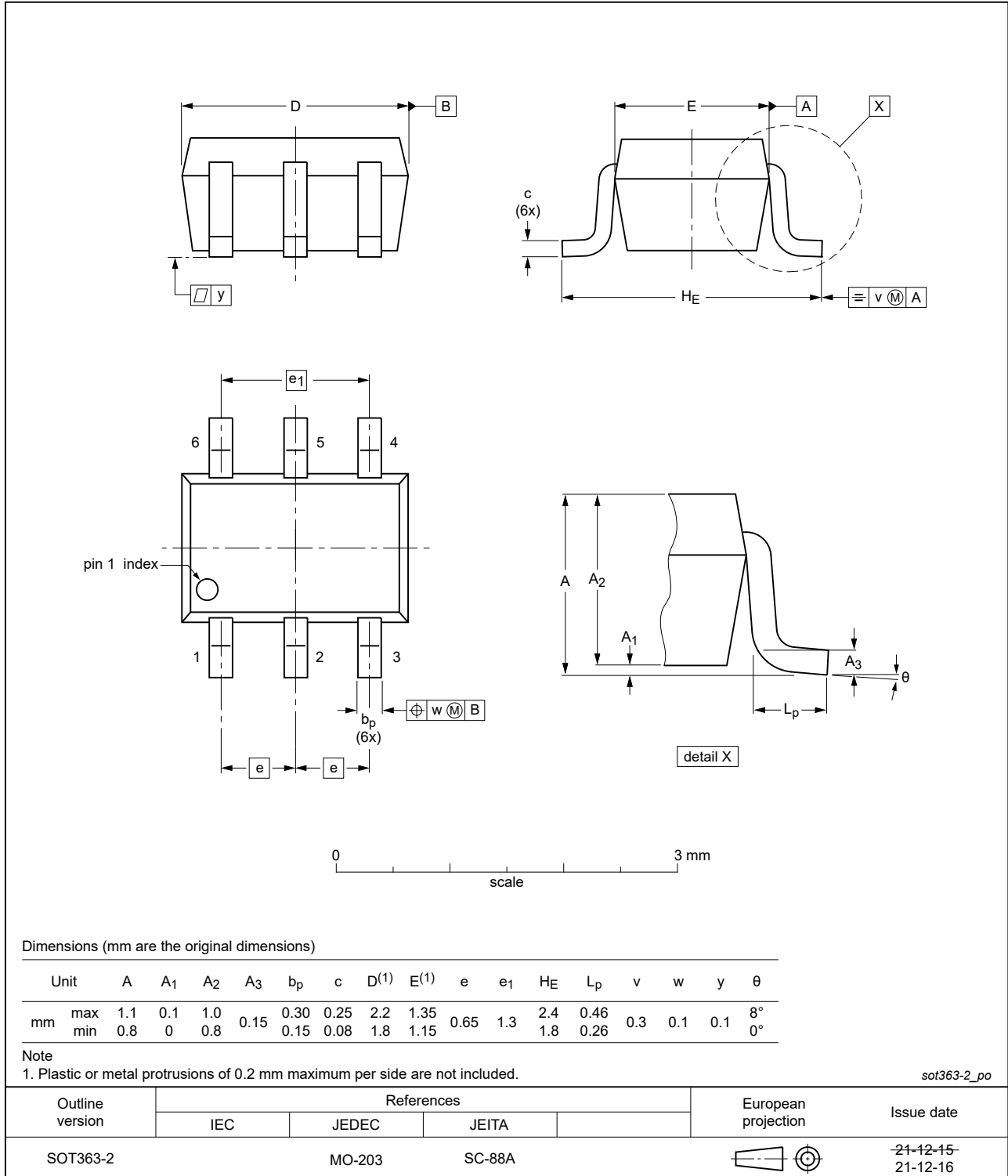


Fig. 20. Package outline SOT363-2 (TSSOP6)

13. Abbreviations

Table 14. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
PRR	Pulse Rate Repetition

14. Revision history

Table 15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
XS5A1T4157 v.2	20220209	Product data sheet	-	XS5A1T4157 v.1
Modifications:	<ul style="list-style-type: none"> Package SOT363 (SC-88) changed to SOT363-2 (TSSOP6). 			
XS5A1T4157 v.1	20210716	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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