LUMISSIL MICROSYSTEMS

A Division of ISSI

X1600/E

AIoT Application Processor

Data Sheet

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1. Overview

X1600/E is a low power consumption, high performance and high integrated application processor, the application is focus on IoT devices. And it can match the requirements of many other embedded products.

NAME	SIP DDR
X1600	32MB, LPDDR2
X1600E	64MB, LPDDR2

1.1 Block Diagram

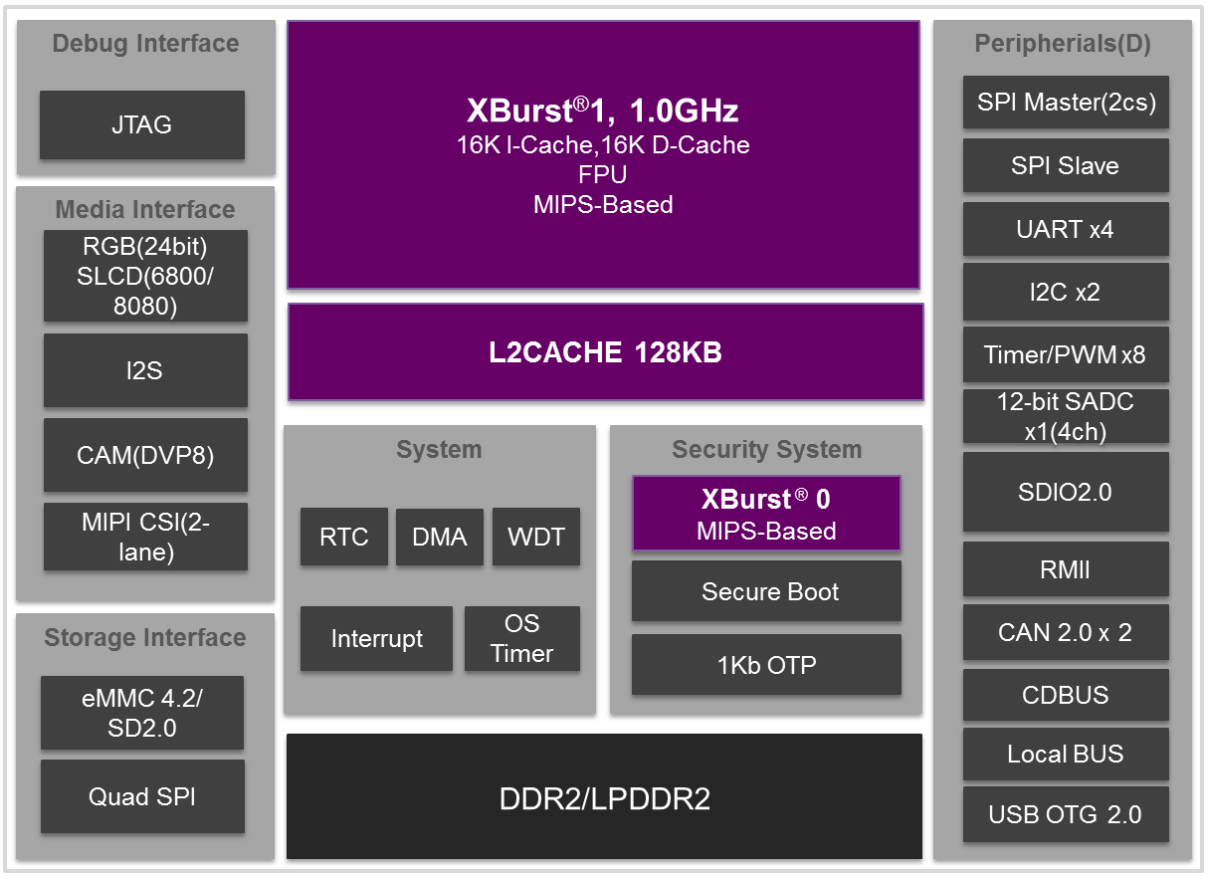


Figure 1-1 X1600/E Diagram

1.2 Features

1.2.1 CPU Core

- XBurst® core
  - XBurst® FPU instruction set supporting both single and double floating point format which are IEEE754 compatible
  - XBurst® 9-stage pipeline micro-architecture, the operating frequency is 1.0GHz
- MMU
  - 32-entry joint-TLB
  - 8 entry instruction TLB
  - 8 entry data TLB
- L1 Cache
  - 16KB instruction cache
  - 16KB data cache
- Hardware debug support
- 16KB tight coupled memory
- L2 Cache
  - 128KB unify cache

1.2.2 Memory Interface

- Integrated DDR on chip
  - Support LPDDR2, DDR2, LVDDR2, 16Bit bus width
- SIP LPDDR2(32MB~64MB)
- SFC Controller
  - 1 group clock and CE pad
  - Support Standard, Dual and Quad SPI DDR protocol
  - Two slave select signal (SFC0_CE0_/ SFC0_CE1_) supporting up to 2 slave devices
  - Clock frequency up to 80MHz in SDR mode
  - Support multiple transfer modes, standard SPI, dual-output/dual-Input SPI, Quad-Output/Quad-Input SPI, Dual-I/O SPI, Quad-I/O SPI, Full Dual-I/O SPI, Full Quad-I/O SPI.

1.2.3 Media Interface

- MIPI-CSI2(v1.0) interface, resolution up to 1280x1080@60fps
  - Support 1-lane, 2-lane mode
- Camera interface module(CIM)
  - Support DVP 8-bit / MIPI input, resolution up to 640x480@60fps
  - Support snapshot control

- Supported data format: RGB888, RGB565, YCbCr 4:2:2, Raw RGB
- Support convert to luma(Y)
- Support area luminance

- AIC controller
  - I2S features
    - 8-, 16-, 18-, 20- and 24- bit audio sample data sizes supported, 16- bit packed sample data is supported
    - Up to 8 channels sample data supported
    - DMA transfer mode supported
    - Stop serial clock supported
    - Programmable Interrupt function supported
    - Support share clock mode and split clock mode.
    - Support mono PCM data to stereo PCM data expansion on audio play back
    - Support endian switch on 16- bit normal audio samples play back
    - Internal programmable or external serial clock and optional system clock supported for I2S or MSB-Justified format
    - Two FIFOs for transmit and receive respectively
- Display controller
  - Input format: RGB888, RGB565, RGB555
  - Output interface:
    - RGB Interface
      - Support 24bit/pixel(R:8bit, G:8bit, B:8bit)
      - Support 18bit/pixel(R:6bit, G:6bit, B:6bit)
      - Support 16bit/pixel(R:5bit, G:6bit, B:5bit)
      - Display size up to 1280x720@60Hz, 24BPP
    - 60/80-Type MCU Interface
      - Support 6800, 8080
      - Support 8/9/16/18/24-bit bus
      - Display size up to 640x480@60Hz, 24BPP
    - 3/4 wire SPI interface
      - Support Serial data transfer interface, 3/4line-spi
      - Support 8/12/16/24-bit bus

1.2.4 System Functions

- Clock generation and power management
  - On-chip 12/24/48MHZ oscillator circuit
  - External 32.768KHZ input
  - Three phase-locked loops (PLL) with programmable multiplier
  - CCLK, HHCLK, H2CLK, PCLK, H0CLK, DDR_CLK frequency can be changed separately for software by setting registers
  - Functional-unit clock gating
  - Supply block power shut down

- TCU
  - 8 channels each channel has two pins
  - Support posedge / negedge / dualedge clock counting
  - Support gate counting(only count for gating signal)
  - Support quadrature counting
  - Support direction counting(add / sub because of input signal)
  - Support counting after posedge / negedge signal
  - Support capture counting, output signal high-level time and total cycle time
  - Support exclk / pclk two clock source
- PWM
  - 8 channels, output signal ~50MHz, signal precision ~500MHz
  - CPU / DMA mode to update config
- OS timer
  - 64-bit counter and 32-bit compare register
  - Support interrupt generation when the counter matches the compare register
  - Two clock sources: RTCLK (real time clock), HCLK (system bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected
- Watchdog timer
  - Generates WDT reset
  - A 16-bit Data register and a 16-bit counter
- Counter clock uses the input clock selected by software RTC (Real Time Clock)
  - Need external 32768Hz oscillator for 32k clock generation
  - 32- bit second counter
  - Programmable and adjustable counter to generate accurate 1 Hz clock
  - Alarm interrupt, 1Hz interrupt
  - Stand alone power supply, work in hibernating mode
  - Power down controller
  - Alarm wakeup
  - External pin wakeup with up to 2s glitch filter
- Interrupt controller
  - Total 64 interrupt sources
  - Each interrupt source can be independently enabled
  - Priority mechanism to indicate highest priority interrupt
  - All the registers are accessed by CPU
  - Unmasked interrupts can wake up the chip in sleep mode
  - Another set of source, mask and pending registers to serve for PDMA
- PDMA controller
  - Support up to 32 independent DMA channels
  - Descriptor or No-Descriptor Transfer mode
  - A simple Xburst® CPU supports smart transfer mode controlled by programmable firmware
  - Transfer data units: 1-byte, 2-byte, 4-byte, 16-byte, 32-byte, 64-byte, 128-byte
  - Transfer number of data unit: 1 ~ 2^{24} - 1
  - Independent source and destination port width: 8-bit, 16-bit, 32-bit

- Fixed three priorities of channel groups: 0~3, highest; 4~11: mid; 12~31: lowest
- An extra INTC IRQ can be bound to one programmable DMA channel

- SAR A/D Controller
  - 4 Channels
  - Resolution: 12-bit
  - Resolution/speed: up to 1.6Msps

1.2.5 Peripherals

- General-Purpose I/O ports
  - Input / output / function port configurable
  - Low/high, rising/falling edge triggering. Every interrupt source can be masked independent
- Two I2C Controller
  - Three speeds
    - Standard mode (100 Kb/s)
    - Fast mode (400 Kb/s)
    - High mode (3.4Mb/s)
  - Device clock is identical with pclk
  - Programmable SCL generator
  - Master or slave I2C operation
  - 7-bit addressing/10-bit addressing
  - 16-level transmit and receive FIFOs
  - Interrupt operation
  - The number of devices that you can connect to the same I2C-bus is limited only by the maximum bus capacitance of 400pF
  - APB interface
  - 2 independent I2C channels (I2C0, I2C1)
- One Normal Speed Synchronous serial interfaces (SPI)
  - 3 protocols support: National's Microwire, TI's SSP, and Motorola's SPI
  - Full-duplex or transmit-only or receive-only operation
  - Programmable transfer order: MSB first or LSB first
  - 128-entry-deep x 32-bit-wide transmit and receive data FIFOs
  - Configurable normal transfer mode or Interval transfer mode
  - Programmable clock phase and polarity for Motorola's SSI format
  - Two slave select signal (SSI0_CE0_ / SSI0_CE1_) supporting up to 2 slave devices
  - Back-to-back character transmission/reception mode
  - Loop back mode for testing
- One Synchronous serial Slave interfaces(SPI Slave)
  - 3 protocols support: National's Microwire, TI's SSP, and Motorola's SPI
  - Full-duplex, transmit-only or receive-only operation for Motorola's SPI and TI's SSP
  - Half-duplex, transmit-only or receive-only operation for National's Microwire
- Four UARTs (UART0, UART1, UART2,UART3)
  - Full-duplex operation

- 5-, 6-, 7- or 8-bit characters with optional no parity or even or odd parity and with 1, 1½, or 2 stop bits
- 64x8 bits transmit FIFO and 64x11 bits receive FIFO
- Independently controlled transmit, receive (data ready or timeout), line status interrupts
- Internal diagnostic capability Loopback control and break, parity, overrun and framing-error is provided
- Separate DMA requests for transmit and receive data services in FIFO mode
- Supports modem flow control by software or hardware
- Slow infrared asynchronous interface that conforms to IrDA specification
- Support wakeup

- Two MMC/SD/SDIO controllers
  - Fully compatible with the MMC System Specification version 4.3
  - Support SD Specification 2.0
  - Support SD I/O Specification 2.0 with 1 command channel and 4 data channels
  - Consumer Electronics Advanced Transport Architecture (CE-ATA – version 1.1)
  - Maximum data rate is 50MBps
  - Support MMC data width 1-bit ,4-bit and 8-bit
  - Built-in programmable frequency divider for MMC/SD bus
  - Built-in Special Descriptor DMA
  - Maskable hardware interrupt for SDIO interrupt, internal status and FIFO status
  - 128 x 32 built-in data FIFO
  - Multi-SD function support including multiple I/O and combined I/O and memory
  - IRQ supported enable card to interrupt MMC/SD controller
  - Single or multi block access to the card including erase operation
  - Stream access to the MMC card
  - Supports SDIO read wait, interrupt detection during 1-bit or 4-bit access
  - Supports CE-ATA digital protocol commands
  - Support Command Completion Signal and interrupt to CPU
  - Command Completion Signal disable feature
  - The maximum block length is 4096bytes
- USB 2.0 OTG interface
  - Complies with the USB 2.0 standard for high-speed (480 Mbps) functions and with the On-The-Go supplement to the USB 2.0 specification
  - Operates either as the function controller of a high- /full-speed USB peripheral or as the host/peripheral in point-to-point or multi-point communications with other USB functions
  - Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP)
  - UTMI+ Level 3 Transceiver Interface
  - Soft connect/disconnect
  - 16 Endpoints
  - Dedicate FIFO
  - Supports control, interrupt, ISO and bulk transfer
  - Support wakeup
  - Support remote-wakeup

- One MAC controller
  - 10/100 Mbps operation
  - Supports RMII PHY interfaces
- CAN2.0B Controller
  - Support CAN 2.0B protocol in ISO-11898-1:2003
  - Arbitration Bit Rate up to 1Mbps
  - Support DMA mode
- CDBUS
  - Support multiple modes: arbitration mode(CDBUS-A), break sync mode(CDBUS-BS), full-duplex and half-duplex
- Security System
  - Xburst®0 MIPS-Based
  - Secret ROM and RAM
  - 16KB Secret ROM
  - 4KB Secret RAM
  - True Random Number Generator
  - Encryption Engine
    - MD5, SHA, SHA2
    - AES, support 256-bit, 192-bit, 128-bit key size Algorithm
  - Support secure boot
- OTP(EFUSE) Slave interface
  - Total 1Kb.

1.2.6 Boot ROM

20KB Boot ROM memory

2 PAD Information

2.1 Pin Map

X1600 Ball Assignment Ver1.0

BGA159, 9mm X 9mm X 1.2mm, 0.65mm pitch, top view

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	MSC0_CLK_SSIO_CLK_SSI_SLV_CLK_PB12	MSC0_D1_SSIO_GPC_I2C1_SCK_PB15	EXCLK_PWM4_TCU6_IN0_PC25	TCK_UART1_TXD_SSIO_CE1__PB02			RAM_VREF		SSIO_CE0__SSI_SLV_CE0__I2C0_SCK_PA28		LCD_D19_CIM_EXPOSURE_AD11_PA19	LCD_D17_AD9_PA17	LCD_D15_SLCD_D15_CIM_D7_AD7_PA15	LCD_D13_SLCD_D13_CIM_D5_AD5_PA13	A
B	MSC0_D3_SSIO_CE0__SSI_SLV_CE0__PB17	MSC0_CMD_SSIO_DT_SSI_SLV_DT_PB13	RTC32K_PWM5_TCU6_IN1_PC26	TDI_UART2_RXD_PB01	PWM2_TCU5_IN0_PC02	PWM0_TCU4_IN0_PC00	DDR_PLLVCCA	SSIO_DR_SSI_SLV_DR_I2C0_SDA_PA29	SSIO_DT_SSI_SLV_DT_UART2_TXD_PA30	LCD_D22_CIM_HSYNC_AD14_PA22	LCD_D20_CIM_PCLK_AD12_PA20	LCD_D16_AD8_PA16	LCD_D14_SLCD_D14_CIM_D6_AD6_PA14	LCD_D11_SLCD_D11_CIM_D3_AD3_PA11	B
C	BOOT_SEL0_PC27	MSC0_D2_SSIO_CE1__I2C1_SDA_PB16	MSC0_D0_SSIO_DR_SSI_SLV_DR_PB14	TDO_UART2_TXD_PB00	PWM1_TCU4_IN1_PC01	DDR_VSSA	RZQ	DDR_ZQ	SSIO_CLK_SSI_SLV_CLK_UART2_RXD_PWM_TCU_TRIG_PA31	LCD_D21_CIM_VSYNC_AD13_PA21	LCD_D18_AD10_PA18	LCD_D12_SLCD_D12_CIM_D4_AD4_PA12	LCD_D10_SLCD_D10_CIM_D2_AD2_PA10	LCD_D9_SLCD_D9_CIM_D1_AD1_PA09	C
D	PLL_AVDD	PLL_VDD	BOOT_SEL1_PC28	TMS_UART1_RXD_PWM_TCU_TRIG_PB03			DDR_VDD1	DDR_VDD1	LCD_D23_SLCD_CE__AD15_PA23			LCD_D8_SLCD_D8_CIM_D0_AD0_PA08	LCD_D6_SLCD_D6_TCU3_IN0_PA06	LCD_D7_SLCD_D7_TCU3_IN1_PA07	D
E		EXCLK_O	PLL_AVSS	TRST	VSS	VDDMEM	VDDMEM	VSS	VSS	VSS		LCD_D5_SLCD_D5_TCU2_IN1_PA05	LCD_D4_SLCD_D4_TCU2_IN0_PA04		E
F	AVDEFUSE	EXCLK_I	PPRST_		VSS	VDDMEM	VDDMEM	VDDMEM	VSS	VSS	VDDIO_LCD	LCD_D3_SLCD_D3_TCU1_IN1_PA03	LCD_D1_SLCD_D1_TCU0_IN1_PA01	LCD_D2_SLCD_D2_TCU1_IN0_PA02	F
G		PWRON	POR_CTL		VSS	VSS			VSS	VDD		LCD_D0_SLCD_D0_TCU0_IN0_PA00	LCD_HSYNC_SLCD_WR_AVD_PA26		G
H	RTCLK	XRTCLK	RST_OUT_		VSS	VSS			VDD	VDD		LCD_PCLK_CIM_MCLK_RD__PA24	LCD_VSYNC_SLCD_DC_WE__PA25	LCD_DE_SLCD_TE_NEMC_CS1__PA27	H
J	RTC_AVDD	RTC_VDD	WKUP_PC31		VSS	VSS	VSS	VDD	VDD	VDD		DRV_VBUS_PWM3_TCU5_IN1_PC24	I2C0_SDA_SFC0_CE1__PB31	I2C0_SCK_CDBUS_TX_EN_PB30	J
K		SFC0_DQ3_HOLD__MSC0_D1_PC22	SFC0_CLK_MSC0_CLK_PC17		VDDIO	VDDIO	VSS	VDDIO_CAN	VSS	SADC_AGND		UART3_RXD_UART1_CTS__CDBUS_TX_EN_PB05	UART3_TXD_UART1_RTS__SFC0_CE1__PB04		K
L	SFC0_DQ0_MSC0_CMD_PC19	SFC0_DQ2_WP_MSC0_D2_PC21	I2S0_RX_DATA_MAC_TXD0_PWM7_TCU7_IN1_PB21			TEST_TE			CSI_VSSA		USB_VSSA	UART0_RTS__PWM7_TCU7_IN1_PB10	UART0_TXD_PB08	UART0_CTS__PWM6_TCU7_IN0_PB09	L
M	SFC0_DQ1_MSC0_D0_PC20	SFC0_CE__MSC0_D3_PC18	I2S0_TX_BCLK_MAC_MDC_PB27	MSC1_CLK_CDBUS_TX_PD00	MSC1_D3_CAN1_RX_UART3_RXD_PD05	MSC1_D0_CAN0_TX_PD02	CSI_DATAN0	CSI_CLKN	CSI_DATAN1	SADC_VIN0	SADC_VIN2	USB0ID	VBUS	UART0_RXD_PB07	M
N	I2S0_TX_LRCK_MAC_MDIO_PB28	I2C1_SCK_MAC_RXD0_PWM5_TCU6_IN1_PB19	I2S0_RX_BCLK_MAC_REF_CLK_PB23	I2S0_TX_MCLK_MAC_TXEN_PB26	MSC1_CMD_CDBUS_RX_PD01	MSC1_D1_CAN0_RX_PD03	CSI_DATAP0	CSI_CLKP	CSI_DATAP1	CSI_VCCA33	SADC_VIN1	SADC_AVDD	USB0PP	USB_AVD11	N
P	I2S0_RX_LRCK_MAC_RXDV_PB24	I2C1_SDA_MAC_RXD1_PWM6_TCU7_IN0_PB20	I2S0_RX_MCLK_MAC_PHY_CLK_PB22	I2S0_TX_DATA_MAC_TXD1_PB25		MSC1_D2_CAN1_TX_UART3_TXD_PD04		CSI_VCCA11			SADC_VIN3	SADC_VREFP	USB0PN	USB_AVD33	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

2.2 Pin Description

2.2.1 GPIO Group A

Ball No.	Ball Name	In/ Out	Pull	Slew Rate	Schmitt	GPIO	Func0	Func1	Func2	Func3	Power
G12	LCD_D0_SLCD_D0_TCU0_IN0_ PA00	IO	PU	Yes	No	GPA[0]	LCD_D0	SLCD_D0	TCU0_IN0		VDDIO_LCD
F13	LCD_D1_SLCD_D1_TCU0_IN1_ PA01	IO	PU	Yes	No	GPA[1]	LCD_D1	SLCD_D1	TCU0_IN1		VDDIO_LCD
F14	LCD_D2_SLCD_D2_TCU1_IN0_ PA02	IO	PU	Yes	No	GPA[2]	LCD_D2	SLCD_D2	TCU1_IN0		VDDIO_LCD
F12	LCD_D3_SLCD_D3_TCU1_IN1_ PA03	IO	PU	Yes	No	GPA[3]	LCD_D3	SLCD_D3	TCU1_IN1		VDDIO_LCD
E13	LCD_D4_SLCD_D4_TCU2_IN0_ PA04	IO	PU	Yes	No	GPA[4]	LCD_D4	SLCD_D4	TCU2_IN0		VDDIO_LCD
E12	LCD_D5_SLCD_D5_TCU2_IN1_ PA05	IO	PU	Yes	No	GPA[5]	LCD_D5	SLCD_D5	TCU2_IN1		VDDIO_LCD
D13	LCD_D6_SLCD_D6_TCU3_IN0_ PA06	IO	PU	Yes	No	GPA[6]	LCD_D6	SLCD_D6	TCU3_IN0		VDDIO_LCD
D14	LCD_D7_SLCD_D7_TCU3_IN1_ PA07	IO	PU	Yes	No	GPA[7]	LCD_D7	SLCD_D7	TCU3_IN1		VDDIO_LCD
D12	LCD_D8_SLCD_D8_CIM_D0_AD0_PA08	IO	PU	Yes	No	GPA[8]	LCD_D8	SLCD_D8	CIM_D0	AD0	VDDIO_LCD
C14	LCD_D9_SLCD_D9_CIM_D1_AD1_PA09	IO	PU	Yes	No	GPA[9]	LCD_D9	SLCD_D9	CIM_D1	AD1	VDDIO_LCD
C13	LCD_D10_SLCD_D10_CIM_D2_AD2_PA10	IO	PU	Yes	No	GPA[10]	LCD_D10	SLCD_D10	CIM_D2	AD2	VDDIO_LCD
B14	LCD_D11_SLCD_D11_CIM_D3_AD3_PA11	IO	PU	Yes	No	GPA[11]	LCD_D11	SLCD_D11	CIM_D3	AD3	VDDIO_LCD
C12	LCD_D12_SLCD_D12_CIM_D4_AD4_PA12	IO	PU	Yes	No	GPA[12]	LCD_D12	SLCD_D12	CIM_D4	AD4	VDDIO_LCD
A14	LCD_D13_SLCD_D13_CIM_D5_AD5_PA13	IO	PU	Yes	No	GPA[13]	LCD_D13	SLCD_D13	CIM_D5	AD5	VDDIO_LCD
B13	LCD_D14_SLCD_D14_CIM_D6_AD6_PA14	IO	PU	Yes	No	GPA[14]	LCD_D14	SLCD_D14	CIM_D6	AD6	VDDIO_LCD
A13	LCD_D15_SLCD_D15_CIM_D7_AD7_PA15	IO	PU	Yes	No	GPA[15]	LCD_D15	SLCD_D15	CIM_D7	AD7	VDDIO_LCD
B12	LCD_D16_AD8_PA16	IO	PU	Yes	No	GPA[16]	LCD_D16			AD8	VDDIO_LCD
A12	LCD_D17_AD9_PA17	IO	PU	Yes	No	GPA[17]	LCD_D17			AD9	VDDIO_LCD
C11	LCD_D18_AD10_PA18	IO	PU	Yes	No	GPA[18]	LCD_D18			AD10	VDDIO_LCD
A11	LCD_D19_CIM_EXPOSURE_AD11_PA19	IO	PU	Yes	No	GPA[19]	LCD_D19		CIM_EXPOSURE	AD11	VDDIO_LCD
B11	LCD_D20_CIM_PCLK_AD12_PA20	IO	PU	Yes	No	GPA[20]	LCD_D20		CIM_PCLK	AD12	VDDIO_LCD
C10	LCD_D21_CIM_VSYNC_AD13_PA21	IO	PU	Yes	No	GPA[21]	LCD_D21		CIM_VSYNC	AD13	VDDIO_LCD
B10	LCD_D22_CIM_HSYNC_AD14_PA22	IO	PU	Yes	No	GPA[22]	LCD_D22		CIM_HSYNC	AD14	VDDIO_LCD

D9	LCD_D23_SLCD_CE__AD15_PA23	IO	PU	Yes	No	GPA[23]	LCD_D23	SLCD_CE_		AD15	VDDIO_LCD
H12	LCD_PCLK_CIM_MCLK_RD__PA24	IO	PU	No	No	GPA[24]	LCD_PCLK		CIM_MCLK	RD_	VDDIO_LCD
H13	LCD_VSYNC_SLCD_DC_WE__PA25	IO	PU	Yes	No	GPA[25]	LCD_VSYNC	SLCD_DC		WE_	VDDIO_LCD
G13	LCD_HSYNC_SLCD_WR_AVD__PA26	IO	PU	Yes	No	GPA[26]	LCD_HSYNC	SLCD_WR		AVD_	VDDIO_LCD
H14	LCD_DE_SLCD_TE_NEMC_CS1__PA27	IO	PU	Yes	No	GPA[27]	LCD_DE	SLCD_TE		CS0_	VDDIO_LCD
A9	SSI0_CE0__SSI_SLV_CE0__I2C0_SCK_PA28	IO	PU	Yes	No	GPA[28]	SSI0_CE0_	SSI1_SLV_CE0_	I2C0_SCK		VDDIO_LCD
B8	SSI0_DR_SSI_SLV_DR_I2C0_SDA_PA29	IO	PU	Yes	No	GPA[29]	SSI0_DR	SSI1_SLV_DR	I2C0_SDA		VDDIO_LCD
B9	SSI0_DT_SSI_SLV_DT_UART2_TXD_PA30	IO	PU	Yes	No	GPA[30]	SSI0_DT	SSI1_SLV_DT	UART2_TXD		VDDIO_LCD
C9	SSI0_CLK_SSI_SLV_CLK_UART2_RXD_PWM_TCU_TRIG_PA31	IO	PU	Yes	No	GPA[31]	SSI0_CLK	SSI1_SLV_CLK	UART2_RXD	PWM_TCU_TRIG	VDDIO_LCD

2.2.2 GPIO Group B

Ball No.	Ball Name	In/ Out	Pull	Slew Rate	Schmitt	GPIO	Func0	Func1	Func2	Func3	Power
C4	TDO_UART2_TXD_PB00	IO	PU_rst	Yes	No	GPB[0]	TDO	UART2_TXD			VDDIO
B4	TDI_UART2_RXD_PB01	IO	PU_rst	Yes	No	GPB[1]	TDI	UART2_RXD			VDDIO
A4	TCK_UART1_TXD_SSI0_CE1__PB02	IO	PU_rst	Yes	No	GPB[2]	TCK	UART1_TXD	SSI0_CE1_		VDDIO
D4	TMS_UART1_RXD_PWM_TCU_TRIG_PB03	IO	PU	Yes	No	GPB[3]	TMS	UART1_RXD	PWM_TCU_TRIG		VDDIO
K13	UART3_TXD_UART1_RTS__SFC0_CE1__PB04	IO	PU	Yes	No	GPB[4]	UART3_TXD	UART1_RTS_	SFC0_CE1_		VDDIO
K12	UART3_RXD_UART1_CTS__CDBUS_TX_EN_PB05	IO	PU	Yes	No	GPB[5]	UART3_RXD	UART1_CTS_	CDBUS_TX_EN		VDDIO
M14	UART0_RXD_PB07	IO	PU	Yes	No	GPB[7]	UART0_RXD				VDDIO
L13	UART0_TXD_PB08	IO	PU	Yes	No	GPB[8]	UART0_TXD				VDDIO
L14	UART0_CTS__PWM6_TCU7_IN0_PB09	IO	PU	Yes	No	GPB[9]	UART0_CTS_	PWM6	TCU7_IN0		VDDIO
L12	UART0_RTS__PWM7_TCU7_IN1_PB10	IO	PU	Yes	No	GPB[10]	UART0_RTS_	PWM7	TCU7_IN1		VDDIO
A1	MSC0_CLK_SSI0_CLK_SSI_SLV_CLK_PB12	IO	PU	No	No	GPB[12]	MSC0_CLK	SSI0_CLK	SSI_SLV_CLK		VDDIO
B2	MSC0_CMD_SSI0_DT_SSI_SLV_DT_PB13	IO	PU	Yes	No	GPB[13]	MSC0_CMD	SSI0_DT	SSI_SLV_DT		VDDIO
C3	MSC0_D0_SSI0_DR_SSI_SLV_DR_PB14	IO	PU	Yes	No	GPB[14]	MSC0_D0	SSI0_DR	SSI_SLV_DR		VDDIO

A2	MSC0_D1_SSI0_GPC_I2C1_SCK_PB15	IO	PU	Yes	No	GPB[15]	MSC0_D1	SSI0_GPC	I2C1_SCK		VDDIO
C2	MSC0_D2_SSI0_CE1__I2C1_SDA_PB16	IO	PU	Yes	No	GPB[16]	MSC0_D2	SSI0_CE1_	I2C1_SDA		VDDIO
B1	MSC0_D3_SSI0_CE0__SSI_SLV_CE0_PB17	IO	PU	Yes	No	GPB[17]	MSC0_D3	SSI0_CE0_	SSI_SLV_CE0_		VDDIO
N2	I2C1_SCK_MAC_RXD0_PWM5_TCU6_IN1_PB19	IO	PU	Yes	No	GPB[19]	I2C1_SCK	MAC_RXD0	PWM5	TCU6_IN1	VDDIO
P2	I2C1_SDA_MAC_RXD1_PWM6_TCU7_IN0_PB20	IO	PU	Yes	No	GPB[20]	I2C1_SDA	MAC_RXD1	PWM6	TCU7_IN0	VDDIO
L3	I2S0_RX_DATA_MAC_TXD0_PWM7_TCU7_IN1_ PB21	IO	PU	Yes	No	GPB[21]	I2S0_RX_DATA	MAC_TXD0	PWM7	TCU7_IN1	VDDIO
P3	I2S0_RX_MCLK_MAC_PHY_CLK_PB2	IO	PU	No	No	GPB[22]	I2S0_RX_MCLK	MAC_PHY_CLK			VDDIO
N3	I2S0_RX_BCLK_MAC_REF_CLK_PB23	IO	PU	Yes	No	GPB[23]	I2S0_RX_BCLK	MAC_REF_CLK			VDDIO
P1	I2S0_RX_LRCK_MAC_RXDV_PB24	IO	PU	Yes	No	GPB[24]	I2S0_RX_LRCK	MAC_RX_DV			VDDIO
P4	I2S0_TX_DATA_MAC_TXD1_PB25	IO	PU	Yes	No	GPB[25]	I2S0_TX_DATA	MAC_TXD1			VDDIO
N4	I2S0_TX_MCLK_MAC_TXEN_PB26	IO	PU	Yes	No	GPB[26]	I2S0_TX_MCLK	MAC_TXEN			VDDIO
M3	I2S0_TX_BCLK_MAC_MDC_PB27	IO	PU	Yes	No	GPB[27]	I2S0_TX_BCLK	MAC_MDC			VDDIO
N1	I2S0_TX_LRCK_MAC_MDIO_PB28	IO	PU	Yes	No	GPB[28]	I2S0_TX_LRCK	MAC_MDIO			VDDIO
J14	I2C0_SCK_CDBUS_TX_EN_PB30	IO	PU	No	Yes	GPB[30]	I2C0_SCK	CDBUS_TX_EN			VDDIO
J13	I2C0_SDA_SFC0_CE1__PB31	IO	PU	No	Yes	GPB[31]	I2C0_SDA	SFC0_CE1_			VDDIO

2.2.3 GPIO Group C

Ball No.	Ball Name	In/ Out	Pull	Slew Rate	Schmitt	GPIO	Func0	Func1	Func2	Func3	Power
B6	PWM0_TCU4_IN0_PC00	IO	PD_rst	Yes	No	GPC[0]	PWM0	TCU4_IN0			VDDIO
C5	PWM1_TCU4_IN1_PC01	IO	PD_rst	Yes	No	GPC[1]	PWM1	TCU4_IN1			VDDIO
B5	PWM2_TCU5_IN0_PC02	IO	PD_rst	Yes	No	GPC[2]	PWM2	TCU5_IN0			VDDIO
K3	SFC0_CLK_MSC0_CLK_PC17	IO	PU	No	No	GPC[17]	SFC0_CLK	MSC0_CLK			VDDIO
M2	SFC0_CE__MSC0_D3_PC18	IO	PU	Yes	No	GPC[18]	SFC0_CE0_	MSC0_D3			VDDIO
L1	SFC0_DQ0_MSC0_CMD_PC19	IO	PU	Yes	No	GPC[19]	SFC0_DQ0/DT	MSC0_CMD			VDDIO
M1	SFC0_DQ1_MSC0_D0_PC20	IO	PU	Yes	No	GPC[20]	SFC0_DQ1/DR	MSC0_D0			VDDIO
L2	SFC0_DQ2_WP__MSC0_D2_PC21	IO	PU	Yes	No	GPC[21]	SFC0_DQ2/WP_	MSC0_D2			VDDIO

K2	SFC0_DQ3_HOLD__MSC0_D1_PC22	IO	PU	Yes	No	GPC[22]	SFC0_DQ3/HOLD_	MSC0_D1			VDDIO
J12	DRV_VBUS_PWM3_TCU5_IN1_PC24	IO	PD_rst	Yes	No	GPC[24]	DRV_VBUS	PWM3	TCU5_IN1		VDDIO
A3	EXCLK_PWM4_TCU6_IN0_PC25	IO	PD_rst	Yes	No	GPC[25]	EXCLK	PWM4	TCU6_IN0		VDDIO
B3	RTC32K_PWM5_TCU6_IN1_PC26	IO	PD_rst	Yes	No	GPC[26]	RTC32K	PWM5	TCU6_IN1		VDDIO
C1	BOOT_SEL0_PC27	IO	PU	No	Yes	GPC[27]	BOOT_SEL0				VDDIO
D3	BOOT_SEL1_PC28	IO	PU	No	Yes	GPC[28]	BOOT_SEL1				VDDIO
J3	WKUP_PC31	IO	PU	No	Yes	GPC[31]	WKUP_				RTC_AVDD

2.2.4 GPIO Group D(5V tolerant)

Ball No.	Ball Name	In/Out	Pull	Slew Rate	Schmitt	GPIO	Func0	Func1	Func2	Func3	Power
M4	MSC1_CLK_CDBUS_TX_PD00	IO	PU	No	No	GPD[0]	MSC1_CLK	CDBUS_TX			VDDIO_CAN
N5	MSC1_CMD_CDBUS_RX_PD01	IO	PU	Yes	No	GPD[1]	MSC1_CMD	CDBUS_RX			VDDIO_CAN
M6	MSC1_D0_CAN0_TX_PD02	IO	PU	Yes	No	GPD[2]	MSC1_D0	CAN0_TX			VDDIO_CAN
N6	MSC1_D1_CAN0_RX_PD03	IO	PU	Yes	No	GPD[3]	MSC1_D1	CAN0_RX			VDDIO_CAN
P6	MSC1_D2_CAN1_TX_UART3_TXD_PD04	IO	PU	Yes	No	GPD[4]	MSC1_D2	CAN1_TX	UART3_TXD		VDDIO_CAN
M5	MSC1_D3_CAN1_RX_UART3_RXD_PD05	IO	PU	Yes	No	GPD[5]	MSC1_D3	CAN1_RX	UART3_RXD		VDDIO_CAN

2.3 X1600/E Analog PAD DESCRIPTION

Table 2-1 X1600/E function pin description

Ball No.	Pin Names	IO	Power	Pin Description
Debug				
E4	TRST	I	VDDIO	JTAG reset
Memory				
D7	DDR_VDD1	P	-	For sdram supply
D8	DDR_VDD1	P	-	For sdram supply
B7	DDRPLL_VCCA	P	-	DDR PHY PLL supply 3.3v
C6	DDR_VSSA	P	-	ground
A7	RAM_VREF	P		for sdram, reference voltage
C7	RZQ	I		for sdram, external reference resistor for output calibrating
Power and Ground				
E6	VDDMEM	P	-	DDR PHY IO powersupply, 1.8V for DDR2(1.2V for LPDDR2)
E7	VDDMEM	P	-	DDR PHY IO powersupply, 1.8V for DDR2(1.2V for LPDDR2)
F6	VDDMEM	P	-	DDR PHY IO powersupply, 1.8V for DDR2(1.2V for LPDDR2)
F7	VDDMEM	P	-	DDR PHY IO powersupply, 1.8V for DDR2(1.2V for LPDDR2)
F8	VDDMEM	P	-	DDR PHY IO powersupply, 1.8V for DDR2(1.2V for LPDDR2)
K5	VDDIO	P	-	IO digital power for GPIO Port B&C, 1.8V~3.3V
K6	VDDIO	P	-	IO digital power for GPIO Port B&C, 1.8V~3.3V
F11	VDDIO_LCD	P	-	IO digital power for GPIO Port A, 1.8V~3.3V
K8	VDDIO_CAN	P	-	IO digital power for GPIO Port D, 3.3V
E5	VSS	P	-	Digital Ground
E8	VSS	P	-	Digital Ground
E9	VSS	P	-	Digital Ground
E10	VSS	P	-	Digital Ground
F5	VSS	P	-	Digital Ground

F9	VSS	P	-	Digital Ground
F10	VSS	P	-	Digital Ground
G5	VSS	P	-	Digital Ground
G6	VSS	P	-	Digital Ground
G9	VSS	P	-	Digital Ground
H5	VSS	P	-	Digital Ground
H6	VSS	P	-	Digital Ground
J5	VSS	P	-	Digital Ground
J6	VSS	P	-	Digital Ground
J7	VSS	P	-	Digital Ground
K7	VSS	P	-	Digital Ground
K9	VSS	P	-	Digital Ground
G10	VDD	P	-	CORE digital power, 1.1V
H9	VDD	P	-	CORE digital power, 1.1V
H10	VDD	P	-	CORE digital power, 1.1V
J8	VDD	P	-	CORE digital power, 1.1V
J9	VDD	P	-	CORE digital power, 1.1V
J10	VDD	P	-	CORE digital power, 1.1V
CSI				
N10	CSI_VCCA33	P	-	3.3V Analog supply
P8	CSI_VCCA11	P	-	1.1V Analog supply
L9	CSI_VSSA	P	-	ground
M7	CSI_DATAN0	AI	CSI_VCCA11	Lane0 negative end
N7	CSI_DATAP0	AI	CSI_VCCA11	Lane0 positive end
M9	CSI_DATAN1	AI	CSI_VCCA11	Lane1 negative end
N9	CSI_DATAP1	AI	CSI_VCCA11	Lane1 positive end
M8	CSI_CLKN	AI	CSI_VCCA11	CLK lane0 negative end
N8	CSI_CLKP	AI	CSI_VCCA11	CLK lane0 positive end
SADC				
N12	SADC_AVDD	P	-	3.3v supply
K10	SADC_AGND	P	-	ground

P12	SADC_VREFP	AI	SADC_AVDD	Positive reference voltage input
M10	SADC_VIN0	AI	SADC_AVDD	Analog input 0
N11	SADC_VIN1	AI	SADC_AVDD	Analog input 1
M11	SADC_VIN2	AI	SADC_AVDD	Analog input 2
P11	SADC_VIN3	AI	SADC_AVDD	Analog input 3
USB OTG				
P14	USB_AVD33	P	-	USB analog power.3.3V
N14	USB_AVD11	P	-	USB analog power.1.1V
L11	USB_VSSA	P	-	USB analog ground
P13	USB0PN	AIO	USB_AVD33	USB OTG data negative
N13	USB0PP	AIO	USB_AVD33	USB OTG data positive
M13	VBUS	AI	USB_AVD33	USB 5-V power supply pin for USB OTG. An external charge pump must provide power to this pin. The required voltage range is 5.25V ~ 4.75V.
M12	USB0ID	AI	USB_AVD33	Used to identify the device attached to the PHY. The state of the pin is one of: high impedance (>1M Ω), or low impedance (<10Ω to ground).
EFUSE				
F1	AVDEFUSE	P	AVDEFUSE	EFUSE programming power, 0V/2.5V
CPM				
F2	EXCLK_I	AI	VDDIO	EXCLK OSC Input
E2	EXCLK_O	AO	VDDIO	EXCLK OSC Output
D1	PLL_AVDD	P	-	PLL analog power
E3	PLL_AVSS	P	-	PLL analog ground
D2	PLL_VDD	P	-	PLL digital power
RTC				
J1	RTC_AVDD	P	-	3.3V power for RTC and hibernating mode controlling that never power down(normally you can use 1.8V instead to reduce power consumption)
J2	RTC_VDD	P	-	1.1v supply to RTC
H1	RTCLK	AI	RTC_AVDD	RTC OSC input.
H2	XRTCLK	AO	RTC_AVDD	RTC OSC output.
G2	PWRON	O	RTC_AVDD	Power on/off control of main power
F3	PPRST_	I	RTC_AVDD	RTC power on reset and RESET-KEY reset input

L6	TEST_TE	I	RTC_AVDD	Manufacture test enable, program readable
G3	POR_CTL	I	RTC_AVDD	POR enable
RESET				
H3	RST_OUT_	O	VDDIO	System reset output

2.4 X1600/E Digital PAD DESCRIPTION

Table 2-2 X1600/E Function Description

Signal Name	In/Out	Description
SLCD(Smart LCD)		
SLCD_D<n>	Output	Smart LCD data output bit n
SLCD_WR	Output	Smart LCD write signal
SLCD_CE_	Output	Smart LCD chip select signal
SLCD_TE	Input	Smart LCD tearing effect signal
SLCD_DC	Output	Smart LCD data/command select signal
LCD		
LCD_D<n>	Output	LCD data output bit n
LCD_PCLK	Output	LCD pixel clock
LCD_VSYNC	Output	LCD frame sync
LCD_HSYNC	Output	LCD line sync
LCD_DE	Output	LCD data enable
CIM(Camera Interface)		
CIM_EXPOSURE	Output	CIM exposure signal to sensor to generate snapshot
CIM_PCLK	Input	CIM pixel clock input
CIM_HSYNC	Input	CIM line horizontal sync input
CIM_VSYNC	Input	CIM vertical sync input
CIM_MCLK	Output	CIM master clock output
CIM_D<n>	Input	CIM data input bit n

I2S		
I2S0_TX_MCLK	Output	I2S master clock out
I2S0_TX_BCLK	Bidirection	I2S bit clock
I2S0_TX_LRCK	Bidirection	I2S LR clock
I2S0_TX_DATA	Output	I2S data output
I2S0_RX_DATA	Input	I2S data input
I2S0_RX_MCLK	Output	I2S master clock out(only for independent clock mode)
I2S0_RX_BCLK	Bidirection	I2S bit clock(only for independent clock mode)
I2S0_RX_LRCK	Bidirection	I2S LR clock(only for independent clock mode)
SFC		
SFC0_CLK	Output	Serial Flash clock output
SFC0_CE_	Output	Serial Flash chip enable 0
SFC0_DQ0	Bidirection	Serial Flash data
SFC0_DQ1	Bidirection	Serial Flash data
SFC0_DQ2_WP_	Bidirection	Serial Flash write protect signal
SFC0_DQ3_HOLD_	Bidirection	Serial Flash hold signal
PWM		
PWM0/TCU0_IN0	Bidirection	PWM/TCU data output/input
PWM1/TCU0_IN1	Bidirection	PWM/TCU data output/input
PWM2/TCU1_IN0	Bidirection	PWM/TCU data output/input
PWM3/TCU1_IN1	Bidirection	PWM/TCU data output/input
PWM4/TCU2_IN0	Bidirection	PWM/TCU data output/input
PWM5/TCU2_IN1	Bidirection	PWM/TCU data output/input
PWM6/TCU3_IN0	Bidirection	PWM/TCU data output/input
PWM7/TCU3_IN1	Bidirection	PWM/TCU data output/input
PWM8/TCU4_IN0	Bidirection	PWM/TCU data output/input
PWM_TCU_TRIG	Input	Use to save PWM/TCU counter
RTC		
RTC32K	Output	32768Hz clock output
I2C		
I2C<n>_SCK	Bidirection	I2C n serial clock

I2C<n>_SDA	Bidirection	I2C n serial data
SSI		
SSI0_CLK	Output	SSI clock output
SSI0_CE0_	Output	SSI chip enable 0
SSI0_CE1_	Output	SSI chip enable 1
SSI0_DT	Output	SSI data output
SSI0_DR	Input	SSI data input
SSI0_GPC	Output	SSI general-purpose control signal
SSI Slave		
SSI_SLV_CLK	Input	SSI Slave clock
SSI_SLV_CE0_	Input	SSI Slave chip enable
SSI_SLV_DT	Output	SSI Slave data output
SSI_SLV_DR	Input	SSI Slave data input
UART		
UART<n>_RXD	Input	UART n receiving data
UART<n>_TXD	Output	UART n transmitting data
UART<n>_CTS_	Input	UART Clear to send control
UART<n>_RTS_	Output	UART Request to send control
MSC		
MSC<n>_D3	Bidirection	MSC(MMC/SD) n data bit 3
MSC<n>_D2	Bidirection	MSC(MMC/SD) n data bit 2
MSC<n>_D1	Bidirection	MSC(MMC/SD) n data bit 1
MSC<n>_D0	Bidirection	MSC(MMC/SD) n data bit 0
MSC<n>_CLK	Output	MSC(MMC/SD) n clock output
MSC<n>_CMD	Bidirection	MSC(MMC/SD) n command
USB 2.0 OTG		
DRV_VBUS	Output	USB OTG VBUS driver control signal
MAC		
MAC_PHY_CLK	Output	Ethernet n PHY clock (50MHz) (n=0，1)
MAC_REF_CLK	Input	RMII reference clock
MAC_RX_DV	Input	Rx data valid

MAC_RXD0	Input	receive data bit 0
MAC_RXD1	Input	receive data bit 1
MAC_TXEN	Output	Ethernet n transmit enable
MAC_TXD0	Output	tx data bit 0
MAC_TXD1	Output	tx data bit 1
MAC_MDC	Output	Ethernet management clock
MAC_MDIO	Bidirection	Ethernet management data
NEMC		
ADn	Bidirection	Address[15:0], Data[15:0] in muxed mode
RD_	Output	NEMC read enable, low active
WE_	Output	NEMC write enable, low active
NEMC_CS1_	Output	NEMC chip select1
CAN		
CAN<n>_TX	Output	CAN n TX output to CAN transceiver
CAN<n>_RX	Input	CAN n RX input from CAN transceiver
CDBUS		
CDBUS_TX_EN	Output	CDBUS Enable output
CDBUS_TX	Output	CDBUS Transmit data
CDBUS_RX	Input	CDBUS Receive data
DEBUG		
TDO	Output	JTAG serial data output
TDI	Input	JTAG serial data input
TCK	Input	JTAG clock
TMS	Input	JTAG mode select

NOTES:

1 The meaning of phases in IO cell characteristics are:

a PU: The IO cell contains a pull-up resistor and the pull-up resistor can be enabled or disabled by setting corresponding register.

b PD: The IO cell contains a pull-down resistor and the pull-down resistor can be enabled or disabled by setting corresponding register.

c PU_rst: these pins are initialed (during reset and after reset) to IO internal pullup enabled.

d PD_rst: these pins are initialed (during reset and after reset) to IO internal pulldown enabled.

e Schmitt: The IO cell is Schmitt trig input.

2 All GPIO shared pins are reset to GPIO input.

3 Electrical Specifications

3.1 Absolute Maximum Ratings

The absolute maximum ratings for the processors are listed in Table 3-1. Do not exceed these parameters or the part may be damaged permanently. Operation at absolute maximum ratings is not guaranteed.

Table 3-1 Absolute Maximum Ratings

Parameter	Min	Max	Unit
Storage Temperature	-65	150	°C
Operation Temperature	-40	85	°C
VDDMEM power supplies voltage	-0.4	1.6	V
DDR_VDD1 power supplies voltage	-0.4	2.3	V
DDR_PLLVCCA power supplies voltage	-0.3	3.6	V
VDDIO power supplies voltage	-0.3	3.6	V
VDDIO_CAN power supplies voltage	-0.3	5.5	V
VDDIO_LCD power supplies voltage	-0.3	3.6	V
VDD core power supplies voltage	-0.2	1.21	V
PLL_VDD power supplies voltage	-0.2	1.21	V
PLL_AVDD power supplies voltage	-0.3	3.6	V
AVDEFUSE power supplies voltage	-0.3	2.75	V
RTC_AVDD power supplies voltage	-0.3	3.6	V
RTC_VDD power supplies voltage	-0.2	1.21	V
USB_AVD33 power supplies voltage	-0.3	3.6	V
USB_AVD11 power supplies voltage	-0.2	1.21	V
SADC_AVDD	-0.3	3.6	V
CSI_ VCCA33	-0.3	3.6	V
CSI_ VCCA11	-0.2	1.21	V
Input voltage to VDDMEM supplied non-supply pins	-0.3	1.32	V
Input voltage to VDDIO supplied non-supply pins	-0.3	3.6	V
Input voltage to VDDIO_CAN supplied non-supply pins	-0.3	5.5	V
Input voltage to VDDIO_LCD supplied non-supply pins	-0.3	3.6	V
Input voltage to RTC_AVDD supplied non-supply pins	-0.3	3.6	V
Input voltage to USB_AVD33 supplied non-supply pins	-0.3	3.6	V
Input voltage to SADC_AVDD supplied non-supply pins	-0.3	3.6	V
Input voltage to CSI_ VCCA33 supplied non-supply pins	-0.3	3.6	V
Output voltage from VDDMEM supplied non-supply pins	-0.3	1.32	V
Output voltage from VDDIO supplied non-supply pins	-0.3	3.6	V
Output voltage from VDDIO_CAN supplied non-supply pins	-0.3	3.6	V
Output voltage from VDDIO_LCD supplied non-supply pins	-0.3	3.6	V
Output voltage from RTC_AVDD supplied non-supply pins	-0.3	3.6	V
Output voltage from USB_AVD33 supplied non-supply pins	-0.3	3.6	V
Maximum ESD stress voltage, Human Body Model; Any pin to any supply pin, either polarity, or Any pin to all non-supply pins together, either polarity. Three stresses maximum.		2000	V

3.2 Recommended operating conditions

Table 3-2 Recommended operating conditions for power supplies

Symbol	Description	Min	Typical	Max	Unit
VMEM	VDDMEM voltage for LPDDR2	1.14	1.2	1.3	V
VDDR1	DDR_VDD1 voltage	1.7	1.8	1.95	V
VDDRPLL	DDR_PLLVCCA voltage	3.0	3.3	3.6	V
VIO(3.3V)	VDDIO voltage, use as 3.3V	3.0	3.3	3.6	V
VIO(1.8V)	VDDIO voltage, use as 1.8V	1.62	1.8	1.98	V
VCAN (3.3V)	VDDIO_CAN voltage, use as 3.3V	3.0	3.3	3.6	V
VLCD(3.3V)	VDDIO_LCD voltage, use as 3.3V	3.0	3.3	3.6	V
VLCD (1.8V)	VDDIO_LCD voltage, use as 1.8V	1.62	1.8	1.98	V
VCORE	VDD core voltage	0.99	1.1	1.21	V
VPLLVDD	PLL_VDD voltage	0.99	1.1	1.21	V
VPLLAVDD(3.3V)	PLL_AVDD voltage, use as 3.3V	3.0	3.3	3.6	V
VPLLAVDD(1.8V)	PLL_AVDD voltage, use as 1.8V	1.62	1.8	1.98	V
VEFUSE	AVDEFUSE voltage	2.25	2.5	2.75	V
VRTCIO(3.3V)	RTC_AVDD voltage, use as 3.3V	2.97	3.3	3.63	V
VRTCIO(1.8V)	RTC_AVDD voltage, use as 1.8V	1.62	1.8	1.98	V
VRTC	RTC_VDD voltage	1.0	1.1	1.21	V
VUSB33	USB_AVD33 voltage	3.0	3.3	3.6	V
VUSB11	USB_AVD11 voltage	0.99	1.1	1.21	V
VADC	SADC_AVDD voltage	2.97	3.3	3.63	V
VCSI33	CSI_ VCCA33 voltage	2.97	3.3	3.63	V
VCSI11	CSI_ VCCA11 voltage	0.99	1.1	1.21	V

Table 3-3 Recommended operating conditions for ADC pins

Symbol	Description	Min	Typical	Max	Unit
SADC_VREFP	SADC_VREFP and SADC_AGND are used as reference for SADC	-	3.3	VADC	V
V_{IADC}	SADC_VIN0, SADC_VIN1, SADC_VIN2, SADC_VIN3 input voltage range	0		VADC	V

Table 3-4 Recommended operating conditions for others

Symbol	Description	Min	Typical	Max	Unit
TA	Ambient temperature	–40		85	°C

3.3 DC Specifications

The DC characteristics for each pin include input-sense levels and output-drive levels and currents. These parameters can be used to determine maximum DC loading, and also to determine maximum transition times for a given load. All DC specification values are valid for the entire temperature range of the device.

Table 3-5 DC characteristics for VREF

Symbol	Parameter	Min	Typical	Max	Unit
RAM_VREF(DC)	Reference voltage supply of DDR	0.49* VMEM	0.5* VMEM	0.51* VMEM	V

NOTE: The ac peak noise on VREF may not allow VREF to deviate from VREF(DC) by more than +/-1% VMEM.

Table 3-6 DC characteristics for VDDIO/VDDIO_LCD/RTC_ VDDIO supplied pins for 3.3V application

Symbol	Parameter		Min	Typical	Max	Unit
V_{IL}	Input Low Voltage		-0.3		0.8	V
V_{IH}	Input High Voltage		2		3.6	V
V_T	Threshold point		1.34	1.45	1.59	V
V_{T+}	Schmitt trig low to high threshold point		1.57	1.68	1.81	V
V_{T-}	Schmitt trig high to low threshold point		1.21	1.32	1.45	V
V_{TPU}	Threshold point with pull-up resistor enabled		1.31	1.42	1.55	V
V_{TPD}	Threshold point with pull-down resistor enabled		1.37	1.49	1.63	V
V_{TPU+}	Schmitt trig low to high threshold point with pull-up resistor enabled		1.54	1.65	1.77	V
V_{TPU-}	Schmitt trig high to low threshold point with pull-down resistor enabled		1.18	1.29	1.41	V
V_{TPD+}	Schmitt trig low to high threshold point with pull-down resistor enabled		1.61	1.72	1.86	V
V_{TPD-}	Schmitt trig high to low threshold point with pull-up resistor enabled		1.23	1.35	1.49	V
I_L	Input Leakage Current @ V_I=1.8V or 0V				±10	µA
I_{OZ}	Tri-State output leakage current @ V_I=1.8V or 0V				±10	µA
R_{PU}	Pull-up Resistor		58	86	133	kΩ
R_{PD}	Pull-down Resistor		52	78	128	kΩ
V_{OL}	Output low voltage				0.4	V
V_{OH}	Output high voltage		2.4			V
I_{OL}	Low level output current @ V_{OL}(max)	8mA	12.7	19.3	25.9	mA
		4mA	8.5	12.9	17.4	mA
I_{OH}	High level output current @ V_{OH}(min)	8mA	18.7	37	62.8	mA
		4mA	13.4	26.5	45	mA

Table 3-7 DC characteristics for VDDIO/VDDIO_LCD/RTC_ VDDIO supplied pins for 1.8V application

Symbol	Parameter	Min	Typical	Max	Unit
V_{IL}	Input Low Voltage	-0.3		0.63	V
V_{IH}	Input High Voltage	1.17		3.6	V
V_T	Threshold point	0.77	0.84	0.91	V
V_{T+}	Schmitt trig low to high threshold point	0.93	1.02	1.11	V

V_{T-}	Schmitt trig high to low threshold point		0.62	0.73	0.82	V
V_{TPU}	Threshold point with pull-up resistor enabled		0.75	0.83	0.9	V
V_{TPD}	Threshold point with pull-down resistor enabled		0.78	0.86	0.93	V
V_{TPU+}	Schmitt trig low to high threshold point with pull-up resistor enabled		0.92	1.01	1.1	V
V_{TPU-}	Schmitt trig high to low threshold point with pull-down resistor enabled		0.61	0.72	0.8	V
V_{TPD+}	Schmitt trig low to high threshold point with pull-down resistor enabled		0.95	1.05	1.13	V
V_{TPD-}	Schmitt trig high to low threshold point with pull-up resistor enabled		0.63	0.74	0.83	V
I_L	Input Leakage Current @ V_I=1.8V or 0V				±10	µA
I_{OZ}	Tri-State output leakage current @ V_I=1.8V or 0V				±10	µA
R_{PU}	Pull-up Resistor		117	194	331	kΩ
R_{PD}	Pull-down Resistor		91	159	291	kΩ
V_{OL}	Output low voltage				0.45	V
V_{OH}	Output high voltage		1.35			V
I_{OL}	Low level output current @ V_{OL}(max)	8mA	6.8	12.2	19.5	mA
		4mA	4.6	8.2	13	mA
I_{OH}	High level output current @ V_{OH}(min)	8mA	4.8	11.4	22.2	mA
		4mA	3.4	8.2	15.9	mA

Table 3-8 DC characteristics for VDDIO_CAN supplied pins for 3.3V application

Symbol	Parameter	Min	Typical	Max	Unit
V_{IL}	Input Low Voltage	-0.3		0.8	V
V_{IH}	Input High Voltage	2		5.5	V
V_T	Threshold point	1.36	1.46	1.58	V
V_{T+}	Schmitt trig low to high threshold point	1.71	1.84	1.94	V
V_{T-}	Schmitt trig high to low threshold point	1.18	1.27	1.4	V
V_{TPU}	Threshold point with pull-up resistor enabled	1.32	1.42	1.55	V
V_{TPD}	Threshold point with pull-down resistor enabled	1.39	1.48	1.6	V
V_{TPU+}	Schmitt trig low to high threshold point with pull-up resistor enabled	1.67	1.8	1.91	V
V_{TPU-}	Schmitt trig high to low threshold point with pull-down resistor enabled	1.14	1.25	1.37	V
V_{TPD+}	Schmitt trig low to high threshold point with pull-down resistor enabled	1.74	1.87	1.99	V
V_{TPD-}	Schmitt trig high to low threshold point with pull-up resistor enabled	1.21	1.31	1.42	V
I_L	Input Leakage Current @ V_I=1.8V or 0V			±10	µA
I_{OZ}	Tri-State output leakage current @ V_I=1.8V or 0V			±10	µA
R_{PU}	Pull-up Resistor	29	41	61	kΩ
R_{PD}	Pull-down Resistor	31	45	74	kΩ
V_{OL}	Output low voltage			0.4	V
V_{OH}	Output high voltage	2.4			V

I_{OL}	Low level output current @ V_{OL}(max)	8mA	8.9	14	19.1	mA
I_{OH}	High level output current @ V_{OH}(min)	8mA	15.7	31	52.3	mA

3.4 SARADC Electrical Characteristics

Table 3-9 SARADC Performance

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Operating Condition						
Analog Supply	AVDD	-	2.97	3.3	3.63	V
SARADC Performance						
Resolution	-	-	-	12	-	bit
Effective Number of Bit	ENOB	-	-	11	-	bit
Differential Nonlinearity	DNL	-	-1	-	+1	LSB
Integral Nonlinearity	INL	-	-2	-	+2	LSB
Reference voltage	VREFP		-	3.3	-	V
Input Capacitance	C_{IN}	-	-	8	-	pF
Sampling Rate	f_S	-	-	-	2	MS/s
Spurious Free Dynamic Range	SFDR	f_S=2MS/s f_{OUT}=1.17KHz	-	70	-	dB
Signal to Noise and Harmonic Ratio	SNDR	-	-	68	-	dB
Power Consumption						
Analog Supply Current	IAVDD	f_S=2MS/s	-	2.5	-	mA
		Power Down	-	1	-	uA

3.5 Power On, Reset and BOOT

3.5.1 Power-On Timing

The external voltage regulator and other power-on devices must provide the X1600/E processor with a specific sequence of power and reset to ensure proper operation. Figure 3-1 shows this sequence and Table 3-10 gives the timing parameters. Following are the name of the power.

RTC_AVDD: RTC_AVDD

RTC_VDD: RTC_VDD

VDDIO: all other digital IO, include DDR power supplies, include VDDIO, VDDIO_CAN, VDDIO_LCD, PLL_AVDD, VDDMEM, DDR_PLLVCCA, DDR_VDD1

AVD33: all analog power supplies, include CSI_VCCA33, SADC_AVDD, USB_AVD33

VDD: all 1.1V power supplies, include VDD, PLL_VDD, CSI_VCCA11, USB_AVD11

AVDEFUSE: AVDEFUSE

Table 3-10 Power-On Timing Parameters

Symbol	Parameter	Min	Max	Unit
t_{D_VDDRTC}	Delay between RTC_AVDD arriving 50% to RTC_VDD arriving 90%[1]	0	–	ms
t_{D_VDDIO}	Delay between RTC_AVDD arriving 50% to VDDIO arriving 50%[1]	0	–	ms
t_{D_VDD}	Delay between VDDIO arriving 50% to VDD arriving 90%[1]	0	–	ms
t_{D_AVD33}	Delay between AVDD arriving 90% to VDDIO to be turned on	20	–	us
$t_{D\_PPRST\_}$	Delay between all power rails get stable and power-on reset PPRST_ de-asserted[2]	TBD[3]	–	ms[2]
$t_{D\_AVDEFUSE}$	Delay between PPRST_ finished and E-fuse programming power apply	0	–	ms
$t_{H\_AVDEFUSE}$	E-fuse programming time	–	200	ms

NOTES:

1 The power rails have same skew.

2 The PPRST_ must be kept at least 1ms. After PPRST_ is deasserted, the corresponding chip reset will be extended 1ms.

3 It must make sure the EXCLK is stable and all power suppliers (except AVDEFUSE) is stable.

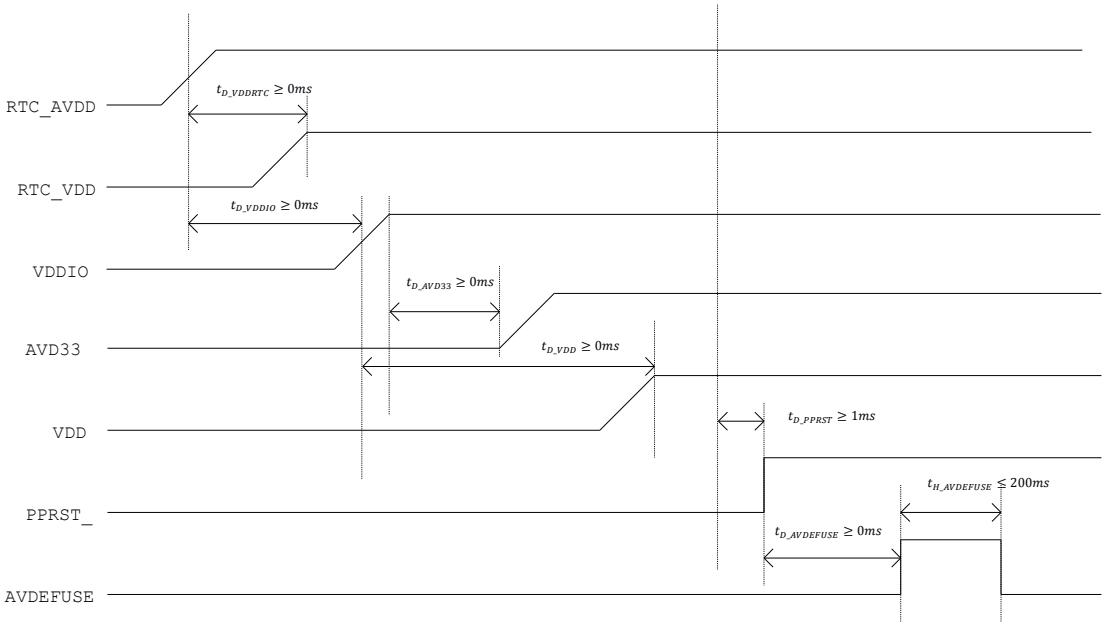


Figure 3-1 Power-On Timing Diagram 1

3.5.2 Power On Reset

X1600/E has an internal POR circuit which can be enabled by pulling the pin POR_CTL up to the power rail. And the POR_CTL is ought to be connected to the GND if the POR circuit is not used.

Table 3-11 POR Characteristic

Symbol	Parameter	Min	Typical	Max	Unit
V_{tha+}	Power up threshold on VDDIO supply[1]	1.85	1.95	2.05	V
V_{tha-}	Power down threshold on VDDIO supply[1]	1.75	1.85	1.95	V
V_{thd+}	Power up threshold on VDD supply[1]	0.67	0.72	0.77	V
V_{thd-}	Power down threshold on VDD supply[1]	0.57	0.62	0.67	V
V_{hysa}	POR hysteresis on VDDIO supply[1]	-	0.1	-	V
V_{hysd}	POR hysteresis on VDD supply[1]	-	0.1	-	V
T_{dr}	Debounce delay time for POR rising edge	-	120	-	us
T_{df}	Debounce delay time for POR falling edge	-	4	-	us
T_{D_POR}	Extend delay time for POR rising edge[2]		15		ms

Note:

1 In order to use the POR circuit to reset X1600/E, please merge the power rail RTC_VDD to the power rail VDD, and merge the power rail RTC_AVDD to the power rail VDDIO. Moreover, the POR circuit is only suitable for the VDDIO 3.3V application, cannot be used for VDDIO 1.8V application.

2 After POR is deasserted, the corresponding chip reset will be extended 15ms.

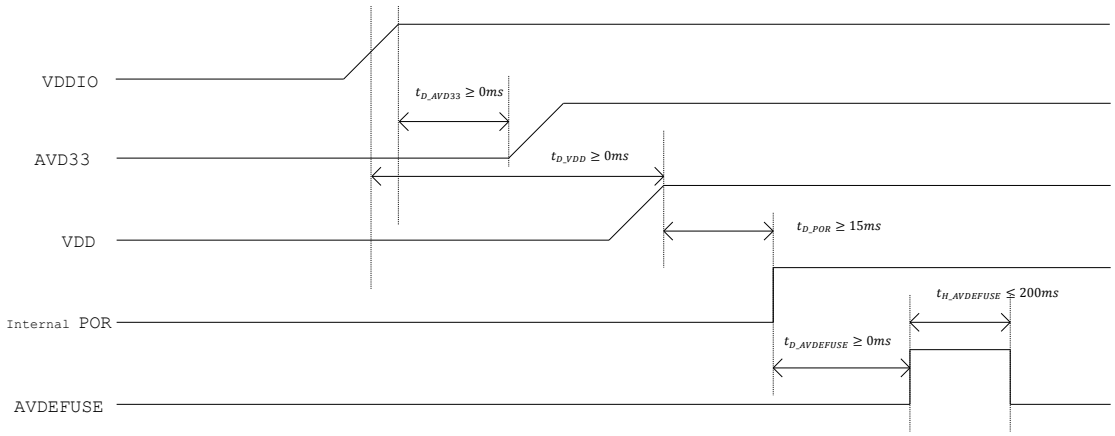


Figure 3-2 Power-On Timing Diagram 2

Following figure shows the sequence where VDDIO rises first and VDD drops first.

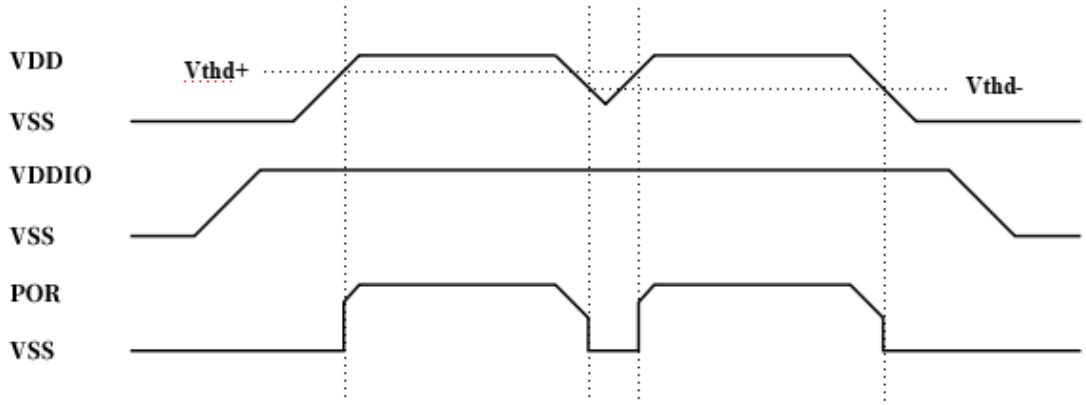


Figure 3-3 POR TIMING 1

Following figure shows the sequence where VDD rises first and VDDIO drops first.

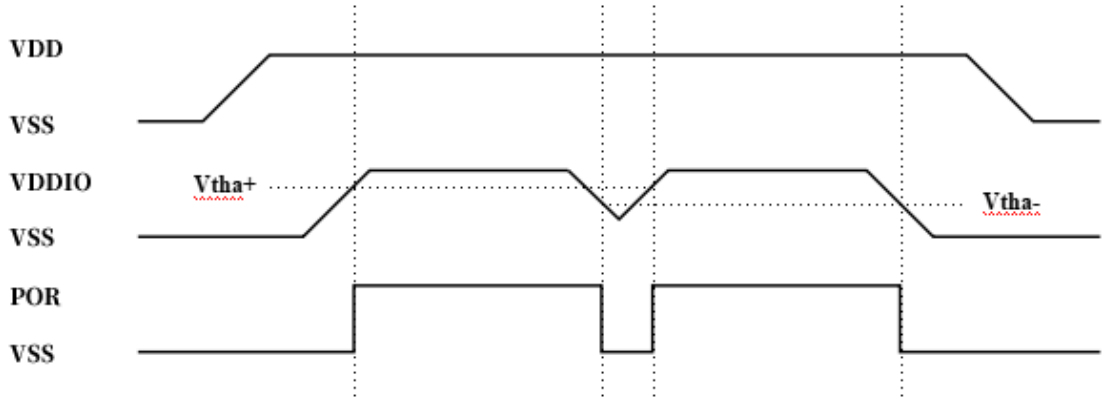


Figure 3-4 POR TIMING 2

3.5.3 Reset procedure

In addition, X1600/E also supports other 3 reset sources: 1 PPRST_ pin reset; 2 WDT timeout reset; and 3 hibernating reset when exiting hibernating mode. After reset, program start from boot. But it is worth mentioning that POR and PPRST_ reset cannot work together.

1 PPRST_ pin reset.
This reset is trigged when PPRST_ pin is put to logic 0. It happens in power on RTC power and RESET-KEY pressed to reset the chip from unknown dead state. The reset end time is about 10ms (512 clock whose frequence is exclk/512) after rising edge of PPRST_.

2 WDT reset.
This reset happens in case of WDT timeout.

3 Hibernating reset.
This reset happens in case of wakeup the main power from power down. The reset keeps for about 125ms as default and can be programed up to 1s, plus 10ms (512 clock whose frequence is exclk/512), start after WKUP_ signal is recognized.

After reset, all GPIO shared pins are put to GPIO input function， except JTAG relate TCK/TMS/TDI /TDO which reset to function mode, and most of their internal pull-up/down resistors are set to on. The PWRON is output 1. The oscillators are on.

3.5.4 BOOT

The boot sequence of the X1600/E is controlled by boot_sel [1:0], GPIO PC27/28 PAD

Table 3-12 Boot Configuration of X1600/E

boot_sel[1]	boot_sel[0]	Boot configuration
0	0	MSC0@PC(17-22)
0	1	SFC0@PC(17-22)
1	0	NOR
1	1	USB

After reset, the boot program on the internal Boot ROM executes as follows:

1 Disable all interrupts, prepare the program running environment.

2 Read and save efuse values, the values to determine whether to set MSC 4-bit transmission data, MSC wait status, gpio HI-Z, hide USB device information, USB eye diagram.

3 Initialize clock and read boot_sel[1:0] to determine the boot method.

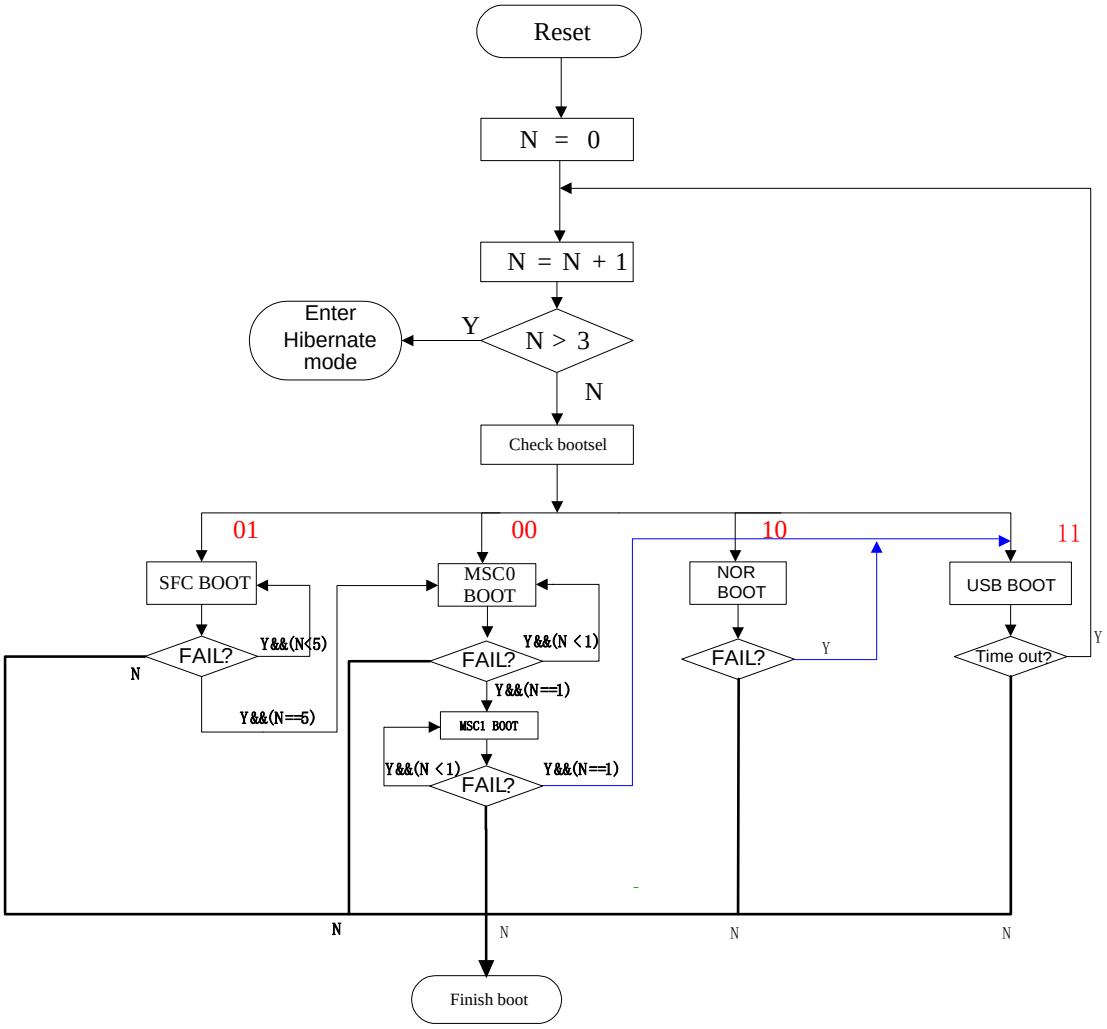
4 If it is boot from MMC/SD card at MSC0, the boot program loads the 26KB data from MMC/SD card to cache and jump to it. The clock 187.5KHz (MSC_CDR=12M, DEV_CLK=12M/64) is used initially. When reading data, the clock 12Mhz is used. If the msc_bus_width_4 efuse value is set to 1, the function pins MSC_D0, MSC_D1, MSC_D2, MSC_D3 are initialized for 4-bit data transmission, otherwise, only the MSC_D0 data bus is used.

5 If it is boot from USB, a block of code will be received through USB cable connected with host PC and be stored in cache. Then branch to this area in cache.

6 If it is boot from SPI nor/nand at SFC, its function pins SFC_CLK, SFC_CE, SFC_DR, SFC_DT, SFC_WP, SFC_HOL are initialized, the boot program loads the spl size bytes code from nor/nand to cache and jump to it

7 If it is boot from NOR Flash, the boot program jump to nor and run directory.

NOTE: The Boot ROM of X1600/E occupies 36KB of cache, its address is from 0x80000000 to 0x80009000.

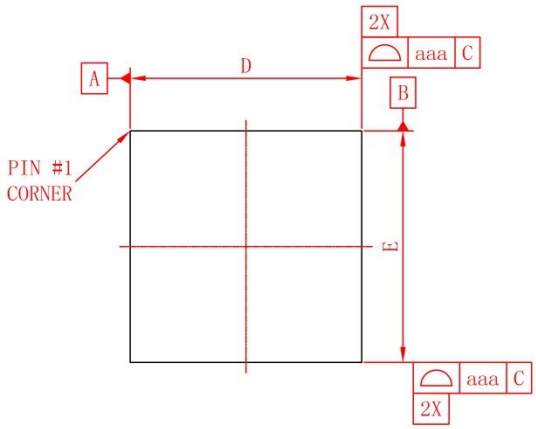


4 Packaging Information

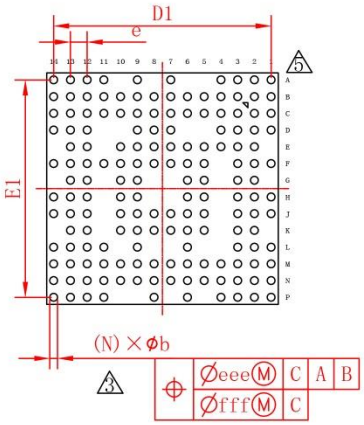
4.1 Overview

X1600/E processor is offered in 159-pin BGA package, which is 9mm x 9mm x 1.38mm outline, 14 x 14 matrix ball grid array and 0.65mm ball pitch, show in Figure 4-1

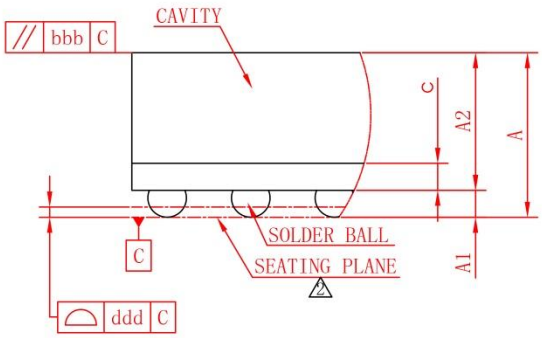
4.2 Device Dimensions



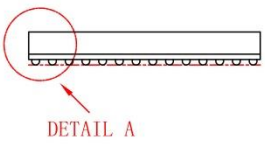
Top View



Bottom View



DETAIL A



Side View

symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.380	---	---	0.054
A1	0.160	0.210	0.260	0.006	0.008	0.010
A2	1.020	1.070	1.120	0.040	0.042	0.044
c	0.180	0.210	0.240	0.007	0.008	0.009
D	8.900	9.000	9.100	0.350	0.354	0.358
E	8.900	9.000	9.100	0.350	0.354	0.358
D1	---	8.450	---	---	0.333	---
E1	---	8.450	---	---	0.333	---
e	---	0.650	---	---	0.026	---
b	0.250	0.300	0.350	0.010	0.012	0.014
aaa	0.100			0.004		
bbb	0.100			0.004		
ddd	0.080			0.003		
eee	0.150			0.006		
fff	0.080			0.003		
Ball Diam	0.300			0.012		
N	159			159		
MD/ME	14/14			14/14		

Figure 4-1 X1600/E package outline drawing

Notes:

1. BALL PAD OPENING: 0.270mm;
2. PRIMARY DATUM C AND SEATING PLANE ARE THE SOLDER BALLS;
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER,PARALLEL TO PRIMARY DATUM C;
4. SPECIAL CHARACTERISTICS C CLASS: bbb, ddd;
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY;
6. BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES.

4.3 Solder Ball Materials

Both the top (joint) and bottom solder ball materials of X1600/E are SAC125.

4.4 Moisture Sensitivity Level

X1600/E package moisture sensitivity is level 3.