

# Mono DAC with 2.6W Class AB/D Speaker Driver, Dynamic Range Controller and ReTune™ Mobile Parametric Equalizer

## DESCRIPTION

The WM9081 is designed to provide high power output at low distortion levels in space-constrained portable applications.

ReTune™ Mobile Parametric EQ with fully programmable coefficients is integrated for optimization of speaker characteristics. Programmable dynamic range control is also available for maximizing loudness, protecting speakers from clipping and preventing premature shutdown due to battery droop.

Digital input enables the power drivers to be located close to the speakers in multi-channel systems without the need for troublesome long analogue connections. Location of the power drivers close to the speakers also removes the need for bulky and expensive class D filters and reduces PCB track lengths, minimising emissions. The digital input can also help to minimise crosstalk to the speaker output signal from high gain microphone inputs, enhancing stability and reducing the risk of 'howling' during speakerphone operation.

Four control interface addresses and four-channel TDM are supported to allow multiple devices to be configured and driven independently.

The device is controlled via a standard 2-wire, 3-wire, or 4-wire control interface or by hardware control pins.

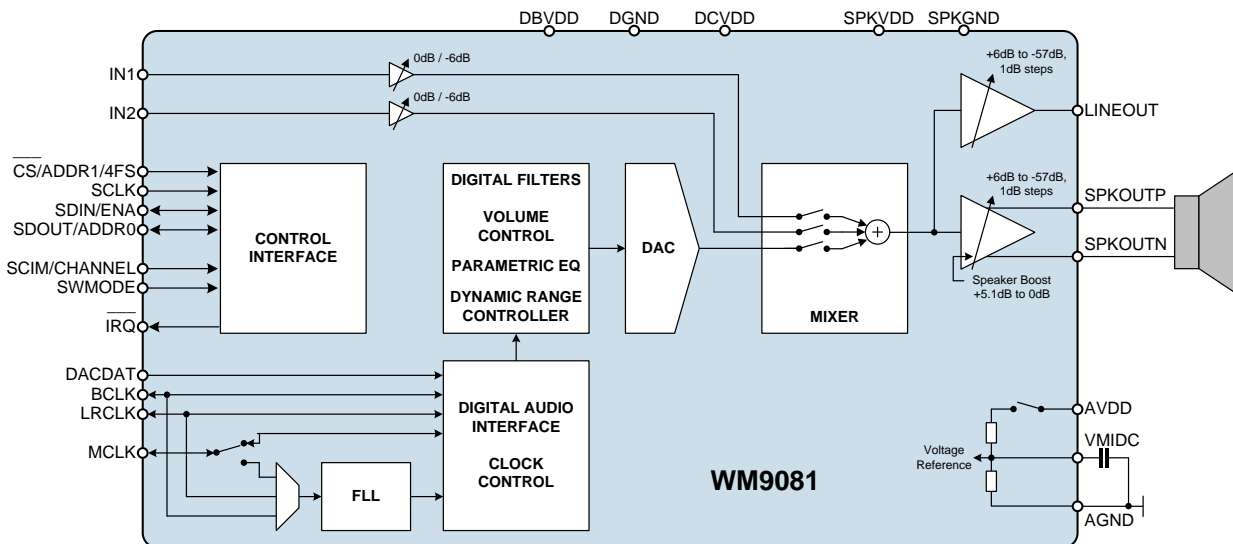
## FEATURES

- High-power, high performance DAC and speaker driver
  - 92dB SNR ('A-weighted') in Class D mode
  - 97dB SNR ('A-weighted') in Class AB mode
  - <0.05% THD+N @0.5W continuous into 4Ω (Class D)
  - <0.10% THD+N @2W continuous into 4Ω (Class D)
  - 2.6W maximum peak power
- ReTune™ Mobile Parametric Equalizer
  - Fully programmable filter coefficients
- Programmable dynamic range controller
  - Boosts small signals to maximise loudness
  - Protects against battery droop and clipping
- Speaker common mode boost
  - Maximises power for a given SPKVDD/AVDD ratio
- Low power FLL
  - Provides all necessary internal clocks
  - 32kHz to 27MHz input frequency
- All common sample rates from 8kHz to 96kHz supported
- Standard 2-wire, 3-wire, 4-wire and hardware control modes
- Data formats: LJ, RJ, I<sup>2</sup>S, DSP, all with TDM support
- Thermal shutdown interrupt
- 4x4 COL package (0.45mm lead pitch)
- Operating temperature range: -40°C to 85°C

## APPLICATIONS

- Portable navigation systems
- Mobile phones
- Flat panel TVs

## BLOCK DIAGRAM

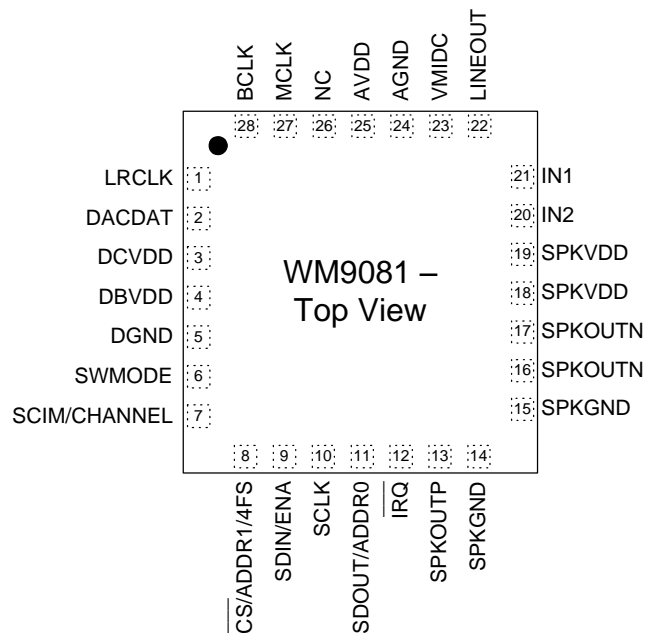


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## PIN CONFIGURATION



## ORDERING INFORMATION

| ORDER CODE    | TEMPERATURE RANGE | PACKAGE  | MOISTURE SENSITIVITY LEVEL | PEAK SOLDERING TEMPERATURE |
|---------------|-------------------|--|----------------------------|----------------------------|
| WM9081GICN/V  | -40°C to +85°C    | 28-lead COL (4x4x0.55mm)<br>(Pb-free)                | MSL3                       | 260°C                      |
| WM9081GICN/RV | -40°C to +85°C    | 28-lead COL (4x4x0.55mm)<br>(Pb-free, Tape and reel) | MSL3                       | 260°C                      |

**Note:**

Reel quantity = 3500

**PIN DESCRIPTION**

| PIN NO | NAME         | TYPE                   | DESCRIPTION  |
|--------|--------------|------------------------|--|
| 1      | LRCLK        | Digital Input / Output | Audio interface DAC left / right clock   |
| 2      | DACDAT       | Digital Input          | DAC digital audio data   |
| 3      | DCVDD        | Supply                 | Digital core supply  |
| 4      | DBVDD        | Supply                 | Digital buffer (I/O) supply  |
| 5      | DGND         | Supply                 | Digital ground (Return path for both DCVDD and DBVDD)  |
| 6      | SWMODE       | Digital Input          | Selects hardware or software control mode  |
| 7      | SCIM/CHANNEL | Digital Input          | 2-wire or 3-wire control select (Software mode) /<br>Left / right data channel select (Hardware mode)                |
| 8      | CS/ADDR1/4FS | Digital Input          | 3-wire chip select or 2-wire address select (Software mode) /<br>Normal fs input or 4fs input select (Hardware mode) |
| 9      | SDIN/ENA     | Digital Input / Output | Control interface data input (Software mode) /<br>Device enable (Hardware mode)                                      |
| 10     | SCLK         | Digital Input          | Control interface clock input (Software mode)  |
| 11     | SDOUT/ADDR0  | Digital Input/ Output  | 4-wire data output or 2-wire address select (Software mode)  |
| 12     | IRQ          | Digital Output         | Interrupt signal   |
| 13     | SPKOUTP      | Analogue Output        | Positive BTL speaker output  |
| 14     | SPKGND       | Supply                 | Speaker ground (1) (Return path for SPKVDD)  |
| 15     | SPKGND       | Supply                 | Speaker ground (2) (Return path for SPKVDD)  |
| 16     | SPKOUTN      | Analogue Output        | Negative BTL speaker output (1)  |
| 17     | SPKOUTN      | Analogue Output        | Negative BTL speaker output (2)  |
| 18     | SPKVDD       | Supply                 | Speaker supply (1)   |
| 19     | SPKVDD       | Supply                 | Speaker supply (2)   |
| 20     | IN2          | Analogue Input         | Line input   |
| 21     | IN1          | Analogue Input         | Line input   |
| 22     | LINEOUT      | Analogue Output        | Line output  |
| 23     | VMIDC        | Reference              | Mid-rail voltage (VMID) decoupling connection  |
| 24     | AGND         | Supply                 | Analogue ground (Return path for AVDD)   |
| 25     | AVDD         | Supply                 | Analogue supply  |
| 26     | NC           |                        | Not connected  |
| 27     | MCLK         | Digital Input / Output | Master clock   |
| 28     | BCLK         | Digital Input / Output | Audio interface bit clock  |

## ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Cirrus Logic tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.

MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

| CONDITION                            | MIN        | MAX         |
|--------------------------------------|------------|-------------|
| Supply voltages (excluding SPKVDD)   | -0.3V      | +4.5V       |
| SPKVDD                               | -0.3V      | +7V         |
| Voltage range digital inputs         | DGND -0.3V | DBVDD +0.3V |
| Voltage range analogue inputs        | AGND -0.3V | AVDD +0.3V  |
| Junction temperature, T <sub>J</sub> | -40°C      | +150°C      |
| Storage temperature after soldering  | -65°C      | +150°C      |

### Notes

- Analogue, digital and speaker grounds must always be within 0.3V of each other.

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER                            | SYMBOL             | MIN  | TYP | MAX  | UNIT |
|--------------------------------------|--------------------|------|-----|------|------|
| Digital supply range (Core)          | DCVDD              | 1.71 | 1.8 | 3.6  | V    |
| Digital supply range (Buffer)        | DBVDD              | 1.71 | 1.8 | 3.6  | V    |
| Analogue supplies range              | AVDD               | 2.7  | 3.3 | 3.6  | V    |
| Speaker supply range                 | SPKVDD             | 2.7  | 5.0 | 5.5  | V    |
| Ground                               | DGND, AGND, SPKGND |      | 0   |      | V    |
| Ambient temperature, T <sub>A</sub>  |                    | -40  |     | +85  | °C   |
| Junction temperature, T <sub>J</sub> |                    | -40  |     | +125 | °C   |

### Notes

- All digital and analogue supplies are completely independent from each other (i.e. not internally connected).
- DCVDD must be less than or equal to AVDD.
- DCVDD must be less than or equal to DBVDD.
- AVDD must be less than or equal to SPKVDD.
- SPKVDD must be high enough to support the peak output voltage when using DCGAIN and ACGAIN functions, to avoid output waveform clipping.
- Junction temperature is a function of ambient temperature and of the device operating conditions. The ambient temperature limits and the junction temperature limits must both be observed.

## ELECTRICAL CHARACTERISTICS

### COMMON TEST CONDITIONS

Unless otherwise stated, the following test conditions apply throughout the following sections:

- DCVDD = DBVDD = 1.8V, AVDD = 3.3V, SPKVDD = 5.0V
- PGA gain = 0dB
- ACGAIN=DCGAIN=1.52
- Audio signal: 1kHz sine wave, sampled at 48kHz with 24-bit data resolution, I<sup>2</sup>S mode
- Ambient temperature: T<sub>A</sub> = +25°C
- C<sub>VMID</sub> = 4.7μF
- VMID\_SEL[1:0] = 01 (2x40kΩ)

Additional, specific test conditions are given within the relevant sections below.

## AUDIO DAC

### TERMINOLOGY

1. Signal-to-Noise Ratio (dB) – SNR is a measure of the difference in level between the maximum theoretical full scale output signal and the output with no input signal applied.
2. Total Harmonic Distortion (dB) – THD is the level of the rms value of the sum of harmonic distortion products relative to the amplitude of the measured output signal.
3. Total Harmonic Distortion plus Noise (dB) – THD+N is the level of the rms value of the sum of harmonic distortion products plus noise in the specified bandwidth relative to the amplitude of the measured output signal.
4. All performance measurements carried out with 20kHz low pass filter, and where noted an A-weighted filter. Failure to use such a filter will result in higher THD and lower SNR readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
5. Mute Attenuation – This is a measure of the difference in level between the full scale output signal and the output with mute applied.

### DAC TO SPEAKER OUTPUT

| PARAMETER   | TEST CONDITIONS                 | MIN | TYP | MAX | UNIT |
|---|---------------------------------|-----|-----|-----|------|
| <b>DAC to Speaker Output (4.1Ω + 22μH BTL Load)</b> |                                 |     |     |     |      |
| SNR (A-weighted)                                    | DAC to speaker output, class D  | 85  | 92  |     | dB   |
| THD+N (P <sub>O</sub> =0.5W)                        |                                 |     |     |     |      |
| THD+N (P <sub>O</sub> =1.0W)                        |                                 |     |     |     |      |
| THD+N (P <sub>O</sub> =2.0W)                        |                                 |     |     |     |      |
| SNR (A-weighted)                                    | DAC to speaker output, class AB | 90  | 97  |     | dB   |
| THD+N (P <sub>O</sub> =0.5W)                        |                                 |     |     |     |      |
| THD+N (P <sub>O</sub> =1.0W)                        |                                 |     |     |     |      |
| THD+N (P <sub>O</sub> =2.0W)                        |                                 |     |     |     |      |

| PARAMETER                                    | TEST CONDITIONS  | MIN | TYP | MAX | UNIT |
|--|--|-----|-----|-----|------|
| <b>Power Supply Rejection (20Hz – 20kHz)</b> |  |     |     |     |      |
| SPKVDD PSRR                                  | 400mV pk-pk at 217Hz on SPKVDD;<br>DAC to speaker output, class D  |     | 75  |     | dB   |
|  | 400mV pk-pk at 217Hz on SPKVDD;<br>DAC to speaker output, class AB |     | 85  |     | dB   |
| AVDD PSRR                                    | 100mV pk-pk at 217Hz on AVDD;<br>DAC to speaker output, class D    |     | 60  |     | dB   |
|  | 100mV pk-pk at 217Hz on AVDD;<br>DAC to speaker output, class AB   |     | 60  |     | dB   |

**DAC TO LINE OUTPUT**

| PARAMETER                                    | TEST CONDITIONS                                     | MIN | TYP | MAX | UNIT |
|--|---|-----|-----|-----|------|
| <b>DAC to Line Output (10kΩ / 50pF Load)</b> |   |     |     |     |      |
| SNR (A-weighted)                             | DAC to line out, 0dBFS input                        | 90  | 99  |     | dB   |
| THD+N  |   |     | -83 | -75 | dB   |
| <b>Power Supply Rejection</b>                |   |     |     |     |      |
| AVDD PSRR                                    | 100mV pk-pk at 217Hz on AVDD;<br>DAC to line output |     | 50  |     | dB   |

**OUTPUT CHARACTERISTICS**

| PARAMETER  | TEST CONDITIONS  | MIN | TYP     | MAX | UNIT |
|--|------------------|-----|---------|-----|------|
| Speaker Load Resistance  |                  | 4   |         |     | Ω    |
| Line Out Load Resistance   |                  | 5   | 10      | 100 | kΩ   |
| Line Out Capacitance   |                  |     |         | 2   | nF   |
| Maximum Continuous Speaker Output Power                                      | Class D mode     |     | 2       |     | W    |
|  | Class AB mode    |     | 2       |     | W    |
| Maximum Peak Speaker Output Power  | Class D mode     |     | 2.6     |     | W    |
|  | Class AB mode    |     | 2.6     |     | W    |
| SPKVDD Leakage Current   | SPKVDD = 5.0V    |     | 0.15    | 1   | μA   |
| <b>Line Output Programmable Gain Amplifier</b>                               |                  |     |         |     |      |
| Minimum Gain   |                  |     | -57     |     | dB   |
| Maximum Gain   |                  |     | +6      |     | dB   |
| Gain Step Size   |                  |     | 1       |     | dB   |
| Mute Attenuation   |                  | 80  | 92      |     | dB   |
| <b>Speaker Output Programmable Gain Amplifier</b>                            |                  |     |         |     |      |
| Minimum Gain   |                  |     | -57     |     | dB   |
| Maximum Gain   |                  |     | +6      |     | dB   |
| Gain Step Size   |                  |     | 1       |     | dB   |
| Mute Attenuation   |                  | 80  | 92      |     | dB   |
| <b>DAC Digital</b>   |                  |     |         |     |      |
| DAC maximum volume   |                  |     | 0       |     | dB   |
| DAC minimum volume   |                  |     | -71.625 |     | dB   |
| DAC volume step size   |                  |     | 0.375   |     | dB   |
| DAC soft mute time (Note: Scales linearly with sample rate)<br>0dBFS to mute | DAC_MUTERATE = 0 |     | 10.7    |     | ms   |
|  | DAC_MUTERATE = 1 |     | 171     |     | ms   |

**ANALOGUE REFERENCE LEVELS**

| PARAMETER                      | TEST CONDITIONS | MIN | TYP    | MAX | EV |
|--------------------------------|-----------------|-----|--------|-----|----|
| <b>Reference Voltages</b>      |                 |     |        |     |    |
| VMID Midrail Reference Voltage |                 | -3% | AVDD/2 | +3% | V  |

**ANALOGUE INPUTS (IN1, IN2)**

| PARAMETER                  | TEST CONDITIONS | MIN | TYP | MAX      | UNIT |
|----------------------------|-----------------|-----|-----|----------|------|
| Maximum Input Signal Level |                 |     |     | AVDD/3.3 | Vrms |
| IN1 Input resistance       | 0dB PGA gain    |     | 25  |          | kΩ   |
|                            | -6dB PGA gain   |     | 50  |          | kΩ   |
| IN2 Input resistance       | 0dB PGA gain    |     | 25  |          | kΩ   |
|                            | -6dB PGA gain   |     | 50  |          | kΩ   |

**DIGITAL INTERFACES**

| PARAMETER                     | TEST CONDITIONS       | MIN           | TYP | MAX           | UNIT |
|-------------------------------|-----------------------|---------------|-----|---------------|------|
| <b>Digital Input / Output</b> |                       |               |     |               |      |
| Input HIGH Level              |                       | 0.7×<br>DBVDD |     |               | V    |
| Input LOW Level               |                       |               |     | 0.3×<br>DBVDD | V    |
| Output HIGH Level             | I <sub>OL</sub> =1mA  | 0.9×<br>DBVDD |     |               | V    |
| Output LOW Level              | I <sub>OH</sub> =-1mA |               |     | 0.1×<br>DBVDD | V    |
| Input Capacitance             |                       |               | 10  |               | pF   |
| Input Leakage                 |                       | -0.5          |     | 0.5           | μA   |

**CLOCKING AND TIMING**

| PARAMETER                                | TEST CONDITIONS | MIN  | TYP | MAX    | UNIT                          |
|--|-----------------|------|-----|--------|-------------------------------|
| <b>FLL</b>                               |                 |      |     |        |                               |
| Input Frequency                          |                 | 8kHz |     | 27MHz  |                               |
| Lock time                                |                 |      |     | TBA    | Reference<br>Clock<br>Periods |
| <b>MCLK</b>                              |                 |      |     |        |                               |
| Input Frequency                          |                 |      |     | 25.000 | MHz                           |
| <b>CLK_SYS</b>                           |                 |      |     |        |                               |
| Frequency                                |                 |      |     | 12.500 | MHz                           |
| <b>Power-up and Power-down Sequences</b> |                 |      |     |        |                               |
| Power-up Time                            | Hardware mode   |      | 42  |        | ms                            |
|  | Software mode   |      | 42  |        | ms                            |
| Power-down Time                          | Hardware mode   |      | 48  |        | ms                            |
|  | Software mode   |      | 48  |        | ms                            |



## TYPICAL POWER CONSUMPTION

The WM9081 power consumption is dependent on many parameters. Most significantly, it depends on supply voltages, sample rates, mode of operation, and output loading.

The power consumption on each supply rail varies approximately with the square of the voltage. Power consumption is greater at fast sample rates than at slower ones. When the digital audio interface is operating in Master mode, the DBVDD current is significantly greater than in Slave mode. The output load conditions (impedance, capacitance and inductance) can also impact significantly on the device power consumption.

## COMMON TEST CONDITIONS

Unless otherwise stated, the following test conditions apply throughout the following sections:

- Ambient temperature = +25°C
- Audio signal = quiescent (zero amplitude)
- Sample rate = 48kHz
- MCLK = 12.288MHz
- Audio interface mode = slave
- Control mode: software

Additional, variant test conditions are quoted within the relevant sections below. Where applicable, power dissipated in the speaker or line loads is included.

## POWER CONSUMPTION MEASUREMENTS

| <b>Off and Standby modes</b>   |      |      |       |      |       |      |        |      |       |
|--|------|------|-------|------|-------|------|--------|------|-------|
| Test conditions:   |      |      |       |      |       |      |        |      |       |
| <ul style="list-style-type: none"> <li>• No clocks applied unless stated</li> <li>• No signal applied unless stated</li> </ul> |      |      |       |      |       |      |        |      |       |
| Variant test conditions  | AVDD |      | DCVDD |      | DBVDD |      | SPKVDD |      | TOTAL |
|  | V    | mA   | V     | mA   | V     | mA   | V      | mA   | mW    |
| Off (default settings)   | 3.3  | 0.05 | 1.8   | 0.01 | 1.8   | 0.01 | 5.0    | 0.00 | 0.18  |
| Off (default settings),<br>DACDAT, MCLK, BCLK and LRCLK applied  | 3.3  | 0.05 | 1.8   | 0.01 | 1.8   | 0.01 | 5.0    | 0.00 | 0.18  |
| Off (lowest power settings)  | 3.3  | 0.01 | 1.8   | 0.00 | 1.8   | 0.00 | 5.0    | 0.00 | 0.03  |

| <b>DAC to Speaker Playback - DAC input to SPKOUTP/SPKOUTN pins with 4.1Ω + 22μH load.</b>   |      |     |       |     |       |     |        |       |        |
|---|------|-----|-------|-----|-------|-----|--------|-------|--------|
| Test conditions:  |      |     |       |     |       |     |        |       |        |
| <ul style="list-style-type: none"> <li>• Slave mode, MCLK = 12.288MHz, LRCLK = 48kHz</li> <li>• Input signal: 0dBFS 1kHz sine wave</li> </ul> |      |     |       |     |       |     |        |       |        |
| Variant test conditions   | AVDD |     | DCVDD |     | DBVDD |     | SPKVDD |       | TOTAL  |
|   | V    | mA  | V     | mA  | V     | mA  | V      | mA    | mW     |
| DAC to Class D Speaker Playback no signal   | 3.3  | 2.7 | 1.8   | 1.3 | 1.8   | 0.0 | 5.0    | 2.7   | 24.9   |
| DAC to Class D Speaker Playback 0.5W  | 3.3  | 2.8 | 1.8   | 1.4 | 1.8   | 0.0 | 5.0    | 120.0 | 611.7  |
| DAC to Class D Speaker Playback 1.0W  | 3.3  | 2.8 | 1.8   | 1.4 | 1.8   | 0.0 | 5.0    | 225.0 | 1136.7 |
| DAC to Class D Speaker Playback 2.0W  | 3.3  | 2.8 | 1.8   | 1.4 | 1.8   | 0.0 | 5.0    | 435.0 | 2186.7 |

**DAC to Lineout Playback** - DAC input to LINEOUT pin with 10kΩ load.

Test conditions:

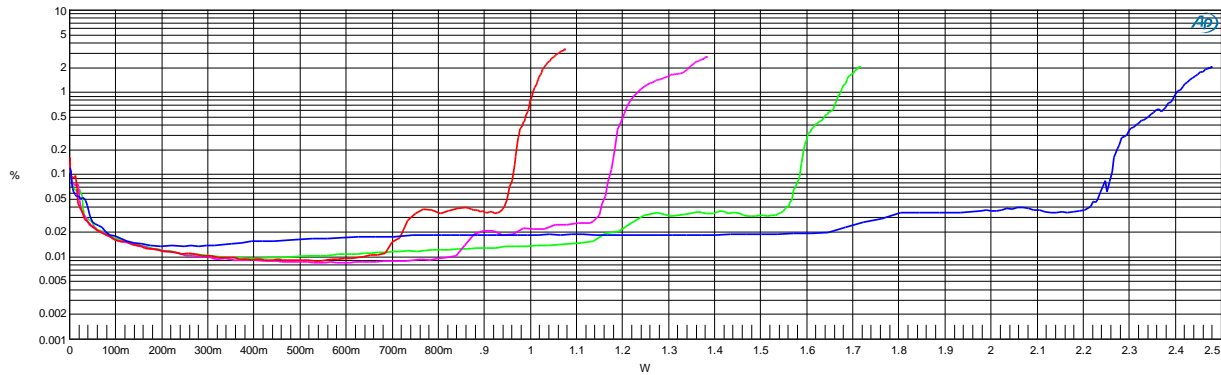
- Slave mode, MCLK = 12.288MHz, LRCLK = 48kHz
- Input signal: 0dBFS 1kHz sine wave

| Variant test conditions            | AVDD |     | DCVDD |     | DBVDD |     | SPKVDD |     | TOTAL |
|------------------------------------|------|-----|-------|-----|-------|-----|--------|-----|-------|
|                                    | V    | mA  | V     | mA  | V     | mA  | V      | mA  | mW    |
| DAC to LINEOUT, no input signal    | 3.3  | 1.9 | 1.8   | 1.3 | 1.8   | 0.0 | 5.0    | 0.0 | 8.5   |
| DAC to LINEOUT, 0dBFS input signal | 3.3  | 1.9 | 1.8   | 1.4 | 1.8   | 0.0 | 5.0    | 0.0 | 9.0   |

## TYPICAL PERFORMANCE DATA

Typical speaker driver THD+N performance is shown below for both 8Ω and 4Ω loads in Class D mode. Curves are shown for four typical SPKVDD supply voltage and gain combinations.

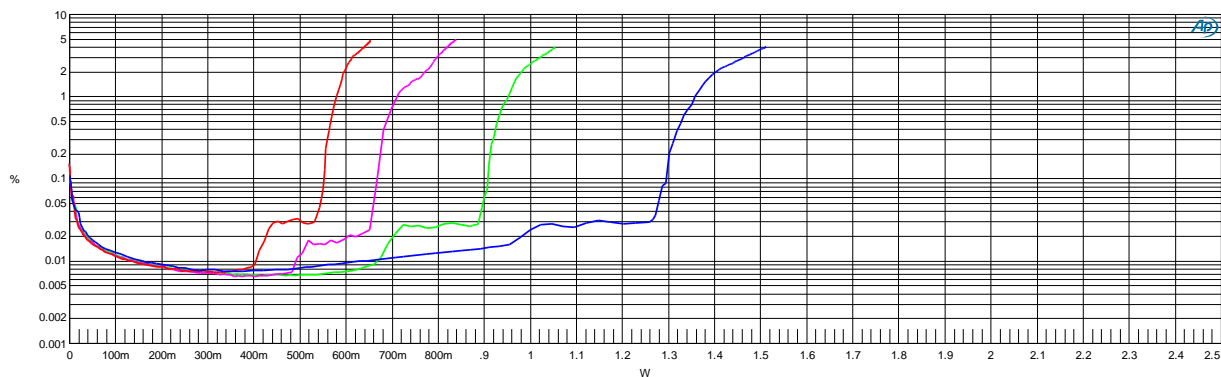
### SPEAKER CLASS D INTO 4Ω + 10μH



| Sweep | Trace | Color   | Line Style | Thick | Data              | Axis | Comment   |
|-------|-------|---------|------------|-------|-------------------|------|---|
| 1     | 1     | Blue    | Solid      | 2     | Anlr.TH+D+N Ratio | Left | SPKVDD = 5.0V, AVDD = 3.3V, DCGAIN = ACGAIN = 3.6dB |
| 2     | 1     | Green   | Solid      | 2     | Anlr.TH+D+N Ratio | Left | SPKVDD = 4.2V, AVDD = 3.3V, DCGAIN = ACGAIN = 2.1dB |
| 3     | 1     | Magenta | Solid      | 2     | Anlr.TH+D+N Ratio | Left | SPKVDD = 3.7V, AVDD = 3.0V, DCGAIN = ACGAIN = 2.1dB |
| 4     | 1     | Red     | Solid      | 2     | Anlr.TH+D+N Ratio | Left | SPKVDD = 3.3V, AVDD = 3.3V, DCGAIN = ACGAIN = 0dB   |

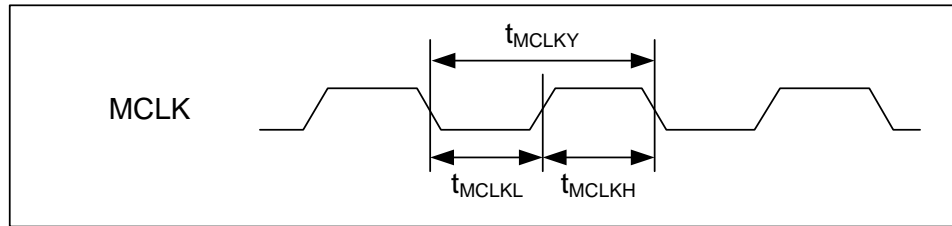
Device: WM9081 MMC=WPF  
 Input Signal: 1KHz; 0dBFS; 24-bit; 256fs (fs=48kHz)  
 Output Path: SPK Class D  
 Supplies: DBVDD=DCVDD=3.3V  
 BW Filter: 22Hz to 20kHz AES17  
 Additional Filtering: none  
 Load = 4R1 + 10uH

### SPEAKER CLASS D INTO 8Ω + 10μH



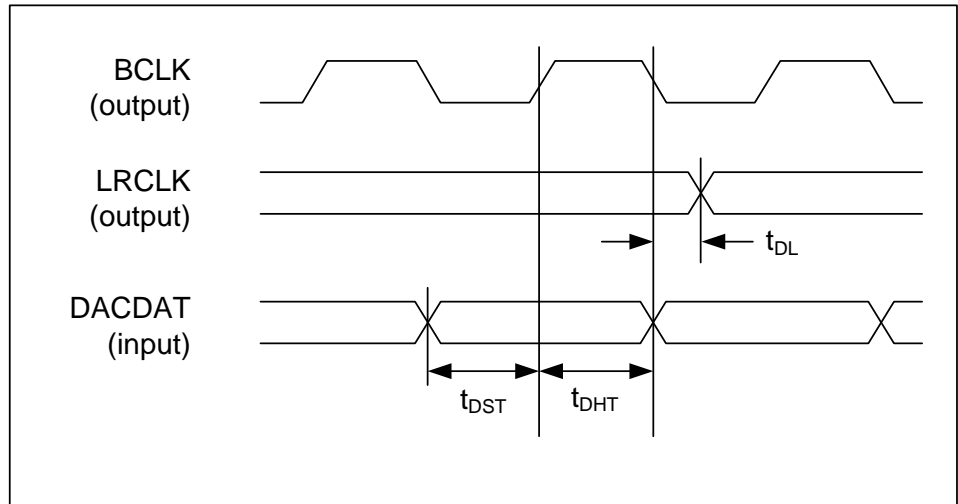
| Sweep | Trace | Color   | Line Style | Thick | Data              | Axis | Comment   |
|-------|-------|---------|------------|-------|-------------------|------|---|
| 1     | 1     | Blue    | Solid      | 2     | Anlr.TH+D+N Ratio | Left | SPKVDD = 5.0V, AVDD = 3.3V, DCGAIN = ACGAIN = 3.6dB |
| 2     | 1     | Green   | Solid      | 2     | Anlr.TH+D+N Ratio | Left | SPKVDD = 4.2V, AVDD = 3.3V, DCGAIN = ACGAIN = 2.1dB |
| 3     | 1     | Magenta | Solid      | 2     | Anlr.TH+D+N Ratio | Left | SPKVDD = 3.7V, AVDD = 3.0V, DCGAIN = ACGAIN = 2.1dB |
| 4     | 1     | Red     | Solid      | 2     | Anlr.TH+D+N Ratio | Left | SPKVDD = 3.3V, AVDD = 3.3V, DCGAIN = ACGAIN = 0dB   |

Device: WM9081 MMC=WPF  
 Input Signal: 1KHz; 0dBFS; 24-bit; 256fs (fs=48kHz)  
 Output Path: SPK Class D  
 Supplies: DBVDD=DCVDD=3.3V  
 BW Filter: 22Hz to 20kHz AES17  
 Additional Filtering: none  
 Load = 8R2 + 10uH

**SIGNAL TIMING REQUIREMENTS**
**SYSTEM CLOCK TIMING**

**Figure 1 System Clock Timing Requirements**
**Test Conditions**

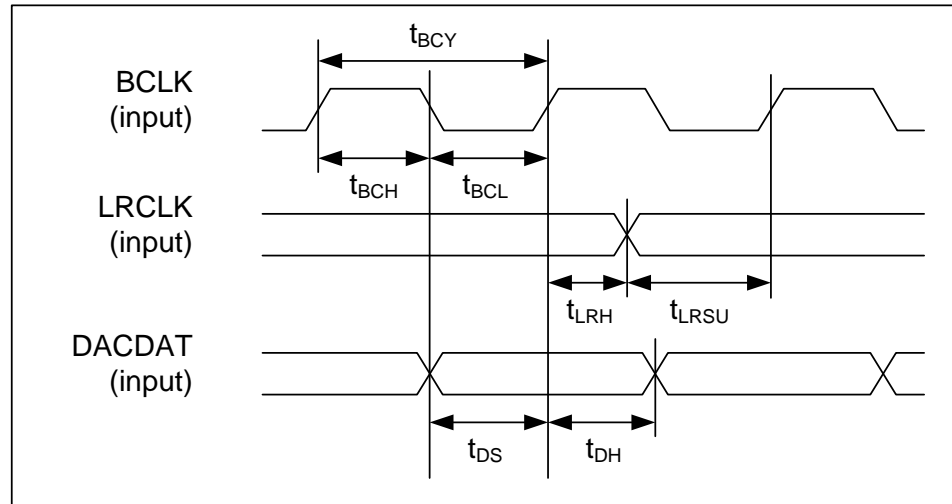
 DCVDD=DBVDD=1.8V, AVDD=3.3V, SPKVDD=5V, DGND=AGND=SPKGND=0V,  $T_A = +25^\circ\text{C}$ 

| PARAMETER                              | SYMBOL      | CONDITIONS              | MIN   | TYP | MAX   | UNIT |
|--|-------------|-------------------------|-------|-----|-------|------|
| <b>System Clock Timing Information</b> |             |                         |       |     |       |      |
| MCLK cycle time                        | $T_{MCLKY}$ |                         | 40    |     |       | ns   |
| MCLK duty cycle                        |             | $= T_{MCLKH}/T_{MCLKL}$ | 60:40 |     | 40:60 |      |

**AUDIO INTERFACE TIMING – MASTER MODE**

**Figure 2 Digital Audio Data Timing - Master Mode**
**Test Conditions**

DCVDD=DBVDD=1.8V, AVDD=3.3V, SPKVDD=5V, DGND=AGND=SPKGND=0V,  $T_A=+25^\circ\text{C}$ , Master Mode,  $f_s=48\text{kHz}$ , MCLK=256fs, 24-bit data, unless otherwise stated.

| PARAMETER                                      | SYMBOL    | MIN | TYP | MAX | UNIT |
|--|-----------|-----|-----|-----|------|
| <b>Audio Data Timing Information</b>           |           |     |     |     |      |
| LRCLK propagation delay from BCLK falling edge | $t_{DL}$  |     |     | 10  | ns   |
| DACDAT setup time to BCLK rising edge          | $t_{DST}$ | 10  |     |     | ns   |
| DACDAT hold time from BCLK rising edge         | $t_{DHT}$ | 10  |     |     | ns   |

**AUDIO INTERFACE TIMING – SLAVE MODE**

**Figure 3 Digital Audio Data Timing – Slave Mode**
**Test Conditions**

DCVDD=DBVDD=1.8V, AVDD=3.3V, SPKVDD=5V, DGND=AGND=SPKGND=0V, T<sub>A</sub>=+25°C, Slave Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

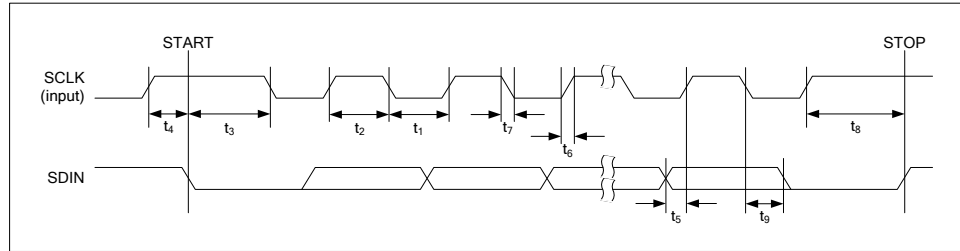
| PARAMETER                                  | SYMBOL            | MIN | TYP | MAX | UNIT |
|--|-------------------|-----|-----|-----|------|
| <b>Audio Data Input Timing Information</b> |                   |     |     |     |      |
| BCLK cycle time                            | t <sub>BCY</sub>  | 80  |     |     | ns   |
| BCLK pulse width high                      | t <sub>BCH</sub>  | 40  |     |     | ns   |
| BCLK pulse width low                       | t <sub>BCL</sub>  | 40  |     |     | ns   |
| LRCLK set-up time to BCLK rising edge      | t <sub>LRSU</sub> | 10  |     |     | ns   |
| LRCLK hold time from BCLK rising edge      | t <sub>LRH</sub>  | 10  |     |     | ns   |
| DACDAT hold time from BCLK rising edge     | t <sub>DH</sub>   | 10  |     |     | ns   |
| DACDAT set-up time to BCLK rising edge     | t <sub>DS</sub>   | 10  |     |     | ns   |

**Note:**

BCLK period should always be greater than or equal to MCLK period.

**CONTROL INTERFACE TIMING – 2-WIRE MODE**

2-wire mode is selected by connecting the SWMODE pin high and connecting the SCIM\_CHANNEL pin low.



**Figure 4 Control Interface Timing – 2-Wire Serial Control Mode**

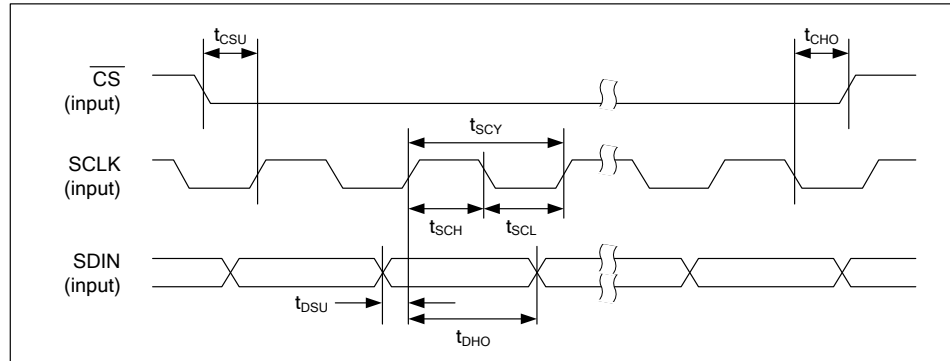
**Test Conditions**

DCVDD=DBVDD=1.8V, AVDD= 3.3V, SPKVDD=5V, DGND=AGND= SPKGND=0V,  $T_A=+25^{\circ}\text{C}$ , Slave Mode,  $f_s=48\text{kHz}$ , MCLK = 256fs, 24-bit data, unless otherwise stated.

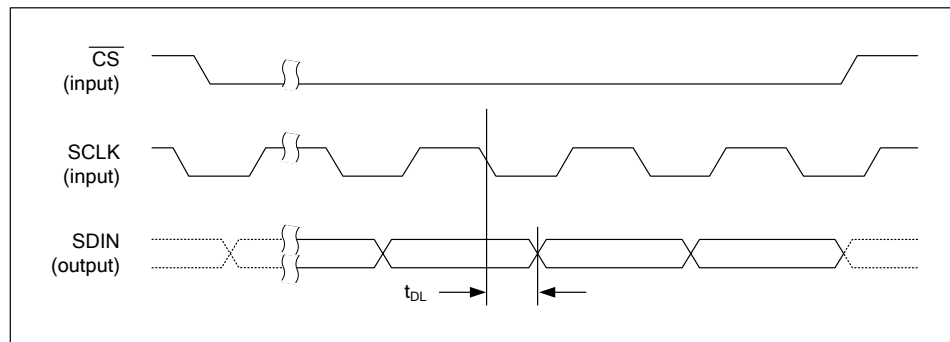
| PARAMETER                                     | SYMBOL   | MIN | TYP | MAX | UNIT |
|---|----------|-----|-----|-----|------|
| <b>Program Register Input Information</b>     |          |     |     |     |      |
| SCLK Frequency                                |          |     |     | 526 | kHz  |
| SCLK Low Pulse-Width                          | $t_1$    | 1.3 |     |     | us   |
| SCLK High Pulse-Width                         | $t_2$    | 600 |     |     | ns   |
| Hold Time (Start Condition)                   | $t_3$    | 600 |     |     | ns   |
| Setup Time (Start Condition)                  | $t_4$    | 600 |     |     | ns   |
| Data Setup Time                               | $t_5$    | 100 |     |     | ns   |
| SDIN, SCLK Rise Time                          | $t_6$    |     |     | 300 | ns   |
| SDIN, SCLK Fall Time                          | $t_7$    |     |     | 300 | ns   |
| Setup Time (Stop Condition)                   | $t_8$    | 600 |     |     | ns   |
| Data Hold Time                                | $t_9$    |     |     | 900 | ns   |
| Pulse width of spikes that will be suppressed | $t_{ps}$ | 0   |     | 5   | ns   |

**CONTROL INTERFACE TIMING – 3-WIRE MODE**

3-wire mode is selected by connecting the SWMODE pin high and connecting the SCIM\_CHANNEL pin high.



**Figure 5 Control Interface Timing – 3-Wire Serial Control Mode (Write Cycle)**



**Figure 6 Control Interface Timing – 3-Wire Serial Control Mode (Read Cycle)**

**Test Conditions**

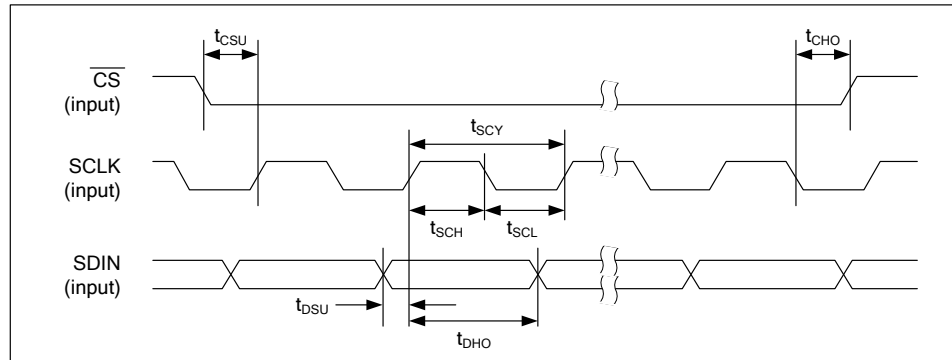
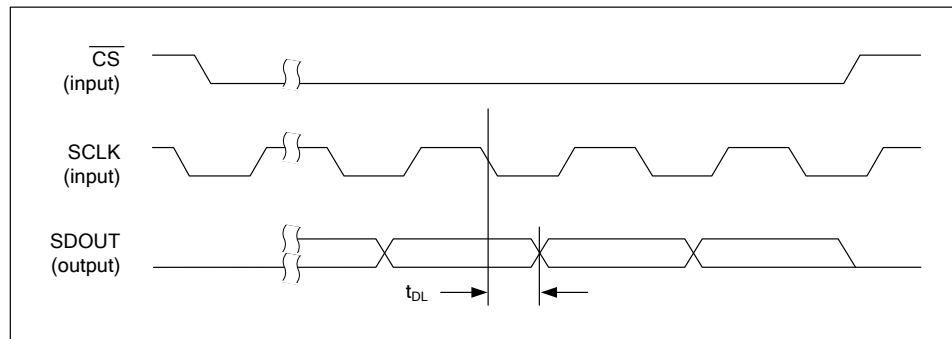
DCVDD=DBVDD=1.8V, AVDD= 3.3V, SPKVDD=5V, DGND=AGND=SPKGND=0V, T<sub>A</sub>=+25°C, Slave Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

| PARAMETER                                     | SYMBOL           | MIN | TYP | MAX | UNIT |
|---|------------------|-----|-----|-----|------|
| <b>Program Register Input Information</b>     |                  |     |     |     |      |
| CSB falling edge to SCLK rising edge          | t <sub>CSU</sub> | 40  |     |     | ns   |
| SCLK rising edge to CSB rising edge           | t <sub>CHO</sub> | 10  |     |     | ns   |
| SCLK pulse cycle time                         | t <sub>SCY</sub> | 160 |     |     | ns   |
| SCLK pulse width low                          | t <sub>SCL</sub> | 80  |     |     | ns   |
| SCLK pulse width high                         | t <sub>SCH</sub> | 80  |     |     | ns   |
| SDIN to SCLK set-up time                      | t <sub>DSU</sub> | 40  |     |     | ns   |
| SDIN to SCLK hold time                        | t <sub>DHO</sub> | 10  |     |     | ns   |
| Pulse width of spikes that will be suppressed | t <sub>ps</sub>  | 0   |     | 5   | ns   |
| SCLK falling edge to SDOOUT transition        | t <sub>DL</sub>  |     |     | 40  | ns   |



**CONTROL INTERFACE TIMING – 4-WIRE MODE**

4-wire mode supports readback via SDOUT.


**Figure 7 Control Interface Timing – 4-Wire Serial Control Mode (Write Cycle)**

**Figure 8 Control Interface Timing – 4-Wire Serial Control Mode (Read Cycle)**
**Test Conditions**

 DCVDD=DBVDD=1.8V, AVDD= 3.3V, SPKVDD=5V, DGND=AGND=SPKGND=0V, T<sub>A</sub>=+25°C, Slave Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

| PARAMETER                                     | SYMBOL           | MIN | TYP | MAX | UNIT |
|---|------------------|-----|-----|-----|------|
| <b>Program Register Input Information</b>     |                  |     |     |     |      |
| SCLK rising edge to CSB falling edge          | t <sub>CSU</sub> | 40  |     |     | ns   |
| SCLK rising edge to CSB rising edge           | t <sub>SHO</sub> | 40  |     |     | ns   |
| SCLK pulse cycle time                         | t <sub>SCY</sub> | 160 |     |     | ns   |
| SCLK pulse width low                          | t <sub>SCL</sub> | 80  |     |     | ns   |
| SCLK pulse width high                         | t <sub>SCH</sub> | 80  |     |     | ns   |
| SDIN to SCLK set-up time                      | t <sub>DSU</sub> | 40  |     |     | ns   |
| SDIN to SCLK hold time                        | t <sub>DHO</sub> | 10  |     |     | ns   |
| SDOUT propagation delay from SCLK rising edge | t <sub>DL</sub>  |     |     | 10  | ns   |
| Pulse width of spikes that will be suppressed | t <sub>ps</sub>  | 0   |     | 5   | ns   |
| SCLK falling edge to SDOUT transition         | t <sub>DL</sub>  |     |     | 40  | ns   |

## DEVICE DESCRIPTION

### INTRODUCTION

The WM9081 is designed to provide high quality, high power output to a loudspeaker at low distortion levels in space-constrained portable applications. The device is well-suited to both mono and multi-channel speaker systems.

Digital input enables the power drivers to be located close to the speakers in multi-channel systems without the need for troublesome long analogue connections. Location of the power drivers close to the speakers also removes the need for bulky and expensive class D filters and reduces PCB track lengths, minimising emissions.

The WM9081 supports both hardware and software control modes.

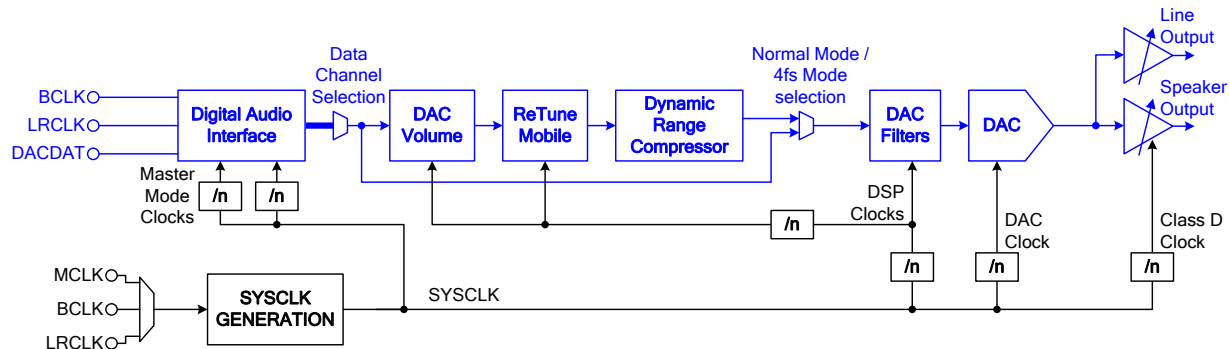
In Hardware control modes, the digital audio interface format is fixed and either the left or right channel can be routed to the Class D speaker driver. The WM9081 is a slave device only on the audio interface; EQ and Dynamic Range Control functions are not supported.

In Software control modes, the digital audio interface is highly programmable. Ready-programmed control sequences can be commanded to enable/disable the speaker driver or line output. Programmable EQ and Dynamic Range Control is supported in the digital domain. Analogue audio input paths can also be mixed into the speaker or line output drivers. The speaker driver can be configured to operate either in Class AB or in Class D mode.

ReTune™ Mobile parametric EQ with fully programmable coefficients is integrated for optimization of speaker characteristics. A simple set-up mode is also available.

A programmable dynamic range controller is also available for maximizing loudness whilst also protecting speakers from being overdriven, preventing battery droop, waveform clipping, thermal overloads and premature system shutdown.

Figure 9 shows the DAC signal path and clocking architecture of the WM9081.



**Figure 9 DAC Signal Path and Clocking Architecture**

Digital audio transmission within the system also reduces crosstalk between, for example, microphone input signals and speaker output signals, enhancing stability and reducing the risk of 'howling' during speakerphone operation where very high microphone gain is used.

Four control interface addresses and four stereo TDM slots are supported to allow multiple WM9081 devices to be configured and driven independently.

## CONTROL INTERFACE (SOFTWARE MODE)

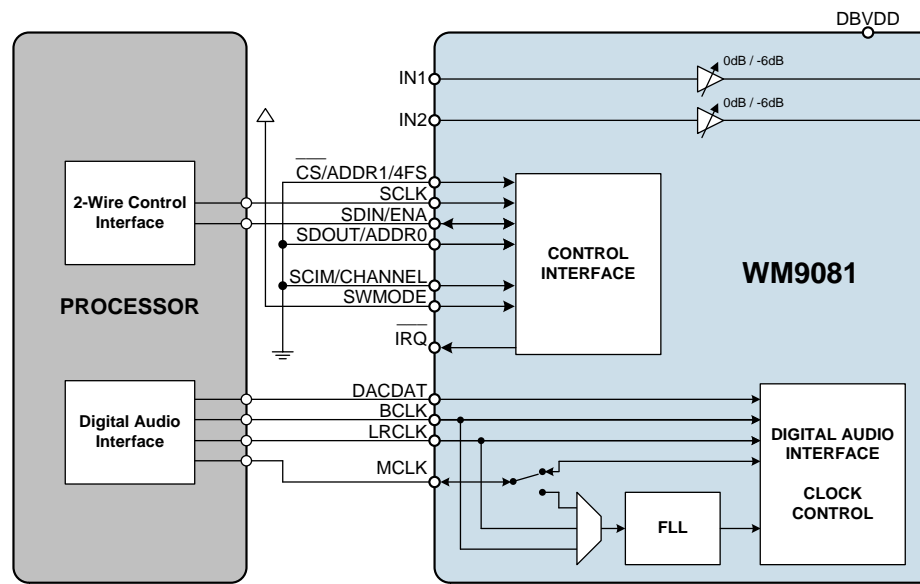
The WM9081 can be controlled in hardware mode or in software modes. In hardware mode, the device is configured according to logic levels applied to hardware pins. In software mode, the device is configured using control register writes via a serial control interface. See “Control Interface (Hardware Mode)” for details of hardware control mode.

Software Control Mode is selected by logic 1 on the SWMODE pin. The logic level is referenced to the DBVDD power domain. When Software Mode is selected, the associated multi-function control pins are defined as described in Table 1.

| PIN           | DESCRIPTION   |
|---------------|---|
| SCIM/CHANNEL  | Software Control Interface Mode<br>0 = 2-wire<br>1 = 3-/4-wire                                |
| SDIN/ENA      | Serial Data Input   |
| SCLK          | Serial Data Clock   |
| SDOUT/ADDR0   | 2 wire mode - Device Address[0]<br>3-wire mode - Not used<br>4-wire mode - Serial Data Output |
| CS /ADDR1/4FS | 2 wire mode - Device Address[1]<br>3-/4-wire mode - Chip Select                               |

**Table 1 Software Control Pin Configuration**

A typical system configuration for software control mode is illustrated in Figure 10.



**Figure 10 Software Control Mode Example – 2-Wire Control, Slave Mode, Device ID = D8h**

In Software Control Mode, the WM9081 is controlled by writing to its control registers. Readback is available for all registers, including device ID and power management status bits. The control interface can operate as a 2-, 3- or 4-wire control interface: Readback is provided on the bi-directional pin SDIN in 2-wire and 3-wire modes. The WM9081 Software Control interface is supplied by the DBVDD power domain.

The available Software Control interface modes are summarised as follows:

- 2-wire mode uses pins SCLK and SDIN.
- 3-wire mode uses pins CS, SCLK and SDIN.
- 4-wire mode uses pins CS, SCLK, SDIN and SDOUT.

2-wire mode is selected by setting the SCIM/CHANNEL pin to logic 0. When this pin is set to logic 1, then 3-wire or 4-wire mode is selected according to the SPI\_4WIRE register bit, as defined in Table 2.

In 4-wire mode, the electrical characteristics of the SDOUT pin are configurable using the SPI\_CFG register bit.

| ADDRESS                 | BIT | LABEL     | DEFAULT | DESCRIPTION   |
|-------------------------|-----|-----------|---------|---|
| R40 (28h)<br>MW Slave 1 | 5   | SPI_CFG   | 0       | Controls the SDOUT pin in 4 wire mode<br>0 = SDOUT output is CMOS<br>1 = SDOUT output is open drain           |
|                         | 4   | SPI_4WIRE | 0       | Selects 3-wire or 4-wire mode<br>0 = 3-wire mode using bi-directional SDIN pin<br>1 = 4-wire mode using SDOUT |

**Table 2 Software Control Mode Configuration**

## 2-WIRE CONTROL MODE

In 2-wire mode, the WM9081 is a slave device on the control interface; SCLK is a clock input, while SDIN is a bi-directional data pin. To allow arbitration of multiple slaves (and/or multiple masters) on the same interface, the WM9081 transmits logic 1 by tri-stating the SDIN pin, rather than pulling it high. An external pull-up resistor is required to pull the SDIN line high so that the logic 1 can be recognised by the master.

In order to allow many devices to share a single 2-wire control bus, every device on the bus has a unique 7-bit device ID (this is not the same as the 8-bit address of each register in the WM9081). The device ID is determined by the logic level on the ADDR0 and ADDR1 pins as shown in Table 3. The LSB of the device ID is the Read/Write bit; this bit is set to logic 1 for “Read” and logic 0 for “Write”.

| ADDR1 | ADDR0 | DEVICE ID       |
|-------|-------|-----------------|
| 0     | 0     | 1101 1000 (D8h) |
| 0     | 1     | 1101 1010 (DAh) |
| 1     | 0     | 1101 1100 (DCh) |
| 1     | 1     | 1101 1110 (DEh) |

**Table 3 Control Interface Device ID Selection**

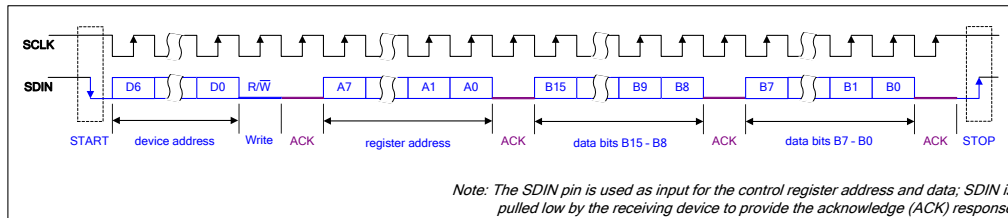
The WM9081 operates as a slave device only. The controller indicates the start of data transfer with a high to low transition on SDIN while SCLK remains high. This indicates that a device ID, register address and data will follow. All devices on the 2-wire bus respond to the start condition and shift in the next eight bits on SDIN (7-bit device ID + Read/Write bit, MSB first). If the device ID received matches the device ID of the WM9081, then the WM9081 responds by pulling SDIN low on the next clock pulse (ACK). If the device ID is not recognised or the R/W bit is ‘1’ when operating in write only mode, the WM9081 returns to the idle condition and waits for a new start condition and valid address.

If the device ID matches the device ID of the WM9081, the data transfer continues as described below. The controller indicates the end of data transfer with a low to high transition on SDIN while SCLK remains high. After receiving a complete address and data sequence the WM9081 returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e. SDIN changes while SCLK is high), the device returns to the idle condition.

The WM9081 supports the following read and write operations:

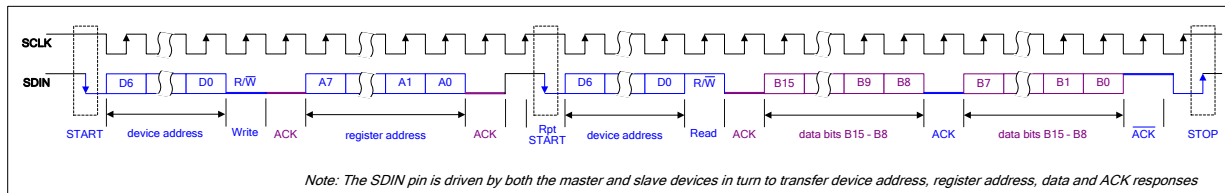
- Single write
- Single read
- Multiple write using auto-increment
- Multiple read using auto-increment

The sequence of signals associated with a single register write operation is illustrated in Figure 11.



**Figure 11 Control Interface 2-wire Register Write**

The sequence of signals associated with a single register read operation is illustrated in Figure 12.



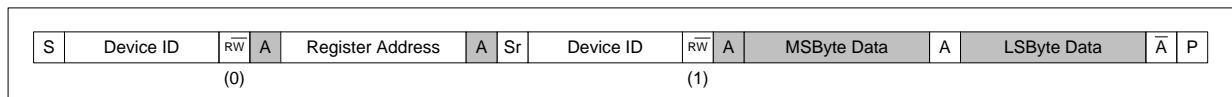
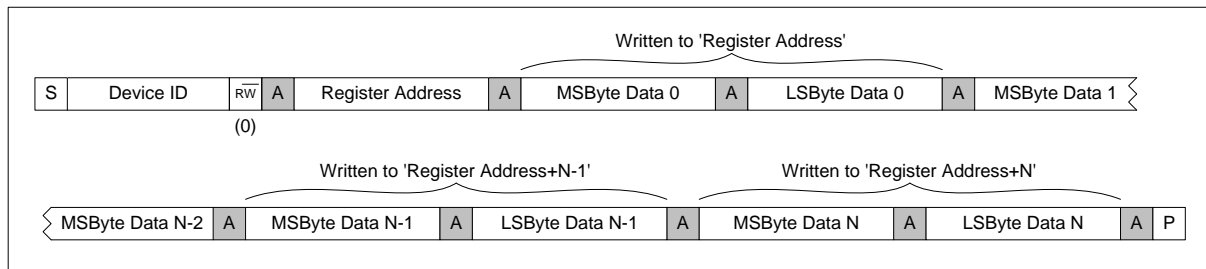
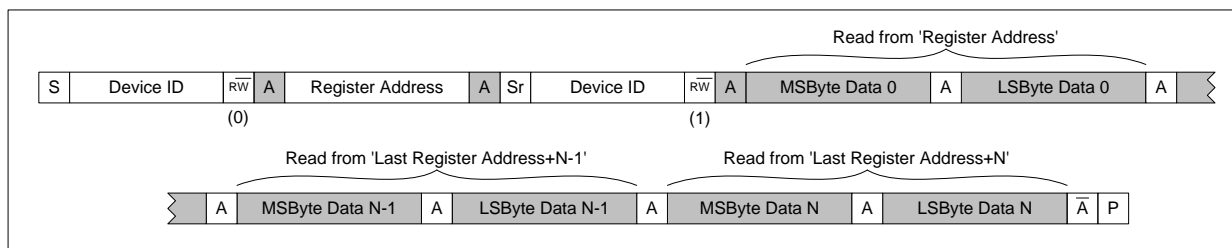
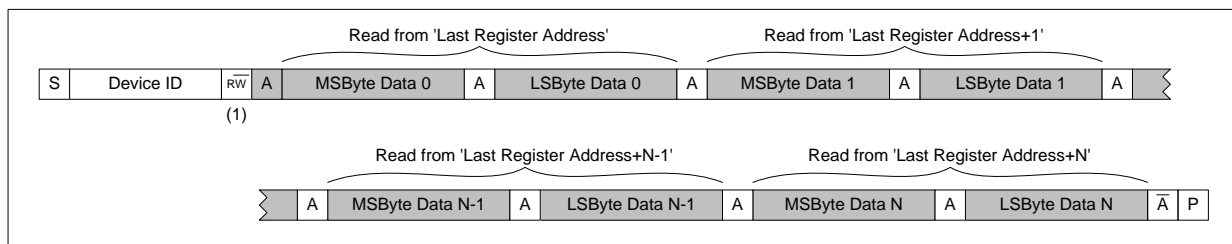
**Figure 12 Control Interface 2-wire Register Read**

The Control Interface also supports other register operations, as listed above. The interface protocol for these operations is summarised below. The terminology used in the following figures is detailed in Table 4.

Note that, for multiple write and multiple read operations, the auto-increment option must be enabled. This feature is enabled by default; it is described in Table 5 below.

| TERMINOLOGY   | DESCRIPTION                         |
|---------------|-------------------------------------|
| S             | Start Condition                     |
| Sr            | Repeated start                      |
| A             | Acknowledge                         |
| P             | Stop Condition                      |
| R/W           | 0 = Write<br>1 = Read               |
| [White field] | Data flow from bus master to WM9081 |
| [Grey field]  | Data flow from WM9081 to bus master |

**Table 4 Control Interface Terminology**


**Figure 13 Single Register Write to Specified Address**

**Figure 14 Single Register Read from Specified Address**

**Figure 15 Multiple Register Write to Specified Address using Auto-increment**

**Figure 16 Multiple Register Read from Specified Address using Auto-increment**

**Figure 17 Multiple Register Read from Last Address using Auto-increment**

Multiple Write and Multiple Read operations enable the host processor to access sequential blocks of the data in the WM9081 register map faster than is possible with single register operations. The auto-increment option is enabled when the AUTO\_INC register bit is set. This bit is defined in Table 5. Auto-increment is enabled by default.

SMBUS Alert Response Address protocol is supported by the WM9081 when the ARA\_ENA register bit is set. This function enables a bus controller to poll multiple devices on the I2C bus simultaneously in order to respond to Interrupt events efficiently. The WM9081 does not support automatic clearing of the SMBALERT# (implemented as IRQ on this device); a host device must service the alert and manually clear the IRQ status before proceeding to any other alerting devices in the system. The WM9081 device address used by this protocol is set as described in Table 5.

| ADDRESS              | BIT | LABEL    | DEFAULT | DESCRIPTION   |
|----------------------|-----|----------|---------|---|
| R40 (28h) MW Slave 1 | 3   | ARA_ENA  | 0       | Alert Response Address protocol enable<br>0 = Disabled<br>1 = Enabled |
|                      | 1   | AUTO_INC | 1       | Enable Auto-Increment function<br>0 = Disabled<br>1 = Enabled         |

**Table 5 Auto-Increment and Alert Response Address Control**

### 3-WIRE CONTROL MODE

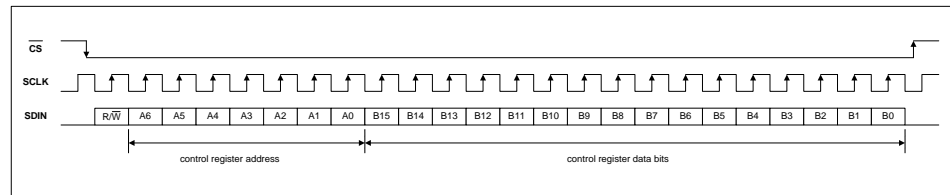
The WM9081 is controlled by writing to registers through a 3-wire serial control interface. A control word consists of 24 bits. The first bit is the read/write bit (R/W), which is followed by 7 address bits (A6 to A0) that determine which control register is accessed. The remaining 16 bits (B15 to B0) are data bits, corresponding to the 16 bits in each control register.

In 3-wire mode, every rising edge of SCLK clocks in one data bit from the SDIN pin. A rising edge on CS latches in a complete control word consisting of the last 24 bits.

In Write operations (R/W=0), all SDIN bits are driven by the controlling device.

In Read operations (R/W=1), the SDIN pin is driven by the controlling device to clock in the register address, after which the WM9081 drives the SDIN pin to output the applicable data bits.

The 3-wire control mode timing is illustrated in Figure 18.



**Figure 18 3-Wire Serial Control Interface**

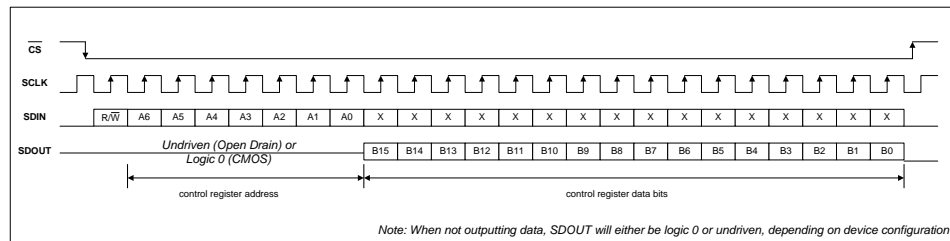
### 4-WIRE CONTROL MODE

In Write operations, this mode is the same as 3-wire Control Mode.

In Read operations, the SDIN pin is ignored following receipt of the valid register address. The data bits are output by the WM9081 on the SDOUT pin.

The SDOUT pin can be configured as CMOS or Open Drain, as described in Table 2. In CMOS mode, SDOUT is driven low when not outputting register data bits. In Open Drain mode, SDOUT is undriven when not outputting register data bits.

The 4-wire control mode timing is illustrated in Figure 19.


**Figure 19 4-Wire Serial Control Interface**

## CONTROL INTERFACE (HARDWARE MODE)

The WM9081 can be controlled in hardware mode or in software modes. In hardware mode, the device is configured according to logic levels applied to hardware pins. In software mode, the device is configured using control register writes via a serial control interface. See “Control Interface (Software Mode)” for details of software control mode.

Hardware Control Mode selected by logic 0 on the SWMODE pin. The logic level is referenced to the DBVDD power domain. When Hardware Mode is selected, the associated multi-function control pins are defined as described in Table 7.

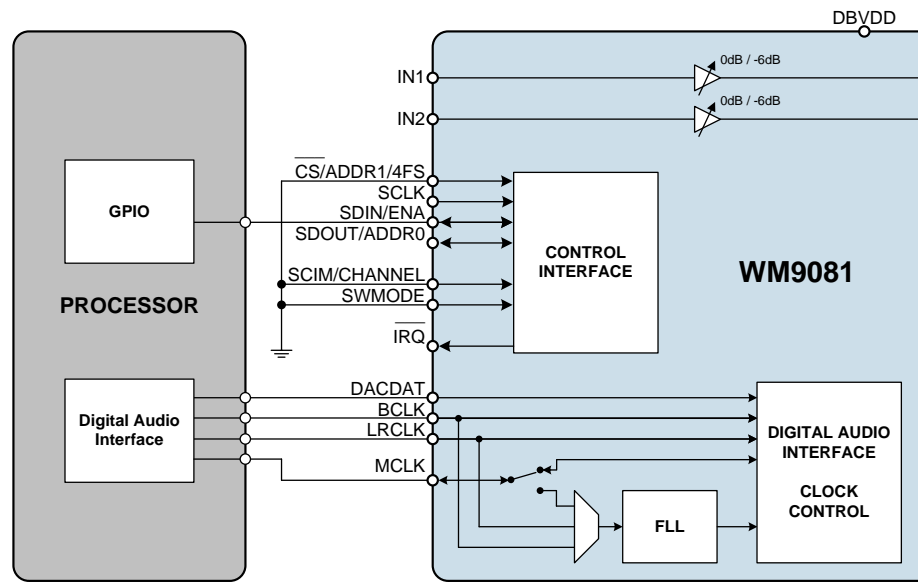
Note that two variants of Hardware Control Mode are supported; these are selected according to the logic level on the CS/ADDR1/4FS pin, as described in Table 7. In Normal mode, the WM9081 is clocked via a 12.288MHz input to the MCLK pin. In 4FS mode, the WM9081 is clocked via the BCLK pin. The selected channel of the received audio signal is routed to the Class D speaker output.

| PIN           | DESCRIPTION  |
|---------------|--|
| SCIM/CHANNEL  | Left/Right Channel select<br>0 = Left channel<br>1 = Right channel |
| SDIN/ENA      | Device Enable (Normal mode)<br>0 = Disabled<br>1 = Enabled         |
| SCLK          | Not used   |
| SDOUT/ADDR0   | Not used   |
| CS /ADDR1/4FS | 4FS Mode select<br>0 = Normal<br>1 = 4FS Mode enabled              |

**Table 6 Hardware Control Pin Configuration**

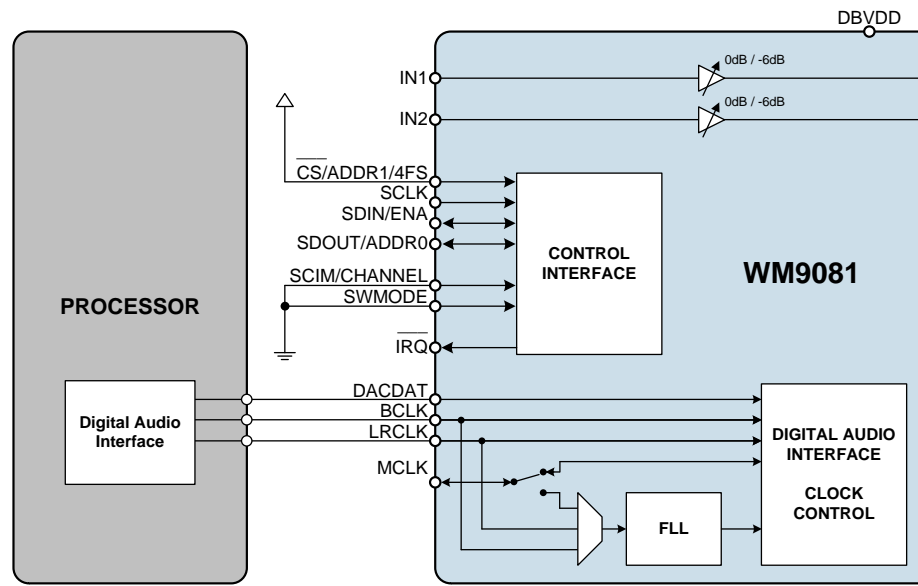
A typical system configuration using hardware (normal) control is illustrated in Figure 20.





**Figure 20 Hardware Control Mode Example – Normal Mode, Left Channel**

A typical system configuration using 4FS mode is illustrated in Figure 21.



**Figure 21 Hardware Control Mode Example – 4FS Mode, Left Channel**

## DEVICE ENABLE

The WM9081 is enabled by logic 1 on the SDIN/ENA pin. The logic level is referenced to the DBVDD power domain.

Note that in 4FS mode (see below), the WM9081 starts up and shuts down automatically according to the BCLK signal. In 4FS mode, the SDIN/ENA pin is ignored and may be set to either Logic 0 or Logic 1.

## LEFT/RIGHT CHANNEL SELECT

The Left/Right channel selection is controlled using the SCIM/CHANNEL pin. The logic level is referenced to the DBVDD power domain. Logic 0 selects Left channel. Logic 1 selects Right channel.

The selected channel from the Digital Audio Interface will be applied to the Class D speaker output. It is recommended that the logic level on the SCIM/CHANNEL pin is not changed while the audio path of the WM9081 is enabled.

## 4FS MODE SELECT

The WM9081 supports two variants of Hardware Control mode. Normal mode is selected by a logic 0 on the CS/ADDR1/4FS pin. 4FS mode is selected by a logic 1 on the CS/ADDR1/4FS pin. The logic level is referenced to the DBVDD power domain. It is recommended that the logic level on the CS/ADDR1/4FS pin is not changed while the audio path of the WM9081 is enabled.

In Normal mode, the WM9081 is clocked via a 12.288MHz input to the MCLK pin. The digital audio interface is configured in 16-bit I<sup>2</sup>S format. The sample rate of the digital audio input must be 48kHz.

In 4FS mode, the WM9081 is clocked via the BCLK pin of the digital audio interface. The digital audio interface is configured in 16-bit I<sup>2</sup>S format. The sample rate of the digital audio input must be 4 x FS, where FS is the normal sample rate of 48kHz. It follows that the BCLK frequency is 6.144MHz. The integrated Frequency Locked Loop (FLL) is used to generate all the necessary internal clocks to operate the device from the BCLK input only.

In 4FS mode, the SDIN/ENA pin is not used as the Device Enable input. Instead, the WM9081 monitors the BCLK input and automatically powers up when BCLK is present and shuts down when BCLK is not present. This enables the WM9081 to operate autonomously with the minimum number of control signals.

## HARDWARE CONTROL MODES SUMMARY

The WM9081 Hardware Control Modes are summarised in Table 7.

See “Digital Audio Interface” for more details of the I<sup>2</sup>S audio interface protocol.

| CONFIGURATION                  | NORMAL MODE                   | 4FS MODE                 |
|--------------------------------|-------------------------------|--------------------------|
| Audio interface data format    | Stereo I <sup>2</sup> S       | Stereo I <sup>2</sup> S  |
| Word length                    | 16                            | 16                       |
| Data channel select            | Selected by SCIM/CHANNEL      | Selected by SCIM/CHANNEL |
| Master/Slave mode              | Slave                         | Slave                    |
| TDM enabled                    | No                            | No                       |
| Clock input source             | MCLK                          | BCLK                     |
| BCLK frequency                 | $\geq 32 \times \text{LRCLK}$ | $32 \times \text{LRCLK}$ |
| Automatic power-up / shut-down | Yes                           | Yes                      |

**Table 7 Hardware Control Modes Summary**

### Notes

1. MCLK must continue to run for 50ms after SDA/ENA is asserted low in order to shutdown the device.

## CONTROL WRITE SEQUENCER

The Control Write Sequencer forms part of the WM9081 control interface logic. It provides the ability to perform a sequence of register write operations with the minimum of demands on the host processor - the sequence may be initiated by a single operation from the host processor and then left to execute independently.

Default sequences for controlling the Speaker and Lineout signal paths are provided (see “Default Sequences” section).

When a sequence is initiated, the sequencer performs a series of pre-defined register writes. The host processor informs the sequencer of the start index of the required sequence within the sequencer’s memory. At each step of the sequence, the contents of the selected register fields are read from the sequencer’s memory and copied into the WM9081 control registers. This continues sequentially through the sequencer’s memory until an “End of Sequence” bit is encountered; at this point, the sequencer stops and an Interrupt status flag is asserted. For cases where the timing of the write sequence is important, the sequencer is programmed with time delays for specific steps within the sequence.

Note that the Control Write Sequencer’s internal clock is derived from the internal clock CLK\_SYS which must be enabled by setting CLK\_SYS\_ENA (see “Clocking and Sample Rates”). The clock division from CLK\_SYS is handled transparently by the WM9081 without user intervention, provided that the CLK\_SYS and sample rate control fields are set correctly.

### INITIATING A SEQUENCE

The Register fields associated with running the Control Write Sequencer are described in Table 8. Note that the operation of the Control Write Sequencer also requires the internal clock CLK\_SYS to be enabled via the CLK\_SYS\_ENA (see “Clocking and Sample Rates”).

The Write Sequencer is enabled by setting the WSEQ\_ENA bit. The start index of the required sequence must be written to the WSEQ\_START\_INDEX field. Setting the WSEQ\_START bit initiates the sequencer at the given start index.

The Write Sequencer can be interrupted by writing a logic 1 to the WSEQ\_ABORT bit.

The current status of the Write Sequencer can be read using two further register fields - when the WSEQ\_BUSY bit is asserted, this indicates that the Write Sequencer is busy. Note that, whilst the Control Write Sequencer is running a sequence (indicated by the WSEQ\_BUSY bit), normal read/write operations to the Control Registers cannot be supported. The index of the current step in the Write Sequencer can be read from the WSEQ\_CURRENT\_INDEX field; this is an indicator of the sequencer’s progress. On completion of a sequence, this field holds the index of the last step within the last commanded sequence.

When the Write Sequencer reaches the end of a sequence, it asserts the WSEQ\_BUSY\_EINT flag in Register R26 (1Ah). (Note that the WSEQ\_BUSY\_EINT flag is asserted to indicate that the WSEQ is NOT busy.) This flag can be used to generate an Interrupt Event on completion of the sequence; this is indicated via the IRQ pin. See “Interrupts” for details of hardware output of the Write Sequencer status via the IRQ pin.

| REGISTER ADDRESS               | BIT | LABEL      | DEFAULT | DESCRIPTION   |
|--------------------------------|-----|------------|---------|---|
| R38 (26h)<br>Write Sequencer 0 | 15  | WSEQ_ENA   | 0       | Write Sequencer Enable.<br>0 = Disabled<br>1 = Enabled  |
|                                | 9   | WSEQ_ABORT | 0       | Writing a 1 to this bit aborts the current sequence and returns control of the device back to the serial control interface. |

| REGISTER ADDRESS               | BIT  | LABEL                                   | DEFAULT  | DESCRIPTION  |
|--------------------------------|------|---|----------|--|
|                                | 8    | WSEQ_START                              | 0        | Writing a 1 to this bit starts the write sequencer at the memory location indicated by the WSEQ_START_INDEX field. The sequence continues until it reaches an "End of sequence" flag. At the end of the sequence, this bit will be reset by the Write Sequencer. |
|                                | 6:0  | WSEQ_START_INDEX [6:0]                  | 000_0000 | Sequence Start Index. This is the memory location of the first command in the selected sequence.   |
| R39 (27h)<br>Write Sequencer 1 | 10:4 | WSEQ_CURRENT_INDEX [6:0]<br>(read only) | 000_0000 | Sequence Current Index. This is the location of the most recently accessed command in the write sequencer memory.  |
|                                | 0    | WSEQ_BUSY<br>(read only)                | 0        | Sequencer Busy flag (Read Only).<br>0 = Sequencer idle<br>1 = Sequencer busy<br>Note: it is not possible to write to control registers via the control interface while the Sequencer is Busy.  |

**Table 8 Write Sequencer Control**

## DEFAULT SEQUENCES

When the WM9081 is powered up, a number of default Control Write Sequences are available in non-volatile memory. The pre-programmed default settings include Start-Up and Shut-Down sequences for each of the output drivers. Note that the internal clock, CLK\_SYS, must be enabled in order to run these sequences.

The following default control sequences are provided:

### 1. Class D Speaker Enable Sequence

Class D Speaker Enable - This sequence powers up the speaker driver in Class D mode, and enables the DAC signal path. The soft-start VMID circuit is selected as part of this sequence. On completion, the Lineout is clamped to VMID.

The Class D Speaker Enable sequence is initiated by writing 8100h to Register 38 (26h). This single operation starts the Control Write Sequencer at Index Address 0 (00h). For typical clocking configurations, this sequence takes approximately 42ms to run.

Note that this sequence is optimized for pop suppression on the Speaker output. For pop suppression on the Line Output, please refer to sequence 3.

### 2. Class D Speaker Disable Sequence

Class D Speaker Disable - This sequence powers down the Class D speaker driver. As part of this sequence, the DAC is muted and disabled, the Lineout is discharged to AGND and the reference/bias circuits are disabled. This sequence is applicable to the Class D speaker mode.

The Class D Speaker Disable sequence is initiated by writing 8115h to Register 38 (26h). This single operation starts the Control Write Sequencer at Index Address 21 (15h). For typical clocking configurations, this sequence takes approximately 48ms to run.

### **3. Lineout Enable Sequence**

Lineout Enable - This sequence powers up the lineout, and enables the DAC signal path. The lineout is discharged initially, and the soft-start VMID circuit is used to suppress pops during power-up.

The Lineout Enable sequence is initiated by writing 812Ah to Register 38 (26h). This single operation starts the Control Write Sequencer at Index Address 42 (2Ah). For typical clocking configurations, this sequence takes approximately 550ms to run.

### **4. Lineout Disable Sequence**

Lineout Disable - This sequence powers down the lineout. As part of this sequence, the DAC is muted and disabled, the Lineout is discharged to AGND and the reference/bias circuits are disabled.

The Lineout disable sequence is initiated by writing 813Fh to Register 38 (26h). This single operation starts the Control Write Sequencer at Index Address 63 (3Fh). For typical clocking configurations, this sequence takes approximately 646ms to run.

### **5. Class AB Speaker Enable Sequence**

Class AB Speaker Enable - This sequence powers up the speaker driver in Class AB mode, and enables the DAC signal path. The soft-start VMID circuit is selected as part of this sequence. On completion, the Lineout is clamped to VMID.

The Class AB Speaker Enable sequence is initiated by writing 8154h to Register 38 (26h). This single operation starts the Control Write Sequencer at Index Address 84 (54h). For typical clocking configurations, this sequence takes approximately 42ms to run.

Note that this sequence is optimized for pop suppression on the Speaker output. For pop suppression on the Line Output, please refer to sequence 3.

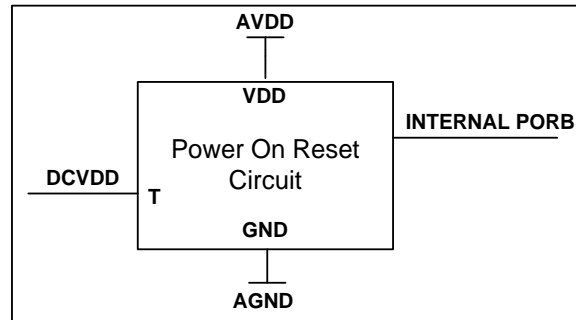
### **6. Class AB Speaker Disable Sequence**

Class AB Speaker Disable - This sequence powers down the Class AB speaker driver. As part of this sequence, the DAC is muted and disabled, the Lineout is discharged to AGND and the reference/bias circuits are disabled.

The Class AB Speaker Disable sequence is initiated by writing 8169h to Register 38 (26h). This single operation starts the Control Write Sequencer at Index Address 105 (69h). For typical clocking configurations, this sequence takes approximately 49ms to run.

### **Notes**

1. For details on the Control Write Sequencer default sequences, refer to the application note WAN\_0204 'WM9081 Control Write Sequencer default sequences'.

**POWER ON RESET CIRCUIT**

**Figure 22 Internal Power on Reset Circuit Schematic**

The WM9081 includes an internal CODEC Power-On-Reset Circuit, as shown in Figure 22, which is used to reset the CODEC digital logic into a default state after power up. The CODEC POR circuit is powered from AVDD and monitors DCVDD. It asserts PORB low if AVDD or DCVDD is below a minimum threshold.

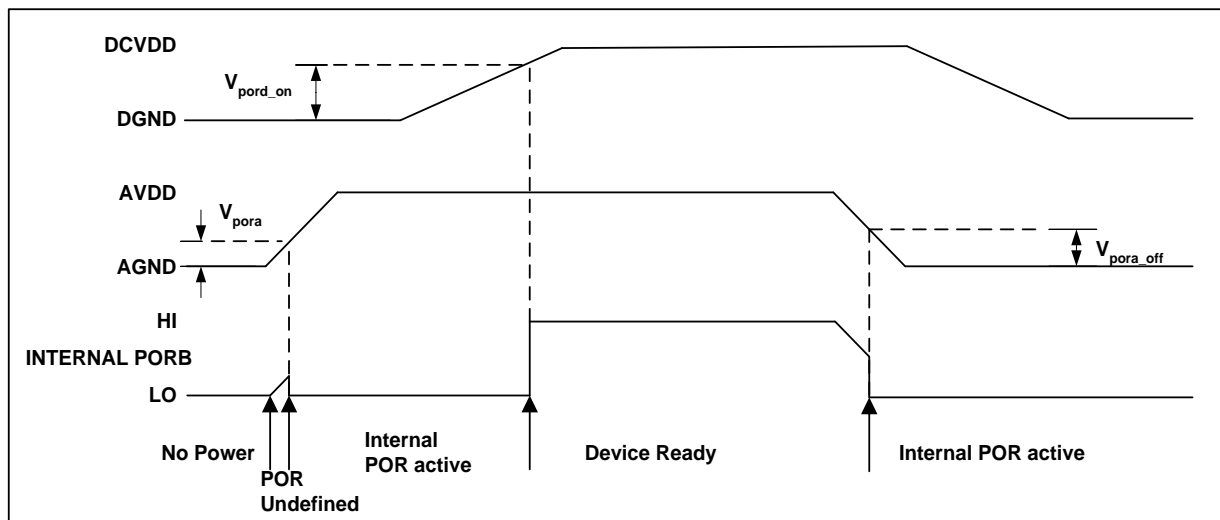
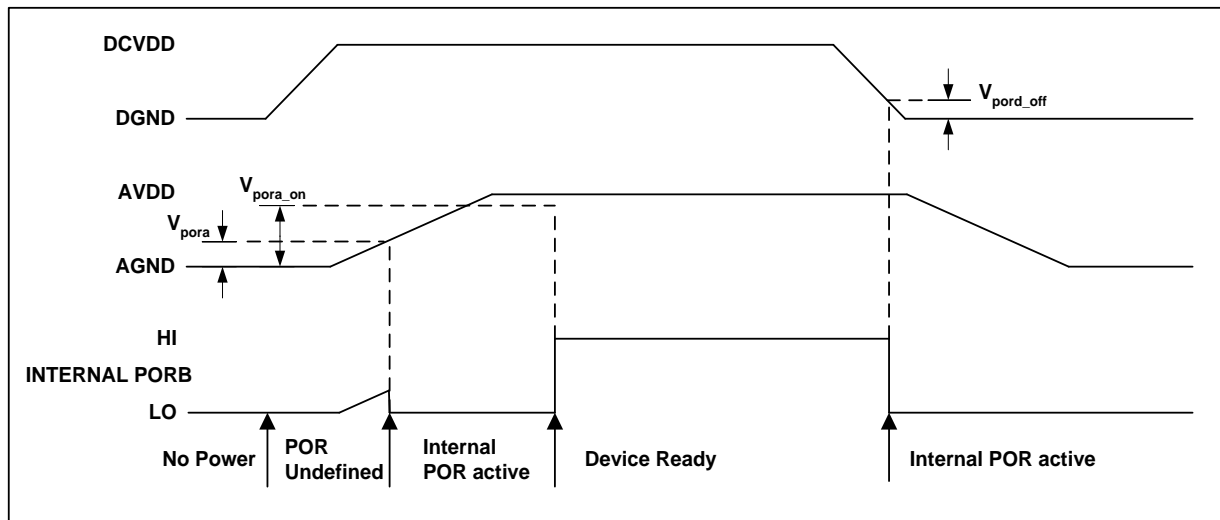

**Figure 23 Typical CODEC Power up Sequence where AVDD is Powered before DCVDD**

Figure 23 shows a typical power-up sequence where AVDD comes up first. When AVDD goes above the minimum threshold,  $V_{pora}$ , there is enough voltage for the circuit to guarantee PORB is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. After AVDD has reached its full supply level, DCVDD rises to  $V_{pord\_on}$  and PORB is released high and all registers are in their default state and writes to the control interface may take place.

On power down, where AVDD falls first, PORB is asserted low whenever AVDD drops below the minimum threshold  $V_{pora\_off}$ .



**Figure 24 Typical Power up Sequence where DCVDD is Powered before AVDD**

Figure 24 shows a typical power-up sequence where DCVDD comes up first. First it is assumed that DCVDD is already up to specified operating voltage. When AVDD goes above the minimum threshold,  $V_{pora}$ , there is enough voltage for the circuit to guarantee PORB is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. When AVDD rises to  $V_{pora\_on}$ , PORB is released high and all registers are in their default state and writes to the control interface may take place.

On power down, where DCVDD falls first, PORB is asserted low whenever DCVDD drops below the minimum threshold  $V_{pord\_off}$ .

| SYMBOL          | MIN | TYP  | MAX | UNIT |
|-----------------|-----|------|-----|------|
| $V_{pora}$      |     | 0.6  |     | V    |
| $V_{pora\_on}$  |     | 1.46 |     | V    |
| $V_{pora\_off}$ |     | 1.44 |     | V    |
| $V_{pord\_on}$  |     | 0.91 |     | V    |
| $V_{pord\_off}$ |     | 0.90 |     | V    |

**Table 9 Typical POR Operation at typical supply voltages**

#### Notes

1. If AVDD and DCVDD suffer a brown-out (i.e. drop below the minimum recommended operating level but do not go below  $V_{pora\_off}$  or  $V_{pord\_off}$ ) then the chip will not reset and will resume normal operation when the voltage is back to the recommended level again.
2. The chip will enter reset at power down when AVDD or DCVDD falls below  $V_{pora\_off}$  or  $V_{pord\_off}$ . This may be important if the supply is turned on and off frequently by a power management system.
3. The minimum  $t_{por}$  period is maintained even if DCVDD and AVDD have zero rise time. This specification is guaranteed by design rather than test.
4.  $V_{pora}$  is a simulated value

## DYNAMIC RANGE CONTROLLER (DRC)

The dynamic range controller (DRC) is a circuit which can be enabled in the digital data path of the WM9081. The function of the DRC is to adjust the signal gain in conditions where the input amplitude is unknown or varies over a wide range. The DRC can apply Compression and Automatic Level Control to the signal path. It incorporates 'anti-clip' and 'quick release' features for handling transients in order to improve intelligibility in the presence of loud impulsive noises.

Using the DRC to normalise the audio signal level can also provide protection from excessive output power conditions, which can lead to battery droop, increased heat dissipation and over-temperature system shutdown.

The DRC is enabled as shown in Table 10. Note that the DRC is not available in hardware control mode.

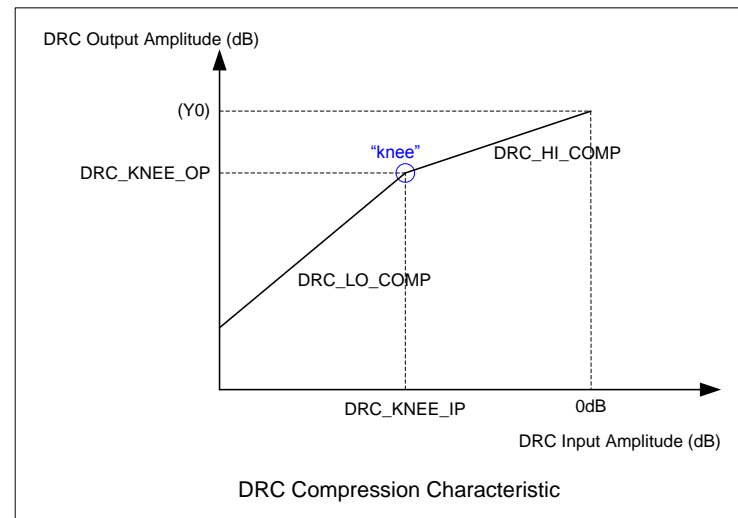
| REGISTER ADDRESS   | BIT | LABEL   | DEFAULT | DESCRIPTION                               |
|--------------------|-----|---------|---------|---|
| R32 (20h)<br>DRC 1 | 15  | DRC_ENA | 0       | DRC enable<br>0 = Disabled<br>1 = Enabled |

**Table 10 DRC Enable**

### COMPRESSION/LIMITING CAPABILITIES

The DRC supports two different compression regions, separated by a 'knee' at a specific input amplitude. In the region above the knee, the compression slope DRC\_HI\_COMP applies; in the region below the knee, the compression slope DRC\_LO\_COMP applies.

The overall DRC compression characteristic in 'steady state' (i.e. where the input amplitude is near-constant) is illustrated in Figure 25.



**Figure 25 DRC Compression Characteristic**

The slope of the DRC response is determined by register fields DRC\_HI\_COMP and DRC\_LO\_COMP. A slope of 1 indicates constant gain in this region. A slope less than 1 represents compression (i.e. a change in input amplitude produces only a smaller change in output amplitude). A slope of 0 indicates that the target output amplitude is the same across a range of input amplitudes; this is infinite compression.

The DRC Compression parameters are listed in Table 11.



| PARAMETER   | DESCRIPTION                   |
|-------------|-------------------------------|
| DRC_KNEE_IP | Input level at the knee (dB)  |
| DRC_KNEE_OP | Output level at the knee (dB) |
| DRC_HI_COMP | Compression ratio above knee  |
| DRC_LO_COMP | Compression ratio below knee  |

**Table 11 DRC Compression Parameters**

The knee Figure 25 is defined by register fields DRC\_KNEE\_IP and DRC\_KNEE\_OP respectively.

Parameter Y0, the output level for a 0dB input, is not specified directly, but can be calculated from the other parameters, using the equation:

$$Y0 = DRC\_KNEE\_OP - (DRC\_KNEE\_IP * DRC\_HI\_COMP)$$

The registers which control the DRC Compression parameters are shown in Table 12.

| REGISTER ADDRESS   | BIT  | LABEL                | DEFAULT | DESCRIPTION  |
|--------------------|------|----------------------|---------|--|
| R34 (22h)<br>DRC 3 | 5:3  | DRC_HI_COMP<br>[2:0] | 000     | Compressor slope (upper region)<br>000 = 1 (no compression)<br>001 = 1/2<br>010 = 1/4<br>011 = 1/8<br>100 = 1/16<br>101 = 0<br>110 = Reserved<br>111 = Reserved                            |
|                    | 2:0  | DRC_LO_COMP<br>[2:0] | 000     | Compressor slope (lower region)<br>000 = 1 (no compression)<br>001 = 1/2<br>010 = 1/4<br>011 = 1/8<br>100 = 0<br>101 = Reserved<br>11X = Reserved  |
| R35 (23h)<br>DRC 4 | 10:5 | DRC_KNEE_IP<br>[5:0] | 00_0000 | Input signal level at the Compressor 'knee'.<br><br>000000 = 0dB<br>000001 = -0.75dB<br>000010 = -1.5dB<br>... (-0.75dB steps)<br>111100 = -45dB<br>111101 = Reserved<br>11111X = Reserved |
|                    | 4:0  | DRC_KNEE_OP<br>[4:0] | 0_0000  | Output signal at the Compressor 'knee'.<br><br>00000 = 0dB<br>00001 = -0.75dB<br>00010 = -1.5dB<br>... (-0.75dB steps)<br>11110 = -22.5dB<br>11111 = Reserved                              |

**Table 12 DRC Compression Control**

**GAIN LIMITS**

The minimum and maximum gain applied by the DRC is set by register fields DRC\_MINGAIN and DRC\_MAXGAIN. These limits can be used to alter the DRC response from that illustrated in Table 13. If the range between maximum and minimum gain is reduced, then the extent of the dynamic range control is reduced. The maximum gain prevents quiet signals (or silence) from being excessively amplified.

| REGISTER ADDRESS   | BIT | LABEL            | DEFAULT | DESCRIPTION  |
|--------------------|-----|------------------|---------|--|
| R33 (21h)<br>DRC 2 | 3:2 | DRC_MINGAIN[1:0] | 00      | Minimum gain the DRC can use to attenuate audio signals<br>00 = 0dB (default)<br>01 = -6dB<br>10 = -12dB<br>11 = -18dB |
|                    | 1:0 | DRC_MAXGAIN[1:0] | 00      | Maximum gain the DRC can use to boost audio signals<br>00 = 12dB<br>01 = 18dB (default)<br>10 = 24dB<br>11 = 36dB      |

**Table 13 DRC Gain Limits**
**DYNAMIC CHARACTERISTICS**

The dynamic behaviour determines how quickly the DRC responds to changing signal levels. Note that the DRC responds to the average (RMS) signal amplitude over a period of time.

The DRC\_ATK register determines how quickly the DRC gain decreases when the signal amplitude is high. The DRC\_DCY register determines how quickly the DRC gain increases when the signal amplitude is low.

These register fields are described in Table 14. Note that the register defaults are suitable for general purpose use.

| REGISTER ADDRESS   | BIT   | LABEL        | DEFAULT | DESCRIPTION  |
|--------------------|-------|--------------|---------|--|
| R33 (21h)<br>DRC 2 | 15:12 | DRC_ATK[3:0] | 0000    | Gain attack rate (seconds/6dB)<br>0000 = Reserved (181us)<br>0001 = 181us<br>0010 = 363us<br>0011 = 726us<br>0100 = 1.45ms (default)<br>0101 = 2.9ms<br>0110 = 5.8ms<br>0111 = 11.6ms<br>1000 = 23.2ms<br>1001 = 46.4ms<br>1010 = 92.8ms<br>1011 = 185.6ms<br>1100-1111 = Reserved |

| REGISTER ADDRESS | BIT  | LABEL        | DEFAULT | DESCRIPTION  |
|------------------|------|--------------|---------|--|
|                  | 11:8 | DRC_DCY[3:0] | 0000    | Gain decay rate (seconds/6dB)<br>0000 = 186ms<br>0001 = 372ms<br>0010 = 743ms (default)<br>0011 = 1.49s<br>0100 = 2.97s<br>0101 = 5.94s<br>0110 = 11.89s<br>0111 = 23.78s<br>1000 = 47.56s<br>1001-1111 = Reserved |

**Table 14 DRC Time Constants**

### ANTI-CLIP CONTROL

The DRC includes an Anti-Clip feature to avoid signal clipping when the input amplitude rises very quickly. This feature uses a feed-forward technique for early detection of a rising signal level. Signal clipping is avoided by dynamically increasing the gain attack rate when required. The Anti-Clip feature is enabled using the DRC\_ANTICLIP bit.

Note that the feed-forward processing increases the latency in the input signal path. For low-latency applications (e.g. telephony), it may be desirable to reduce the delay, although this will also reduce the effectiveness of the anti-clip feature. The latency is determined by the DRC\_FF\_DLY bit. If necessary, the latency can be minimised by disabling the anti-clip feature altogether.

The DRC Anti-Clip control bits are described in Table 15.

| REGISTER ADDRESS   | BIT | LABEL        | DEFAULT | DESCRIPTION  |
|--------------------|-----|--------------|---------|--|
| R32 (20h)<br>DRC 1 | 5   | DRC_FF_DLY   | 1       | Feed-forward delay for anti-clip feature<br>0 = 5 samples<br>1 = 9 samples<br>Time delay can be calculated as $5/f_s$ or $9/f_s$ , where $f_s$ is the sample rate. |
|                    | 1   | DRC_ANTICLIP | 1       | Anti-clip enable<br>0 = Disabled<br>1 = Enabled  |

**Table 15 DRC Anti-Clip Control**

Note that the Anti-Clip feature operates entirely in the digital domain, i.e. on the input path to the DAC. It cannot be used to prevent signal clipping in the analogue domain (e.g. in the output PGA), nor in the source signal. Analogue clipping can only be prevented by reducing the analogue signal gain or by adjusting the source signal.

### QUICK RELEASE CONTROL

The DRC includes a Quick-Release feature to handle short transient peaks that are not related to the intended source signal. The Quick Release feature ensures that these transients do not cause the intended signal to be masked by the longer time constants of DRC\_DCY.

The Quick-Release feature is enabled by setting the DRC\_QR bit. When this bit is enabled, the DRC measures the crest factor (peak to RMS ratio) of the input signal. A high crest factor is indicative of a transient peak that may not be related to the intended source signal. If the crest factor exceeds the level set by DRC\_QR\_THR, then the normal decay rate (DRC\_DCY) is ignored and a faster decay rate (DRC\_QR\_DCY) is used instead.

The DRC Quick-Release control bits are described in Table 16.

| REGISTER ADDRESS   | BIT | LABEL            | DEFAULT | DESCRIPTION  |
|--------------------|-----|------------------|---------|--|
| R32 (20h)<br>DRC 1 | 2   | DRC_QR           | 1       | Quick release enable<br>0 = Disabled<br>1 = Enabled  |
| R33 (21h)<br>DRC 2 | 7:6 | DRC_QR_THR [1:0] | 00      | Quick release crest factor threshold<br>00 = 12dB (default)<br>01 = 18dB<br>10 = 24dB<br>11 = 30dB             |
|                    | 5:4 | DRC_QR_DCY [1:0] | 00      | Quick release decay rate (seconds/6dB)<br>00 = 0.725ms (default)<br>01 = 1.45ms<br>10 = 5.8ms<br>11 = Reserved |

**Table 16 DRC Quick-Release Control**

### INITIALISATION

When the DRC is initialised, the gain is set to the level determined by the DRC\_STARTUP\_GAIN register field. The default setting is 0dB, but values from -3dB to +6dB are available, as described in Table 17.

| REGISTER ADDRESS   | BIT  | LABEL                  | DEFAULT | DESCRIPTION   |
|--------------------|------|------------------------|---------|---|
| R32 (20h)<br>DRC 1 | 10:6 | DRC_STARTUP_GAIN [4:0] | 0_0110  | Initial gain at DRC startup<br>00000 = -3dB<br>00001 = -2.5dB<br>00010 = -2dB<br>00011 = -1.5dB<br>00100 = -1dB<br>00101 = -0.5dB<br>00110 = 0dB (default)<br>00111 = 0.5dB<br>01000 = 1dB<br>01001 = 1.5dB<br>01010 = 2dB<br>01011 = 2.5dB<br>01100 = 3dB<br>01101 = 3.5dB<br>01110 = 4dB<br>01111 = 4.5dB<br>10000 = 5dB<br>10001 = 5.5dB<br>10010 = 6dB<br>10011 to 11111 = Reserved |

**Table 17 DRC Initialisation**

## RETUNE MOBILE PARAMETRIC EQUALIZER (EQ)

The ReTune™ Mobile Parametric EQ is a circuit which can be enabled in the DAC digital signal path. The function of the EQ is to adjust the frequency characteristic of the output in order to compensate for unwanted frequency characteristics in the loudspeaker (or other output transducer). It can also be used to tailor the response according to user preferences, for example to accentuate or attenuate specific frequency bands to emulate different sound profiles or environments e.g. concert hall, rock etc.

The EQ is enabled as shown in Table 18.

| REGISTER ADDRESS | BIT | LABEL  | DEFAULT | DESCRIPTION                              |
|------------------|-----|--------|---------|--|
| R42 (2Ah)<br>EQ1 | 0   | EQ_ENA | 0       | EQ Enable<br>0 = Disabled<br>1 = Enabled |

**Table 18 ReTune Mobile Parametric EQ Enable**

The EQ can be configured to operate in two modes - "Default" mode or "ReTune Mobile" mode.

### DEFAULT MODE (5-BAND PARAMETRIC EQ)

In default mode, the cut-off / centre frequencies are fixed as per Table 19. The filter bandwidths are also fixed in default mode. The gain of the individual bands (-12dB to +12dB) can be controlled as described in Table 20. A full definition of the EQ Gain settings is provided in Table 21.

Note that the cut-off / centre frequencies noted in Table 19 are applicable to a DAC Sample Rate of 48kHz. When using other sample rates, these frequencies will be scaled in proportion to the selected sample rate.

| EQ BAND | CUT-OFF/CENTRE FREQUENCY |
|---------|--------------------------|
| 1       | 100 Hz                   |
| 2       | 300 Hz                   |
| 3       | 875 Hz                   |
| 4       | 2400 Hz                  |
| 5       | 6900 Hz                  |

**Table 19 EQ Band Cut-off / Centre Frequencies**

| REGISTER ADDRESS | BIT   | LABEL               | DEFAULT | DESCRIPTION   |
|------------------|-------|---------------------|---------|---|
| R42 (2Ah)<br>EQ1 | 15:11 | EQ_B1_GAIN<br>[4:0] | 0_0000  | EQ Band 1 Gain<br>00000 = -12dB<br>00001 = -11dB<br>....<br>11000 = +12dB |
|                  | 10:6  | EQ_B2_GAIN<br>[4:0] | 0_0000  | EQ Band 2 Gain<br>00000 = -12dB<br>00001 = -11dB<br>....<br>11000 = +12dB |
|                  | 5:1   | EQ_B3_GAIN<br>[4:0] | 0_0000  | EQ Band 3 Gain<br>00000 = -12dB<br>00001 = -11dB<br>....<br>11000 = +12dB |
| R43 (2Bh)        | 15:11 | EQ_B4_GAIN          | 0_0000  | EQ Band 4 Gain  |

| REGISTER ADDRESS | BIT  | LABEL               | DEFAULT | DESCRIPTION   |
|------------------|------|---------------------|---------|---|
| EQ2              |      | [4:0]               |         | 00000 = -12dB<br>00001 = -11dB<br>....<br>11000 = +12dB                   |
|                  | 10:6 | EQ_B5_GAIN<br>[4:0] | 0_0000  | EQ Band 5 Gain<br>00000 = -12dB<br>00001 = -11dB<br>....<br>11000 = +12dB |

**Table 20 EQ Band Gain Control**

| EQ GAIN SETTING | GAIN (DB) |
|-----------------|-----------|
| 00000           | -12       |
| 00001           | -11       |
| 00010           | -10       |
| 00011           | -9        |
| 00100           | -8        |
| 00101           | -7        |
| 00110           | -6        |
| 00111           | -5        |
| 01000           | -4        |
| 01001           | -3        |
| 01010           | -2        |
| 01011           | -1        |
| 01100           | 0         |
| 01101           | +1        |
| 01110           | +2        |
| 01111           | +3        |
| 10000           | +4        |
| 10001           | +5        |
| 10010           | +6        |
| 10011           | +7        |
| 10100           | +8        |
| 10101           | +9        |
| 10110           | +10       |
| 10111           | +11       |
| 11000           | +12       |
| 11001 to 11111  | Reserved  |

**Table 21 EQ Gain Control**

### RETUNE MOBILE MODE

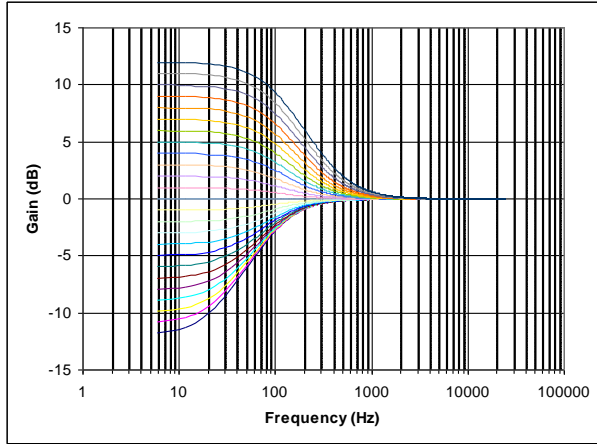
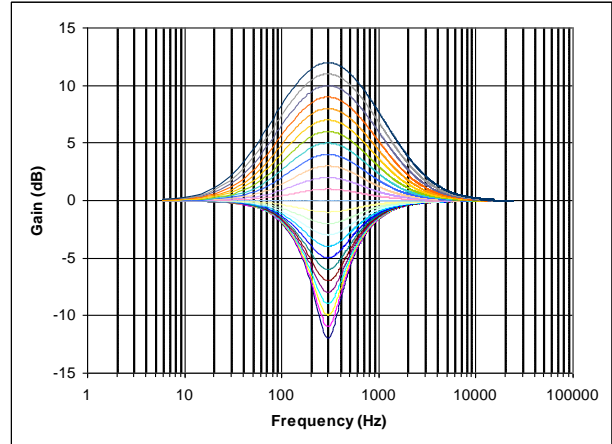
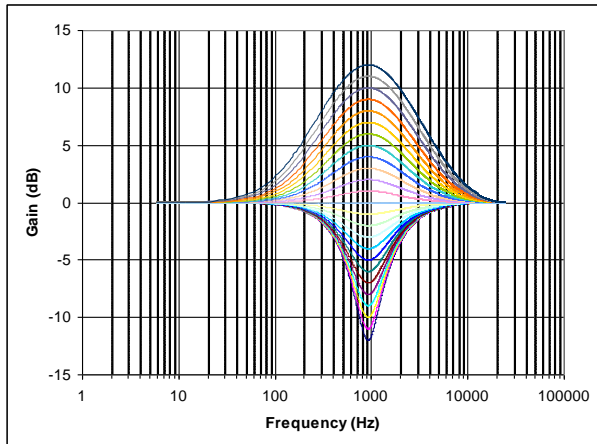
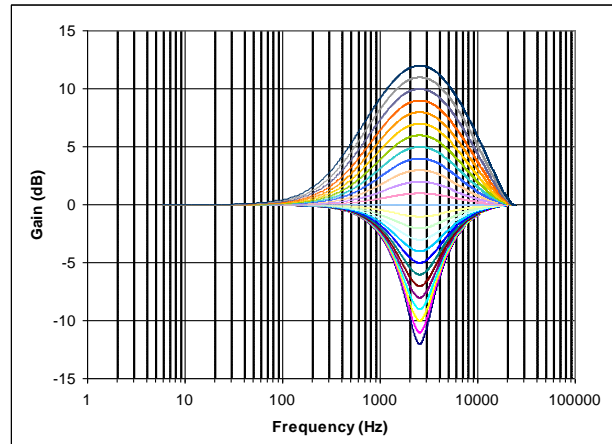
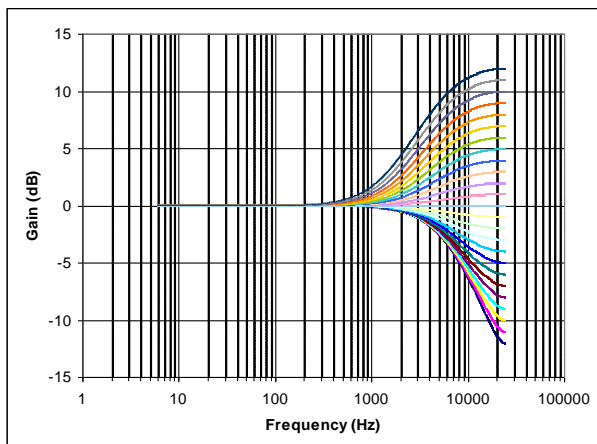
ReTune Mobile mode provides a comprehensive facility for the user to define the cut-off/centre frequencies and filter bandwidth for each EQ band, in addition to the gain controls already described. This enables the EQ to be accurately customised for a specific transducer characteristic or desired sound profile.

The EQ enable and EQ gain controls are the same as defined for the default mode. The additional coefficients used in ReTune Mobile mode are held in registers R44 to R61. These coefficients are derived using tools provided in Cirrus Logic's WISCE™ evaluation board control software.

Please contact your local Cirrus Logic representative for more details.

**EQ FILTER CHARACTERISTICS**

The filter characteristics for each frequency band are shown in Figure 26 to Figure 30. These figures show the frequency response for all available gain settings, using default cut-off/centre frequencies and bandwidth.


**Figure 26 EQ Band 1 – Low Freq Shelf Filter Response**

**Figure 27 EQ Band 2 – Peak Filter Response**

**Figure 28 EQ Band 3 – Peak Filter Response**

**Figure 29 EQ Band 4 – Peak Filter Response**

**Figure 30 EQ Band 5 – High Freq Shelf Filter Response**

## DIGITAL TO ANALOGUE CONVERTER (DAC)

The WM9081 DAC receives digital input data from the DACDAT pin. The digital audio data is converted to oversampled bit streams in the on-chip, true 24-bit digital interpolation filters. The bitstream data enters a multi-bit, sigma-delta DAC, which converts it to a high quality analogue audio signal. The multi-bit DAC architecture reduces high frequency noise and sensitivity to clock jitter. It also uses a Dynamic Element Matching technique for high linearity and low distortion.

The analogue outputs from the DAC can then be mixed with other analogue inputs using the analogue mixer and can be output to the speaker amplifier or the line output.

The DAC is enabled by the DAC\_ENA register bit.

| REGISTER ADDRESS              | BIT | LABEL   | DEFAULT | DESCRIPTION                               |
|-------------------------------|-----|---------|---------|---|
| R11 (0Bh)<br>Power Management | 0   | DAC_ENA | 0       | DAC Enable<br>0 = Disabled<br>1 = Enabled |

**Table 22 DAC Enable Control**

### DAC DIGITAL VOLUME CONTROL

The output level of each DAC can be controlled digitally over a range from -71.625dB to 0dB in 0.375dB steps. The level of attenuation for an eight-bit code X is given by:

$$0.375 \times (X-192) \text{ dB for } 1 \leq X \leq 192; \quad \text{MUTE for } X = 0 \quad 0\text{dB for } 192 \leq X \leq 255$$

| REGISTER ADDRESS           | BIT | LABEL         | DEFAULT   | DESCRIPTION  |
|----------------------------|-----|---------------|-----------|--|
| R30 (1Eh)<br>DAC Digital 1 | 7:0 | DAC_VOL [7:0] | 1100_0000 | DAC Volume and MUTE<br>0000 0000 = MUTE<br>0000 0001 = -71.625dB<br><br>... in steps of 0.375dB to<br><br>1100 0000 = 0dB<br>1100 0001 to 1111 1111 = reserved |

**Table 23 DAC Digital Volume Control**

### DAC SOFT MUTE AND SOFT UN-MUTE

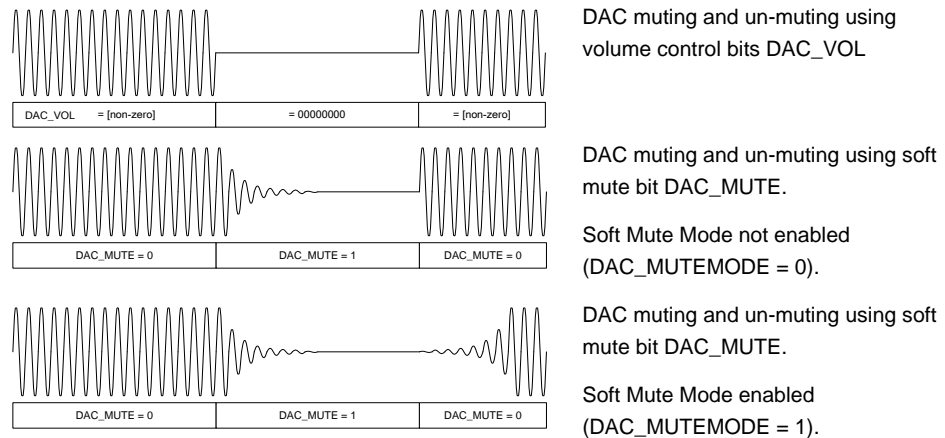
The WM9081 has a soft mute function which, when enabled, gradually attenuates the volume of the DAC output. When soft mute is disabled, the gain will either gradually ramp back up to the digital gain setting, or return instantly to the digital gain setting, depending on the DAC\_MUTEMODE register bit.

The DAC is soft-muted by default (DAC\_MUTE = 1). To play back an audio signal, this function must first be disabled by setting DAC\_MUTE to 0.

Soft Mute Mode would typically be enabled (DAC\_MUTEMODE = 1) when using DAC\_MUTE during playback of audio data so that when DAC\_MUTE is subsequently disabled, the sudden volume increase will not create pop noise by jumping immediately to the previous volume level (e.g. resuming playback after pausing).

Soft Mute Mode would typically be disabled (DAC\_MUTEMODE = 0) when un-muting at the start of audio playback, in order that the first part of the audio stream is not attenuated.





**Figure 31 DAC Mute Control**

The volume ramp rate during soft mute and un-mute is controlled by the DAC\_MUTERATE bit. Ramp rates of  $f_s/32$  and  $f_s/2$  are selectable as shown in Table 24. The ramp rate determines the rate at which the volume will be increased or decreased. The actual ramp time depends on the extent of the difference between the muted and un-muted volume settings.

| REGISTER ADDRESS           | BIT | LABEL        | DEFAULT | DESCRIPTION   |
|----------------------------|-----|--------------|---------|---|
| R31 (1Fh)<br>DAC Digital 2 | 10  | DAC_MUTERATE | 0       | DAC Soft Mute Ramp Rate<br>0 = Fast ramp ( $f_s/2$ , maximum ramp time is 10.7ms at $f_s=48k$ )<br>1 = Slow ramp ( $f_s/32$ , maximum ramp time is 171ms at $f_s=48k$ )<br>(Note: ramp rate scales with sample rate.)                                 |
|                            | 9   | DAC_MUTEMODE | 0       | DAC Unmute Ramp select<br>0 = Disabling soft-mute (DAC_MUTE=0) will cause the DAC volume to change immediately to the DAC_VOL setting.<br>1 = Disabling soft-mute (DAC_MUTE=0) will cause the DAC volume to ramp up gradually to the DAC_VOL setting. |
|                            | 3   | DAC_MUTE     | 1       | DAC Soft Mute Control<br>0 = DAC Un-mute<br>1 = DAC Mute  |

**Table 24 DAC Soft-Mute Control**

### DAC DE-EMPHASIS

Digital de-emphasis can be applied to the DAC playback data (e.g. when the data comes from a CD with pre-emphasis used in the recording). De-emphasis filtering is available for sample rates of 48kHz, 44.1kHz and 32kHz. See "Digital Filter Characteristics" for details of de-emphasis filter characteristics.

| REGISTER ADDRESS           | BIT | LABEL       | DEFAULT | DESCRIPTION  |
|----------------------------|-----|-------------|---------|--|
| R31 (1Fh)<br>DAC Digital 2 | 2:1 | DEEMPH[1:0] | 00      | DAC De-Emphasis Control<br>00 = No de-emphasis<br>01 = 32kHz sample rate<br>10 = 44.1kHz sample rate<br>11 = 48kHz sample rate |

**Table 25 DAC De-Emphasis Control**

## SIGNAL PATH CONTROL

The inputs and outputs to the WM9081 are independently controlled as described in this section. The input signal paths comprise two line inputs and the digital audio interface input. The output signal paths comprise a line output and a selectable Class AB/D speaker driver.

### INPUT SIGNAL PATH

There are three input signal paths to the analogue mixer. These are Line Input IN1, Line Input IN2 and the output from the DAC. These inputs can be mixed together as illustrated in Figure 32.

Line inputs IN1 and IN2 are enabled by the IN1\_ENA and IN2\_ENA registers. An optional -6dB gain can be selected in either path if required, using IN1\_VOL and IN2\_VOL.

The signal path from the DAC to the mixer is enabled by setting DAC\_SEL, as described in Table 26. The DAC volume can be controlled in the digital domain as described in the “Digital to Analogue Converter (DAC)” section.

| REGISTER ADDRESS           | BIT | LABEL   | DEFAULT | DESCRIPTION                                    |
|----------------------------|-----|---------|---------|--|
| R7 (07h)<br>Analogue Mixer | 4   | DAC_SEL | 0       | DAC Path Enable<br>0 = Disabled<br>1 = Enabled |
|                            | 3   | IN2_VOL | 0       | IN2 Volume Control<br>0 = 0dB<br>1 = -6dB      |
|                            | 2   | IN2_ENA | 0       | IN2 Path Enable<br>0 = Disabled<br>1 = Enabled |
|                            | 1   | IN1_VOL | 0       | IN1 Volume Control<br>0 = 0dB<br>1 = -6dB      |
|                            | 0   | IN1_ENA | 0       | IN1 Path Enable<br>0 = Disabled<br>1 = Enabled |

Table 26 Input Signal Path Control

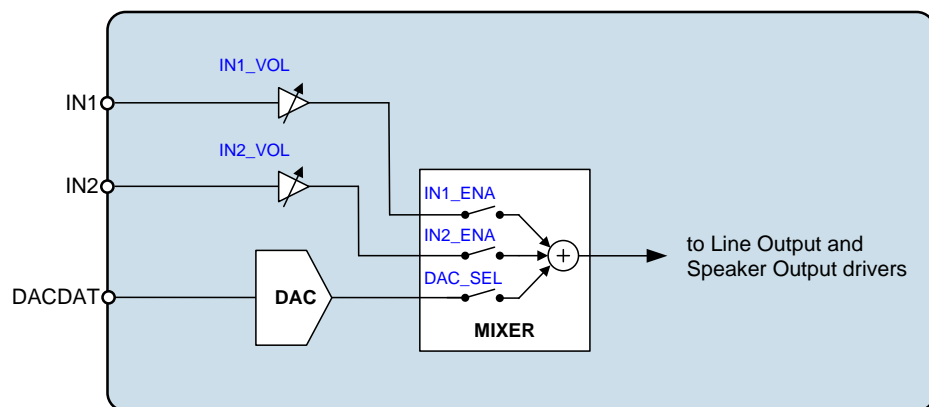


Figure 32 Input Signal Mixing

**OUTPUT SIGNAL PATH**

There are two output signal paths from the analogue mixer. These are the Line Output (on the LINEOUT pin) and the speaker output (on SPKOUTP and SPKOUTN).

The Line Output driver is enabled by setting LINEOUT\_ENA. The Line Output can be muted or adjusted using the LINEOUT\_MUTE and LINEOUT\_VOL register fields, as described in Table 27.

The Speaker Output signal path is enabled in two parts, using SPKPGA\_ENA and SPK\_ENA. When powering up the speaker driver, the SPKPGA\_ENA bit should be set before the SPK\_ENA bit is set. The reverse sequence should be followed when powering down the speaker driver. The Speaker Output can be muted or adjusted using the SPKPGA\_MUTE and SPKPGA\_VOL register fields, as described in Table 27.

The speaker driver incorporates pop suppression circuits controlled by the SPK\_INV\_MUTE and OUT\_SPK\_CTRL registers. The default setting of these bits is logic 1. In normal operation, these bits must be set to logic 0. In Class D mode, these bits are controlled automatically by the WM9081 when SPK\_ENA is written to. In Class AB mode, these bits must be set to logic 0 before SPK\_ENA is enabled.

To prevent "zipper noise", a zero-cross function is provided on the Line Output and Speaker Output volume controls. When this feature is enabled, volume updates will not take place until a zero-crossing is detected. In the case of a long period without zero-crossings, a timeout function is provided. When the zero-cross function is enabled, the volume will update after the timeout period if no earlier zero-cross has occurred. The timeout clock is enabled using CLK\_TO\_ENA, the timeout period is set by CLK\_TO\_DIV. See "Clocking and Sample Rates" for more information on these fields.

| REGISTER ADDRESS                    | BIT | LABEL                | DEFAULT   | DESCRIPTION  |
|-------------------------------------|-----|----------------------|-----------|--|
| R2 (02h)<br>Analogue<br>Lineout     | 7   | LINEOUT_MUTE         | 1         | LINEOUT Mute<br>0 = Un-mute<br>1 = Mute  |
|                                     | 6   | LINEOUT_ZC           | 0         | LINEOUT Zero Cross Detection<br>0 = Change gain immediately<br>1 = Change gain on zero cross only        |
|                                     | 5:0 | LINEOUT_VOL<br>[5:0] | 11_1001   | LINEOUT Volume<br>00 0000 = -57dB<br>00 0001 = -56dB<br>...<br>11 1001 = 0dB<br>...<br>11 1111 = 6dB     |
| R3 (03h)<br>Analogue<br>Speaker PGA | 7   | SPKPGA_MUTE          | 1         | Speaker PGA Mute<br>0 = Un-mute<br>1 = Mute  |
|                                     | 6   | SPKPGA_ZC            | 0         | Speaker PGA Zero Cross Detection<br>0 = Change gain immediately<br>1 = Change gain on zero cross only    |
|                                     | 5:0 | SPKPGA_VOL<br>[5:0]  | 39h (0dB) | Speaker PGA Volume<br>00 0000 = -57dB<br>00 0001 = -56dB<br>...<br>11 1001 = 0dB<br>...<br>11 1111 = 6dB |

| REGISTER ADDRESS                   | BIT | LABEL        | DEFAULT | DESCRIPTION  |
|------------------------------------|-----|--------------|---------|--|
| R10 (0Ah)<br>Analogue<br>Speaker 2 | 4   | SPK_INV_MUTE | 1       | Controls a pop-suppression circuit for Speaker start-up. Controlled automatically by SPK_ENA in Class D mode. Must be set to 0 before enabling SPK_ENA in Class AB mode.<br>0 = Normal operation<br>1 = SPK_INV_MUTE enabled |
|                                    | 3   | OUT_SPK_CTRL | 1       | Controls a pop-suppression circuit for Speaker start-up. Controlled automatically by SPK_ENA in Class D mode. Must be set to 0 before enabling SPK_ENA in Class AB mode.<br>0 = Normal operation<br>1 = OUT_SPK_CTRL enabled |
| R11 (0Bh)<br>Power<br>Management   | 4   | LINEOUT_ENA  | 0       | LINEOUT Enable<br>0 = Disabled<br>1 = Enabled  |
|                                    | 2   | SPKPGA_ENA   | 0       | Speaker PGA Enable<br>0 = Disabled<br>1 = Enabled  |
|                                    | 1   | SPK_ENA      | 0       | Speaker Output Enable<br>0 = Disabled<br>1 = Enabled   |

**Table 27 Output Signal Path Control**

## ANALOGUE OUTPUTS

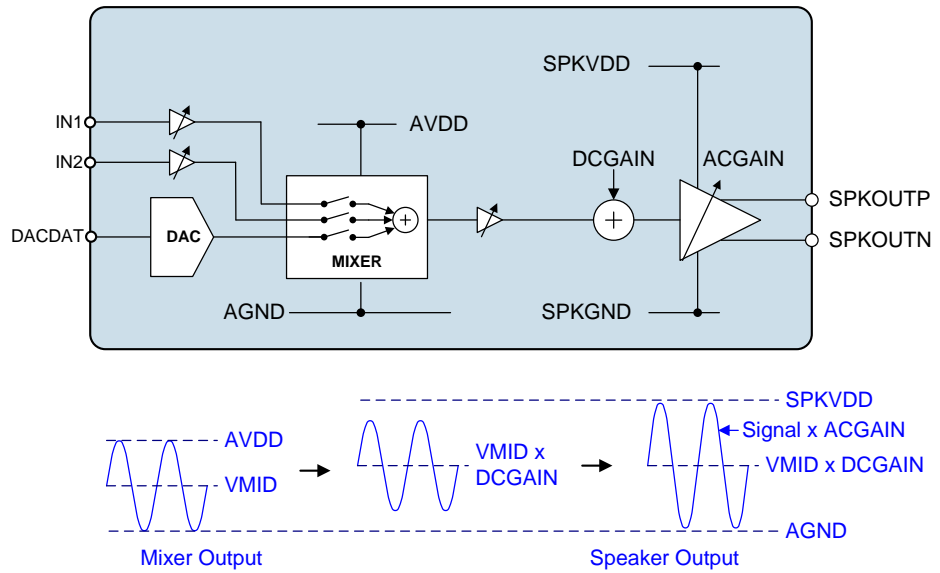
The WM9081 provides a mono Line Output and a mono Speaker Output. These are described individually in the subsections below.

### SPEAKER OUTPUT CONFIGURATION

The speaker output is a Class D BTL configuration by default. The speaker driver can be configured to operate in Class AB mode by setting SPK\_MODE = 1.

The analogue mixer circuit and the speaker PGA are powered by AVDD, whilst the speaker driver is powered by SPKVDD. Six levels of AC and DC signal boost are provided in order to deliver maximum output power for many commonly-used SPKVDD/AVDD combinations. These boost options are available in both Class AB and Class D modes. The boost levels from 0dB to +5.1dB are selected using register bits SPK\_DCGAIN and SPK\_ACGAIN. Note that the BTL output configuration provides an additional 6dB gain. To prevent pop noise, these registers should not be modified while the speaker outputs are enabled. Figure 33 illustrates the available mixing and speaker output configuration. Table 28 shows the gain/boost options.

Ultra-low leakage and high PSRR allow the speaker supply SPKVDD to be directly connected to a lithium battery. Note that an appropriate SPKVDD supply voltage must be provided to prevent waveform clipping when speaker boost is used.


**Figure 33 Speaker Gain Control**

| DC GAIN [5:3] AND AC GAIN [2:0] FROM OUTPUT MIXER OUTPUT TO SPEAKER AMP INPUT |           |          |
|---|-----------|----------|
| DC GAIN = AC GAIN   | Gain [dB] | Gain     |
| 000   | 0         | 1.00x    |
| 001   | 2.1       | 1.27x    |
| 010   | 2.9       | 1.40x    |
| 011   | 3.6       | 1.52x    |
| 100   | 4.5       | 1.67x    |
| 101   | 5.1       | 1.8x     |
| 110 – 111   | Reserved  | Reserved |

**Table 28 DC gain and AC gain**

The speaker mode select and the speaker gain controls are described in Table 29. Note that the BTL output configuration provides an additional 6dB gain.

| REGISTER ADDRESS                   | BIT | LABEL            | DEFAULT         | DESCRIPTION   |
|------------------------------------|-----|------------------|-----------------|---|
| R9 (09h)<br>Analogue<br>Speaker 1  | 5:3 | SPK_DCGAIN [2:0] | 011<br>(+3.6dB) | Speaker Output DC Gain<br>000 = x1 boost (0dB)<br>001 = x1.27 boost (2.1dB)<br>010 = x1.4 boost (2.9dB)<br>011 = x1.52 boost (3.6dB)<br>100 = x1.67 boost (4.5dB)<br>101 = x1.8 boost (5.1dB)<br>110-111 = Reserved |
|                                    | 2:0 | SPK_ACGAIN [2:0] | 011<br>(+3.6dB) | Speaker Output AC Gain<br>000 = x1 boost (0dB)<br>001 = x1.27 boost (2.1dB)<br>010 = x1.4 boost (2.9dB)<br>011 = x1.52 boost (3.6dB)<br>100 = x1.67 boost (4.5dB)<br>101 = x1.8 boost (5.1dB)<br>110-111 = Reserved |
| R10 (0Ah)<br>Analogue<br>Speaker 2 | 6   | SPK_MODE         | 0               | Speaker Mode Select<br>0 = Class D mode<br>1 = Class AB mode  |

**Table 29 Speaker Output Control**

### LINE OUTPUT CONFIGURATION

The line output, LINEOUT, provides a single-ended analogue output for connection to other circuits. Note that the line output is referenced to VMID, and external DC-blocking capacitors are required when connecting this output to other devices.

The line output is enabled and controlled using the registers described in the “Output Signal Path” section.

## POP SUPPRESSION CONTROL

The WM9081 incorporates a number of features, including Cirrus Logic's SilentSwitch™ technology, designed to suppress pops normally associated with Start-Up, Shut-Down or signal path control. To achieve maximum benefit from these features, careful attention is required to the sequence and timing of these controls. Note that, under the recommended usage conditions of the WM9081, these features will be configured automatically by running the default control sequences as described in the "Control Write Sequencer" section. In these cases, the user does not need to set these register fields directly. Additional bias controls, also pre-programmed into Control Write Sequencer, are described in the "Reference Voltages and Master Bias" section.

### DISABLED LINE OUTPUT CONTROL

The line output is biased to VMID in normal operation. In order to avoid audible pops caused by a disabled signal path dropping to AGND, the WM9081 can maintain LINEOUT at VMID when this output is disabled. This is achieved by connecting a buffered VMID reference to LINEOUT. The buffered VMID reference is enabled by setting VMID\_BUF\_ENA. When the line output is disabled, the reference is connected to LINEOUT by setting LINEOUT\_CLAMP. The output resistance can be either 500Ω or 20kΩ, depending on the LINEOUT\_VROI register bit.

| REGISTER ADDRESS            | BIT | LABEL         | DEFAULT | DESCRIPTION  |
|-----------------------------|-----|---------------|---------|--|
| R4 (04h)<br>VMID Control    | 5   | VMID_BUF_ENA  | 0       | Enables VMID reference for lineout and inputs clamps<br>0 = Disabled<br>1 = Enabled  |
| R8 (08h)<br>AntiPop Control | 1   | LINEOUT_VROI  | 0       | Buffered VMID to LINEOUT Resistance. This applies when LINEOUT_ENA = 0 and LINEOUT_CLAMP = 1.<br>0 = 20kΩ from buffered VMID to output<br>1 = 500Ω from buffered VMID to output                            |
|                             | 0   | LINEOUT_CLAMP | 0       | Clamp LINEOUT to buffered VMID. VMID_BUF_ENA must be set. This bit is only effective when LINEOUT_ENA = 0. The resistance is set by LINEOUT_VROI.<br>0 = Disabled<br>1 = Enabled (LINEOUT clamped to VMID) |

**Table 30 Disabled Line Output Control**

### LINE OUTPUT DISCHARGE CONTROL

The line output can be actively discharged to AGND through an internal resistor if desired. This is desirable at start-up in order to achieve a known output stage condition prior to enabling the soft-start VMID reference voltage. This is also desirable in shut-down to prevent the external connections from being affected by the internal circuits. The LINEOUT pin is discharged to AGND by setting LINEOUT\_DISCH.

| REGISTER ADDRESS            | BIT | LABEL         | DEFAULT | DESCRIPTION  |
|-----------------------------|-----|---------------|---------|--|
| R8 (08h)<br>AntiPop Control | 2   | LINEOUT_DISCH | 0       | Discharges LINEOUT via approx 5kohm resistor<br>0 = Not active<br>1 = Actively discharging LINEOUT |

**Table 31 Line Output Discharge Control**

---

## DIGITAL AUDIO INTERFACE

The digital audio interface is used for inputting DAC data to the WM9081. The digital audio interface uses three pins:

- DACDAT: DAC data input
- LRCLK: Left/Right data alignment clock
- BCLK: Bit clock, for synchronisation

In Software Control mode, many different audio data formats can be selected. In Hardware Control mode, only a limited range of formats is supported.

### SOFTWARE CONTROL MODE

In Software Control mode, the clock signals BCLK and LRCLK can be configured individually as inputs or outputs, enabling master or slave modes of operation.

The WM9081 receives either the Left channel or the Right channel data from a stereo digital audio source. Four different audio data formats are supported:

- Left justified
- Right justified
- I<sup>2</sup>S
- DSP mode

PCM operation is supported using the DSP mode. All four of these modes are MSB first. They are described in Audio Data Formats, below. Refer to the “Signal Timing Requirements” section for timing information.

The word length of the audio data can be selected; the WM9081 supports 8, 16, 20, 24 and 32 bit word lengths. A-law and  $\mu$ -law companding is supported in 8-bit mode.

Time Division Multiplexing (TDM) is available in all four data format modes. The WM9081 can be programmed to receive data in any of up to four stereo time slots.

### HARDWARE CONTROL MODE

In Hardware Control mode, the WM9081 operates in slave mode, where the clock signals BCLK and LRCLK are both inputs. The only supported sample rate is 48kHz; the controlling device must ensure that the clocks and the data input are consistent with this.

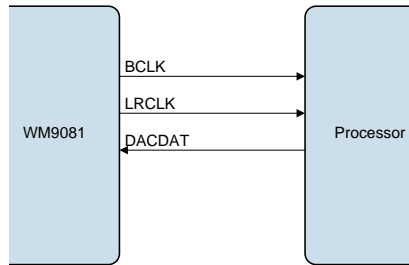
The data format is 16-bit I<sup>2</sup>S mode, as described in “Audio Data Formats (Normal Mode)” below. The Left/Right channel selection is made using the SCIM/CHANNEL pin, as described in “Control Interface (Hardware Mode)”.

Companding and TDM modes are not supported in Hardware Control mode.

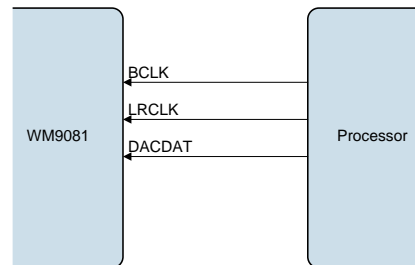


## MASTER AND SLAVE MODE OPERATION

The WM9081 digital audio interface can operate as a master or slave as shown in Figure 34 and Figure 35.



**Figure 34 Master Mode**



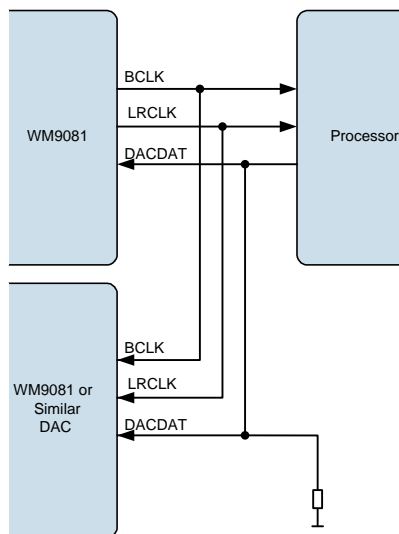
**Figure 35 Slave Mode**

The Audio Interface output control is illustrated above. BCLK and LRCLK are configured as inputs or outputs using the BCLK\_DIR and LRCLK\_DIR register fields - see "Digital Audio Interface Control".

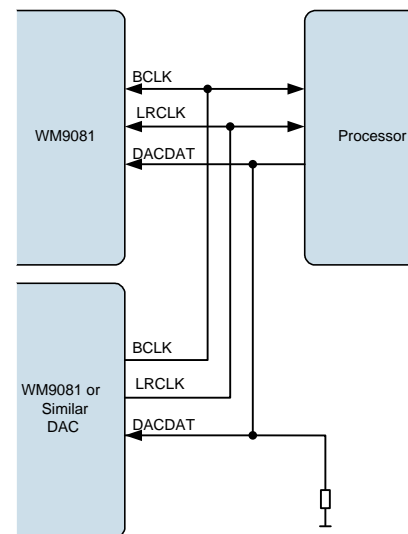
Note that BCLK and LRCLK can be configured independently as inputs or outputs, allowing mixed Master/Slave operation.

## OPERATION WITH TDM

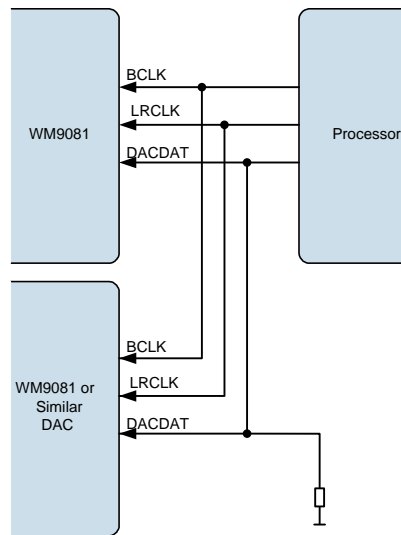
Time division multiplexing (TDM) allows multiple devices to transfer data simultaneously on the same bus. The WM9081 DAC supports TDM in master and slave modes for all data formats and word lengths. TDM is enabled and configured using register bits defined in the "Digital Audio Interface Control" section.



**Figure 36 TDM with WM9081 as Master**



**Figure 37 TDM with Other DAC as Master**



**Figure 38 TDM with Processor as Master**

**Note:** The WM9081 is a 24-bit device. If the user operates the WM9081 in 32-bit mode then the 8 LSBs will be ignored by the DAC. To ensure the DACDAT line is never left floating (eg. when using a mixture or 24-bit and 32-bit devices), it is recommended to add a pull-down resistor to the DACDAT line.

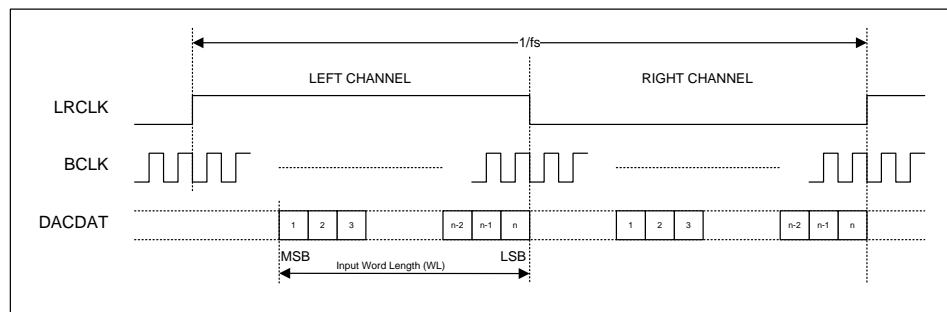
### BCLK FREQUENCY

The BCLK frequency is controlled relative to CLK\_SYS by the BCLK\_DIV divider. Internal clock divide and phase control mechanisms ensure that the BCLK and LRCLK edges will occur in a predictable and repeatable position relative to each other and relative to the data for a given combination of DAC sample rate and BCLK\_DIV settings.

BCLK\_DIV is defined in the “Digital Audio Interface Control” section. See also “Clocking and Sample Rates” section for more information.

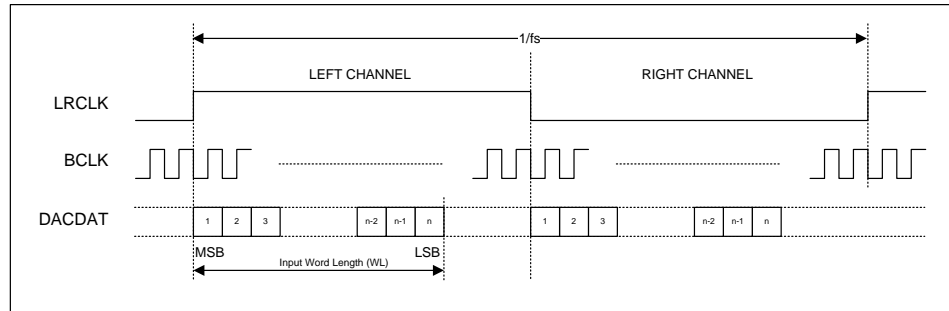
### AUDIO DATA FORMATS (NORMAL MODE)

In Right Justified mode, the LSB is available on the last rising edge of BCLK before a LRCLK transition. All other bits are transmitted before (MSB first). Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles after each LRCLK transition.



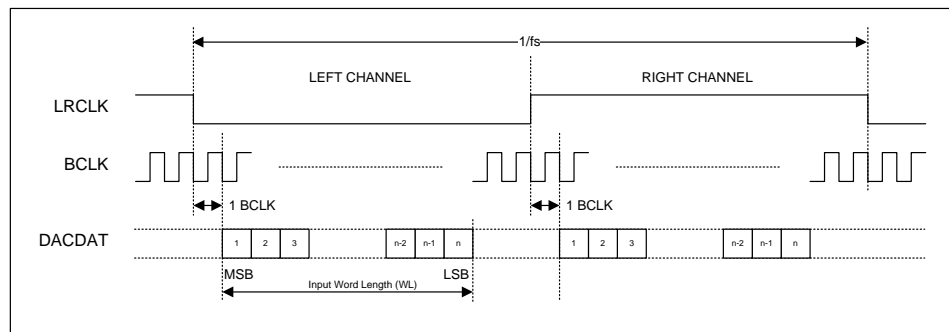
**Figure 39 Right Justified Audio Interface (assuming n-bit word length)**

In Left Justified mode, the MSB is available on the first rising edge of BCLK following a LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles before each LRCLK transition.



**Figure 40 Left Justified Audio Interface (assuming n-bit word length)**

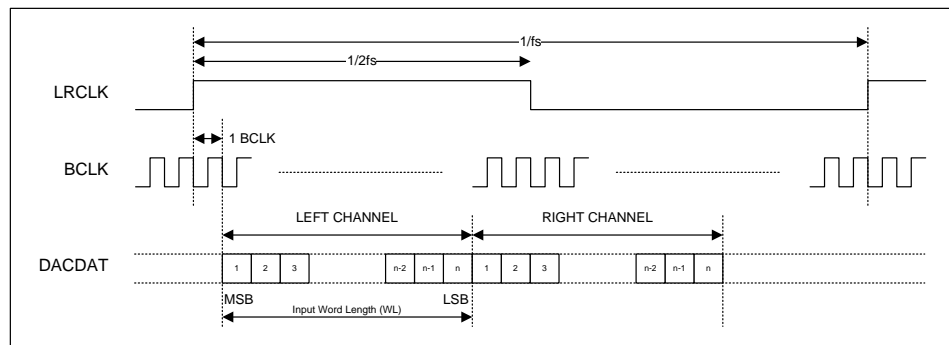
In I<sup>2</sup>S mode, the MSB is available on the second rising edge of BCLK following a LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.



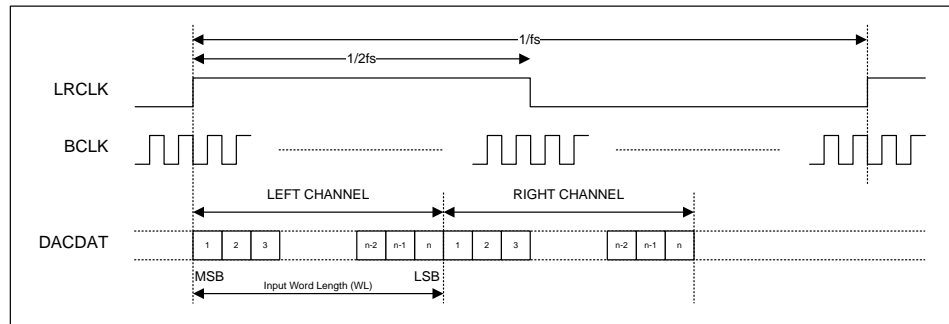
**Figure 41 I2S Justified Audio Interface (assuming n-bit word length)**

In DSP mode, the left channel MSB is available on either the 1<sup>st</sup> (mode B) or 2<sup>nd</sup> (mode A) rising edge of BCLK (selectable by AIF\_LRCLK\_INV) following a rising edge of LRCLK. Right channel data immediately follows left channel data. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of the right channel data and the next sample.

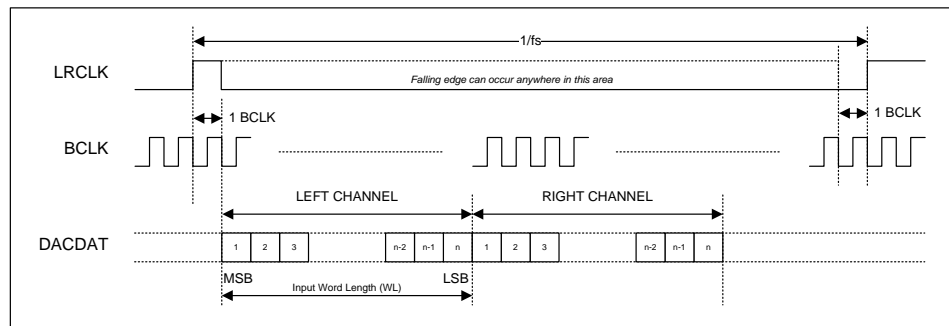
In device master mode, the LRCLK output will resemble the frame pulse shown in Figure 42 and Figure 43. In device slave mode, Figure 44 and Figure 45, it is possible to use any length of frame pulse less than 1/fs, providing the falling edge of the frame pulse occurs greater than one BCLK period before the rising edge of the next frame pulse.



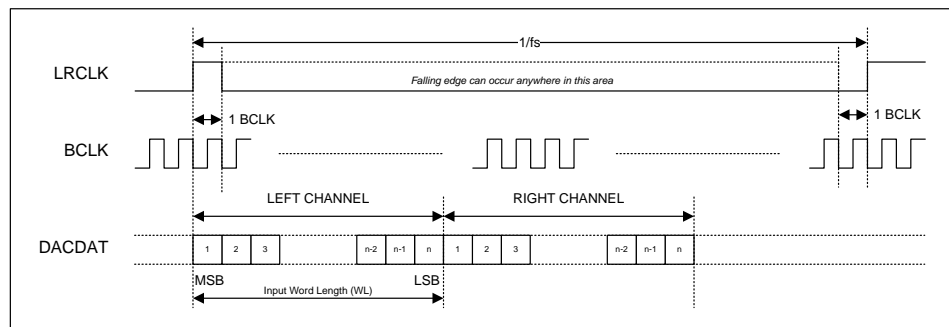
**Figure 42 DSP Mode Audio Interface (mode A, AIF\_LRCLK\_INV=0, Master)**



**Figure 43 DSP Mode Audio Interface (mode B, AIF\_LRCLK\_INV=1, Master)**



**Figure 44 DSP Mode Audio Interface (mode A, AIF\_LRCLK\_INV=0, Slave)**



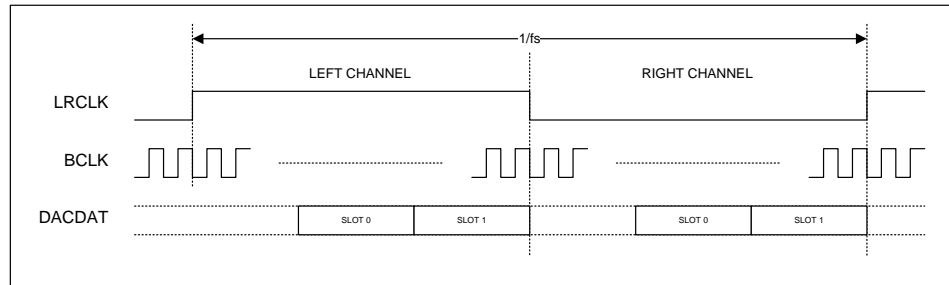
**Figure 45 DSP Mode Audio Interface (mode B, AIF\_LRCLK\_INV=1, Slave)**

PCM operation is supported in DSP interface mode. Mono PCM data received by the WM9081 will be treated as Left Channel data. The left channel must be selected by the WM9081 in order for this data to be routed to the output drivers.

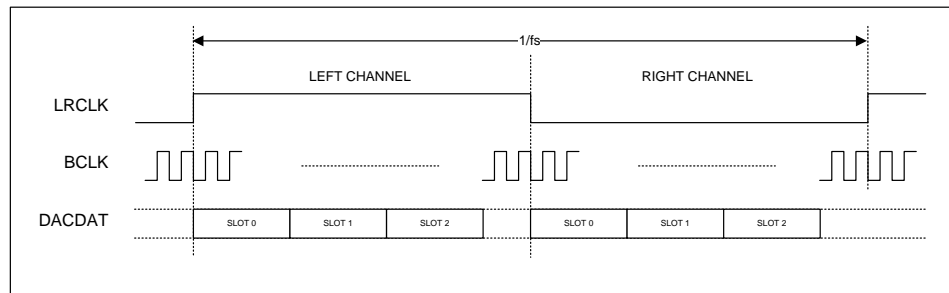
### AUDIO DATA FORMATS (TDM MODE)

TDM is supported in master and slave mode and is enabled using the AIFDAC\_TDM\_MODE register field. All audio interface data formats support time division multiplexing (TDM). The AIFDAC\_TDM\_MODE identifies the number of stereo time slots in the received data. Up to four stereo time slots can be selected. The AIFDAC\_TDM\_SLOT field identifies which of the available time slots contains the data that is to be received by the WM9081.

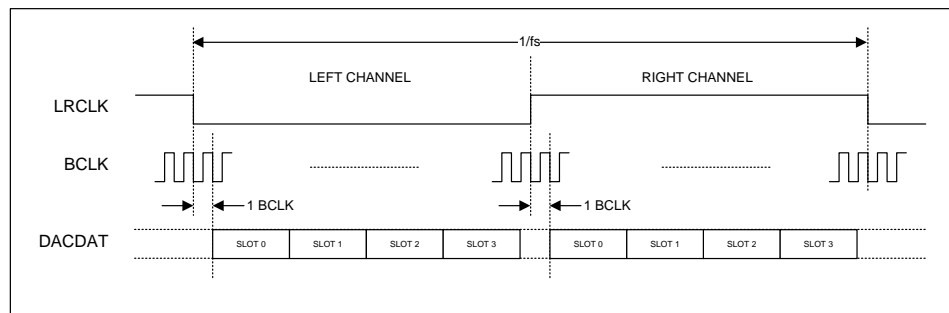
When TDM is enabled, BCLK frequency must be high enough to allow data from all time slots to be transferred. The relative timing of the audio interface timeslots depends upon the selected data format as shown in Figure 46 to Figure 50. A maximum of four stereo time slots can be supported in each data format. The following figures illustrate only a subset of the available options.



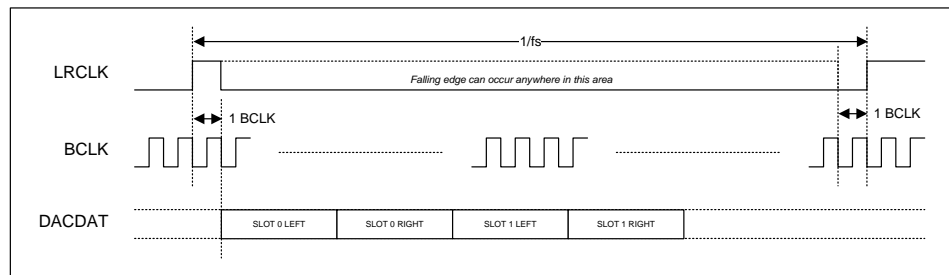
**Figure 46 TDM in Right-Justified Mode - 2 Stereo Time Slots**



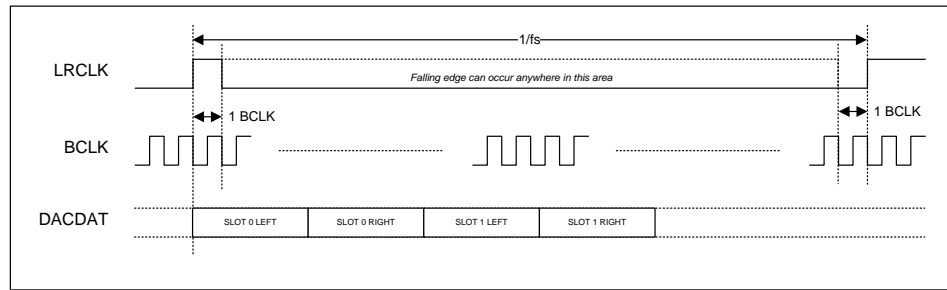
**Figure 47 TDM in Left-Justified Mode - 3 Stereo Time Slots**



**Figure 48 TDM in I²S Mode - 4 Stereo Time Slots**



**Figure 49 TDM in DSP Mode A - 2 Stereo Time Slots**



**Figure 50 TDM in DSP Mode B - 2 Stereo Time Slots**

## DIGITAL AUDIO INTERFACE CONTROL

The register bits controlling audio data format, word length, left/right channel data source and TDM are summarised in Table 32.

| REGISTER ADDRESS               | BIT | LABEL           | DEFAULT | DESCRIPTION  |
|--------------------------------|-----|-----------------|---------|--|
| R22 (16h)<br>Audio Interface 1 | 6   | AIFDAC_CHAN     | 0       | DAC Data Source Select<br>0 = DAC selects left channel data<br>1 = DAC selects right channel data  |
|                                | 5:4 | AIFDAC_TDM_SLOT | 00      | DAC TDM Slot Select<br>00 = Select slot 0 (Left/Right)<br>01 = Select slot 1 (Left/Right)<br>10 = Select slot 2 (Left/Right)<br>11 = Select slot 3 (Left/Right)  |
|                                | 3:2 | AIFDAC_TDM_MODE | 00      | DAC TDM Mode Select<br>00 = 1 stereo slot (TDM off)<br>01 = 2 stereo slots<br>10 = 3 stereo slots<br>11 = 4 stereo slots   |
| R23 (17h)<br>Audio Interface 2 | 8   | DAC_DAT_INV     | 0       | DACDAT Invert<br>0 = DACDAT not inverted<br>1 = DACDAT inverted  |
|                                | 7   | AIF_BCLK_INV    | 0       | BCLK Invert<br>0 = BCLK not inverted<br>1 = BCLK inverted  |
|                                | 4   | AIF_LRCLK_INV   | 0       | Right, left and I <sup>2</sup> S modes – LRCLK polarity:<br>0 = normal LRCLK polarity<br>1 = invert LRCLK polarity<br><br>DSP Mode – mode A/B select :<br>0 = MSB is available on 2nd BCLK rising edge after LRC rising edge (mode A)<br>1 = MSB is available on 1st BCLK rising edge after LRC rising edge (mode B) |
|                                | 3:2 | AIF_WL [1:0]    | 00      | Digital Audio Interface Word Length<br>00 = 16 bits<br>01 = 20 bits<br>10 = 24 bits<br>11 = 32 bits<br>Note - see “Companding” for the selection of 8-bit mode.  |

| REGISTER ADDRESS | BIT | LABEL         | DEFAULT | DESCRIPTION  |
|------------------|-----|---------------|---------|--|
|                  | 1:0 | AIF_FMT [1:0] | 10      | Digital Audio Interface Format<br>00 = Right justified<br>01 = Left justified<br>10 = I <sup>2</sup> S Format<br>11 = DSP Mode |

**Table 32 Digital Audio Interface Data Control**

### AUDIO INTERFACE OUTPUT TRI-STATE

Register bit AIF\_TRIS can be used to tri-state the audio interface pins LRCLK and BCLK as described in Table 33. This function tri-states the audio interface pins regardless of the state of other registers which control these pin configurations.

| REGISTER ADDRESS               | BIT | LABEL    | DEFAULT | DESCRIPTION  |
|--------------------------------|-----|----------|---------|--|
| R23 (17h)<br>Audio Interface 2 | 9   | AIF_TRIS | 0       | Audio Interface Tristate<br>0 = Audio interface pins operate normally<br>1 = Tristate all audio interface pins |

**Table 33 Digital Audio Interface Tri-State Control**

### BCLK AND LRCLK CONTROL

The audio interface can be programmed to operate in master mode or slave mode by configuring BCLK and LRCLK as outputs or inputs respectively. The direction of these signals is configured using the BCLK\_DIR and LRCLK\_DIR register fields.

In master mode, the BCLK and LRCLK signals are generated by the WM9081 when the DAC is enabled. In slave mode, the BCLK and LRCLK clock outputs are disabled by default to allow another digital audio interface to drive these pins.

Note that BCLK and LRCLK can be configured independently as inputs or outputs, allowing mixed Master/Slave operation.

In master mode, BCLK is derived from CLK\_SYS via a programmable division set by BCLK\_DIV.

In master mode, LRCLK is derived from BCLK via a programmable division set by LRCLK\_RATE. The BCLK input to this divider may be internal or external, allowing mixed master and slave modes.

The BCLK and LRCLK control fields are defined in Table 34.

| REGISTER ADDRESS               | BIT | LABEL     | DEFAULT | DESCRIPTION  |
|--------------------------------|-----|-----------|---------|--|
| R23 (17h)<br>Audio Interface 2 | 6   | BCLK_DIR  | 0       | BCLK Direction<br>(Forces BCLK clock to be output in slave mode)<br>0 = BCLK normal operation<br>1 = BCLK clock output enabled     |
|                                | 5   | LRCLK_DIR | 0       | LRCLK Direction<br>(Forces LRCLK clock to be output in slave mode)<br>0 = LRCLK normal operation<br>1 = LRCLK clock output enabled |

| REGISTER ADDRESS               | BIT  | LABEL             | DEFAULT       | DESCRIPTION  |
|--------------------------------|------|-------------------|---------------|--|
| R24 (18h)<br>Audio Interface 3 | 4:0  | BCLK_DIV [4:0]    | 0_1000        | BCLK Rate<br>00000 = CLK_SYS<br>00001 = CLK_SYS / 1.5<br>00010 = CLK_SYS / 2<br>00011 = CLK_SYS / 3<br>00100 = CLK_SYS / 4<br>00101 = CLK_SYS / 5<br>00110 = CLK_SYS / 5.5<br>00111 = CLK_SYS / 6<br>01000 = CLK_SYS / 8<br>01001 = CLK_SYS / 10<br>01010 = CLK_SYS / 11<br>01011 = CLK_SYS / 12<br>01100 = CLK_SYS / 16<br>01101 = CLK_SYS / 20<br>01110 = CLK_SYS / 22<br>01111 = CLK_SYS / 24<br>10000 = CLK_SYS / 25<br>10001 = CLK_SYS / 30<br>10010 = CLK_SYS / 32<br>10011 = CLK_SYS / 44<br>10100 = CLK_SYS / 48 |
| R25 (19h)<br>Audio Interface 4 | 10:0 | LRCLK_RATE [10:0] | 000_0010_0010 | LRCLK Rate<br>LRCLK clock output = BCLK / LRCLK_RATE<br><br>Integer (LSB = 1)<br>Valid from 8..2047  |

**Table 34 Digital Audio Interface Clock Control**

### COMPANDING

The WM9081 supports A-law and  $\mu$ -law companding as shown in Table 35.

| REGISTER ADDRESS               | BIT | LABEL        | DEFAULT | DESCRIPTION  |
|--------------------------------|-----|--------------|---------|--|
| R22 (16h)<br>Audio Interface 1 | 1   | DAC_COMP     | 0       | DAC Companding Enable<br>0 = Disabled<br>1 = Enabled |
|                                | 0   | DAC_COMPMODE | 0       | DAC Companding Type<br>0 = $\mu$ -law<br>1 = A-law   |

**Table 35 Companding Control**

Companding involves using a piecewise linear approximation of the following equations (as set out by ITU-T G.711 standard) for data compression:



$\mu$ -law (where  $\mu=255$  for the U.S. and Japan):

$$F(x) = \ln(1 + \mu|x|) / \ln(1 + \mu) \quad -1 \leq x \leq 1$$

A-law (where  $A=87.6$  for Europe):

$$F(x) = A|x| / (1 + \ln A) \quad \text{for } x \leq 1/A$$

$$F(x) = (1 + \ln A|x|) / (1 + \ln A) \quad \text{for } 1/A \leq x \leq 1$$

The companded data is also inverted as recommended by the G.711 standard (all 8 bits are inverted for  $\mu$ -law, all even data bits are inverted for A-law). The data will be transmitted as the first 8 MSBs of data.

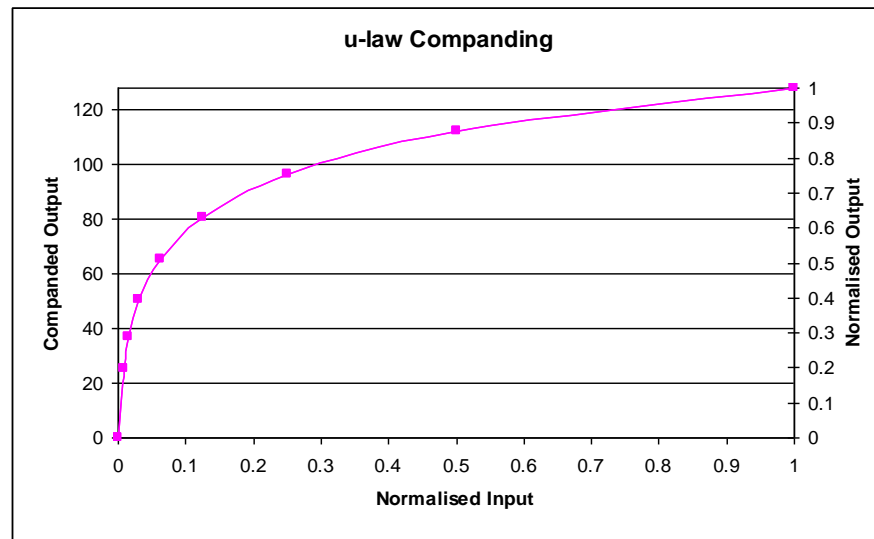
Companding converts 13 bits ( $\mu$ -law) or 12 bits (A-law) to 8 bits using non-linear quantization. This provides greater precision for low amplitude signals than for high amplitude signals, resulting in a greater usable dynamic range than 8 bit linear quantization. The companded signal is an 8-bit word comprising sign (1 bit), exponent (3 bits) and mantissa (4 bits).

8-bit mode is selected whenever  $DAC\_COMP=1$ . The use of 8-bit data allows samples to be passed using as few as 8 BCLK cycles per LRCLK frame. When using DSP mode B, 8-bit data words may be transferred consecutively every 8 BCLK cycles.

8-bit mode (without Companding) may be enabled by setting  $DAC\_COMPMODE=1$  when  $DAC\_COMP=0$ .

| BIT7 | BIT[6:4] | BIT[3:-0] |
|------|----------|-----------|
| SIGN | EXPONENT | MANTISSA  |

**Table 36 8-bit Companded Word Composition**



**Figure 51  $\mu$ -Law Companding**

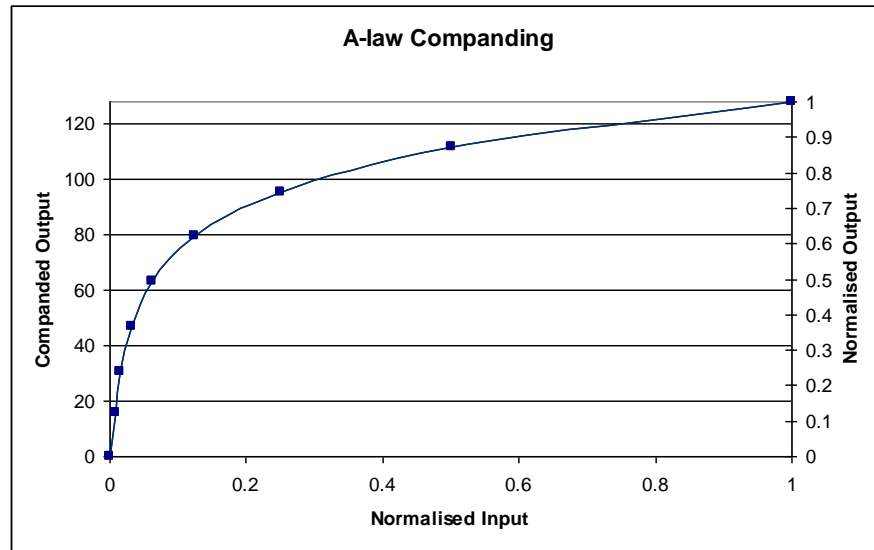


Figure 52 A-Law Comping

## CLOCKING AND SAMPLE RATES

The internal clocks for the WM9081 are all derived from a common internal clock source, CLK\_SYS. This clock is the reference for the DSP / DAC core functions, digital audio interface, Class D switching amplifier, write sequencer and other internal functions.

CLK\_SYS can either be derived directly from MCLK, or may be generated from a Frequency Locked Loop (FLL) using MCLK, BCLK or LRCLK as a reference. All commonly-used audio sample rates can be derived directly from typical MCLK frequencies; the FLL provides additional flexibility for a wider range of MCLK frequencies. To avoid audible glitches, all clock configurations must be set up before enabling playback. The FLL can be used to generate a free-running clock in the absence of an external reference source; see "Frequency Locked Loop (FLL)" for further details.

The WM9081 supports a wide range of standard audio sample rates from 8kHz to 96kHz. The core clocking requirements of the WM9081 are automatically configured according to the selected Sample Rate and the applicable CLK\_SYS / fs ratio. These parameters are contained in the SAMPLE\_RATE and CLK\_SYS\_RATE register fields respectively.

A slow clock, TOCLK, is used to set the timeout period for volume updates when zero-cross detect is used. This clock is enabled by CLK\_TO\_ENA and controlled by CLK\_TO\_DIV.

A clock output, OPCLK, can be derived from CLK\_SYS and output on the MCLK pin to provide clocking to other devices. This clock is enabled by CLK\_OP\_ENA and controlled by CLK\_OP\_DIV. This feature is only available when MCLK is not selected as an input to the WM9081.

In master mode, BCLK is derived from CLK\_SYS via a programmable divider set by BCLK\_DIV. In master mode, the LRCLK is derived from BCLK via a programmable divider LRCLK\_RATE. The LRCLK can be derived from an internal or external BCLK source, allowing mixed master/slave operation. See "Digital Audio Interface Control" for details of the BCLK and LRCLK configuration.

The control registers associated with Clocking and Sample Rates are shown in Table 37 to Table 39.

The overall clocking scheme for the WM9081 is illustrated in Figure 53.

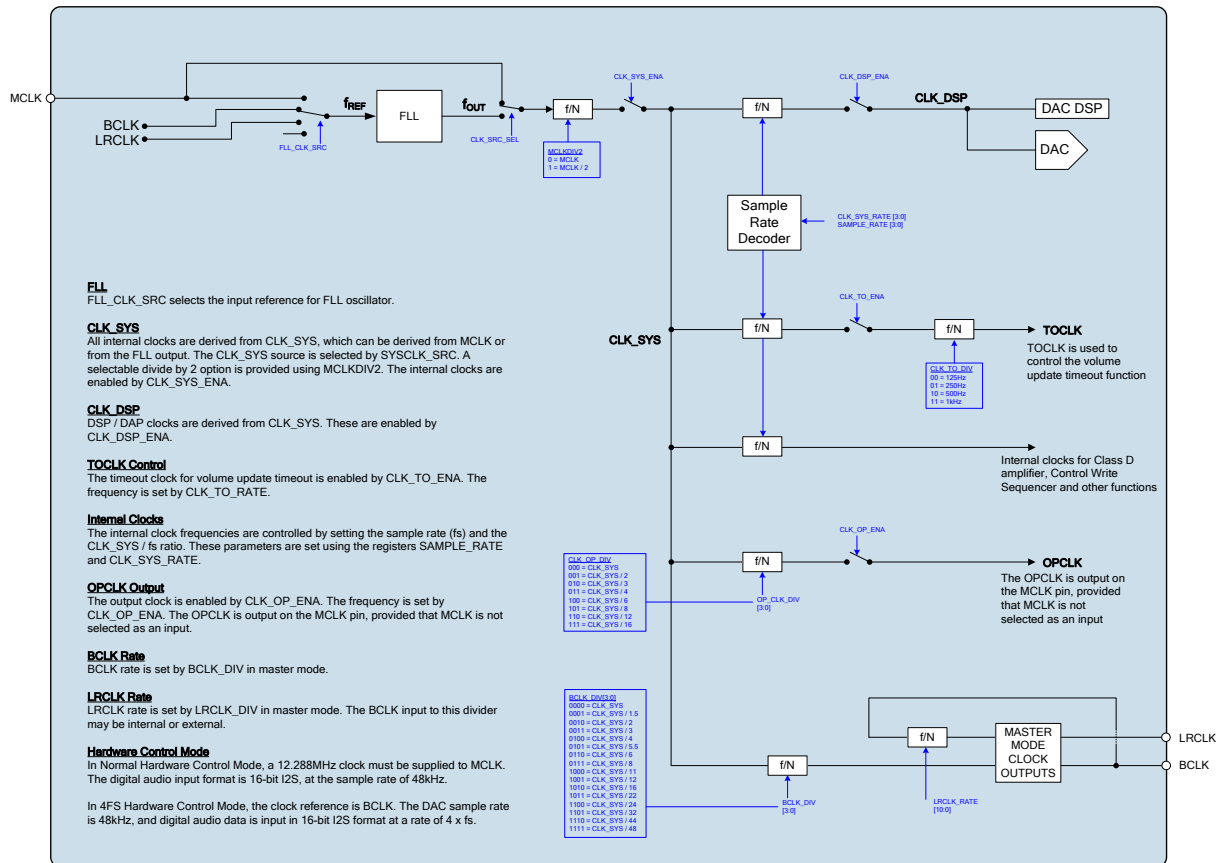


Figure 53 WM9081 Clocking Overview

## CLK\_SYS CONTROL

The CLK\_SRC\_SEL bit is used to select the source for CLK\_SYS. The source can be either MCLK or the FLL output. The selected source may also be adjusted by the MCLKDIV2 divider to generate CLK\_SYS. These register fields are described in Table 37. See “Frequency Locked Loop (FLL)” for more details of the Frequency Locked Loop clock generator.

The CLK\_SYS signal is enabled by register bit CLK\_SYS\_ENA. This bit should be set to 0 when reconfiguring clock sources or when no clock source is present. It is not recommended to change MCLK\_SRC or CLK\_SRC\_SEL while the CLK\_SYS\_ENA bit is set.

The core clocking requirements are configured by setting the SAMPLE\_RATE and CLK\_SYS\_RATE fields as described in Table 37. The WM9081 supports DAC sample rates (fs) from 8kHz up to 96kHz. The CLK\_SYS\_RATE field must be set according to the ratio of CLK\_SYS to fs.

The DSP / DAC clock function is enabled by register bit CLK\_DSP\_ENA.

| REGISTER ADDRESS            | BIT | LABEL              | DEFAULT | DESCRIPTION   |
|-----------------------------|-----|--------------------|---------|---|
| R12 (0Ch)<br>Clock Control1 | 7   | MCLKDIV2           | 0       | MCLK Divider<br>0 = MCLK<br>1 = MCLK / 2  |
| R13 (0Dh)<br>Clock Control2 | 7:4 | CLK_SYS_RATE [3:0] | 0011    | Selects the CLK_SYS / fs ratio<br>0000 = 64<br>0001 = 128<br>0010 = 192<br>0011 = 256<br>0100 = 384<br>0101 = 512<br>0110 = 768<br>0111 = 1024<br>1000 = 1408<br>1001 = 1536  |
|                             | 3:0 | SAMPLE_RATE [3:0]  | 1000    | Selects the Sample Rate (fs)<br>0000 = 8kHz<br>0001 = 11.025kHz<br>0010 = 12kHz<br>0011 = 16kHz<br>0100 = 22.05kHz<br>0101 = 24kHz<br>0110 = 32kHz<br>0111 = 44.1kHz<br>1000 = 48kHz<br>1001 = 88.2kHz<br>1010 = 96kHz<br>1011 to 1111 = Reserved |
| R14 (0Eh)<br>Clock Control3 | 13  | CLK_SRC_SEL        | 0       | CLK_SYS Source Select<br>0 = MCLK<br>1 = FLL output   |
|                             | 1   | CLK_DSP_ENA        | 0       | CLK_DSP enable<br>0 = Disabled<br>1 = Enabled   |
|                             | 0   | CLK_SYS_ENA        | 0       | CLK_SYS enable<br>0 = Disabled<br>1 = Enabled   |

**Table 37 CLK\_SYS Control**

### TOCLK CONTROL

A timeout clock (TOCLK) is derived from CLK\_SYS as an input to the zero-cross volume update function. This clock is enabled by register bit CLK\_TO\_ENA, and its frequency is controlled by CLK\_TO\_RATE, as described in Table 38.

| REGISTER ADDRESS            | BIT | LABEL            | DEFAULT | DESCRIPTION   |
|-----------------------------|-----|------------------|---------|---|
| R12 (0Ch)<br>Clock Control1 | 9:8 | CLK_TO_DIV [1:0] | 00      | TOCLK (timeout/ slow clock) frequency select<br>00 = 125Hz<br>01 = 250Hz<br>10 = 500Hz<br>11 = 1kHz |
| R14 (0Eh)<br>Clock Control3 | 2   | CLK_TO_ENA       | 0       | TOCLK (timeout/ slow clock) Enable<br>0 = Disabled<br>1 = Enabled                                   |

**Table 38 TOCLK Control**

### OPCLK CONTROL

A clock output (OPCLK) derived from CLK\_SYS may be output on the MCLK pin. This clock is enabled by register bit CLK\_OP\_ENA, and its frequency is controlled by CLK\_OP\_DIV.

This output is only supported when MCLK is not selected as an input to the WM9081.

| REGISTER ADDRESS            | BIT   | LABEL            | DEFAULT | DESCRIPTION   |
|-----------------------------|-------|------------------|---------|---|
| R12 (0Ch)<br>Clock Control1 | 12:10 | CLK_OP_DIV [2:0] | 000     | OPCLK Clock Divider<br>000 = CLK_SYS<br>001 = CLK_SYS / 2<br>010 = CLK_SYS / 3<br>011 = CLK_SYS / 4<br>100 = CLK_SYS / 6<br>101 = CLK_SYS / 8<br>110 = CLK_SYS / 12<br>111 = CLK_SYS / 16 |
| R14 (0Eh)<br>Clock Control3 | 5     | CLK_OP_ENA       | 0       | Clock Output Enable<br>0 = Disabled<br>1 = Enabled<br>This bit enables OPCLK output on the MCLK pin.<br>Frequency is set by CLK_OP_DIV.   |

**Table 39 OPCLK Control**

### FREQUENCY LOCKED LOOP (FLL)

The integrated FLL can be used to generate CLK\_SYS from a wide variety of different reference sources and frequencies. The FLL can use either MCLK, BCLK or LRCLK as its reference, which may be a high frequency (eg. 12.288MHz) or low frequency (eg. 32.768kHz) reference. The FLL is tolerant of jitter and may be used to generate a stable CLK\_SYS from a less stable input signal. The FLL characteristics are summarised in “Electrical Characteristics”.

Note that the FLL can be used to generate a free-running clock in the absence of an external reference source. This is described in the “Free-Running FLL Clock” section below.

The FLL is enabled using the FLL\_ENA register bit. Note that, when changing FLL settings, it is recommended that the digital circuit be disabled via FLL\_ENA and then re-enabled after the other register settings have been updated. When changing the input reference frequency  $F_{REF}$ , it is recommended that the FLL be reset by setting FLL\_ENA to 0.

The field FLL\_CLK\_REF\_DIV provides the option to divide the input reference (MCLK, BCLK or LRCLK) by 1, 2, 4 or 8. This field should be set to bring the reference down to 13.5MHz or below. For best performance, it is recommended that the highest possible frequency - within the 13.5MHz limit - should be selected.

The field FLL\_CTRL\_RATE controls internal functions within the FLL; it is recommended that only the default setting be used for this parameter. FLL\_GAIN controls the internal loop gain and should be set to the recommended value.

The FLL output frequency is directly determined from FLL\_FRATIO, FLL\_OUTDIV and the real number represented by FLL\_N and FLL\_K. The field FLL\_N is an integer (LSB = 1); FLL\_K is the fractional portion of the number (MSB = 0.5). The fractional portion is only valid when enabled by the field FLL\_FRAC. It is recommended that FLL\_FRAC is enabled at all times.

The FLL output frequency is generated according to the following equation:

$$F_{OUT} = (F_{VCO} / FLL\_OUTDIV)$$

The FLL operating frequency,  $F_{VCO}$  is set according to the following equation:

$$F_{VCO} = (F_{REF} \times N.K \times FLL\_FRATIO)$$

$F_{REF}$  is the input frequency, as determined by FLL\_CLK\_REF\_DIV.

$F_{VCO}$  must be in the range 90-100 MHz. Frequencies outside this range cannot be supported.

Note that the output frequencies that do not lie within the ranges quoted above cannot be guaranteed across the full range of device operating temperatures.

In order to follow the above requirements for  $F_{VCO}$ , the value of FLL\_OUTDIV should be selected according to the desired output  $F_{OUT}$ , as described in Table 40.

| OUTPUT FREQUENCY $F_{OUT}$ | FLL_OUTDIV        |
|----------------------------|-------------------|
| 2.8125 MHz - 3.125 MHz     | 4h (divide by 32) |
| 5.625 MHz - 6.25 MHz       | 3h (divide by 16) |
| 11.25 MHz - 12.5 MHz       | 2h (divide by 8)  |
| 22.5 MHz - 25 MHz          | 1h (divide by 4)  |

**Table 40 Selection of FLL\_OUTDIV**

The value of FLL\_FRATIO should be selected as described in Table 41.

| REFERENCE FREQUENCY $F_{REF}$ | FLL_FRATIO        |
|-------------------------------|-------------------|
| 1MHz - 13.5MHz                | 0h (divide by 1)  |
| 256kHz - 1MHz                 | 1h (divide by 2)  |
| 128kHz - 256kHz               | 2h (divide by 4)  |
| 64kHz - 128kHz                | 3h (divide by 8)  |
| Less than 64kHz               | 4h (divide by 16) |

**Table 41 Selection of FLL\_FRATIO**

In order to determine the remaining FLL parameters, the FLL operating frequency,  $F_{VCO}$ , must be calculated, as given by the following equation:

$$F_{VCO} = (F_{OUT} \times FLL\_OUTDIV)$$

The value of FLL\_N and FLL\_K can then be determined as follows:

$$N.K = F_{VCO} / (FLL\_FRATIO \times F_{REF})$$

Note that  $F_{REF}$  is the input frequency, after division by FLL\_CLK\_REF\_DIV, where applicable.

For best performance, FLL Fractional Mode should always be used. Therefore, if the calculations yield an integer value of N.K, then it is recommended to adjust FLL\_FRATIO in order to obtain a non-integer value of N.K.

The register fields that control the FLL are described in Table 42. Example settings for a variety of reference frequencies and output frequencies are shown in Table 43.

| REGISTER ADDRESS           | BIT  | LABEL               | DEFAULT | DESCRIPTION   |
|----------------------------|------|---------------------|---------|---|
| R16 (10h)<br>FLL Control 1 | 3    | FLL_HOLD            | 0       | FLL Hold Select<br>0 = Disabled<br>1 = Enabled<br><br>This feature enables free-running mode in FLL when reference clock is removed   |
|                            | 2    | FLL_FRAC            | 0       | Fractional enable<br>0 = Integer Mode<br>1 = Fractional Mode<br><br>Fractional Mode is recommended in all cases   |
|                            | 0    | FLL_ENA             | 0       | FLL Enable<br>0 = Disabled<br>1 = Enabled   |
| R17 (11h)<br>FLL Control 2 | 10:8 | FLL_OUTDIV [2:0]    | 010     | $F_{OUT}$ clock divider<br>000 = 2<br>001 = 4<br>010 = 8<br>011 = 16<br>100 = 32<br>101 = 64<br>110 = 128<br>111 = 256<br><br>( $F_{OUT} = F_{VCO} / FLL\_OUTDIV$ )   |
|                            | 6:4  | FLL_CTRL_RATE [2:0] | 000     | Frequency of the FLL control block<br>000 = $F_{VCO} / 1$ (Recommended value)<br>001 = $F_{VCO} / 2$<br>010 = $F_{VCO} / 3$<br>011 = $F_{VCO} / 4$<br>100 = $F_{VCO} / 5$<br>101 = $F_{VCO} / 6$<br>110 = $F_{VCO} / 7$<br>111 = $F_{VCO} / 8$<br><br>Recommended that this register is not changed from default. |

| REGISTER ADDRESS           | BIT  | LABEL                 | DEFAULT                      | DESCRIPTION  |
|----------------------------|------|-----------------------|------------------------------|--|
|                            | 2:0  | FLL_FRATIO [2:0]      | 000                          | <p><math>F_{VCO}</math> clock divider</p> <p>000 = 1<br/>001 = 2<br/>010 = 4<br/>011 = 8<br/>1XX = 16</p> <p>000 recommended for high <math>F_{REF}</math><br/>011 recommended for low <math>F_{REF}</math></p>  |
| R18 (12h)<br>FLL Control 3 | 15:0 | FLL_K[15:0]           | 0000_0000<br>_0000_0000<br>0 | Fractional multiply for $F_{REF}$<br>(MSB = 0.5)   |
| R19 (13h)<br>FLL Control 4 | 14:5 | FLL_N[9:0]            | 00_0001_0<br>000             | Integer multiply for $F_{REF}$<br>(LSB = 1)  |
|                            | 3:0  | FLL_GAIN [3:0]        | 0100                         | <p>Gain applied to error</p> <p>0000 = x 1 (Recommended value)<br/>0001 = x 2<br/>0010 = x 4<br/>0011 = x 8<br/>0100 = x 16<br/>0101 = x 32<br/>0110 = x 64<br/>0111 = x 128<br/>1000 = x 256</p> <p>Recommended that this register is not changed from default.</p>                               |
| R20 (14h)<br>FLL Control 5 | 4:3  | FLL_CLK_REF_DIV [1:0] | 00                           | <p>FLL Clock Reference Divider</p> <p>00 = MCLK / 1<br/>01 = MCLK / 2<br/>10 = MCLK / 4<br/>11 = MCLK / 8</p> <p>MCLK (or other input reference) must be divided down to <math>\leq 13.5</math>MHz.<br/>For lower power operation, the reference clock can be divided down further if desired.</p> |
|                            | 1:0  | FLL_CLK_SRC [1:0]     | 00                           | <p>FLL Clock source</p> <p>00 - BCLK<br/>01 - MCLK<br/>10 - LRCLK<br/>11 = Reserved</p>  |

**Table 42 FLL Register Map**



### FREE-RUNNING FLL CLOCK

The FLL can generate a clock signal even when no external reference is available. However, it should be noted that the accuracy of this clock is reduced, and a reference source should always be used where possible. Note that, in free-running modes, the FLL is not sufficiently accurate for hi-fi audio applications. However, the free-running modes are suitable for clocking other functions, including the Write Sequencer and Class D loudspeaker driver. The free-running mode can be used to support the analogue (DAC bypass) audio path.

A clock reference is required for initial configuration of the FLL as described above. For free-running operation, the FLL\_HOLD bit should be set, as described in Table 42. When FLL\_HOLD is set, the FLL will continue to generate a stable output clock after the reference input is stopped or disconnected.

### EXAMPLE FLL CALCULATION

To generate 12.288 MHz output ( $F_{OUT}$ ) from a 12.000 MHz reference clock ( $F_{REF}$ ):

- Set FLL\_CLK\_REF\_DIV in order to generate  $F_{REF} \leq 13.5\text{MHz}$ :  
FLL\_CLK\_REF\_DIV = 00 (divide by 1)
- Set FLL\_CTRL\_RATE to the recommended setting:  
FLL\_CTRL\_RATE = 000 (divide by 1)
- Set FLL\_GAIN to the recommended setting:  
FLL\_GAIN = 0000 (multiply by 1)
- Set FLL\_OUTDIV for the required output frequency as shown in Table 40:-  
 $F_{OUT} = 12.288\text{ MHz}$ , therefore FLL\_OUTDIV = 2h (divide by 8)
- Set FLL\_FRATIO for the given reference frequency as shown in Table 41:  
 $F_{REF} = 12\text{MHz}$ , therefore FLL\_FRATIO = 0h (divide by 1)
- Calculate  $F_{VCO}$  as given by  $F_{VCO} = F_{OUT} \times FLL\_OUTDIV$ :-  
 $F_{VCO} = 12.288 \times 8 = 98.304\text{MHz}$
- Calculate N.K as given by  $N.K = F_{VCO} / (FLL\_FRATIO \times F_{REF})$ :  
 $N.K = 98.304 / (1 \times 12) = 8.192$
- Determine FLL\_N and FLL\_K from the integer and fractional portions of N.K:-  
FLL\_N is 8. FLL\_K is 0.192
- Confirm that N.K is a fractional quantity and set FLL\_FRAC:  
N.K is fractional. Set FLL\_FRAC = 1.  
Note that, if N.K is an integer, then an alternative value of FLL\_FRATIO should be selected in order to produce a fractional value of N.K.

**EXAMPLE FLL SETTINGS**

Table 43 provides example FLL settings for generating common CLK\_SYS frequencies from a variety of low and high frequency reference inputs.

| F <sub>REF</sub> | F <sub>OUT</sub> | FLL_CLK_REF_DIV     | F <sub>VCO</sub> | FLL_N         | FLL_K               | FLL_FRATIO | FLL_OUTDIV | FLL_FRAC |
|------------------|------------------|---------------------|------------------|---------------|---------------------|------------|------------|----------|
| 32.000 kHz       | 12.288 MHz       | 0h<br>(divide by 1) | 98.304 MHz       | 384<br>(180h) | 0<br>(0000h)        | 8<br>(3h)  | 8<br>(2h)  | 0        |
| 32.000 kHz       | 11.2896 MHz      | 0h<br>(divide by 1) | 90.3168 MHz      | 352<br>(160h) | 0.8<br>(CCCCCh)     | 8<br>(3h)  | 8<br>(2h)  | 1        |
| 32.768 kHz       | 12.288 MHz       | 0h<br>(divide by 1) | 98.304 MHz       | 187<br>(0BBh) | 0.5<br>(8000h)      | 16<br>(4h) | 8<br>(2h)  | 1        |
| 32.768 kHz       | 11.288576 MHz    | 0h<br>(divide by 1) | 90.308608 MHz    | 344<br>(158h) | 0.5<br>(8000h)      | 8<br>(3h)  | 8<br>(2h)  | 1        |
| 32.768 kHz       | 11.2896 MHz      | 0h<br>(divide by 1) | 90.3168 MHz      | 344<br>(158h) | 0.53125<br>(8800h)  | 8<br>(3h)  | 8<br>(2h)  | 1        |
| 48 kHz           | 12.288 MHz       | 0h<br>(divide by 1) | 98.304 MHz       | 256<br>(100h) | 0<br>(0000h)        | 8<br>(3h)  | 8<br>(2h)  | 0        |
| 11.3636 MHz      | 12.368544 MHz    | 0h<br>(divide by 1) | 98.948354 MHz    | 8<br>(008h)   | 0.707483<br>(B51Dh) | 1<br>(0h)  | 8<br>(2h)  | 1        |
| 12.000 MHz       | 12.288 MHz       | 0h<br>(divide by 1) | 98.3040 MHz      | 8<br>(008h)   | 0.192<br>(3127h)    | 1<br>(0h)  | 8<br>(2h)  | 1        |
| 12.000 MHz       | 11.289597 MHz    | 0h<br>(divide by 1) | 90.3168 MHz      | 7<br>(007h)   | 0.526398<br>(86C2h) | 1<br>(0h)  | 8<br>(2h)  | 1        |
| 12.288 MHz       | 12.288 MHz       | 0h<br>(divide by 1) | 98.304 MHz       | 8<br>(008h)   | 0<br>(0000h)        | 1<br>(0h)  | 8<br>(2h)  | 0        |
| 12.288 MHz       | 11.2896 MHz      | 0h<br>(divide by 1) | 90.3168 MHz      | 7<br>(007h)   | 0.35<br>(599Ah)     | 1<br>(0h)  | 8<br>(2h)  | 1        |
| 13.000 MHz       | 12.287990 MHz    | 0h<br>(divide by 1) | 98.3040 MHz      | 7<br>(007h)   | 0.56184<br>(8FD5h)  | 1<br>(0h)  | 8<br>(2h)  | 1        |
| 13.000 MHz       | 11.289606 MHz    | 0h<br>(divide by 1) | 90.3168 MHz      | 6<br>(006h)   | 0.94745<br>(F28Ch)  | 1<br>(0h)  | 8<br>(2h)  | 1        |
| 19.200 MHz       | 12.287988 MHz    | 1h<br>(divide by 2) | 98.3039 MHz      | 5<br>(005h)   | 0.119995<br>(1EB8h) | 1<br>(0h)  | 8<br>(2h)  | 1        |
| 19.200 MHz       | 11.289588 MHz    | 1h<br>(divide by 2) | 90.3168 MHz      | 4<br>(004h)   | 0.703995<br>(B439h) | 1<br>(0h)  | 8<br>(2h)  | 1        |

**Table 43 Example FLL Settings**

**THERMAL SHUTDOWN**

The WM9081 incorporates a temperature sensor which detects when the device temperature is within normal limits or if the device is approaching a hazardous temperature condition. The TEMP\_SHUT flag can be polled at any time to determine the temperature status. The temperature status can also be indicated via the IRQ pin.

The temperature sensor is configured by default to automatically disable the audio outputs of the WM9081 in response to an over-temperature condition.

The temperature sensor is enabled when the TSENSE\_ENA register bit is set. When the TSHUT\_ENA bit is also set, then a device over-temperature condition will cause the speaker output to be disabled; this response is intended to prevent any damage to the device attributable to the large currents of the output drivers.

See "Interrupts" for details of hardware output of the Temperature Sensor status via the IRQ pin.

| REGISTER ADDRESS              | BIT | LABEL      | DEFAULT | DESCRIPTION  |
|-------------------------------|-----|------------|---------|--|
| R11 (0Bh)<br>Power Management | 8   | TSHUT_ENA  | 1       | Thermal shutdown control<br>(Causes audio outputs to be disabled if an over-temperature occurs. The thermal sensor must also be enabled.)<br>0 = Disabled<br>1 = Enabled |
|                               | 7   | TSENSE_ENA | 1       | Thermal sensor enable<br>0 = Disabled<br>1 = Enabled   |
|                               | 6   | TEMP_SHUT  | 0       | Thermal Sensor status (Read Only)<br>0 = Temperature limit not exceeded<br>1 = Temperature limit exceeded  |

**Table 44 Thermal Shutdown**

**INTERRUPTS**

The interrupt controller has two inputs; these are the Temperature Sensor and the Control Write Sequencer. Any combination of these inputs can be used to trigger an Interrupt (IRQ) event.

There is an Interrupt Status field associated with each of the IRQ inputs. These are listed within the Interrupt Status Register, R26 (1Ah), as described in Table 45. The status of the IRQ inputs can be read at any time from this register or else in response to the interrupt event being signalled via the IRQ pin.

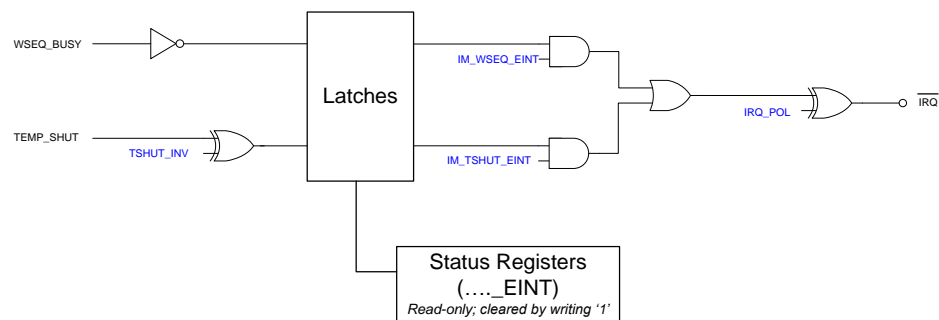
Individual mask bits can select or deselect different functions from the Interrupt controller. These are listed within the Interrupt Status Mask Register, R27 (1Bh), as described in Table 45. Note that the status fields remain valid, even when masked, but the masked bits will not cause the IRQ to be asserted.

The interrupt output represents the logical 'OR' of all the unmasked IRQ inputs. Each bit within the Interrupt Status register R26 (1Ah) is a latching bit - once it is set, it remains at logic 1 even if the trigger condition is cleared. The interrupt status bits are cleared by writing a logic 1 to the relevant register bit. Accordingly, the IRQ output is not reset until each of the unmasked IRQ inputs has been reset.

When the temperature sensor is used as an interrupt event, the polarity can be set using TSHUT\_INV. This allows the IRQ event to be used to indicate either the normal temperature condition or the over-temperature condition. Under default conditions (TSHUT\_INV = 0), the interrupt will be triggered in response to an over-temperature condition.

By default, the IRQ output is Active Low. The polarity can be inverted using IRQ\_POL. The IRQ output may be configured as either CMOS or Open-Drain type. In Open Drain mode, a logic 1 is asserted by tri-stating the IRQ pin, rather than pulling it high. An external pull-up resistor is required to pull the IRQ high so that the logic 1 can be recognised by another device.

The WM9081 Interrupt Controller circuit is illustrated in Figure 54. The associated control fields are described in Table 45. Note that CLK\_SYS is required for the interrupt circuit.



**Figure 54** Interrupt Controller

| REGISTER ADDRESS                   | BIT | LABEL             | DEFAULT | DESCRIPTION  |
|------------------------------------|-----|-------------------|---------|--|
| R26 (1Ah)<br>Interrupt Status      | 2   | WSEQ_BUSY_EINT    | 0       | Write Sequencer Interrupt<br>0 = Interrupt not set<br>1 = Interrupt is set<br><br>The Write Sequencer asserts this flag when it has completed a programmed sequence - ie it indicates that the Write Sequencer is NOT Busy. It is cleared when a '1' is written. |
|                                    | 0   | TSHUT_EINT        | 0       | Thermal Shutdown Interrupt<br>0 = Interrupt not set<br>1 = Interrupt is set<br><br>This flag is asserted a thermal shutdown condition has been detected. It is cleared when a '1' is written.  |
| R27 (1Bh)<br>Interrupt Status Mask | 2   | IM_WSEQ_BUSY_EINT | 1       | Write Sequencer interrupt mask<br>0 = do not mask interrupt<br>1 = mask interrupt  |
|                                    | 0   | IM_TSHUT_EINT     | 0       | Thermal Shutdown interrupt mask<br>0 = do not mask interrupt<br>1 = mask interrupt   |
| R28 (1Ch)<br>Interrupt Polarity    | 0   | TSHUT_INV         | 0       | Thermal Shutdown interrupt polarity<br>0 = active low (interrupt is triggered when temperature threshold is exceeded)<br>1 = active high (interrupt is triggered when temperature is normal)   |
| R29 (1Dh)<br>Interrupt Control     | 15  | IRQ_POL           | 0       | Interrupt output polarity<br>0 = Active low<br>1 = Active high   |
|                                    | 0   | IRQ_OP_CTRL       | 0       | IRQ Output pin configuration<br>0 = CMOS<br>1 = Open Drain   |

**Table 45 Interrupt Control**

**REFERENCE VOLTAGES AND MASTER BIAS**

This section describes the analogue reference voltage and bias current controls. It also describes the VMID soft-start circuit for pop suppressed start-up and shut-down. Note that, under the recommended usage conditions of the WM9081, these features will be configured by running the default control sequences as described in the “Control Write Sequencer” section. In these cases, the user does not need to set these register fields directly.

The analogue circuits in the WM9081 require a mid-rail analogue reference voltage, VMID. This reference is generated from AVDD via a programmable resistor chain. Together with the external VMID decoupling capacitor, the programmable resistor chain results in a slow, normal, or fast charging characteristic on VMID. This is controlled by VMID\_SEL[1:0], and can be used to optimise the reference for normal operation, low power standby or for fast start-up as described in Table 46.

The analogue circuits in the WM9081 require a bias current. The normal bias current is enabled by setting BIAS\_ENA. Note that the normal bias current source requires VMID to be enabled also.

| REGISTER ADDRESS           | BIT | LABEL          | DEFAULT | DESCRIPTION   |
|----------------------------|-----|----------------|---------|---|
| R4 (04h)<br>VMID Control   | 2:1 | VMID_SEL [1:0] | 00      | VMID Divider Enable and Select<br>00 = VMID disabled (for OFF mode)<br>01 = 2 x 40kΩ divider (for normal operation)<br>10 = 2 x 240kΩ divider (for low power standby)<br>11 = 2 x 5kΩ divider (for fast start-up) |
| R5 (05h)<br>Bias Control 1 | 1   | BIAS_ENA       | 0       | Enables the Normal bias current generator (for all analogue functions)<br>0 = Disabled<br>1 = Enabled   |

**Table 46 Reference Voltages and Master Bias Enable**

A pop-suppressed start-up requires VMID to be enabled smoothly, without the step change normally associated with the initial stage of the VMID capacitor charging. A pop-suppressed start-up also requires the analogue bias current to be enabled throughout the signal path prior to the VMID reference voltage being applied. The WM9081 incorporates pop-suppression circuits which address these requirements.

An alternate bias current source (Start-Up Bias) is provided for pop-free start-up; this is enabled by the STARTUP\_BIAS\_ENA register bit. The start-up bias is selected (in place of the normal bias) using the BIAS\_SRC bit. It is recommended that the start-up bias is used during start-up, before switching back to the higher quality, normal bias.

A soft-start circuit is provided in order to control the switch-on of the VMID reference. The soft-start control circuit offers two slew rates for enabling the VMID reference. The soft-start feature is selected by setting VMID\_RAMP; the slew rate is controlled by VMID\_FAST\_ST. When the soft-start circuit is enabled prior to enabling VMID\_SEL, the reference voltage rises smoothly, without the step change that would otherwise occur. It is recommended that the soft-start circuit and the output signal path be enabled before VMID is enabled by VMID\_SEL.

A soft shut-down is provided, using the soft-start control circuit and the start-up bias current generator. The soft shut-down of VMID is achieved by setting VMID\_RAMP, STARTUP\_BIAS\_ENA and BIAS\_SRC to select the start-up bias current and soft-start circuit prior to setting VMID\_SEL=00. The slew rate is controlled by VMID\_FAST\_ST.

The VMID soft-start register controls are defined in Table 47.

| REGISTER ADDRESS           | BIT | LABEL            | DEFAULT | DESCRIPTION  |
|----------------------------|-----|------------------|---------|--|
| R4 (04h)<br>VMID Control   | 3   | VMID_RAMP        | 0       | VMID Soft Start control<br>0 = Normal<br>1 = Soft Start                    |
|                            | 0   | VMID_FAST_ST     | 1       | VMID Slew Rate control<br>0 = Slow<br>1 = Fast                             |
| R5 (05h)<br>Bias Control 1 | 6   | BIAS_SRC         | 1       | Selects the bias current source<br>0 = Normal bias<br>1 = Start-Up bias    |
|                            | 0   | STARTUP_BIAS_ENA | 0       | Enables the Start-Up bias current generator<br>0 = Disabled<br>1 = Enabled |

**Table 47 Soft Start Control**

The master bias current is configurable using the BIAS\_LVL register. This enables power consumption to be reduced under selected operating conditions. The normal bias current is recommended for all active operating modes.

If a low power standby configuration is required, (for example, if the WM9081 is powered up and configured, but is not actually generating an audio output), then the master bias may be switched to a standby level, enabling further reduction in power consumption. The standby bias level is enabled using STBY\_BIAS\_ENA and is configured using STBY\_BIAS\_LVL, as described in Table 48.

| REGISTER ADDRESS           | BIT | LABEL          | DEFAULT | DESCRIPTION   |
|----------------------------|-----|----------------|---------|---|
| R5 (05h)<br>Bias Control 1 | 5   | STBY_BIAS_LVL  | 1       | Standby bias current select<br>0 = Normal bias x 0.5<br>1 = Normal bias x 0.25  |
|                            | 4   | STBY_BIAS_ENA  | 0       | Selects the Standby bias level<br>0 = Disabled (Bias set by BIAS_LVL)<br>1 = Enabled (Bias set by STBY_BIAS_LVL)              |
|                            | 3:2 | BIAS_LVL [1:0] | 10      | Master bias current select<br>00 = Normal bias x 0.5<br>01 = Normal bias x 0.75<br>10 = Normal bias<br>11 = Normal bias x 1.5 |

**Table 48 Master Bias Level Control**

**POWER MANAGEMENT**

The WM9081 has many control registers that allow users to select which functions are active. For minimum power consumption, unused functions should be disabled. To minimise pop or click noise, it is important to enable or disable functions in the correct order. Note that, under the recommended usage conditions of the WM9081, these features will be configured by running the default control sequences as described in the “Control Write Sequencer” section. In these cases, many of these register fields will be configured automatically.

| REGISTER ADDRESS              | BIT | LABEL          | DEFAULT | DESCRIPTION   |
|-------------------------------|-----|----------------|---------|---|
| R4 (04h)<br>VMID Control      | 2:1 | VMID_SEL [1:0] | 00      | VMID Divider Enable and Select<br>00 = VMID disabled (for OFF mode)<br>01 = 2 x 40kΩ divider (for normal operation)<br>10 = 2 x 240kΩ divider (for low power standby)<br>11 = 2 x 5kΩ divider (for fast start-up) |
| R5 (05h)<br>Bias Control 1    | 1   | BIAS_ENA       | 0       | Enables the Normal bias current generator (for all analogue functions)<br>0 = Disabled<br>1 = Enabled   |
| R11 (0Bh)<br>Power Management | 8   | TSHUT_ENA      | 1       | Thermal shutdown control (Causes audio outputs to be disabled if an over-temperature occurs. The thermal sensor must also be enabled.)<br>0 = Disabled<br>1 = Enabled   |
|                               | 7   | TSENSE_ENA     | 1       | Thermal sensor enable<br>0 = Disabled<br>1 = Enabled  |
|                               | 4   | LINEOUT_ENA    | 0       | LINEOUT Enable<br>0 = Disabled<br>1 = Enabled   |
|                               | 2   | SPKPGA_ENA     | 0       | Speaker PGA Enable<br>0 = Disabled<br>1 = Enabled   |
|                               | 1   | SPK_ENA        | 0       | Speaker Output Enable<br>0 = Disabled<br>1 = Enabled  |
|                               | 0   | DAC_ENA        | 0       | DAC Enable<br>0 = Disabled<br>1 = Enabled   |
| R14 (0Eh)<br>Clock Control 3  | 5   | CLK_OP_ENA     | 0       | Clock Output Enable<br>0 = Disabled<br>1 = Enabled<br>This bit enables OPCLK output on the MCLK pin.<br>Frequency is set by CLK_OP_DIV.   |
|                               | 2   | CLK_TO_ENA     | 0       | TOCLK (timeout/ slow clock) Enable<br>0 = Disabled<br>1 = Enabled   |
|                               | 1   | CLK_DSP_ENA    | 0       | CLK_DSP enable<br>0 = Disabled<br>1 = Enabled   |



| REGISTER ADDRESS               | BIT | LABEL       | DEFAULT | DESCRIPTION  |
|--------------------------------|-----|-------------|---------|--|
|                                | 0   | CLK_SYS_ENA | 0       | CLK_SYS enable<br>0 = Disabled<br>1 = Enabled          |
| R16 (10h)<br>FLL Control 1     | 0   | FLL_ENA     | 0       | FLL Enable<br>0 = Disabled<br>1 = Enabled              |
| R32 (20h)<br>DRC1              | 15  | DRC_ENA     | 0       | DRC enable<br>0 = Disabled<br>1 = Enabled              |
| R38 (26h)<br>Write Sequencer 1 | 15  | WSEQ_ENA    | 0       | Write Sequencer Enable.<br>0 = Disabled<br>1 = Enabled |
| R42 (2Ah)<br>EQ1               | 0   | EQ_ENA      | 0       | EQ Enable<br>0 = Disabled<br>1 = Enabled               |

**Table 49 Power Management**

## CHIP RESET AND ID

The device ID can be read back from register 0. Writing to this register will reset the device.

| REGISTER ADDRESS           | BIT  | LABEL                | DEFAULT | DESCRIPTION   |
|----------------------------|------|----------------------|---------|---|
| R0 (00h)<br>Software Reset | 15:0 | SW_RST_DEV_ID [15:0] | 9081h   | Writing to this register resets all registers to their default state.<br>Reading from this register will indicate device family ID 9081h. |

**Table 50 Chip Reset and ID**

## REGISTER MAP

| Reg       | Name                     | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8                   | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Default |      |      |
|-----------|--------------------------|----|----|----|----|----|----|---|---------------------|---|---|---|---|---|---|---|---|---------|------|------|
| R0 (0h)   | Software Reset           |    |    |    |    |    |    |   | SW_RST_DEV_ID[15:0] |   |   |   |   |   |   |   |   |         | 0    | 000h |
| R2 (2h)   | Analogue Lineout         | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 008h    |      |      |
| R3 (3h)   | Analogue Speaker<br>PGA  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 008h    |      |      |
| R4 (4h)   | VIMD Control             | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 000h    |      |      |
| R5 (5h)   | Bias Control 1           | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 008h    |      |      |
| R7 (7h)   | Analogue Mixer           | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 000h    |      |      |
| R8 (8h)   | Anti Pop Control         | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 000h    |      |      |
| R9 (9h)   | Analogue Speaker<br>1    | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 000h    |      |      |
| R10 (Ah)  | Analogue Speaker<br>2    | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 018h    |      |      |
| R11 (Bh)  | Power<br>Management      | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 018h    |      |      |
| R12 (Ch)  | Clock Control 1          | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 000h    |      |      |
| R13 (Dh)  | Clock Control 2          | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 003h    |      |      |
| R14 (Eh)  | Clock Control 3          | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 000h    |      |      |
| R16 (10h) | FLL Control 1            | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 000h    |      |      |
| R17 (11h) | FLL Control 2            | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 020h    |      |      |
| R18 (12h) | FLL Control 3            |    |    |    |    |    |    |   | FLL_N[15:0]         |   |   |   |   |   |   |   |   |         | 000h |      |
| R19 (13h) | FLL Control 4            |    |    |    |    |    |    |   | FLL_N9[0]           |   |   |   |   |   |   |   |   |         | 024h |      |
| R20 (14h) | FLL Control 5            | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 000h    |      |      |
| R22 (16h) | Audio Interface 1        | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 000h    |      |      |
| R23 (17h) | Audio Interface 2        | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 000h    |      |      |
| R24 (18h) | Audio Interface 3        | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 000h    |      |      |
| R25 (19h) | Audio Interface 4        | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 002h    |      |      |
| R26 (1Ah) | Interrupt Status         | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 000h    |      |      |
| R27 (1Bh) | Interrupt Status<br>Mask | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 006h    |      |      |
| R28 (1Ch) | Interrupt Polarity       | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 000h    |      |      |
| R29 (1Dh) | Interrupt Control        | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 000h    |      |      |
| R30 (1Eh) | DAC Digital 1            | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00C2h   |      |      |
| R31 (1Fh) | DAC Digital 2            | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 000h    |      |      |
| R32 (20h) | DRC1                     | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 006Fh   |      |      |
| R33 (21h) | DRC2                     |    |    |    |    |    |    |   | DRC_ATK[3:0]        |   |   |   |   |   |   |   |   |         | 421h |      |
| R34 (22h) | DRC3                     | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 000h    |      |      |
| R35 (23h) | DRC4                     | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 000h    |      |      |
| R38 (26h) | Write Sequencer 1        | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 000h    |      |      |
| R39 (27h) | Write Sequencer 2        | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 000h    |      |      |

| Reg       | Name       | 15             | 14 | 13             | 12 | 11             | 10 | 9              | 8 | 7              | 6 | 5              | 4        | 3              | 2 | 1              | 0 | Default |
|-----------|------------|----------------|----|----------------|----|----------------|----|----------------|---|----------------|---|----------------|----------|----------------|---|----------------|---|---------|
| R40 (28h) | MW Slave 1 | 0              | 0  | 0              | 0  | 0              | 0  | 0              | 0 | 0              | 0 | SPL_CFG        | SPL_WIRE | ARL_ENA        | 0 | AUTO_INC       | 0 | 002h    |
| R42 (29h) | EQ 1       | EQ_B1_GAN[F:0] |    | EQ_B1_GAN[F:0] |    | EQ_B2_GAN[F:0] |    | EQ_B2_GAN[F:0] |   | EQ_B3_GAN[F:0] |   | EQ_B3_GAN[F:0] |          | EQ_B3_GAN[F:0] |   | EQ_ENA         |   | 000h    |
| R43 (29h) | EQ 2       | EQ_B4_GAN[F:0] |    | EQ_B4_GAN[F:0] |    | EQ_B5_GAN[F:0] |    | EQ_B5_GAN[F:0] |   | EQ_B5_GAN[F:0] |   | EQ_B5_GAN[F:0] |          | EQ_B5_GAN[F:0] |   | EQ_B5_GAN[F:0] |   | 000h    |
| R44 (2Ch) | EQ 3       | EQ_B1_A[15:0]  |    | EQ_B1_A[15:0]  |    | EQ_B1_B[15:0]  |    | EQ_B1_B[15:0]  |   | EQ_B1_PG[15:0] |   | EQ_B2_A[15:0]  |          | EQ_B2_A[15:0]  |   | EQ_B2_B[15:0]  |   | 0FC4h   |
| R45 (2Dh) | EQ 4       | EQ_B1_B[15:0]  |    | EQ_B1_B[15:0]  |    | EQ_B1_PG[15:0] |    | EQ_B2_A[15:0]  |   | EQ_B2_A[15:0]  |   | EQ_B2_B[15:0]  |          | EQ_B2_C[15:0]  |   | EQ_B2_C[15:0]  |   | 040h    |
| R46 (2Eh) | EQ 5       | EQ_B2_A[15:0]  |    | EQ_B2_A[15:0]  |    | EQ_B2_B[15:0]  |    | EQ_B2_B[15:0]  |   | EQ_B2_C[15:0]  |   | EQ_B2_PG[15:0] |          | EQ_B3_A[15:0]  |   | EQ_B3_A[15:0]  |   | 00Bh    |
| R47 (2Fh) | EQ 6       | EQ_B3_B[15:0]  |    | EQ_B3_B[15:0]  |    | EQ_B3_C[15:0]  |    | EQ_B3_C[15:0]  |   | EQ_B3_PG[15:0] |   | EQ_B4_A[15:0]  |          | EQ_B4_A[15:0]  |   | EQ_B4_B[15:0]  |   | 1E8h    |
| R48 (30h) | EQ 7       | EQ_B4_A[15:0]  |    | EQ_B4_A[15:0]  |    | EQ_B4_B[15:0]  |    | EQ_B4_B[15:0]  |   | EQ_B4_C[15:0]  |   | EQ_B4_PG[15:0] |          | EQ_B5_A[15:0]  |   | EQ_B5_A[15:0]  |   | F45h    |
| R49 (31h) | EQ 8       | EQ_B5_A[15:0]  |    | EQ_B5_A[15:0]  |    | EQ_B5_B[15:0]  |    | EQ_B5_B[15:0]  |   | EQ_B5_C[15:0]  |   | EQ_B5_PG[15:0] |          | EQ_B5_PG[15:0] |   | EQ_B5_PG[15:0] |   | 0B7h    |
| R50 (32h) | EQ 9       | EQ_B5_PG[15:0] |    | EQ_B5_PG[15:0] |    | EQ_B5_PG[15:0] |    | EQ_B5_PG[15:0] |   | EQ_B5_PG[15:0] |   | EQ_B5_PG[15:0] |          | EQ_B5_PG[15:0] |   | EQ_B5_PG[15:0] |   | 01C5h   |
| R51 (33h) | EQ 10      | EQ_B5_PG[15:0] |    | EQ_B5_PG[15:0] |    | EQ_B5_PG[15:0] |    | EQ_B5_PG[15:0] |   | EQ_B5_PG[15:0] |   | EQ_B5_PG[15:0] |          | EQ_B5_PG[15:0] |   | EQ_B5_PG[15:0] |   | 1B8Eh   |
| R52 (34h) | EQ 11      | EQ_B5_PG[15:0] |    | EQ_B5_PG[15:0] |    | EQ_B5_PG[15:0] |    | EQ_B5_PG[15:0] |   | EQ_B5_PG[15:0] |   | EQ_B5_PG[15:0] |          | EQ_B5_PG[15:0] |   | EQ_B5_PG[15:0] |   | F82h    |
| R53 (35h) | EQ 12      | EQ_B5_PG[15:0] |    | EQ_B5_PG[15:0] |    | EQ_B5_PG[15:0] |    | EQ_B5_PG[15:0] |   | EQ_B5_PG[15:0] |   | EQ_B5_PG[15:0] |          | EQ_B5_PG[15:0] |   | EQ_B5_PG[15:0] |   | 07ADh   |
| R54 (36h) | EQ 13      | EQ_B5_PG[15:0] |    | EQ_B5_PG[15:0] |    | EQ_B5_PG[15:0] |    | EQ_B5_PG[15:0] |   | EQ_B5_PG[15:0] |   | EQ_B5_PG[15:0] |          | EQ_B5_PG[15:0] |   | EQ_B5_PG[15:0] |   | 1103h   |
| R55 (37h) | EQ 14      | EQ_B5_PG[15:0] |    | EQ_B5_PG[15:0] |    | EQ_B5_PG[15:0] |    | EQ_B5_PG[15:0] |   | EQ_B5_PG[15:0] |   | EQ_B5_PG[15:0] |          | EQ_B5_PG[15:0] |   | EQ_B5_PG[15:0] |   | 1C8Bh   |
| R56 (38h) | EQ 15      | EQ_B5_PG[15:0] |    | EQ_B5_PG[15:0] |    | EQ_B5_PG[15:0] |    | EQ_B5_PG[15:0] |   | EQ_B5_PG[15:0] |   | EQ_B5_PG[15:0] |          | EQ_B5_PG[15:0] |   | EQ_B5_PG[15:0] |   | F373h   |
| R57 (39h) | EQ 16      | EQ_B5_PG[15:0] |    | EQ_B5_PG[15:0] |    | EQ_B5_PG[15:0] |    | EQ_B5_PG[15:0] |   | EQ_B5_PG[15:0] |   | EQ_B5_PG[15:0] |          | EQ_B5_PG[15:0] |   | EQ_B5_PG[15:0] |   | 04C4h   |
| R58 (3Ah) | EQ 17      | EQ_B5_PG[15:0] |    | EQ_B5_PG[15:0] |    | EQ_B5_PG[15:0] |    | EQ_B5_PG[15:0] |   | EQ_B5_PG[15:0] |   | EQ_B5_PG[15:0] |          | EQ_B5_PG[15:0] |   | EQ_B5_PG[15:0] |   | 058Bh   |
| R59 (3Bh) | EQ 18      | EQ_B5_PG[15:0] |    | EQ_B5_PG[15:0] |    | EQ_B5_PG[15:0] |    | EQ_B5_PG[15:0] |   | EQ_B5_PG[15:0] |   | EQ_B5_PG[15:0] |          | EQ_B5_PG[15:0] |   | EQ_B5_PG[15:0] |   | 0564h   |
| R60 (3Ch) | EQ 19      | EQ_B5_PG[15:0] |    | EQ_B5_PG[15:0] |    | EQ_B5_PG[15:0] |    | EQ_B5_PG[15:0] |   | EQ_B5_PG[15:0] |   | EQ_B5_PG[15:0] |          | EQ_B5_PG[15:0] |   | EQ_B5_PG[15:0] |   | 058Bh   |
| R61 (3Dh) | EQ 20      | EQ_B5_PG[15:0] |    | EQ_B5_PG[15:0] |    | EQ_B5_PG[15:0] |    | EQ_B5_PG[15:0] |   | EQ_B5_PG[15:0] |   | EQ_B5_PG[15:0] |          | EQ_B5_PG[15:0] |   | EQ_B5_PG[15:0] |   | 400h    |

**REGISTER BITS BY ADDRESS**

| REGISTER ADDRESS           | BIT  | LABEL                | DEFAULT | DESCRIPTION   | REFER TO         |
|----------------------------|------|----------------------|---------|---|------------------|
| R0 (00h)<br>Software Reset | 15:0 | SW_RST_DEV_ID1[15:0] | 9081h   | Writing to this register resets all registers to their default state.<br>Reading from this register will indicate device family ID 9081h. | Power Management |

**Register 00h** Software Reset

| REGISTER ADDRESS             | BIT | LABEL            | DEFAULT | DESCRIPTION  | REFER TO            |
|------------------------------|-----|------------------|---------|--|---------------------|
| R2 (02h)<br>Analogue Lineout | 7   | LINEOUT_MUTE     | 1       | LINEOUT Mute<br>0 = Un-mute<br>1 = Mute  | Signal Path Control |
|                              | 6   | LINEOUTZC        | 0       | LINEOUT Zero Cross Detection<br>0 = Change gain immediately<br>1 = Change gain on zero cross only    | Signal Path Control |
|                              | 5:0 | LINEOUT_VOL[5:0] | 11_1001 | LINEOUT Volume<br>00 0000 = -57dB<br>00 0001 = -56dB<br>...<br>11 1001 = 0dB<br>...<br>11 1111 = 6dB | Signal Path Control |

**Register 02h** Analogue Lineout

| REGISTER ADDRESS                 | BIT | LABEL           | DEFAULT | DESCRIPTION  | REFER TO            |
|----------------------------------|-----|-----------------|---------|--|---------------------|
| R3 (03h)<br>Analogue Speaker PGA | 7   | SPKPGA_MUTE     | 1       | Speaker PGA Mute<br>0 = Un-mute<br>1 = Mute  | Signal Path Control |
|                                  | 6   | SPKPGAZC        | 0       | Speaker PGA Zero Cross Detection<br>0 = Change gain immediately<br>1 = Change gain on zero cross only    | Signal Path Control |
|                                  | 5:0 | SPKPGA_VOL[5:0] | 11_1001 | Speaker PGA Volume<br>00 0000 = -57dB<br>00 0001 = -56dB<br>...<br>11 1001 = 0dB<br>...<br>11 1111 = 6dB | Signal Path Control |

**Register 03h** Analogue Speaker PGA

| REGISTER ADDRESS         | BIT | LABEL        | DEFAULT | DESCRIPTION   | REFER TO                |
|--------------------------|-----|--------------|---------|---|-------------------------|
| R4 (04h)<br>VMID Control | 5   | VMID_BUF_ENA | 0       | Enables VMID reference for lineout and inputs clamps<br>0 = Disabled<br>1 = Enabled | Pop Suppression Control |
|                          | 3   | VMID_RAMP    | 0       | VMID Soft Start control   | Reference Voltages and  |

| REGISTER ADDRESS | BIT | LABEL         | DEFAULT | DESCRIPTION   | REFER TO   |
|------------------|-----|---------------|---------|---|--|
|                  |     |               |         | 0 = Normal<br>1 = Soft Start  | master bias  |
|                  | 2:1 | VMID_SEL[1:0] | 00      | VMID Divider Enable and Select<br>00 = VMID disabled (for OFF mode)<br>01 = 2 x 40kΩ divider (for normal operation)<br>10 = 2 x 240kΩ divider (for low power standby)<br>11 = 2 x 5kΩ divider (for fast start-up) | Reference Voltages and master bias<br><br>Power Management |
|                  | 0   | VMID_FAST_ST  | 1       | VMID Slew Rate control<br>0 = Slow<br>1 = Fast  | Reference Voltages and master bias                         |

**Register 04h** VMID Control

| REGISTER ADDRESS        | BIT | LABEL            | DEFAULT | DESCRIPTION   | REFER TO   |
|-------------------------|-----|------------------|---------|---|--|
| R5 (05h) Bias Control 1 | 6   | BIAS_SRC         | 1       | Selects the bias current source<br>0 = Normal bias<br>1 = Start-Up bias   | Reference Voltages and master bias                         |
|                         | 5   | STBY_BIAS_LVL    | 1       | Standby bias current select<br>0 = Normal bias x 0.5<br>1 = Normal bias x 0.25  | Reference Voltages and master bias                         |
|                         | 4   | STBY_BIAS_ENA    | 0       | Selects the Standby bias level<br>0 = Disabled (Bias set by BIAS_LVL)<br>1 = Enabled (Bias set by STBY_BIAS_LVL)              | Reference Voltages and master bias                         |
|                         | 3:2 | BIAS_LVL[1:0]    | 10      | Master bias current select<br>00 = Normal bias x 0.5<br>01 = Normal bias x 0.75<br>10 = Normal bias<br>11 = Normal bias x 1.5 | Reference Voltages and master bias                         |
|                         | 1   | BIAS_ENA         | 0       | Enables the Normal bias current generator (for all analogue functions)<br>0 = Disabled<br>1 = Enabled                         | Reference Voltages and master bias<br><br>Power Management |
|                         | 0   | STARTUP_BIAS_ENA | 0       | Enables the Start-Up bias current generator<br>0 = Disabled<br>1 = Enabled  | Reference Voltages and master bias                         |

**Register 05h** Bias Control 1

| REGISTER ADDRESS        | BIT | LABEL   | DEFAULT | DESCRIPTION                                    | REFER TO            |
|-------------------------|-----|---------|---------|--|---------------------|
| R7 (07h) Analogue Mixer | 4   | DAC_SEL | 0       | DAC Path Enable<br>0 = Disabled<br>1 = Enabled | Signal Path Control |
|                         | 3   | IN2_VOL | 0       | IN2 Volume Control<br>0 = 0dB<br>1 = -6dB      | Signal Path Control |
|                         | 2   | IN2_ENA | 0       | IN2 Path Enable<br>0 = Disabled<br>1 = Enabled | Signal Path Control |

| REGISTER ADDRESS | BIT | LABEL   | DEFAULT | DESCRIPTION                                    | REFER TO            |
|------------------|-----|---------|---------|--|---------------------|
|                  | 1   | IN1_VOL | 0       | IN1 Volume Control<br>0 = 0dB<br>1 = -6dB      | Signal Path Control |
|                  | 0   | IN1_ENA | 0       | IN1 Path Enable<br>0 = Disabled<br>1 = Enabled | Signal Path Control |

**Register 07h** Analogue Mixer

| REGISTER ADDRESS          | BIT | LABEL          | DEFAULT | DESCRIPTION  | REFER TO                |
|---------------------------|-----|----------------|---------|--|-------------------------|
| R8 (08h) Anti Pop Control | 2   | LINEOUT_DISC H | 0       | Discharges LINEOUT via approx 5kohm resistor<br>0 = Not active<br>1 = Actively discharging LINEOUT   | Pop Suppression Control |
|                           | 1   | LINEOUT_VROI   | 0       | Buffered VMID to LINEOUT Resistance. This applies when LINEOUT_ENA = 0 and LINEOUT_CLAMP = 1.<br>0 = 20kΩ from buffered VMID to output<br>1 = 500Ω from buffered VMID to output                            | Pop Suppression Control |
|                           | 0   | LINEOUT_CLAMP  | 0       | Clamp LINEOUT to buffered VMID. VMID_BUF_ENA must be set. This bit is only effective when LINEOUT_ENA = 0. The resistance is set by LINEOUT_VROI.<br>0 = Disabled<br>1 = Enabled (LINEOUT clamped to VMID) | Pop Suppression Control |

**Register 08h** Anti Pop Control

| REGISTER ADDRESS            | BIT | LABEL           | DEFAULT      | DESCRIPTION  | REFER TO         |
|-----------------------------|-----|-----------------|--------------|--|------------------|
| R9 (09h) Analogue Speaker 1 | 5:3 | SPK_DCGAIN[2:0] | 011 (+3.6dB) | Speaker Output DC Gain<br>000 = x1 boost (0dB)<br>001 = x1.27 boost(2.1dB)<br>010 = x1.4 boost (2.9dB)<br>011 = x1.52 boost (3.6dB)<br>100 = x1.67 boost (4.5dB)<br>101 = x1.8 boost (5.1dB)<br>110-111 = Reserved | Analogue Outputs |
|                             | 2:0 | SPK_ACGAIN[2:0] | 011 (+3.6dB) | Speaker Output AC Gain<br>000 = x1 boost (0dB)<br>001 = x1.27 boost(2.1dB)<br>010 = x1.4 boost (2.9dB)<br>011 = x1.52 boost (3.6dB)<br>100 = x1.67 boost (4.5dB)<br>101 = x1.8 boost (5.1dB)<br>110-111 = Reserved | Analogue Outputs |

**Register 09h** Analogue Speaker 1

| REGISTER ADDRESS             | BIT | LABEL    | DEFAULT | DESCRIPTION  | REFER TO         |
|------------------------------|-----|----------|---------|--|------------------|
| R10 (0Ah) Analogue Speaker 2 | 6   | SPK_MODE | 0       | Speaker Mode Select<br>0 = Class D mode<br>1 = Class AB mode | Analogue Outputs |

| REGISTER ADDRESS | BIT | LABEL        | DEFAULT | DESCRIPTION  | REFER TO            |
|------------------|-----|--------------|---------|--|---------------------|
|                  | 4   | SPK_INV_MUTE | 1       | Controls a pop-suppression circuit for Speaker start-up. Controlled automatically by SPK_ENA in Class D mode. Must be set to 0 before enabling SPK_ENA in Class AB mode.<br>0 = Normal operation<br>1 = SPK_INV_MUTE enabled | Signal Path Control |
|                  | 3   | OUT_SPK_CTRL | 1       | Controls a pop-suppression circuit for Speaker start-up. Controlled automatically by SPK_ENA in Class D mode. Must be set to 0 before enabling SPK_ENA in Class AB mode.<br>0 = Normal operation<br>1 = OUT_SPK_CTRL enabled | Signal Path Control |

**Register 0Ah** Analogue Speaker 2

| REGISTER ADDRESS              | BIT | LABEL       | DEFAULT | DESCRIPTION  | REFER TO  |
|-------------------------------|-----|-------------|---------|--|---|
| R11 (0Bh)<br>Power Management | 8   | TSHUT_ENA   | 1       | Thermal shutdown control<br>(Causes audio outputs to be disabled if an over-temperature occurs. The thermal sensor must also be enabled.)<br>0 = Disabled<br>1 = Enabled | Thermal Shutdown<br><br>Power Management                    |
|                               | 7   | TSENSE_ENA  | 1       | Thermal sensor enable<br>0 = Disabled<br>1 = Enabled   | Thermal Shutdown<br><br>Power Management                    |
|                               | 6   | TEMP_SHUT   | 0       | Thermal Sensor status (Read Only)<br>0 = Temperature limit not exceeded<br>1 = Temperature limit exceeded  | Thermal Shutdown  |
|                               | 4   | LINEOUT_ENA | 0       | LINEOUT Enable<br>0 = Disabled<br>1 = Enabled  | Signal Path Control<br><br>Power Management                 |
|                               | 2   | SPKPGA_ENA  | 0       | Speaker PGA Enable<br>0 = Disabled<br>1 = Enabled  | Signal Path Control<br><br>Power Management                 |
|                               | 1   | SPK_ENA     | 0       | Speaker Output Enable<br>0 = Disabled<br>1 = Enabled   | Signal Path Control<br><br>Power Management                 |
|                               | 0   | DAC_ENA     | 0       | DAC Enable<br>0 = Disabled<br>1 = Enabled  | Digital to Analogue Converter (DAC)<br><br>Power Management |

**Register 0Bh** Power Management

| REGISTER ADDRESS             | BIT   | LABEL           | DEFAULT | DESCRIPTION   | REFER TO                  |
|------------------------------|-------|-----------------|---------|---|---------------------------|
| R12 (0Ch)<br>Clock Control 1 | 12:10 | CLK_OP_DIV[2:0] | 000     | OPCLK Clock Divider<br>000 = CLK_SYS<br>001 = CLK_SYS / 2<br>010 = CLK_SYS / 3<br>011 = CLK_SYS / 4<br>100 = CLK_SYS / 6<br>101 = CLK_SYS / 8<br>110 = CLK_SYS / 12<br>111 = CLK_SYS / 16 | Clocking and Sample Rates |
|                              | 9:8   | CLK_TO_DIV[1:0] | 00      | TOCLK (timeout/ slow clock) frequency select<br>00 = 125Hz<br>01 = 250Hz<br>10 = 500Hz<br>11 = 1kHz   | Clocking and Sample Rates |
|                              | 7     | MCLKDIV2        | 0       | MCLK Divider<br>0 = MCLK<br>1 = MCLK / 2  | Clocking and Sample Rates |

**Register 0Ch** Clock Control 1

| REGISTER ADDRESS             | BIT | LABEL             | DEFAULT | DESCRIPTION   | REFER TO                  |
|------------------------------|-----|-------------------|---------|---|---------------------------|
| R13 (0Dh)<br>Clock Control 2 | 7:4 | CLK_SYS_RATE[3:0] | 0011    | Selects the CLK_SYS / fs ratio<br>0000 = 64<br>0001 = 128<br>0010 = 192<br>0011 = 256<br>0100 = 384<br>0101 = 512<br>0110 = 768<br>0111 = 1024<br>1000 = 1408<br>1001 = 1536  | Clocking and Sample Rates |
|                              | 3:0 | SAMPLE_RATE[3:0]  | 1000    | Selects the Sample Rate (fs)<br>0000 = 8kHz<br>0001 = 11.025kHz<br>0010 = 12kHz<br>0011 = 16kHz<br>0100 = 22.05kHz<br>0101 = 24kHz<br>0110 = 32kHz<br>0111 = 44.1kHz<br>1000 = 48kHz<br>1001 = 88.2kHz<br>1010 = 96kHz<br>1011 to 1111 = Reserved | Clocking and Sample Rates |

**Register 0Dh** Clock Control 2

| REGISTER ADDRESS           | BIT | LABEL       | DEFAULT | DESCRIPTION           | REFER TO            |
|----------------------------|-----|-------------|---------|-----------------------|---------------------|
| R14 (0Eh)<br>Clock Control | 13  | CLK_SRC_SEL | 0       | CLK_SYS Source Select | Clocking and Sample |



| REGISTER ADDRESS | BIT | LABEL       | DEFAULT | DESCRIPTION   | REFER TO  |
|------------------|-----|-------------|---------|---|---|
| 3                |     |             |         | 0 = MCLK<br>1 = FLL output  | Rates   |
|                  | 5   | CLK_OP_ENA  | 0       | Clock Output Enable<br>0 = Disabled<br>1 = Enabled<br>This bit enables OPCLK output on the MCLK pin.<br>Frequency is set by CLK_OP_DIV. | Clocking and Sample Rates<br><br>Power Management |
|                  | 2   | CLK_TO_ENA  | 0       | TOCLK (timeout/ slow clock) Enable<br>0 = Disabled<br>1 = Enabled   | Clocking and Sample Rates<br><br>Power Management |
|                  | 1   | CLK_DSP_ENA | 0       | CLK_DSP enable<br>0 = Disabled<br>1 = Enabled   | Clocking and Sample Rates<br><br>Power Management |
|                  | 0   | CLK_SYS_ENA | 0       | CLK_SYS enable<br>0 = Disabled<br>1 = Enabled   | Clocking and Sample Rates<br><br>Power Management |

**Register 0Eh** Clock Control 3

| REGISTER ADDRESS           | BIT | LABEL    | DEFAULT | DESCRIPTION   | REFER TO  |
|----------------------------|-----|----------|---------|---|---|
| R16 (10h)<br>FLL Control 1 | 3   | FLL_HOLD | 0       | FLL Hold Select<br>0 = Disabled<br>1 = Enabled<br>This feature enables free-running mode in FLL when reference clock is removed | Clocking and Sample Rates                         |
|                            | 2   | FLL_FRAC | 0       | Fractional enable<br>0 = Integer Mode<br>1 = Fractional Mode<br><br>Fractional Mode is recommended in all cases                 | Clocking and Sample Rates                         |
|                            | 0   | FLL_ENA  | 0       | FLL Enable<br>0 = Disabled<br>1 = Enabled   | Clocking and Sample Rates<br><br>Power Management |

**Register 10h** FLL Control 1

| REGISTER ADDRESS           | BIT  | LABEL           | DEFAULT | DESCRIPTION  | REFER TO                  |
|----------------------------|------|-----------------|---------|--|---------------------------|
| R17 (11h)<br>FLL Control 2 | 10:8 | FLL_OUTDIV[2:0] | 010     | F <sub>OUT</sub> clock divider<br>000 = 2<br>001 = 4 | Clocking and Sample Rates |

| REGISTER ADDRESS | BIT | LABEL              | DEFAULT | DESCRIPTION   | REFER TO                  |
|------------------|-----|--------------------|---------|---|---------------------------|
|                  |     |                    |         | 010 = 8<br>011 = 16<br>100 = 32<br>101 = 64<br>110 = 128<br>111 = 256<br><br>$(F_{OUT} = F_{VCO} / FLL\_OUTDIV)$  |                           |
|                  | 6:4 | FLL_CTRL_RATE[2:0] | 000     | Frequency of the FLL control block<br>000 = $F_{VCO} / 1$ (Recommended value)<br>001 = $F_{VCO} / 2$<br>010 = $F_{VCO} / 3$<br>011 = $F_{VCO} / 4$<br>100 = $F_{VCO} / 5$<br>101 = $F_{VCO} / 6$<br>110 = $F_{VCO} / 7$<br>111 = $F_{VCO} / 8$<br><br>Recommended that this register is not changed from default. | Clocking and Sample Rates |
|                  | 2:0 | FLL_FRATIO[2:0]    | 000     | $F_{VCO}$ clock divider<br>000 = 1<br>001 = 2<br>010 = 4<br>011 = 8<br>1XX = 16<br><br>000 recommended for high $F_{REF}$<br>011 recommended for low $F_{REF}$  | Clocking and Sample Rates |

**Register 11h FLL Control 2**

| REGISTER ADDRESS           | BIT  | LABEL       | DEFAULT                      | DESCRIPTION                                      | REFER TO                  |
|----------------------------|------|-------------|------------------------------|--|---------------------------|
| R18 (12h)<br>FLL Control 3 | 15:0 | FLL_K[15:0] | 0000_0000<br>_0000_0000<br>0 | Fractional multiply for $F_{REF}$<br>(MSB = 0.5) | Clocking and Sample Rates |

**Register 12h FLL Control 3**

| REGISTER ADDRESS           | BIT  | LABEL         | DEFAULT          | DESCRIPTION  | REFER TO                  |
|----------------------------|------|---------------|------------------|--|---------------------------|
| R19 (13h)<br>FLL Control 4 | 14:5 | FLL_N[9:0]    | 00_0001_0<br>000 | Integer multiply for $F_{REF}$<br>(LSB = 1)  | Clocking and Sample Rates |
|                            | 3:0  | FLL_GAIN[3:0] | 0100             | Gain applied to error<br>0000 = x 1 (Recommended value)<br>0001 = x 2<br>0010 = x 4<br>0011 = x 8<br>0100 = x 16<br>0101 = x 32<br>0110 = x 64 | Clocking and Sample Rates |

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION   | REFER TO |
|------------------|-----|-------|---------|---|----------|
|                  |     |       |         | 0111 = x 128<br>1000 = x 256<br><br>Recommended that this register is not changed from default. |          |

**Register 13h** FLL Control 4

| REGISTER ADDRESS           | BIT | LABEL                | DEFAULT | DESCRIPTION   | REFER TO                  |
|----------------------------|-----|----------------------|---------|---|---------------------------|
| R20 (14h)<br>FLL Control 5 | 4:3 | FLL_CLK_REF_DIV[1:0] | 00      | FLL Clock Reference Divider<br>00 = MCLK / 1<br>01 = MCLK / 2<br>10 = MCLK / 4<br>11 = MCLK / 8<br><br>MCLK (or other input reference) must be divided down to <=13.5MHz.<br>For lower power operation, the reference clock can be divided down further if desired. | Clocking and Sample Rates |
|                            | 1:0 | FLL_CLK_SRC[1:0]     | 00      | FLL Clock source<br>00 - BCLK<br>01 - MCLK<br>10 - LRCLK<br>11 = Reserved   | Clocking and Sample Rates |

**Register 14h** FLL Control 5

| REGISTER ADDRESS               | BIT | LABEL                | DEFAULT | DESCRIPTION   | REFER TO                        |
|--------------------------------|-----|----------------------|---------|---|---------------------------------|
| R22 (16h)<br>Audio Interface 1 | 6   | AIFDAC_CHAN          | 0       | DAC Data Source Select<br>0 = DAC selects left channel data<br>1 = DAC selects right channel data   | Digital audio interface control |
|                                | 5:4 | AIFDAC_TDM_SLOT[1:0] | 00      | DAC TDM Slot Select<br>00 = Select slot 0 (Left/Right)<br>01 = Select slot 1 (Left/Right)<br>10 = Select slot 2 (Left/Right)<br>11 = Select slot 3 (Left/Right) | Digital audio interface control |
|                                | 3:2 | AIFDAC_TDM_MODE[1:0] | 00      | DAC TDM Mode Select<br>00 = 1 stereo slot (TDM off)<br>01 = 2 stereo slots<br>10 = 3 stereo slots<br>11 = 4 stereo slots  | Digital audio interface control |
|                                | 1   | DAC_COMP             | 0       | DAC Companding Enable<br>0 = Disabled<br>1 = Enabled  | Digital audio interface control |
|                                | 0   | DAC_COMPMODE         | 0       | DAC Companding Type<br>0 = $\mu$ -law<br>1 = A-law  | Digital audio interface control |

**Register 16h** Audio Interface 1

| REGISTER ADDRESS               | BIT | LABEL         | DEFAULT | DESCRIPTION  | REFER TO                        |
|--------------------------------|-----|---------------|---------|--|---------------------------------|
| R23 (17h)<br>Audio Interface 2 | 9   | AIF_TRIS      | 0       | Audio Interface Tristate<br>0 = Audio interface pins operate normally<br>1 = Tristate all audio interface pins   | Digital audio interface control |
|                                | 8   | DAC_DAT_INV   | 0       | DACDAT Invert<br>0 = DACDAT not inverted<br>1 = DACDAT inverted  | Digital audio interface control |
|                                | 7   | AIF_BCLK_INV  | 0       | BCLK Invert<br>0 = BCLK not inverted<br>1 = BCLK inverted  | Digital audio interface control |
|                                | 6   | BCLK_DIR      | 0       | BCLK Direction<br>(Forces BCLK clock to be output in slave mode)<br>0 = BCLK normal operation<br>1 = BCLK clock output enabled   | Digital audio interface control |
|                                | 5   | LRCLK_DIR     | 0       | LRCLK Direction<br>(Forces LRCLK clock to be output in slave mode)<br>0 = LRCLK normal operation<br>1 = LRCLK clock output enabled   | Digital audio interface control |
|                                | 4   | AIF_LRCLK_INV | 0       | Right, left and I <sup>2</sup> S modes – LRCLK polarity:<br>0 = normal LRCLK polarity<br>1 = invert LRCLK polarity<br><br>DSP Mode – mode A/B select :<br>0 = MSB is available on 2nd BCLK rising edge after LRC rising edge (mode A)<br>1 = MSB is available on 1st BCLK rising edge after LRC rising edge (mode B) | Digital audio interface control |
|                                | 3:2 | AIF_WL[1:0]   | 00      | Digital Audio Interface Word Length<br>00 = 16 bits<br>01 = 20 bits<br>10 = 24 bits<br>11 = 32 bits<br>Note - see "Companding" for the selection of 8-bit mode.  | Digital audio interface control |
|                                | 1:0 | AIF_FMT[1:0]  | 10      | Digital Audio Interface Format<br>00 = Right justified<br>01 = Left justified<br>10 = I <sup>2</sup> S Format<br>11 = DSP Mode   | Digital audio interface control |

**Register 17h** Audio Interface 2

| REGISTER ADDRESS               | BIT | LABEL         | DEFAULT | DESCRIPTION  | REFER TO                        |
|--------------------------------|-----|---------------|---------|--|---------------------------------|
| R24 (18h)<br>Audio Interface 3 | 4:0 | BCLK_DIV[4:0] | 0_1000  | BCLK Rate<br>00000 = CLK_SYS<br>00001 = CLK_SYS / 1.5<br>00010 = CLK_SYS / 2<br>00011 = CLK_SYS / 3<br>00100 = CLK_SYS / 4<br>00101 = CLK_SYS / 5<br>00110 = CLK_SYS / 5.5<br>00111 = CLK_SYS / 6<br>01000 = CLK_SYS / 8<br>01001 = CLK_SYS / 10 | Digital audio interface control |

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION  | REFER TO |
|------------------|-----|-------|---------|--|----------|
|                  |     |       |         | 01010 = CLK_SYS / 11<br>01011 = CLK_SYS / 12<br>01100 = CLK_SYS / 16<br>01101 = CLK_SYS / 20<br>01110 = CLK_SYS / 22<br>01111 = CLK_SYS / 24<br>10000 = CLK_SYS / 25<br>10001 = CLK_SYS / 30<br>10010 = CLK_SYS / 32<br>10011 = CLK_SYS / 44<br>10100 = CLK_SYS / 48 |          |

**Register 18h** Audio Interface 3

| REGISTER ADDRESS               | BIT  | LABEL            | DEFAULT       | DESCRIPTION   | REFER TO                        |
|--------------------------------|------|------------------|---------------|---|---------------------------------|
| R25 (19h)<br>Audio Interface 4 | 10:0 | LRCLK_RATE[10:0] | 000_0010_0010 | LRCLK Rate<br>LRCLK clock output = BCLK / LRCLK_RATE<br><br>Integer (LSB = 1)<br>Valid from 8..2047 | Digital audio interface control |

**Register 19h** Audio Interface 4

| REGISTER ADDRESS              | BIT | LABEL          | DEFAULT | DESCRIPTION  | REFER TO   |
|-------------------------------|-----|----------------|---------|--|------------|
| R26 (1Ah)<br>Interrupt Status | 2   | WSEQ_BUSY_EINT | 0       | Write Sequencer Interrupt<br>0 = Interrupt not set<br>1 = Interrupt is set<br>The Write Sequencer asserts this flag when it has completed a programmed sequence - ie it indicates that the Write Sequencer is NOT Busy. It is cleared when a '1' is written. | Interrupts |
|                               | 0   | TSHUT_EINT     | 0       | Thermal Shutdown Interrupt<br>0 = Interrupt not set<br>1 = Interrupt is set<br>This flag is asserted a thermal shutdown condition has been detected. It is cleared when a '1' is written.  | Interrupts |

**Register 1Ah** Interrupt Status

| REGISTER ADDRESS                   | BIT | LABEL             | DEFAULT | DESCRIPTION  | REFER TO   |
|------------------------------------|-----|-------------------|---------|--|------------|
| R27 (1Bh)<br>Interrupt Status Mask | 2   | IM_WSEQ_BUSY_EINT | 1       | Write Sequencer interrupt mask<br>0 = do not mask interrupt<br>1 = mask interrupt  | Interrupts |
|                                    | 0   | IM_TSHUT_EINT     | 0       | Thermal Shutdown interrupt mask<br>0 = do not mask interrupt<br>1 = mask interrupt | Interrupts |

**Register 1Bh** Interrupt Status Mask

| REGISTER ADDRESS                | BIT | LABEL     | DEFAULT | DESCRIPTION  | REFER TO   |
|---------------------------------|-----|-----------|---------|--|------------|
| R28 (1Ch)<br>Interrupt Polarity | 0   | TSHUT_INV | 0       | Thermal Shutdown interrupt polarity<br>0 = active low (interrupt is triggered when temperature threshold is exceeded)<br>1 = active high (interrupt is triggered when temperature is normal) | Interrupts |

**Register 1Ch** Interrupt Polarity

| REGISTER ADDRESS               | BIT | LABEL       | DEFAULT | DESCRIPTION  | REFER TO   |
|--------------------------------|-----|-------------|---------|--|------------|
| R29 (1Dh)<br>Interrupt Control | 15  | IRQ_POL     | 0       | Interrupt output polarity<br>0 = Active low<br>1 = Active high | Interrupts |
|                                | 0   | IRQ_OP_CTRL | 0       | IRQ Output pin configuration<br>0 = CMOS<br>1 = Open Drain     | Interrupts |

**Register 1Dh** Interrupt Control

| REGISTER ADDRESS           | BIT | LABEL        | DEFAULT   | DESCRIPTION  | REFER TO                            |
|----------------------------|-----|--------------|-----------|--|-------------------------------------|
| R30 (1Eh)<br>DAC Digital 1 | 7:0 | DAC_VOL[7:0] | 1100_0000 | DAC Volume and MUTE<br>0000 0000 = MUTE<br>0000 0001 = -71.625dB<br><br>... in steps of 0.375dB to<br><br>1100 0000 = 0dB<br>1100 0001 to 1111 1111 = reserved | Digital to Analogue Converter (DAC) |

**Register 1Eh** DAC Digital 1

| REGISTER ADDRESS           | BIT | LABEL        | DEFAULT | DESCRIPTION   | REFER TO                            |
|----------------------------|-----|--------------|---------|---|-------------------------------------|
| R31 (1Fh)<br>DAC Digital 2 | 10  | DAC_MUTERATE | 0       | DAC Soft Mute Ramp Rate<br>0 = Fast ramp (fs/2, maximum ramp time is 10.7ms at fs=48k)<br>1 = Slow ramp (fs/32, maximum ramp time is 171ms at fs=48k)<br>(Note: ramp rate scales with sample rate.)   | Digital to Analogue Converter (DAC) |
|                            | 9   | DAC_MUTEMODE | 0       | DAC Unmute Ramp select<br>0 = Disabling soft-mute (DAC_MUTE=0) will cause the DAC volume to change immediately to the DAC_VOL setting.<br>1 = Disabling soft-mute (DAC_MUTE=0) will cause the DAC volume to ramp up gradually to the DAC_VOL setting. | Digital to Analogue Converter (DAC) |
|                            | 3   | DAC_MUTE     | 1       | DAC Soft Mute Control<br>0 = DAC Un-mute<br>1 = DAC Mute  | Digital to Analogue Converter (DAC) |
|                            | 2:1 | DEEMPH[1:0]  | 00      | DAC De-Emphasis Control<br>00 = No de-emphasis<br>01 = 32kHz sample rate<br>10 = 44.1kHz sample rate  | Digital to Analogue Converter (DAC) |

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION            | REFER TO |
|------------------|-----|-------|---------|------------------------|----------|
|                  |     |       |         | 11 = 48kHz sample rate |          |

**Register 1Fh DAC Digital 2**

| REGISTER ADDRESS   | BIT  | LABEL                 | DEFAULT | DESCRIPTION   | REFER TO   |
|--------------------|------|-----------------------|---------|---|--|
| R32 (20h)<br>DRC 1 | 15   | DRC_ENA               | 0       | DRC enable<br>0 = Disabled<br>1 = Enabled   | Dynamic Range Controller (DRC)<br><br>Power Management |
|                    | 10:6 | DRC_STARTUP_GAIN[4:0] | 0_0110  | Initial gain at DRC startup<br>00000 = -3dB<br>00001 = -2.5dB<br>00010 = -2dB<br>00011 = -1.5dB<br>00100 = -1dB<br>00101 = -0.5dB<br>00110 = 0dB (default)<br>00111 = 0.5dB<br>01000 = 1dB<br>01001 = 1.5dB<br>01010 = 2dB<br>01011 = 2.5dB<br>01100 = 3dB<br>01101 = 3.5dB<br>01110 = 4dB<br>01111 = 4.5dB<br>10000 = 5dB<br>10001 = 5.5dB<br>10010 = 6dB<br>10011 to 11111 = Reserved | Dynamic Range Controller (DRC)                         |
|                    | 5    | DRC_FF_DLY            | 1       | Feed-forward delay for anti-clip feature<br>0 = 5 samples<br>1 = 9 samples<br>Time delay can be calculated as $5/f_s$ or $9/f_s$ , where $f_s$ is the sample rate.  | Dynamic Range Controller (DRC)                         |
|                    | 2    | DRC_QR                | 1       | Quick release enable<br>0 = Disabled<br>1 = Enabled   | Dynamic Range Controller (DRC)                         |
|                    | 1    | DRC_ANTICLIP          | 1       | Anti-clip enable<br>0 = Disabled<br>1 = Enabled   | Dynamic Range Controller (DRC)                         |

**Register 20h DRC 1**

| REGISTER ADDRESS   | BIT   | LABEL        | DEFAULT | DESCRIPTION   | REFER TO                 |
|--------------------|-------|--------------|---------|---|--------------------------|
| R33 (21h)<br>DRC 2 | 15:12 | DRC_ATK[3:0] | 0100    | Gain attack rate (seconds/6dB)<br>0000 = Reserved (181us) | Dynamic Range Controller |

| REGISTER ADDRESS | BIT  | LABEL            | DEFAULT | DESCRIPTION   | REFER TO                       |
|------------------|------|------------------|---------|---|--------------------------------|
|                  |      |                  |         | 0001 = 181us<br>0010 = 363us<br>0011 = 726us<br>0100 = 1.45ms (default)<br>0101 = 2.9ms<br>0110 = 5.8ms<br>0111 = 11.6ms<br>1000 = 23.2ms<br>1001 = 46.4ms<br>1010 = 92.8ms<br>1011 = 185.6ms<br>1100-1111 = Reserved | (DRC)                          |
|                  | 11:8 | DRC_DCY[3:0]     | 0010    | Gain decay rate (seconds/6dB)<br>0000 = 186ms<br>0001 = 372ms<br>0010 = 743ms (default)<br>0011 = 1.49s<br>0100 = 2.97s<br>0101 = 5.94s<br>0110 = 11.89s<br>0111 = 23.78s<br>1000 = 47.56s<br>1001-1111 = Reserved    | Dynamic Range Controller (DRC) |
|                  | 7:6  | DRC_QR_THR[1:0]  | 00      | Quick release crest factor threshold<br>00 = 12dB (default)<br>01 = 18dB<br>10 = 24dB<br>11 = 30dB  | Dynamic Range Controller (DRC) |
|                  | 5:4  | DRC_QR_DCY[1:0]  | 00      | Quick release decay rate (seconds/6dB)<br>00 = 0.725ms (default)<br>01 = 1.45ms<br>10 = 5.8ms<br>11 = Reserved  | Dynamic Range Controller (DRC) |
|                  | 3:2  | DRC_MINGAIN[1:0] | 00      | Minimum gain the DRC can use to attenuate audio signals<br>00 = 0dB (default)<br>01 = -6dB<br>10 = -12dB<br>11 = -18dB  | Dynamic Range Controller (DRC) |
|                  | 1:0  | DRC_MAXGAIN[1:0] | 01      | Maximum gain the DRC can use to boost audio signals<br>00 = 12dB<br>01 = 18dB (default)<br>10 = 24dB<br>11 = 36dB   | Dynamic Range Controller (DRC) |

**Register 21h DRC 2**

| REGISTER ADDRESS   | BIT | LABEL            | DEFAULT | DESCRIPTION   | REFER TO                       |
|--------------------|-----|------------------|---------|---|--------------------------------|
| R34 (22h)<br>DRC 3 | 5:3 | DRC_HI_COMP[2:0] | 000     | Compressor slope (upper region)<br>000 = 1 (no compression)<br>001 = 1/2<br>010 = 1/4 | Dynamic Range Controller (DRC) |



| REGISTER ADDRESS | BIT | LABEL            | DEFAULT | DESCRIPTION   | REFER TO                       |
|------------------|-----|------------------|---------|---|--------------------------------|
|                  |     |                  |         | 011 = 1/8<br>100 = 1/16<br>101 = 0<br>110 = Reserved<br>111 = Reserved  |                                |
|                  | 2:0 | DRC_LO_COMP[2:0] | 000     | Compressor slope (lower region)<br>000 = 1 (no compression)<br>001 = 1/2<br>010 = 1/4<br>011 = 1/8<br>100 = 0<br>101 = Reserved<br>11X = Reserved | Dynamic Range Controller (DRC) |

**Register 22h DRC 3**

| REGISTER ADDRESS   | BIT  | LABEL            | DEFAULT | DESCRIPTION  | REFER TO                       |
|--------------------|------|------------------|---------|--|--------------------------------|
| R35 (23h)<br>DRC 4 | 10:5 | DRC_KNEE_IP[5:0] | 00_0000 | Input signal level at the Compressor 'knee'.<br><br>000000 = 0dB<br>000001 = -0.75dB<br>000010 = -1.5dB<br>... (-0.75dB steps)<br>111100 = -45dB<br>111101 = Reserved<br>11111X = Reserved | Dynamic Range Controller (DRC) |
|                    | 4:0  | DRC_KNEE_OP[4:0] | 0_0000  | Output signal at the Compressor 'knee'.<br><br>00000 = 0dB<br>00001 = -0.75dB<br>00010 = -1.5dB<br>... (-0.75dB steps)<br>11110 = -22.5dB<br>11111 = Reserved                              | Dynamic Range Controller (DRC) |

**Register 23h DRC 4**

| REGISTER ADDRESS               | BIT | LABEL       | DEFAULT  | DESCRIPTION  | REFER TO  |
|--------------------------------|-----|-------------|----------|--|---|
| R38 (26h)<br>Write Sequencer 1 | 15  | WSEQ_ENA    | 0        | Write Sequencer Enable.<br>0 = Disabled<br>1 = Enabled   | Control Write sequencer<br><br>Power Management |
|                                | 9   | WSEQ_ABORT  | 0        | Writing a 1 to this bit aborts the current sequence and returns control of the device back to the serial control interface.  | Control Write sequencer                         |
|                                | 8   | WSEQ_START  | 0        | Writing a 1 to this bit starts the write sequencer at the memory location indicated by the WSEQ_START_INDEX field. The sequence continues until it reaches an "End of sequence" flag. At the end of the sequence, this bit will be reset by the Write Sequencer. | Control Write sequencer                         |
|                                | 6:0 | WSEQ_START_ | 000_0000 | Sequence Start Index. This is the memory location of the   | Control Write                                   |

| REGISTER ADDRESS | BIT | LABEL      | DEFAULT | DESCRIPTION                             | REFER TO  |
|------------------|-----|------------|---------|---|-----------|
|                  |     | INDEX[6:0] |         | first command in the selected sequence. | sequencer |

**Register 26h** Write Sequencer 1

| REGISTER ADDRESS               | BIT  | LABEL                       | DEFAULT  | DESCRIPTION   | REFER TO                |
|--------------------------------|------|-----------------------------|----------|---|-------------------------|
| R39 (27h)<br>Write Sequencer 2 | 10:4 | WSEQ_CURRE<br>NT_INDEX[6:0] | 000_0000 | Sequence Current Index. This is the location of the most recently accessed command in the write sequencer memory.   | Control Write sequencer |
|                                | 0    | WSEQ_BUSY                   | 0        | Sequencer Busy flag (Read Only).<br>0 = Sequencer idle<br>1 = Sequencer busy<br>Note: it is not possible to write to control registers via the control interface while the Sequencer is Busy. | Control Write sequencer |

**Register 27h** Write Sequencer 2

| REGISTER ADDRESS        | BIT | LABEL     | DEFAULT | DESCRIPTION  | REFER TO                          |
|-------------------------|-----|-----------|---------|--|-----------------------------------|
| R40 (28h)<br>MW Slave 1 | 5   | SPI_CFG   | 0       | Controls the SDOOUT pin in 4 wire mode<br>0 = SDOOUT output is CMOS<br>1 = SDOOUT output is open drain         | Control Interface (software mode) |
|                         | 4   | SPI_4WIRE | 0       | Selects 3-wire or 4-wire mode<br>0 = 3-wire mode using bi-directional SDIN pin<br>1 = 4-wire mode using SDOOUT | Control Interface (software mode) |
|                         | 3   | ARA_ENA   | 0       | Alert Response Address protocol enable<br>0 = Disabled<br>1 = Enabled  | Control Interface (software mode) |
|                         | 1   | AUTO_INC  | 1       | Enable Auto-Increment function<br>0 = Disabled<br>1 = Enabled  | Control Interface (software mode) |

**Register 28h** MW Slave 1

| REGISTER ADDRESS  | BIT   | LABEL               | DEFAULT | DESCRIPTION   | REFER TO                                |
|-------------------|-------|---------------------|---------|---|---|
| R42 (2Ah)<br>EQ 1 | 15:11 | EQ_B1_GAIN[4:<br>0] | 0_0000  | EQ Band 1 Gain<br>00000 = -12dB<br>00001 = -11dB<br>....<br>11000 = +12dB | ReTune Mobile Parametric Equalizer (EQ) |
|                   | 10:6  | EQ_B2_GAIN[4:<br>0] | 0_0000  | EQ Band 2 Gain<br>00000 = -12dB<br>00001 = -11dB<br>....<br>11000 = +12dB | ReTune Mobile Parametric Equalizer (EQ) |
|                   | 5:1   | EQ_B3_GAIN[4:<br>0] | 0_0000  | EQ Band 3 Gain<br>00000 = -12dB<br>00001 = -11dB<br>....<br>11000 = +12dB | ReTune Mobile Parametric Equalizer (EQ) |

| REGISTER ADDRESS | BIT | LABEL  | DEFAULT | DESCRIPTION                              | REFER TO   |
|------------------|-----|--------|---------|--|--|
|                  | 0   | EQ_ENA | 0       | EQ Enable<br>0 = Disabled<br>1 = Enabled | ReTune<br>Mobile<br>Parametric<br>Equalizer<br>(EQ)<br><br>Power<br>Management |

**Register 2Ah EQ 1**

| REGISTER ADDRESS  | BIT   | LABEL           | DEFAULT | DESCRIPTION   | REFER TO  |
|-------------------|-------|-----------------|---------|---|---|
| R43 (2Bh)<br>EQ 2 | 15:11 | EQ_B4_GAIN[4:0] | 0_0000  | EQ Band 4 Gain<br>00000 = -12dB<br>00001 = -11dB<br>....<br>11000 = +12dB | ReTune<br>Mobile<br>Parametric<br>Equalizer<br>(EQ) |
|                   | 10:6  | EQ_B5_GAIN[4:0] | 0_0000  | EQ Band 5 Gain<br>00000 = -12dB<br>00001 = -11dB<br>....<br>11000 = +12dB | ReTune<br>Mobile<br>Parametric<br>Equalizer<br>(EQ) |

**Register 2Bh EQ 2**

| REGISTER ADDRESS  | BIT  | LABEL         | DEFAULT                     | DESCRIPTION                    | REFER TO  |
|-------------------|------|---------------|-----------------------------|--------------------------------|---|
| R44 (2Ch)<br>EQ 3 | 15:0 | EQ_B1_A[15:0] | 0000_1111<br>_1100_101<br>0 | 5 Band EQ Band 1 coefficient A | ReTune<br>Mobile<br>Parametric<br>Equalizer<br>(EQ) |

**Register 2Ch EQ 3**

| REGISTER ADDRESS  | BIT  | LABEL         | DEFAULT                     | DESCRIPTION                    | REFER TO  |
|-------------------|------|---------------|-----------------------------|--------------------------------|---|
| R45 (2Dh)<br>EQ 4 | 15:0 | EQ_B1_B[15:0] | 0000_0100<br>_0000_000<br>0 | 5 Band EQ Band 1 coefficient B | ReTune<br>Mobile<br>Parametric<br>Equalizer<br>(EQ) |

**Register 2Dh EQ 4**

| REGISTER ADDRESS  | BIT  | LABEL          | DEFAULT                     | DESCRIPTION                     | REFER TO  |
|-------------------|------|----------------|-----------------------------|---------------------------------|---|
| R46 (2Eh)<br>EQ 5 | 15:0 | EQ_B1_PG[15:0] | 0000_0000<br>_1011_100<br>0 | 5 Band EQ Band 1 coefficient PG | ReTune<br>Mobile<br>Parametric<br>Equalizer<br>(EQ) |

**Register 2Eh EQ 5**

| REGISTER ADDRESS  | BIT  | LABEL         | DEFAULT                     | DESCRIPTION                    | REFER TO  |
|-------------------|------|---------------|-----------------------------|--------------------------------|---|
| R47 (2Fh)<br>EQ 6 | 15:0 | EQ_B2_A[15:0] | 0001_1110<br>_1011_010<br>1 | 5 Band EQ Band 2 coefficient A | ReTune<br>Mobile<br>Parametric<br>Equalizer<br>(EQ) |

**Register 2Fh EQ 6**

| REGISTER ADDRESS  | BIT  | LABEL         | DEFAULT                     | DESCRIPTION                    | REFER TO  |
|-------------------|------|---------------|-----------------------------|--------------------------------|---|
| R48 (30h) EQ<br>7 | 15:0 | EQ_B2_B[15:0] | 1111_0001<br>_0100_010<br>1 | 5 Band EQ Band 2 coefficient B | ReTune<br>Mobile<br>Parametric<br>Equalizer<br>(EQ) |

**Register 30h EQ 7**

| REGISTER ADDRESS  | BIT  | LABEL         | DEFAULT                     | DESCRIPTION                    | REFER TO  |
|-------------------|------|---------------|-----------------------------|--------------------------------|---|
| R49 (31h) EQ<br>8 | 15:0 | EQ_B2_C[15:0] | 0000_1011<br>_0111_010<br>1 | 5 Band EQ Band 2 coefficient C | ReTune<br>Mobile<br>Parametric<br>Equalizer<br>(EQ) |

**Register 31h EQ 8**

| REGISTER ADDRESS  | BIT  | LABEL              | DEFAULT                     | DESCRIPTION                     | REFER TO  |
|-------------------|------|--------------------|-----------------------------|---------------------------------|---|
| R50 (32h) EQ<br>9 | 15:0 | EQ_B2_PG[15:0<br>] | 0000_0001<br>_1100_010<br>1 | 5 Band EQ Band 2 coefficient PG | ReTune<br>Mobile<br>Parametric<br>Equalizer<br>(EQ) |

**Register 32h EQ 9**

| REGISTER ADDRESS   | BIT  | LABEL         | DEFAULT                     | DESCRIPTION                    | REFER TO  |
|--------------------|------|---------------|-----------------------------|--------------------------------|---|
| R51 (33h) EQ<br>10 | 15:0 | EQ_B3_A[15:0] | 0001_0110<br>_1001_111<br>0 | 5 Band EQ Band 3 coefficient A | ReTune<br>Mobile<br>Parametric<br>Equalizer<br>(EQ) |

**Register 33h EQ 10**

| REGISTER ADDRESS   | BIT  | LABEL         | DEFAULT                     | DESCRIPTION                    | REFER TO  |
|--------------------|------|---------------|-----------------------------|--------------------------------|---|
| R52 (34h) EQ<br>11 | 15:0 | EQ_B3_B[15:0] | 1111_1000<br>_0010_100<br>1 | 5 Band EQ Band 3 coefficient B | ReTune<br>Mobile<br>Parametric<br>Equalizer<br>(EQ) |

**Register 34h EQ 11**

| REGISTER ADDRESS | BIT  | LABEL         | DEFAULT                     | DESCRIPTION                    | REFER TO                                |
|------------------|------|---------------|-----------------------------|--------------------------------|---|
| R53 (35h) EQ 12  | 15:0 | EQ_B3_C[15:0] | 0000_0111<br>_1010_110<br>1 | 5 Band EQ Band 3 coefficient C | ReTune Mobile Parametric Equalizer (EQ) |

**Register 35h EQ 12**

| REGISTER ADDRESS | BIT  | LABEL               | DEFAULT                     | DESCRIPTION                     | REFER TO                                |
|------------------|------|---------------------|-----------------------------|---------------------------------|---|
| R54 (36h) EQ 13  | 15:0 | EQ_B3_PG[15:0]<br>] | 0001_0001<br>_0000_001<br>1 | 5 Band EQ Band 3 coefficient PG | ReTune Mobile Parametric Equalizer (EQ) |

**Register 36h EQ 13**

| REGISTER ADDRESS | BIT  | LABEL         | DEFAULT                     | DESCRIPTION                    | REFER TO                                |
|------------------|------|---------------|-----------------------------|--------------------------------|---|
| R55 (37h) EQ 14  | 15:0 | EQ_B4_A[15:0] | 0001_1100<br>_0101_100<br>0 | 5 Band EQ Band 4 coefficient A | ReTune Mobile Parametric Equalizer (EQ) |

**Register 37h EQ 14**

| REGISTER ADDRESS | BIT  | LABEL         | DEFAULT                     | DESCRIPTION                    | REFER TO                                |
|------------------|------|---------------|-----------------------------|--------------------------------|---|
| R56 (38h) EQ 15  | 15:0 | EQ_B4_B[15:0] | 1111_0011<br>_0111_001<br>1 | 5 Band EQ Band 4 coefficient B | ReTune Mobile Parametric Equalizer (EQ) |

**Register 38h EQ 15**

| REGISTER ADDRESS | BIT  | LABEL         | DEFAULT                     | DESCRIPTION                    | REFER TO                                |
|------------------|------|---------------|-----------------------------|--------------------------------|---|
| R57 (39h) EQ 16  | 15:0 | EQ_B4_C[15:0] | 0000_1010<br>_0101_010<br>0 | 5 Band EQ Band 4 coefficient C | ReTune Mobile Parametric Equalizer (EQ) |

**Register 39h EQ 16**

| REGISTER ADDRESS | BIT  | LABEL               | DEFAULT                     | DESCRIPTION                     | REFER TO                           |
|------------------|------|---------------------|-----------------------------|---------------------------------|------------------------------------|
| R58 (3Ah) EQ 17  | 15:0 | EQ_B4_PG[15:0]<br>] | 0000_0101<br>_0101_100<br>0 | 5 Band EQ Band 2 coefficient PG | ReTune Mobile Parametric Equalizer |

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|------------------|-----|-------|---------|-------------|----------|
|                  |     |       |         |             | (EQ)     |

Register 3Ah EQ 17

| REGISTER ADDRESS   | BIT  | LABEL         | DEFAULT                     | DESCRIPTION                    | REFER TO  |
|--------------------|------|---------------|-----------------------------|--------------------------------|---|
| R59 (3Bh)<br>EQ 18 | 15:0 | EQ_B5_A[15:0] | 0000_0101<br>_0110_010<br>0 | 5 Band EQ Band 5 coefficient A | ReTune<br>Mobile<br>Parametric<br>Equalizer<br>(EQ) |

Register 3Bh EQ 18

| REGISTER ADDRESS   | BIT  | LABEL         | DEFAULT                     | DESCRIPTION                    | REFER TO  |
|--------------------|------|---------------|-----------------------------|--------------------------------|---|
| R60 (3Ch)<br>EQ 19 | 15:0 | EQ_B5_B[15:0] | 0000_0101<br>_0101_100<br>1 | 5 Band EQ Band 5 coefficient B | ReTune<br>Mobile<br>Parametric<br>Equalizer<br>(EQ) |

Register 3Ch EQ 19

| REGISTER ADDRESS   | BIT  | LABEL              | DEFAULT                     | DESCRIPTION                     | REFER TO  |
|--------------------|------|--------------------|-----------------------------|---------------------------------|---|
| R61 (3Dh)<br>EQ 20 | 15:0 | EQ_B5_PG[15:0<br>] | 0100_0000<br>_0000_000<br>0 | 5 Band EQ Band 5 coefficient PG | ReTune<br>Mobile<br>Parametric<br>Equalizer<br>(EQ) |

Register 3Dh EQ 20

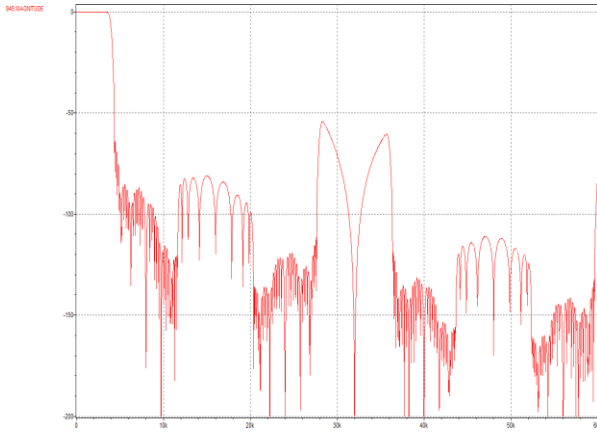
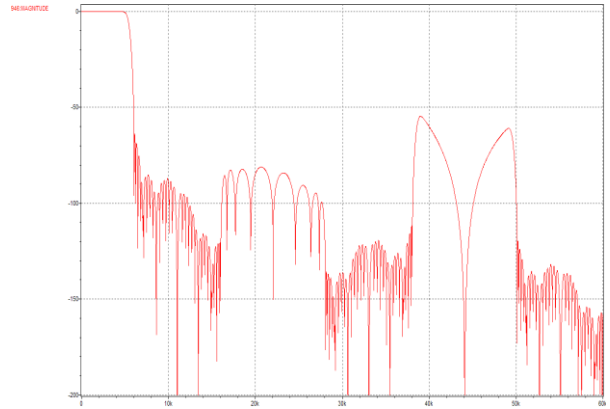
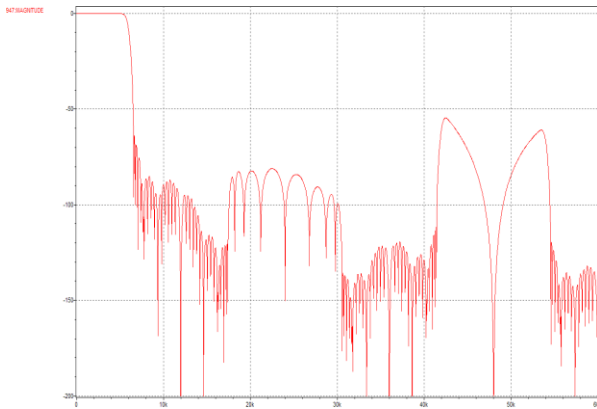
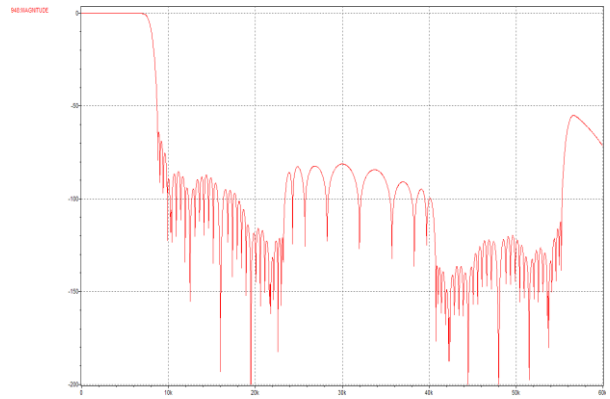
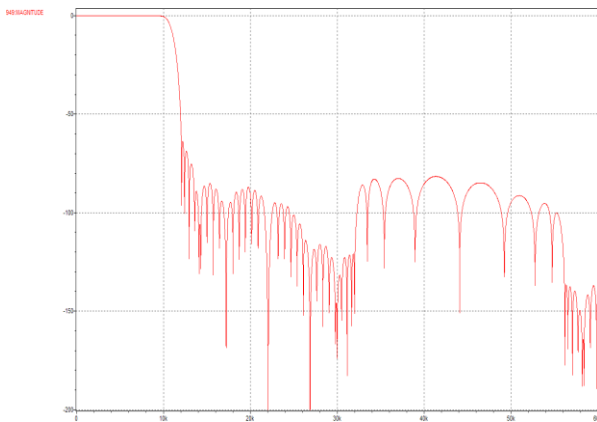
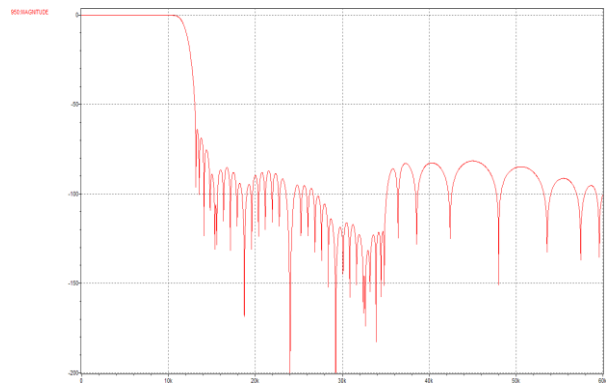
**DIGITAL FILTER CHARACTERISTICS**

| PARAMETER                          | TEST CONDITIONS | MIN      | TYP    | MAX      | UNIT |
|------------------------------------|-----------------|----------|--------|----------|------|
| <b>DAC Normal Filter</b>           |                 |          |        |          |      |
| Passband                           | +/- 0.05dB      | 0        |        | 0.454 fs |      |
|                                    | -6dB            |          | 0.5 fs |          |      |
| Passband Ripple                    | 0.454 fs        |          |        | +/- 0.03 | dB   |
| Stopband                           |                 | 0.546 fs |        |          |      |
| Stopband Attenuation               | F > 0.546 fs    | -50      |        |          | dB   |
| <b>DAC Sloping Stopband Filter</b> |                 |          |        |          |      |
| Passband                           | +/- 0.03dB      | 0        |        | 0.25 fs  |      |
|                                    | +/- 1dB         | 0.25 fs  |        | 0.454 fs |      |
|                                    | -6dB            |          | 0.5 fs |          |      |
| Passband Ripple                    | 0.25 fs         |          |        | +/- 0.03 | dB   |
| Stopband 1                         |                 | 0.546 fs |        | 0.7 fs   |      |
| Stopband 1 Attenuation             | f > 0.546 fs    | -60      |        |          | dB   |
| Stopband 2                         |                 | 0.7 fs   |        | 1.4 fs   |      |
| Stopband 2 Attenuation             | f > 0.7 fs      | -85      |        |          | dB   |
| Stopband 3                         |                 | 1.4 fs   |        |          |      |
| Stopband 3 Attenuation             | F > 1.4 fs      | -55      |        |          | dB   |

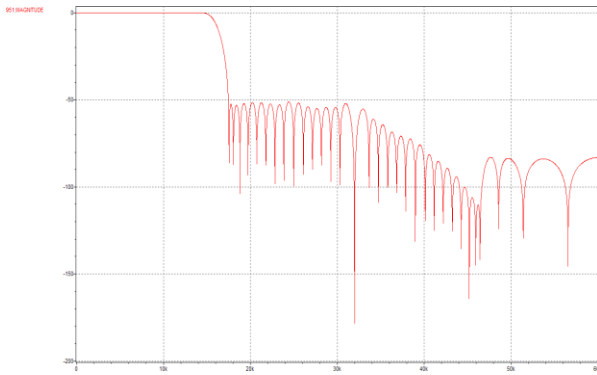
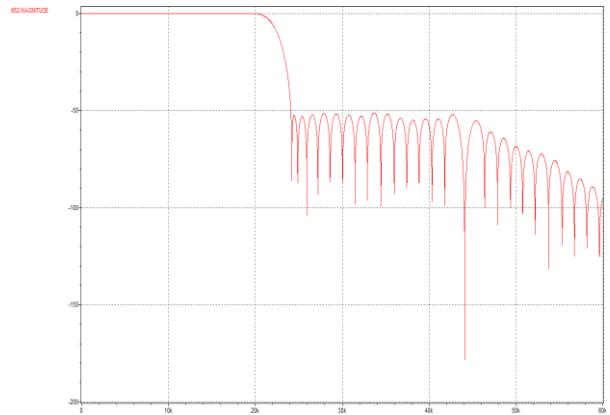
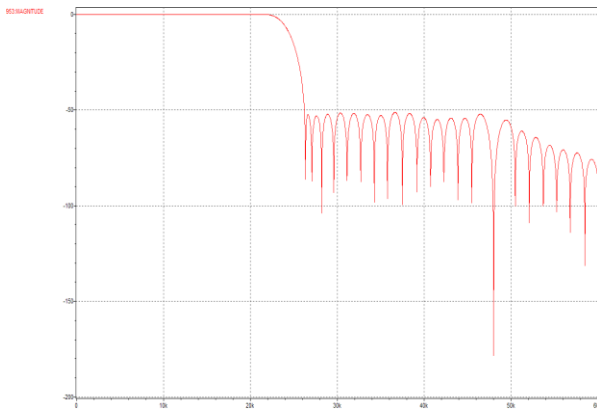
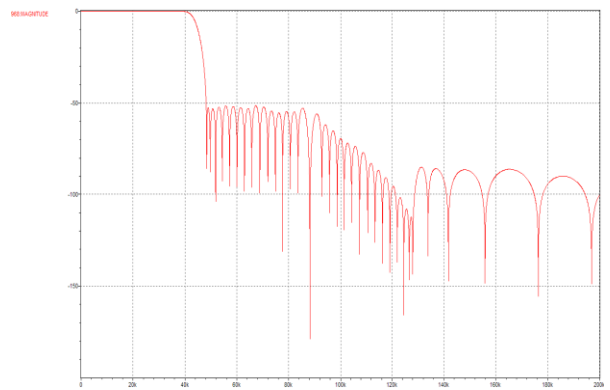
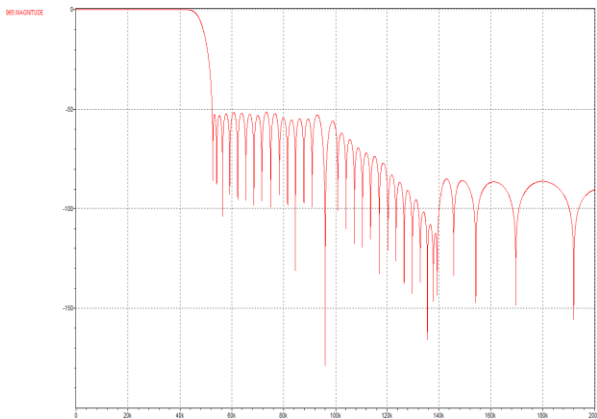
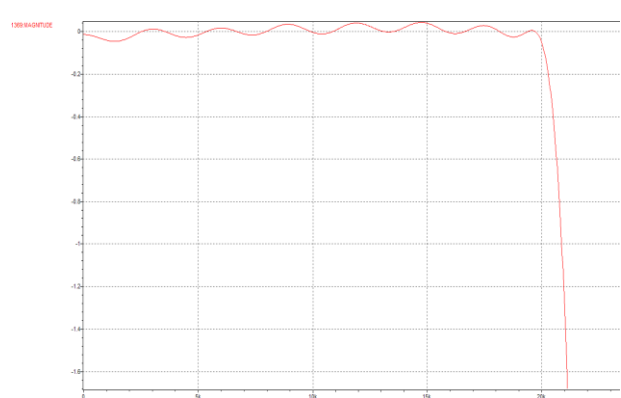
| <b>DAC FILTER GROUP DELAY</b> |             |
|-------------------------------|-------------|
| Mode                          | Group Delay |
| Normal                        | 16.5 / fs   |
| Sloping Stopband              | 18 / fs     |
| 4fs Mode                      | TBA         |

**TERMINOLOGY**

1. Stop Band Attenuation (dB) – the degree to which the frequency spectrum is attenuated (outside audio band)
2. Pass-band Ripple – any variation of the frequency response in the pass-band region

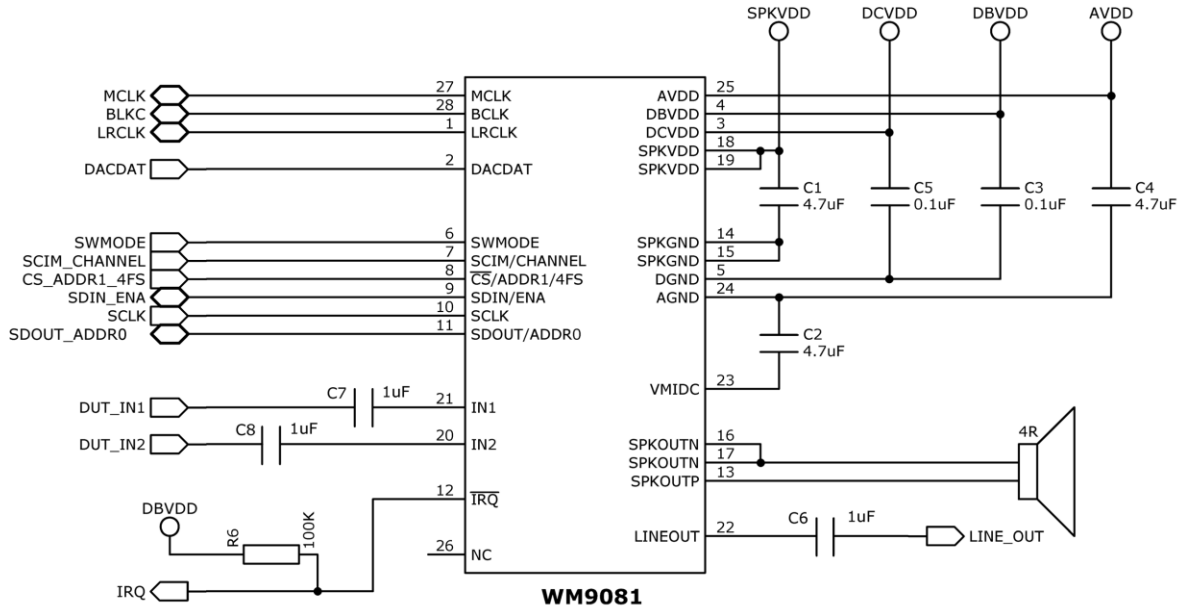
**DAC FILTER RESPONSES**

**Figure 55 DAC Filter Response (fs=8kHz)**

**Figure 56 DAC Filter Response (fs=11.025kHz)**

**Figure 57 DAC Filter Response (fs=12kHz)**

**Figure 58 DAC Filter Response (fs=16kHz)**

**Figure 59 DAC Filter Response (fs=22.05kHz)**

**Figure 60 DAC Filter Response (fs=24kHz)**




**Figure 61 DAC Filter Response (fs=32kHz)**

**Figure 62 DAC Filter Response (fs=44.1kHz)**

**Figure 63 DAC Filter Response (fs=48kHz)**

**Figure 64 DAC Filter Response (fs=88.2kHz)**

**Figure 65 DAC Filter Response (fs=96kHz)**

**Figure 66 DAC Filter Passband Ripple (fs=44.1kHz)**

## APPLICATIONS INFORMATION

### RECOMMENDED EXTERNAL COMPONENTS



**Figure 67 Recommended external components**

#### Notes

1. Cirrus Logic recommends using a single, common ground reference. Where this is not possible, care should be taken to optimise split ground configuration for audio performance.
2. Supply decoupling capacitors on DCVDD, DBVDD, SPKVDD and AVDD should be positioned as close to the WM9081 as possible.
3. Capacitor types should be chosen carefully. Capacitors with very low ESR are recommended for optimum performance.
4. The speakers should be connected as close as possible to the WM9081. When this is not possible, filtering should be placed on the speaker outputs close the WM9081.

## SPEAKER SELECTION

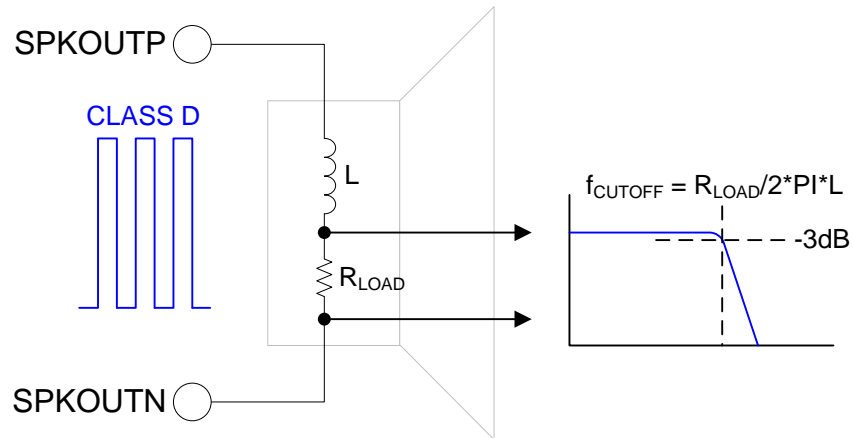
For filterless operation, it is important to select a speaker with appropriate internal inductance. The internal inductance and the speaker's load resistance create a low-pass filter with a cut-off frequency of:

$$f_c = R_L / (2\pi L)$$

For an 4Ω speaker and required cut-off frequency of 20kHz, the speaker should be chosen to have an inductance of:

$$L = R_L / (2\pi f_c) = 4\Omega / (2\pi * 20\text{kHz}) = 32\mu\text{H}$$

Care should be taken to ensure that the cut-off frequency of the speaker's internal filtering is low enough to prevent speaker damage. The class D output of the WM9081 operate at much higher frequencies than is recommended for most speakers, and the cut-off frequency of the filter should be low enough to protect the speaker.



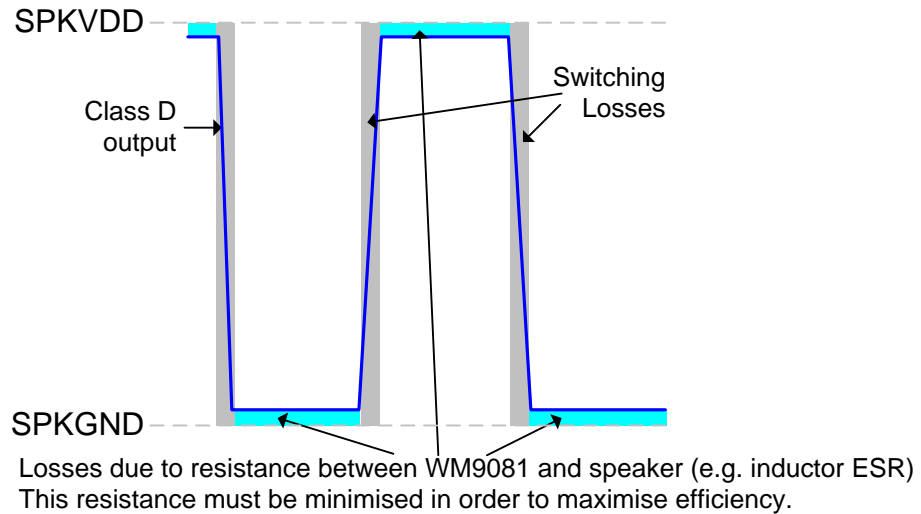
**Figure 68 Speaker Equivalent Circuit**

### Notes

1. For further information on speaker selection, refer to the application note WAN\_0200 - *Speaker Selection for Class D output drivers*.

## PCB LAYOUT CONSIDERATIONS

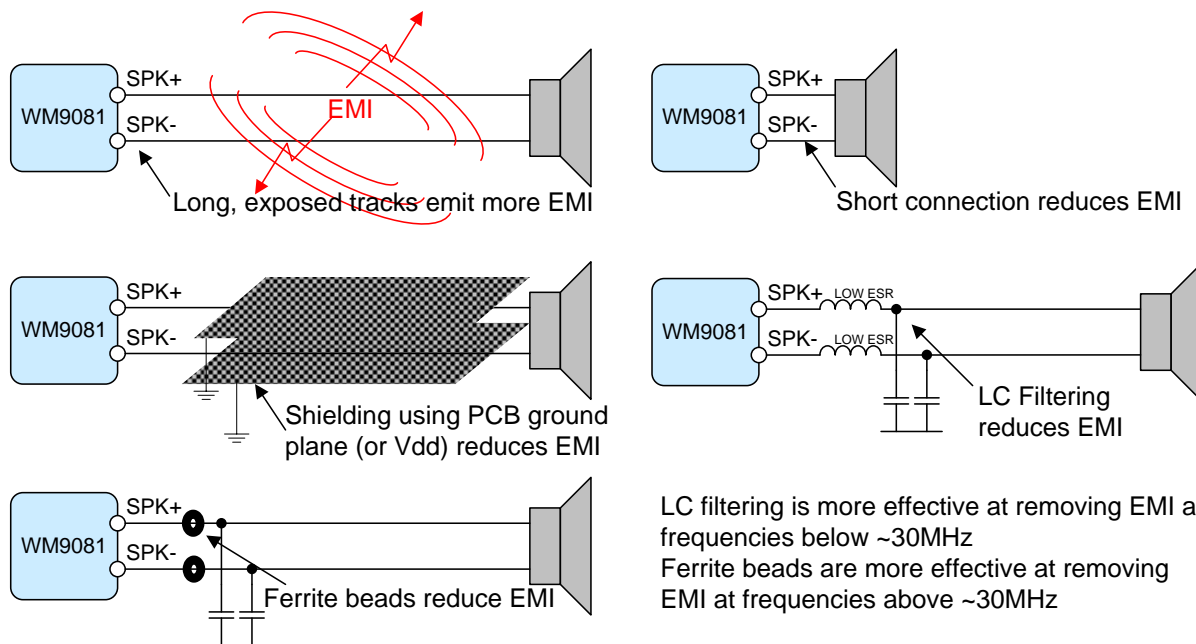
The efficiency of the speaker driver is affected by the series resistance between the WM9081 and the speaker (e.g. inductor ESR) as shown in Figure 69. This resistance should be as low as possible to maximise efficiency.



**Figure 69 Speaker Connection Losses**

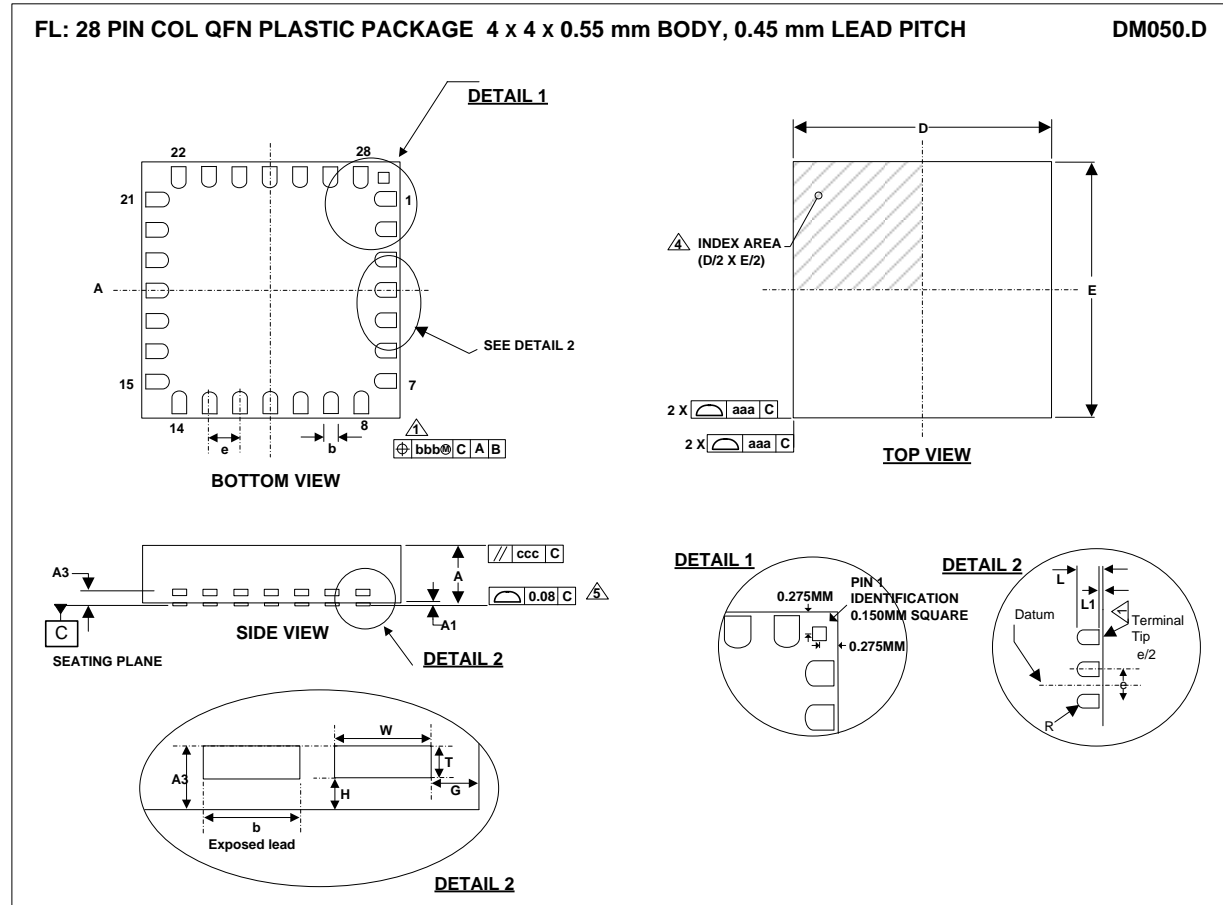
The distance between the WM9081 and the speaker should be kept to a minimum to reduce series resistance, and also to reduce EMI. Further reductions in EMI can be achieved by additional passive filtering and/or shielding as shown in Figure 70. When additional passive filtering is used, low ESR components should be chosen to minimise series resistance between the WM9081 and the speaker, maximising efficiency.

LC passive filtering will usually be effective at reducing EMI at frequencies up to around 30MHz. To reduce emissions at higher frequencies, ferrite beads placed as close to the device as possible will be more effective.



**Figure 70 EMI Reduction Techniques**

Refer to the application note WAN\_0118 - *Guidelines on How to Use QFN Packages and Create Associated PCB Footprints*.

**PACKAGE DIMENSIONS**


| Symbols                                | Dimensions (mm) |               |       | NOTE |
|--|-----------------|---------------|-------|------|
|  | MIN             | NOM           | MAX   |      |
| <b>A</b>                               | 0.500           | 0.550         | 0.600 |      |
| <b>A1</b>                              | 0               | 0.035         | 0.050 |      |
| <b>A3</b>                              |                 | 0.152 REF     |       |      |
| <b>b</b>                               | 0.180           | 0.230         | 0.280 | 1    |
| <b>D</b>                               | 3.950           | 4.000         | 4.050 |      |
| <b>E</b>                               | 3.950           | 4.000         | 4.050 |      |
| <b>e</b>                               |                 | 0.450 BSC     |       |      |
| <b>G</b>                               |                 | 0.200 REF     |       |      |
| <b>H</b>                               |                 | 0.075 REF     |       |      |
| <b>L</b>                               |                 | 0.400 REF     |       |      |
| <b>L1</b>                              |                 | 0.000 REF     |       | 5    |
| <b>T</b>                               |                 | 0.077 REF     |       |      |
| <b>W</b>                               |                 | 0.150 REF     |       |      |
| <b>Tolerances of Form and Position</b> |                 |               |       |      |
| <b>aaa</b>                             |                 | 0.100         |       |      |
| <b>bbb</b>                             |                 | 0.100         |       |      |
| <b>ccc</b>                             |                 | 0.100         |       |      |
| <b>REF:</b>                            |                 | JEDEC, MO-220 |       |      |

**NOTES:**

1. DIMENSION **b** APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 mm AND 0.30 mm FROM TERMINAL TIP.
2. ALL DIMENSIONS ARE IN MILLIMETRES.
3. COPLANARITY APPLIES TO THE TERMINALS.
4. REFER TO APPLICATIONS NOTE WAN\_0118 FOR FURTHER INFORMATION REGARDING PCB FOOTPRINTS AND QFN PACKAGE SOLDERING.
5. DEPENDING ON THE METHOD OF LEAD TERMINATION AT THE EDGE OF THE PACKAGE, PULL BACK (L1) MAY BE PRESENT.
6. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.

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**IMPORTANT NOTICE**

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**Contacting Cirrus Logic Support**

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.

To find one nearest you, go to [www.cirrus.com](http://www.cirrus.com).

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**REVISION HISTORY**

| DATE     | REV | DESCRIPTION OF CHANGES  | CHANGED BY |
|----------|-----|---|------------|
| 20/12/16 | 4.0 | <ul style="list-style-type: none"><li>• DACDAT set-up time to BCLK rising edge changed to min 10ns (Figure 3)</li><li>• Package Drawing updated (POD 050.D)</li></ul> | CT<br>PH   |