VN920
VN920-B5 / VN920SO

SINGLE CHANNEL HIGH SIDE SOLID STATE RELAY

| TYPE	$R_{DS(on)}$	I_{OUT}	V_{CC}
VN920 VN920-B5 VN920SO	16mΩ	30 A	36 V

- CMOS COMPATIBLE INPUT
- PROPORTIONAL LOAD CURRENT SENSE
- SHORTED LOAD PROTECTION
- UNDERVOLTAGE AND OVERVOLTAGE SHUTDOWN
- OVERVOLTAGE CLAMP
- THERMAL SHUTDOWN
- CURRENT LIMITATION
- PROTECTION AGAINST LOSS OF GROUND AND LOSS OF V_{CC}
- VERY LOW STAND-BY POWER DISSIPATION
- REVERSE BATTERY PROTECTION (*)

PENTAWATT   **P²PAK**

SO-16L

| ORDER CODES		
PACKAGE	TUBE	T&R
PENTAWATT	VN920	-
P²PAK	VN920-B5	VN920-B513TR
SO-16L	VN920SO	VN920SO13TR

DESCRIPTION

The VN920, VN920-B5, VN920SO is a monolithic device made by using STMicroelectronics VIPower M0-3 Technology, intended for driving any kind of load with one side connected to ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table). Active current limitation combined with thermal shutdown and automatic restart protect the device against overload. The device integrates an analog current sense output which delivers a current proportional to the load current. Device automatically turns off in case of ground pin disconnection.

BLOCK DIAGRAM
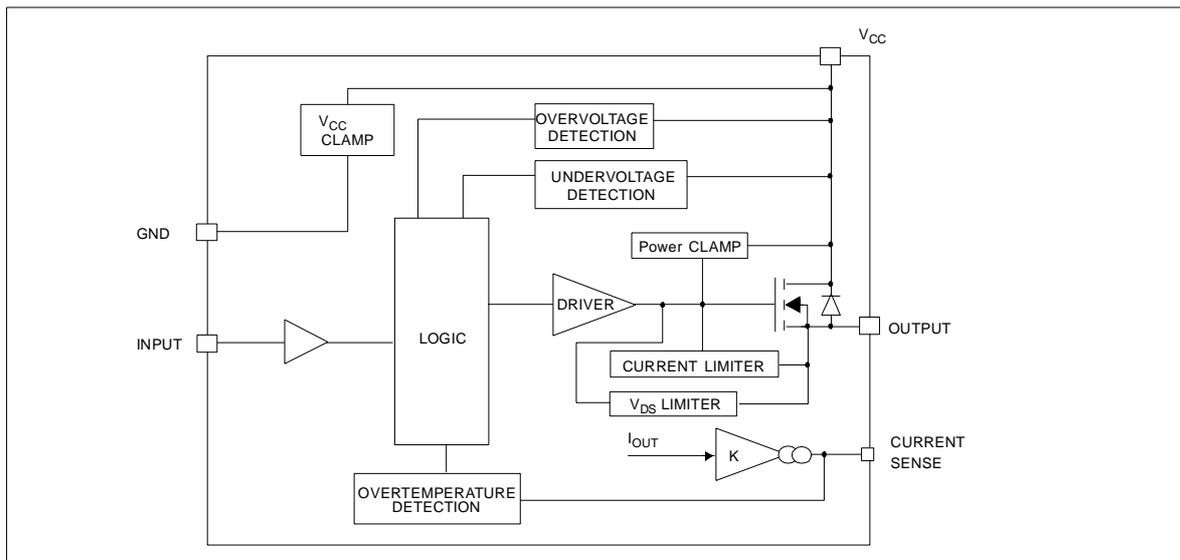
(*) See application schematic at page 8

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value			Unit
		PENTAWATT	P²PAK	SO-16L	
V_{CC}	DC Supply Voltage	41			V
$-V_{CC}$	Reverse DC Supply Voltage	-0.3			V
$-I_{GND}$	DC Reverse Ground Pin Current	-200			mA
I_{OUT}	DC Output Current	Internally Limited			A
$-I_{OUT}$	Reverse DC Output Current	-21			A
I_{IN}	DC Input Current	$+/-10$			mA
V_{CSENSE}	Current Sense Maximum Voltage	-3			V
		$+15$			V
V_{ESD}	Electrostatic Discharge (Human Body Model: R=1.5KΩ; C=100pF) - INPUT - CURRENT SENSE - OUTPUT - V_{CC}	4000 2000 5000 5000			V V V V
E_{MAX}	Maximum Switching Energy (L=0.25mH; R_L=0Ω; V_{bat}=13.5V; T_{jstart}=150ºC; I_L=45A)		364	352	mJ
P_{TOT}	Power Dissipation T_C≤25°C	96.1	96.1	8.3	W
T_j	Junction Operating Temperature	Internally limited			°C
T_c	Case Operating Temperature	-40 to 150			°C
T_{STG}	Storage Temperature	-55 to 150			°C

CONNECTION DIAGRAM (TOP VIEW)

PENTAWATT
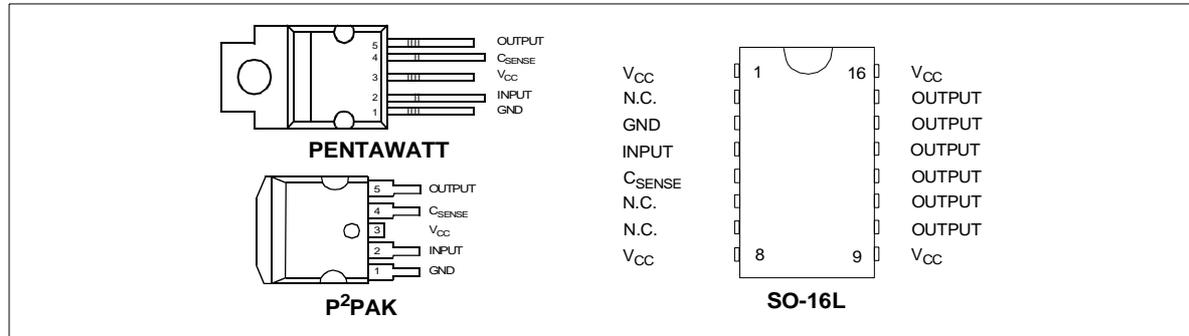
P²PAK

SO-16L

CURRENT AND VOLTAGE CONVENTIONS
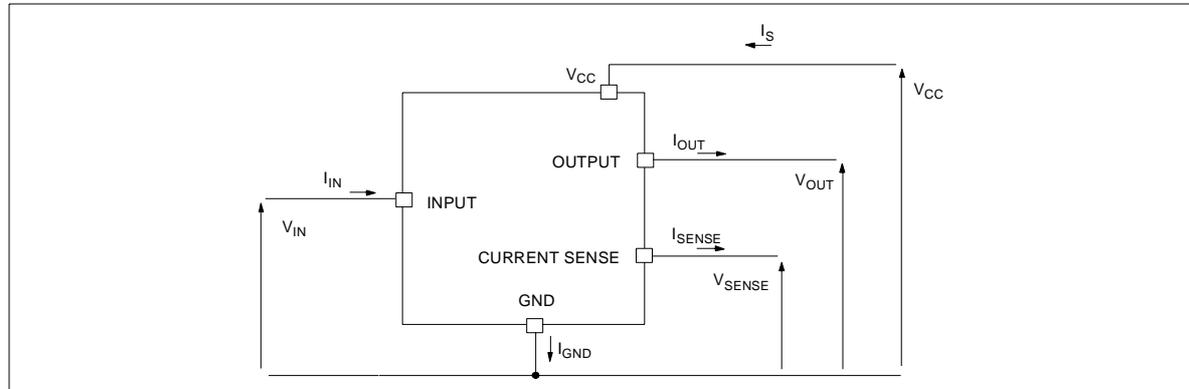
THERMAL DATA

Symbol	Parameter		Value			Unit
			PENTAWATT	P^{2}PAK	SO-16L	
$R_{thj-case}$	Thermal Resistance Junction-case	Max	1.3	1.3		°C/W
$R_{thj-lead}$	Thermal Resistance Junction-lead	Max			15	°C/W
$R_{thj-amb}$	Thermal Resistance Junction-ambient	Max	61.3	51.3 (*)	65 (**)	°C/W

(*) When mounted on a standard single-sided FR-4 board with 0.5cm^2 of Cu (at least 35µm thick).

(**) When mounted on a standard single-sided FR-4 board with 0.5cm^2 of Cu (at least 35µm thick) connected to all V_{CC} pins.

ELECTRICAL CHARACTERISTICS (8V<V_{CC}<36V; -40°C<T_j<150°C unless otherwise specified)

POWER

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{CC}	Operating Supply Voltage		5.5	13	36	V
V_{USD}	Undervoltage Shut-down		3	4	5.5	V
V_{OV}	Overvoltage Shut-down		36			V
R_{ON}	On State Resistance	I_{OUT}=10A; T_j=25°C			16	mΩ
		I_{OUT}=10A			32	mΩ
		I_{OUT}=3A; V_{CC}=6V			55	mΩ
V_{clamp}	Clamp Voltage	I_{CC}=20mA (See note 1)	41	48	55	V
I_S	Supply Current	Off State; V_{CC}=13V; V_{IN}=V_{OUT}=0V		10	25	µA
		Off State; V_{CC}=13V; V_{IN}=V_{OUT}=0V; T_j=25°C		10	20	µA
		On State; V_{CC}=13V; V_{IN}=5V; I_{OUT}=0A; R_{SENSE}=3.9KΩ			5	mA
$I_{L(off1)}$	Off State Output Current	V_{IN}=V_{OUT}=0V	0		50	µA
$I_{L(off2)}$	Off State Output Current	V_{IN}=0V; V_{OUT}=3.5V	-75		0	µA
$I_{L(off3)}$	Off State Output Current	V_{IN}=V_{OUT}=0V; Vcc=13V; T_j=125°C			5	µA
$I_{L(off4)}$	Off State Output Current	V_{IN}=V_{OUT}=0V; Vcc=13V; T_j=25°C			3	µA

SWITCHING (V_{CC}=13V)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on Delay Time	R_L=1.3Ω (see figure 2)		50		µs
$t_{d(off)}$	Turn-off Delay Time	R_L=1.3Ω (see figure 2)		50		µs
$dV_{OUT}/dt_{(on)}$	Turn-on Voltage Slope	R_L=1.3Ω (see figure 2)		See relative diagram		V/µs
$dV_{OUT}/dt_{(off)}$	Turn-off Voltage Slope	R_L=1.3Ω (see figure 2)		See relative diagram		V/µs

LOGIC INPUT

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IL}	Input Low Level				1.25	V
I_{IL}	Low Level Input Current	V_{IN}=1.25V	1			µA
V_{IH}	Input High Level		3.25			V
I_{IH}	High Level Input Current	V_{IN}=3.25V			10	µA
$V_{I(hyst)}$	Input Hysteresis Voltage		0.5			V
V_{ICL}	Input Clamp Voltage	I_{IN}=1mA	6	6.8	8	V
		I_{IN}=-1mA		-0.7		V

Note 1: V_{clamp} and V_{OV} are correlated. Typical difference is 5V.

![ST logo]

ELECTRICAL CHARACTERISTICS (continued)

CURRENT SENSE ($9V \leq V_{CC} \leq 16V$) (See Fig. 1)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
K_1	I_{OUT}/I_{SENSE}	I_{OUT}=1A; V_{SENSE}=0.5V; T_j= -40°C...150°C	3300	4400	6000	
dK_1/K_1	Current Sense Ratio Drift	I_{OUT}=1A; V_{SENSE}=0.5V; T_j= -40°C...+150°C	-10		+10	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT}=10A; V_{SENSE}=4V; T_j=-40°C T_j=25°C...150°C	4200 4400	4900 4900	6000 5750	
dK_2/K_2	Current Sense Ratio Drift	I_{OUT}=10A; V_{SENSE}=4V; T_j=-40°C...+150°C	-8		+8	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT}=30A; V_{SENSE}=4V; T_j=-40°C T_j=25°C...150°C	4200 4400	4900 4900	5500 5250	
dK_3/K_3	Current Sense Ratio Drift	I_{OUT}=30A; V_{SENSE}=4V; T_j=-40°C...+150°C	-6		+6	%
I_{SENSEO}	Analog Sense Leakage Current	V_{CC}=6...16V; I_{OUT}=0A; V_{SENSE}=0V; T_j=-40°C...+150°C	0		10	µA
V_{SENSE}	Max Analog Sense Output Voltage	V_{CC}=5.5V; I_{OUT}=5A; R_{SENSE}=10KΩ V_{CC}>8V; I_{OUT}=10A; R_{SENSE}=10KΩ	2 4			V V
V_{SENSEH}	Sense Voltage in Overtemperature conditions	V_{CC}=13V; R_{SENSE}=3.9KΩ		5.5		V
$R_{VSENSEH}$	Analog Sense Output Impedance in Overtemperature Condition	V_{CC}=13V; T_j>T_{TSD}; Output Open		400		Ω
t_{DSENSE}	Current sense delay response	to 90% I_{SENSE} (see note 2)			500	µs

PROTECTIONS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
T_{TSD}	Shut-down Temperature		150	175	200	°C
T_R	Reset Temperature		135			°C
T_{hyst}	Thermal Hysteresis		7	15		°C
I_{lim}	DC Short Circuit Current	V_{CC}=13V 5V<V_{CC}<36V	30	45	75 75	A A
V_{demag}	Turn-off Output Clamp Voltage	I_{OUT}=2A; V_{IN}=0V; L=6mH	V_{CC}-41	V_{CC}-48	V_{CC}-55	V
V_{ON}	Output Voltage Drop Limitation	I_{OUT}=1A; T_j=-40°C....+150°C		50		mV

Note 2: current sense signal delay after positive input slope
Note: sense pin doesn't have to be left floating.

**Figure 1:** I_{OUT}/I_{SENSE} versus I_{OUT}
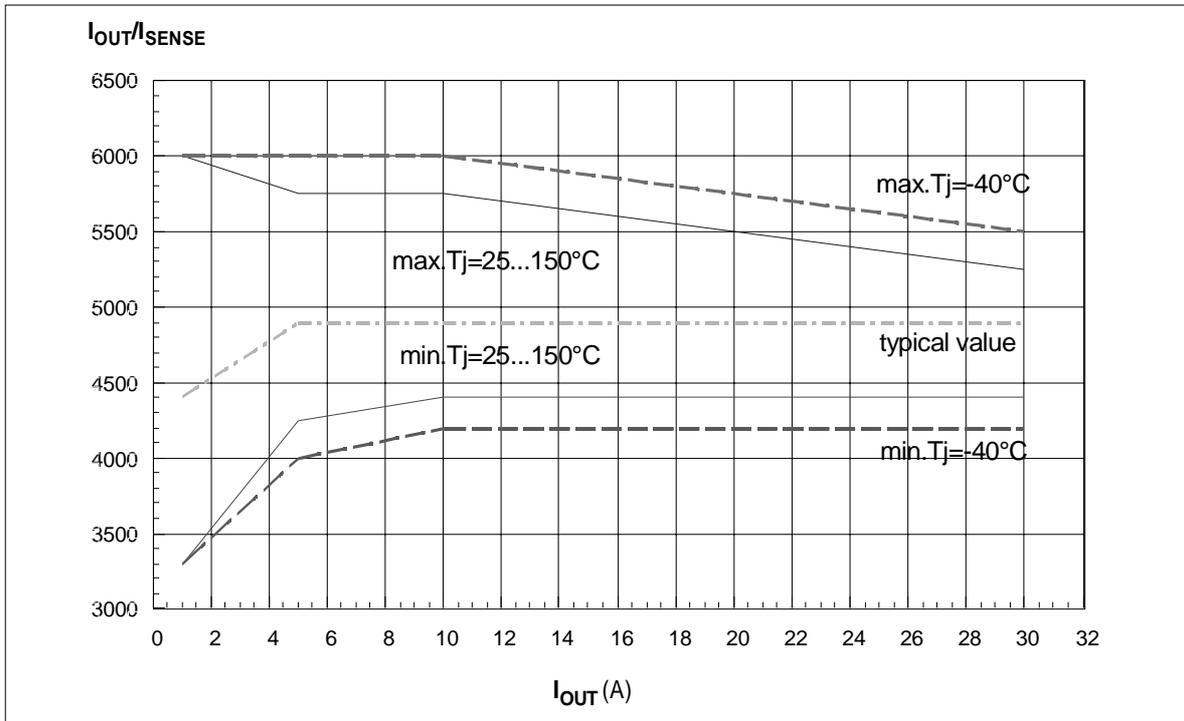
Figure 2: Switching Characteristics (Resistive load $R_L = 1.3\Omega$)

VN920 / VN920-B5 / VN920SO
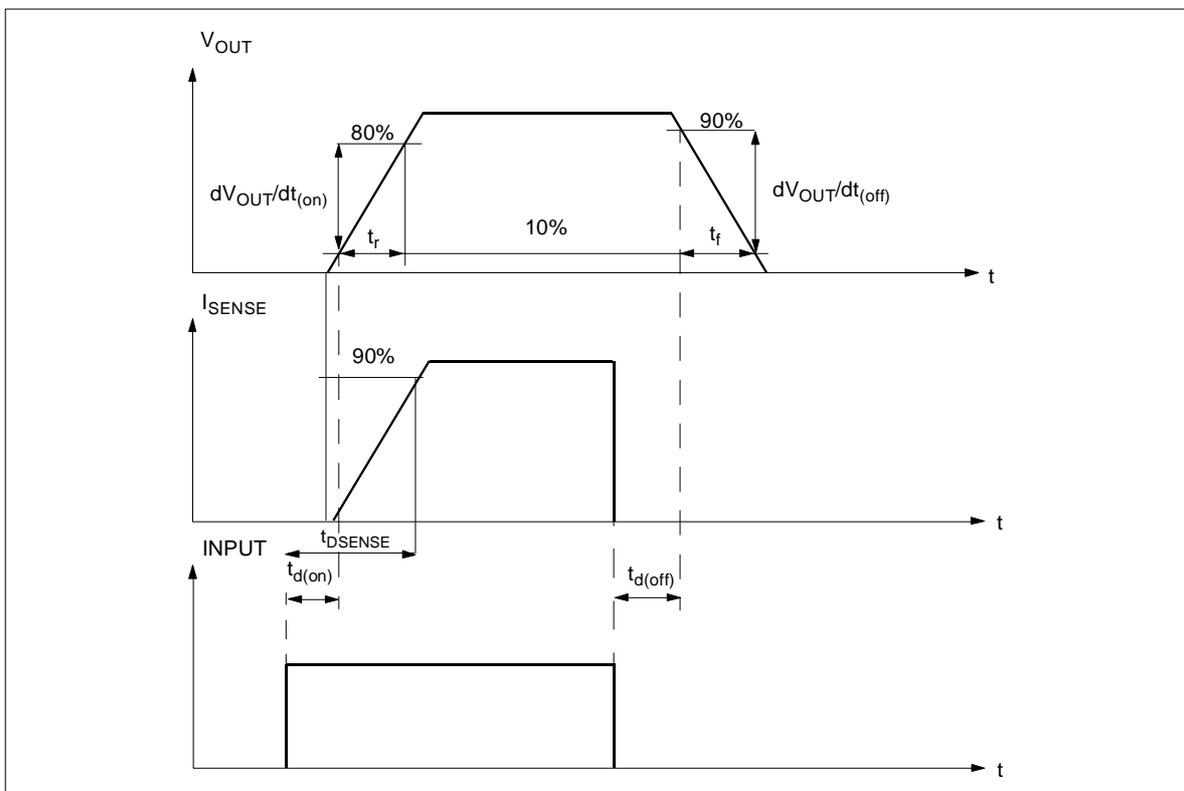
TRUTH TABLE

CONDITIONS	INPUT	OUTPUT	SENSE
Normal operation	L H	L H	0 Nominal
Overtemperature	L H	L L	0 V_{SENSEH}
Undervoltage	L H	L L	0 0
Overvoltage	L H	L L	0 0
Short circuit to GND	L H H	L L L	0 $(T_j<T_{TSD})$ 0 $(T_j>T_{TSD})$ V_{SENSEH}
Short circuit to V_{CC}	L H	H H	0 < Nominal
Negative output voltage clamp	L	L	0

ELECTRICAL TRANSIENT REQUIREMENTS

ISO T/R 7637/1 Test Pulse	TEST LEVELS				
	I	II	III	IV	Delays and Impedance
1	-25 V	-50 V	-75 V	-100 V	2 ms 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 µs 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 µs 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

ISO T/R 7637/1 Test Pulse	TEST LEVELS RESULTS			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

CLASS	CONTENTS
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

Figure 3: Waveforms

NORMAL OPERATION

INPUT
LOAD CURRENT
SENSE

UNDERVOLTAGE

V_{CC}
$V_{USDhyst}$
V_{USD}
INPUT
LOAD CURRENT
SENSE

OVERVOLTAGE

V_{OV}
V_{CC}
$V_{CC} > V_{USD}$
V_{OVhyst}
INPUT
LOAD CURRENT
SENSE

SHORT TO GROUND

INPUT
LOAD CURRENT
LOAD VOLTAGE
SENSE

SHORT TO V_{CC}

INPUT
LOAD VOLTAGE
LOAD CURRENT
SENSE
<Nominal   <Nominal

OVERTEMPERATURE

T_j
T_{TSD}
T_R
INPUT
LOAD CURRENT
SENSE
$I_{SENSE} = \dfrac{V_{SENSEH}}{R_{SENSE}}$
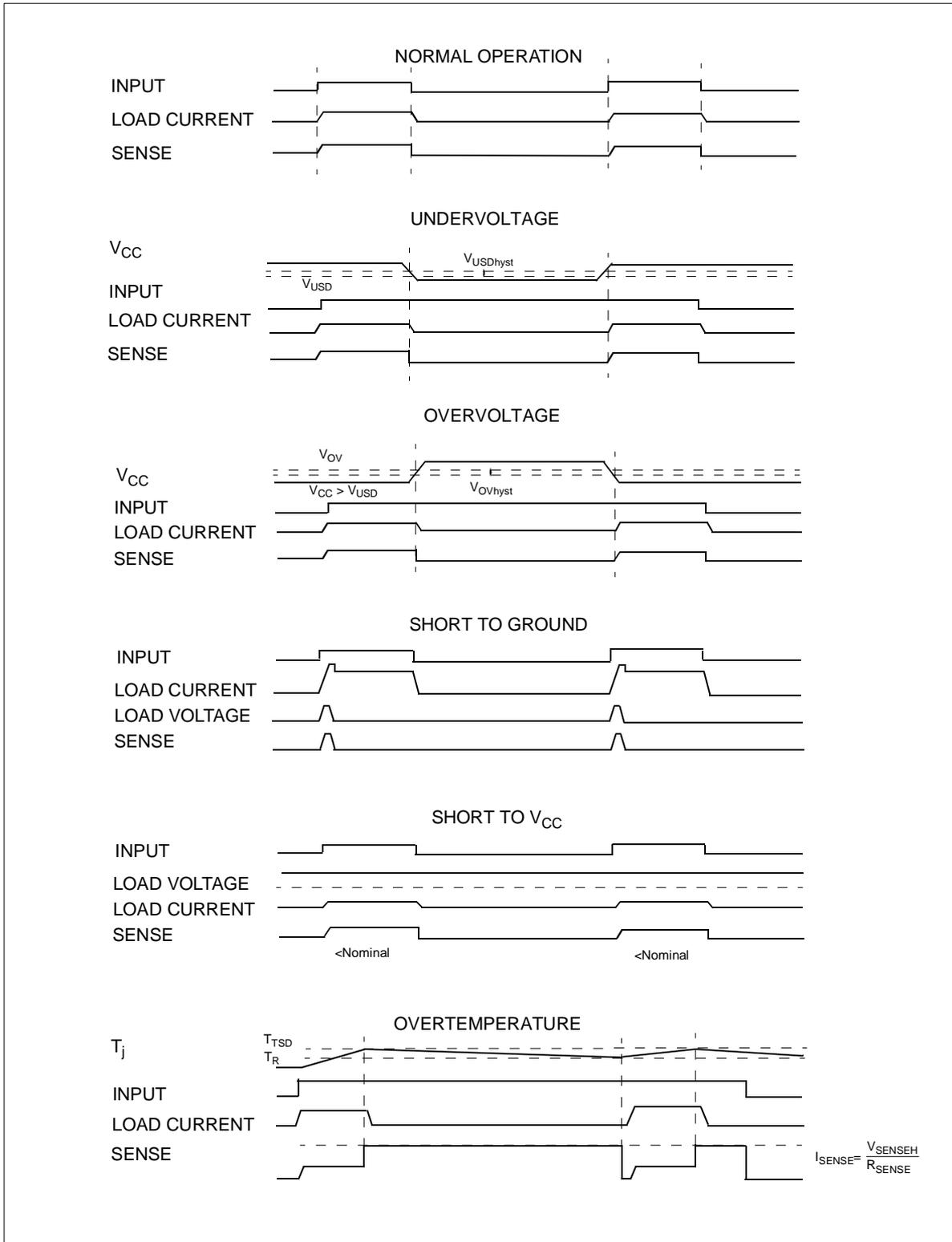
APPLICATION SCHEMATIC
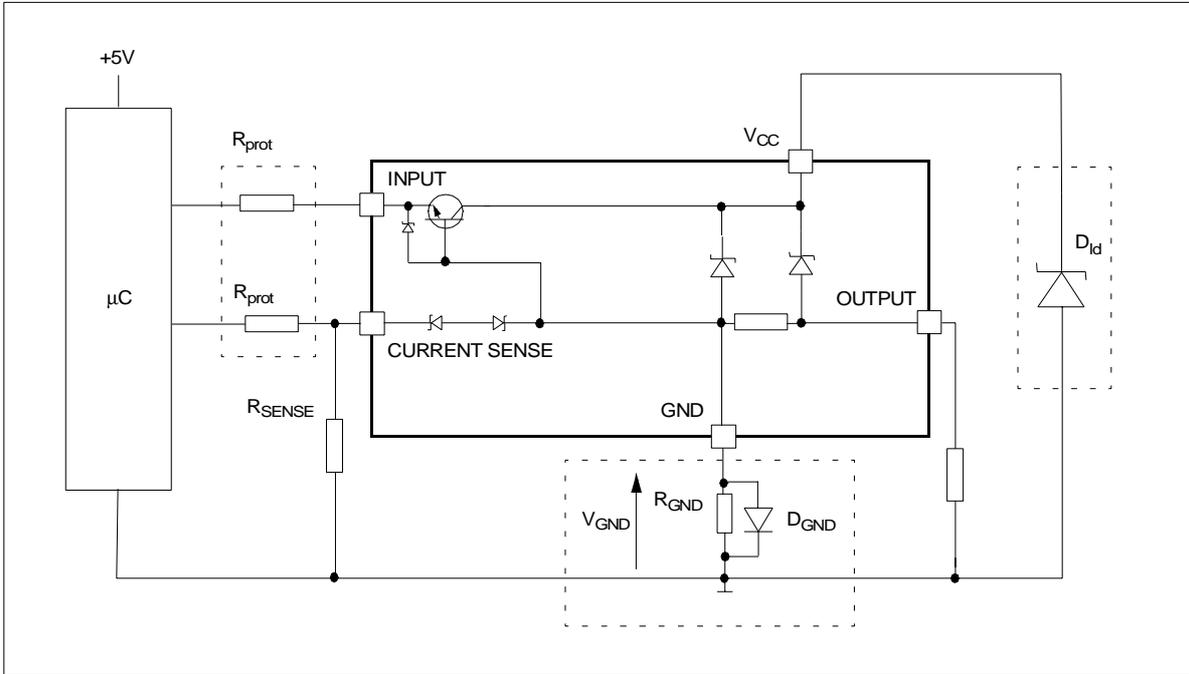
GND PROTECTION NETWORK AGAINST REVERSE BATTERY

Solution 1: Resistor in the ground line (R_{GND} only). This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

1) $R_{GND} \leq 600mV / (I_{S(on)max})$.

2) $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power Dissipation in R_{GND} (when $V_{CC}<0$: during reverse battery situations) is:

$P_D = (-V_{CC})^2/R_{GND}$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the R_{GND} will produce a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND}.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggests to utilize Solution 2 (see below).

Solution 2: A diode (D_{GND}) in the ground line.

A resistor ($R_{GND}=1k\Omega$) should be inserted in parallel to D_{GND} if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift ($\approx 600mV$) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

LOAD DUMP PROTECTION

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds V_{CC} max DC rating. The same applies if the device will be subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/1 table.

μC I/Os PROTECTION:

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the μC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of μC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of μC I/Os.

$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C}-V_{IH}-V_{GND}) / I_{IHmax}$

Calculation example:

For $V_{CCpeak}= - 100V$ and $I_{latchup} \geq 20mA$; $V_{OH\mu C} \geq 4.5V$

$5k\Omega \leq R_{prot} \leq 65k\Omega$.

Recommended R_{prot} value is $10k\Omega$.

Off State Output Current
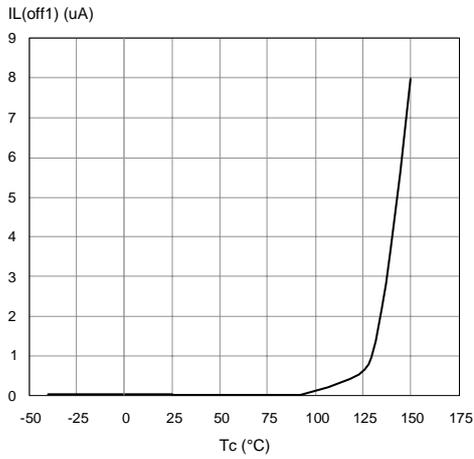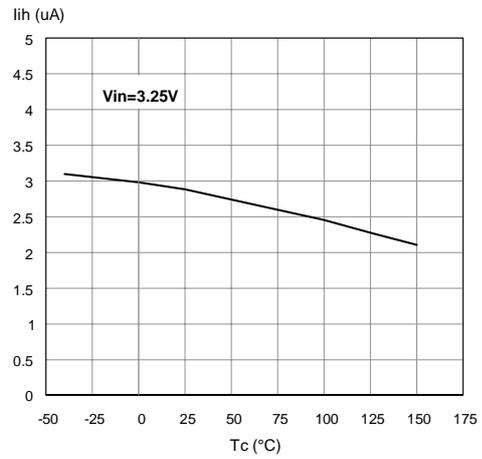
IL(off1) (uA)

Tc (°C)

High Level Input Current

Iih (uA)
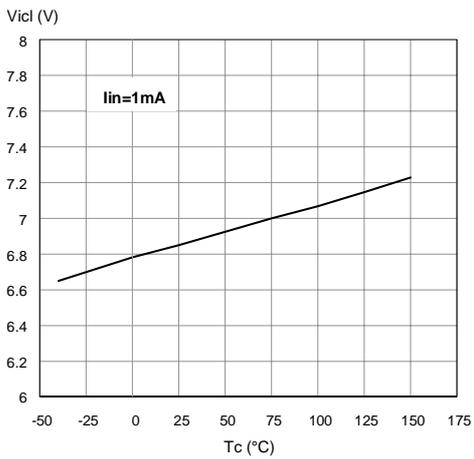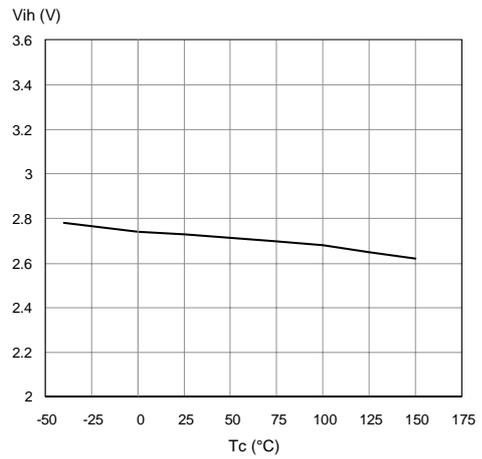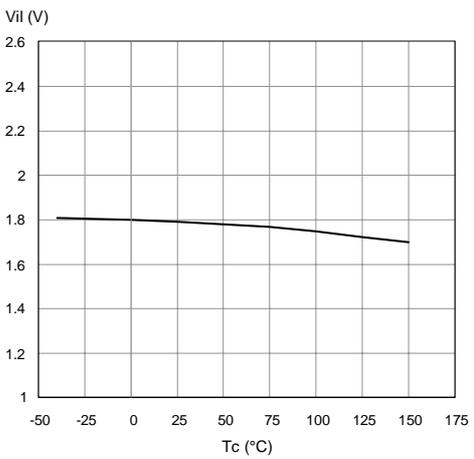
Vin=3.25V

Tc (°C)

Input Clamp Voltage

Vicl (V)

Iin=1mA

Tc (°C)

Input High Level

Vih (V)

Tc (°C)

Input Low Level

Vil (V)

Tc (°C)

Input Hysteresis Voltage

Vhyst (V)

Tc (°C)

Overvoltage Shutdown

Vov (V)

I_{LIM} Vs T_{case}

Ilim (A)

Vcc=13V

Turn-on Voltage Slope

dVout/dt(on) (V/ms)

Vcc=13V
RI=1.3Ohm

Turn-off Voltage Slope

dVout/dt(off) (V/ms)

Vcc=13V
RI=1.3Ohm

On State Resistance Vs T_{case}

Ron (mOhm)

Iout=10A
Vcc=8V; 36V

On State Resistance Vs V_{CC}

Ron (mOhm)

Tc= 150ºC

Tc= 25ºC
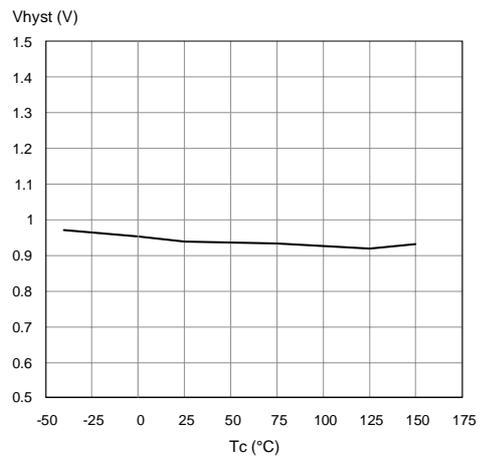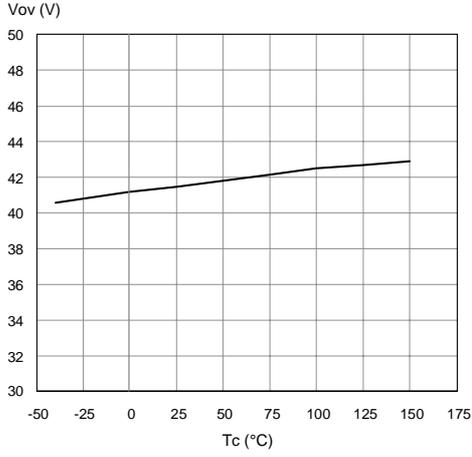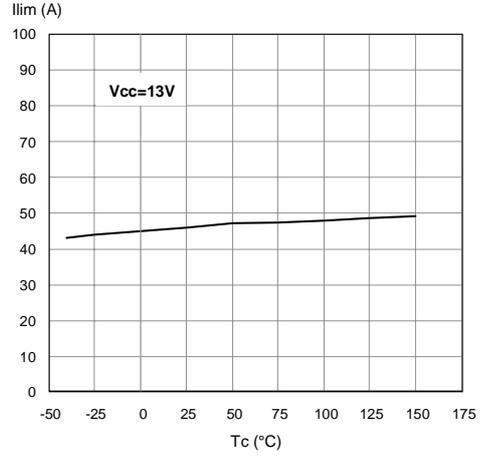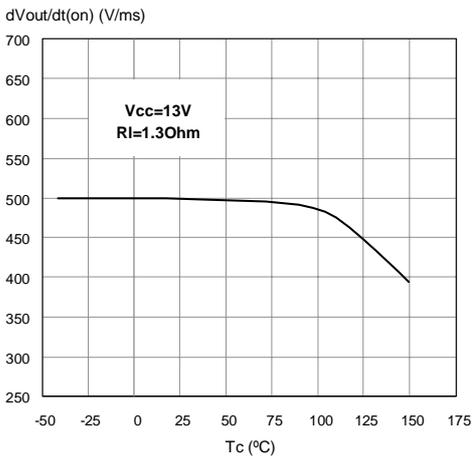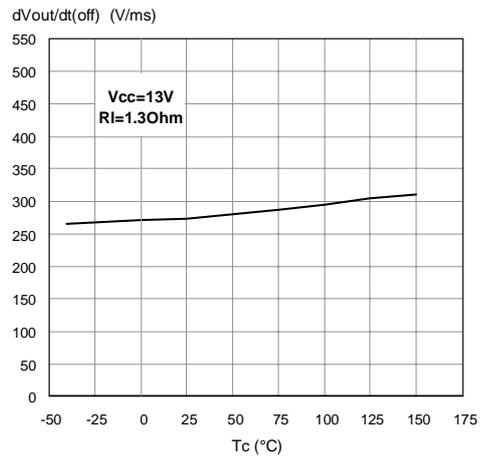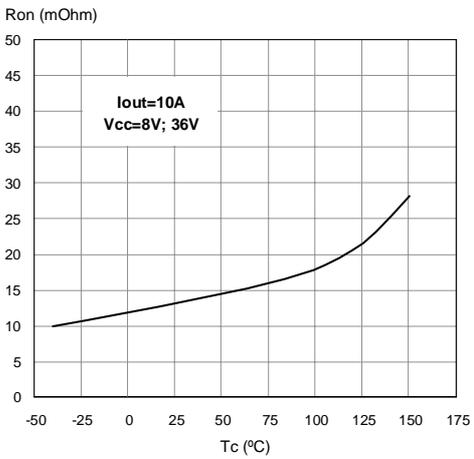
Tc= - 40ºC
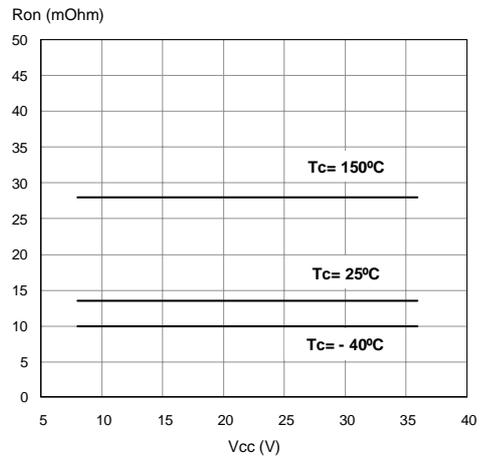
SO-16L Maximum turn off current versus load inductance
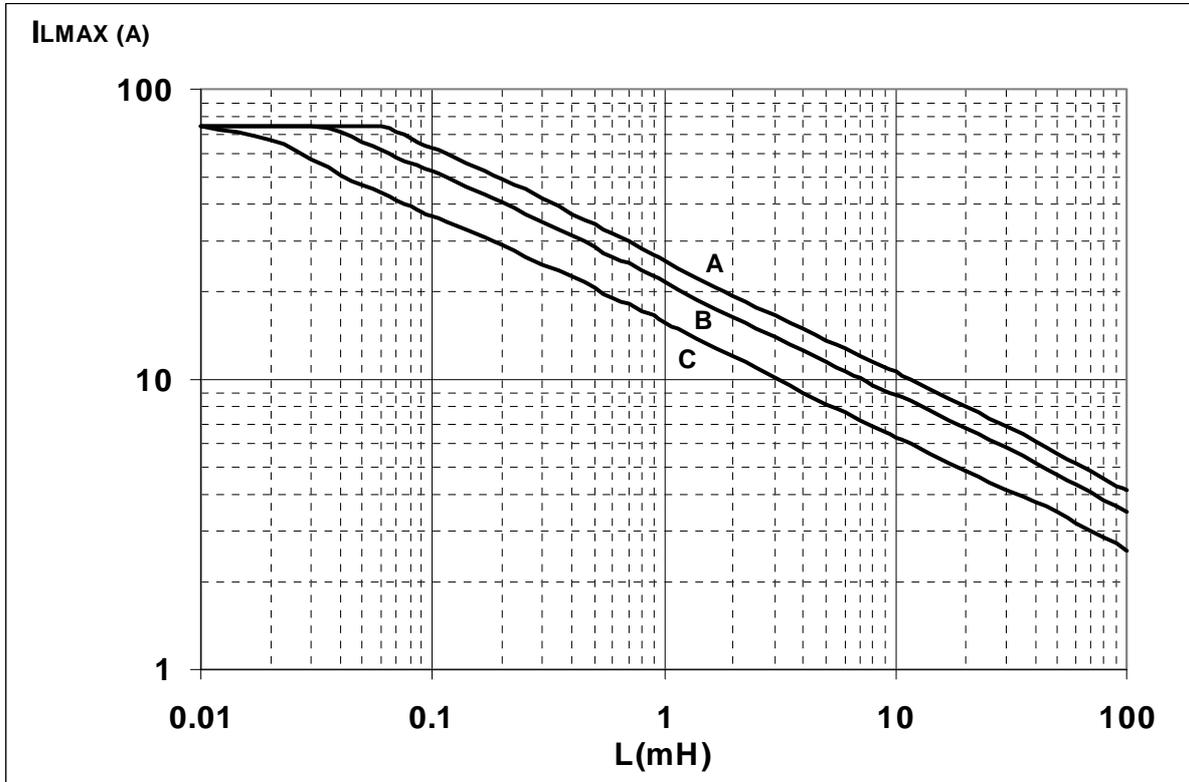
I_{LMAX} (A)

A = Single Pulse at T_{Jstart}=150ºC

B= Repetitive pulse at T_{Jstart}=100ºC

C= Repetitive Pulse at T_{Jstart}=125ºC

Conditions:

V_{CC}=13.5V

Values are generated with R_L=0Ω

In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

V_{IN}, I_L

**P^{2}PAK Maximum turn off current versus load inductance**
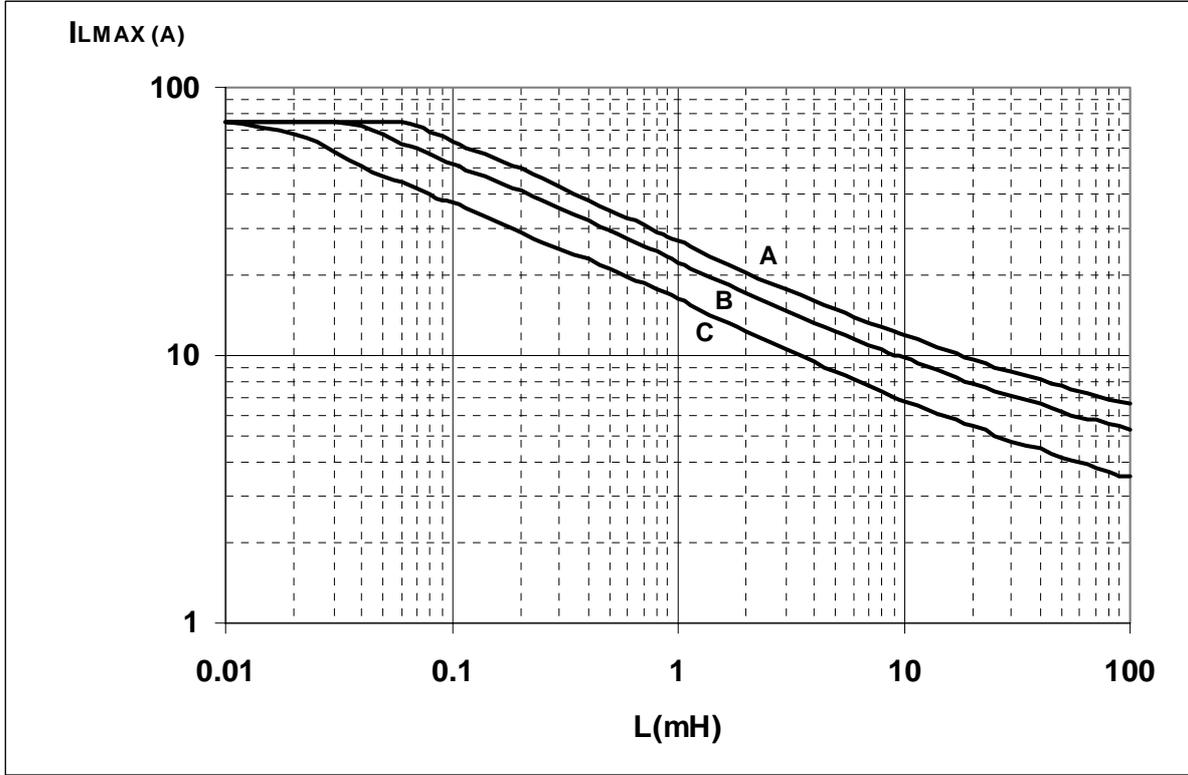
A = Single Pulse at T$_{Jstart}$=150ºC

B= Repetitive pulse at T$_{Jstart}$=100ºC

C= Repetitive Pulse at T$_{Jstart}$=125ºC

Conditions:

V$_{CC}$=13.5V

Values are generated with R$_L$=0Ω

In case of repetitive pulses, T$_{jstart}$ (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.
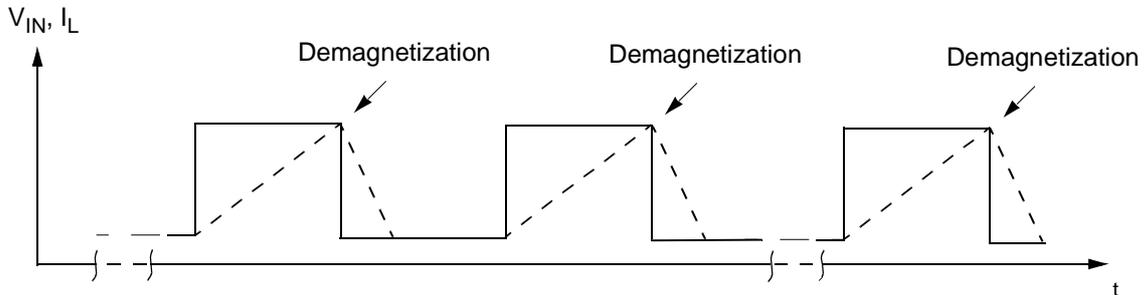
P^{2}PAK THERMAL DATA

P^{2}PAK PC Board
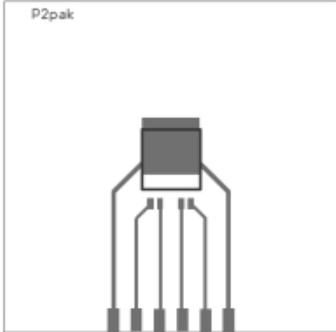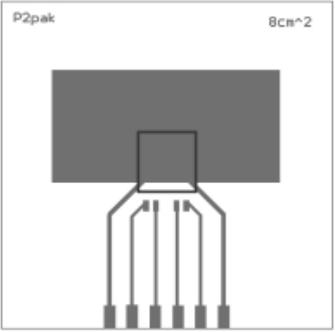
Layout condition of R$_{th}$ and Z$_{th}$ measurements (PCB FR4 area= 60mm x 60mm, PCB thickness=2mm, Cu thickness=35μm, Copper areas: 0.97cm^2, 8cm^2).

**R$_{thj-amb}$ Vs PCB copper area in open box free air condition**
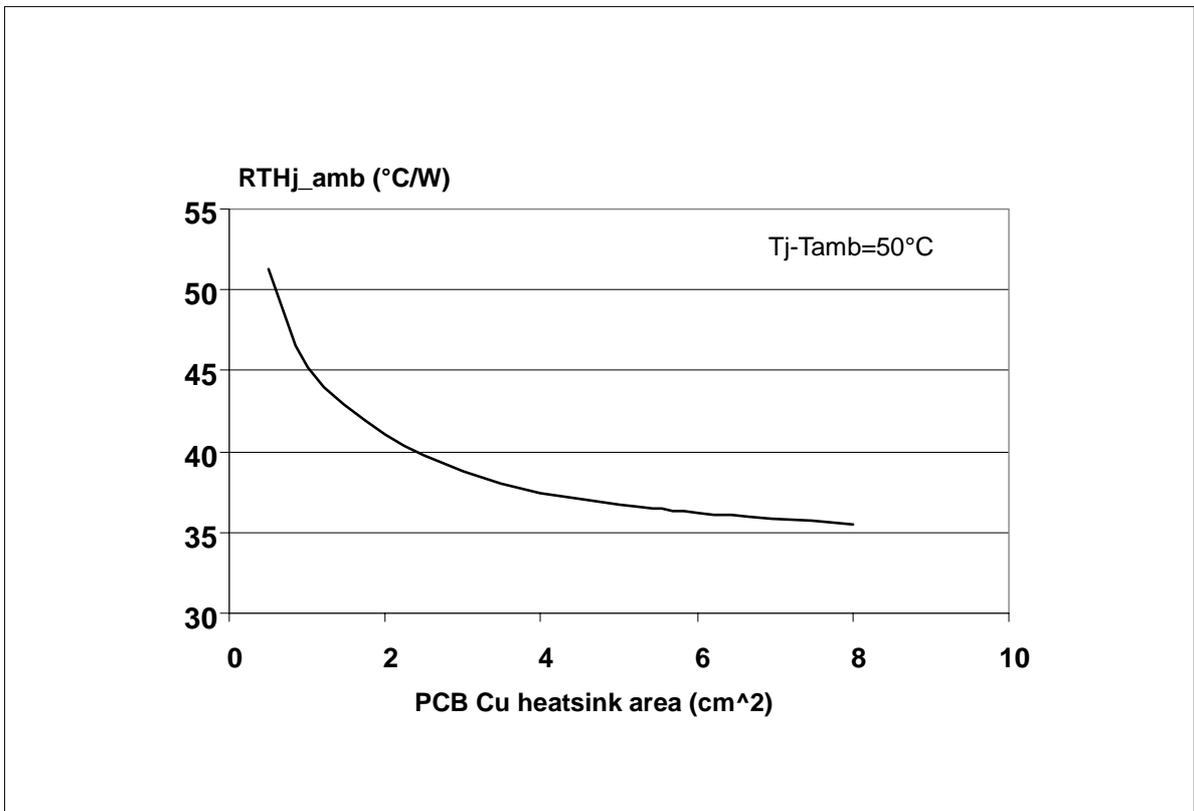
## SO-16L THERMAL DATA

SO-16L PC Board

Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area= 41mm x 48mm, PCB thickness=2mm, Cu thickness=35μm, Copper areas: $0.5cm^2$, $6cm^2$).
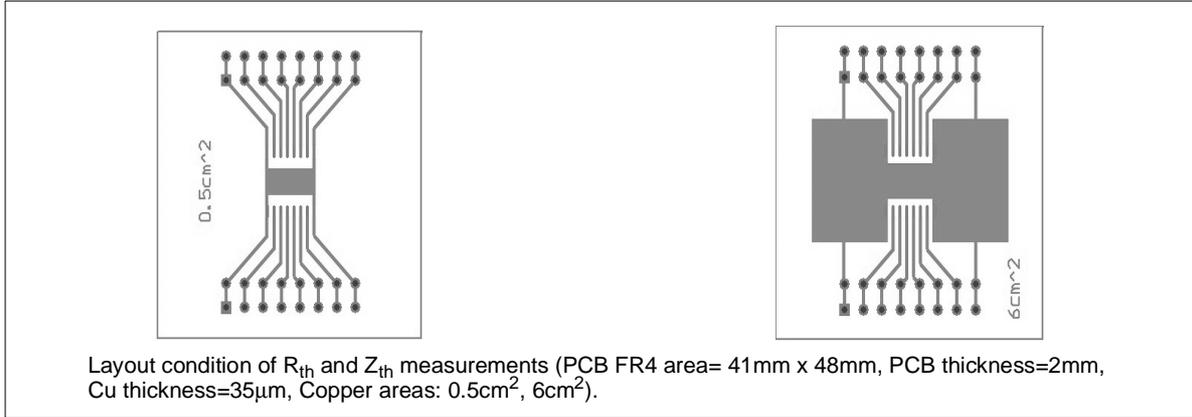
$R_{thj-amb}$ Vs PCB copper area in open box free air condition
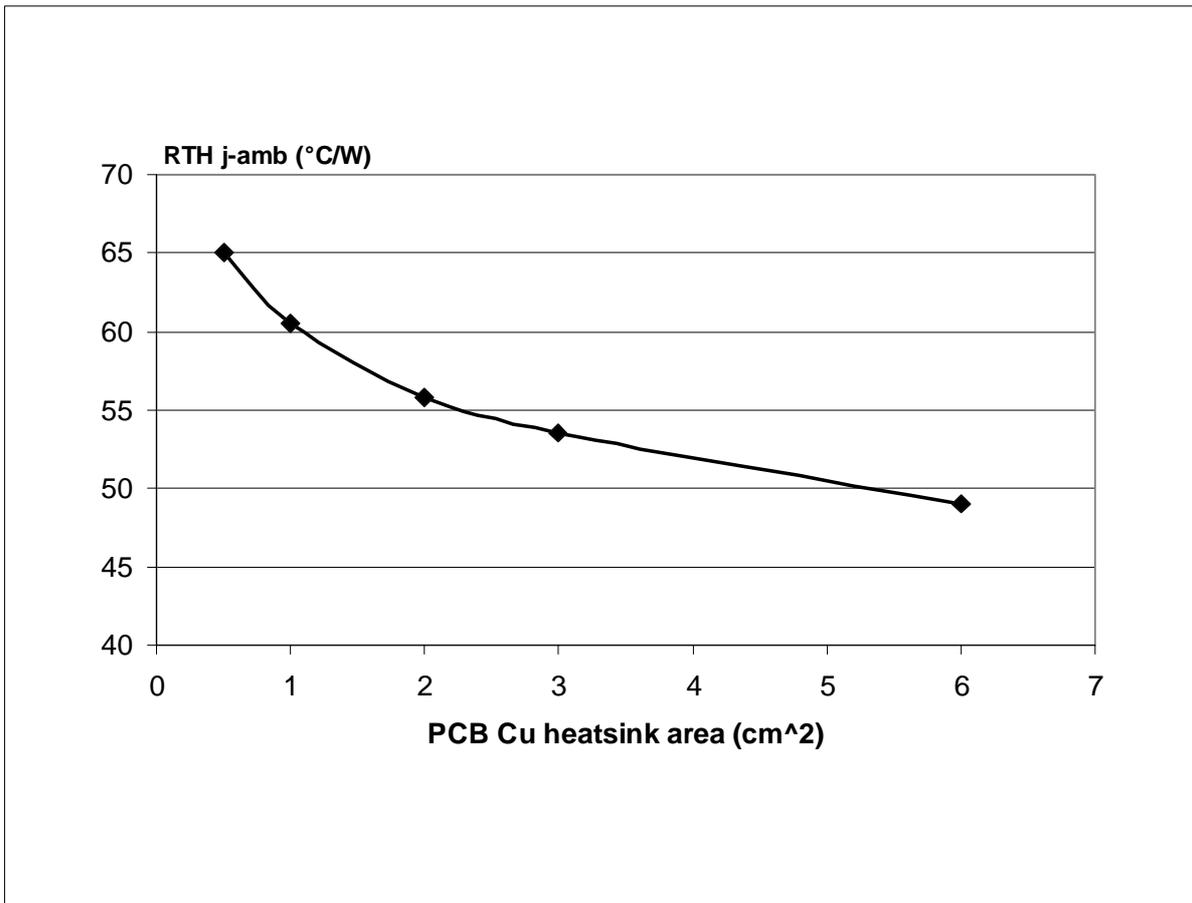
SO-16L Thermal Impedance Junction Ambient Single Pulse

ZTH (°C/W)

Time (s)
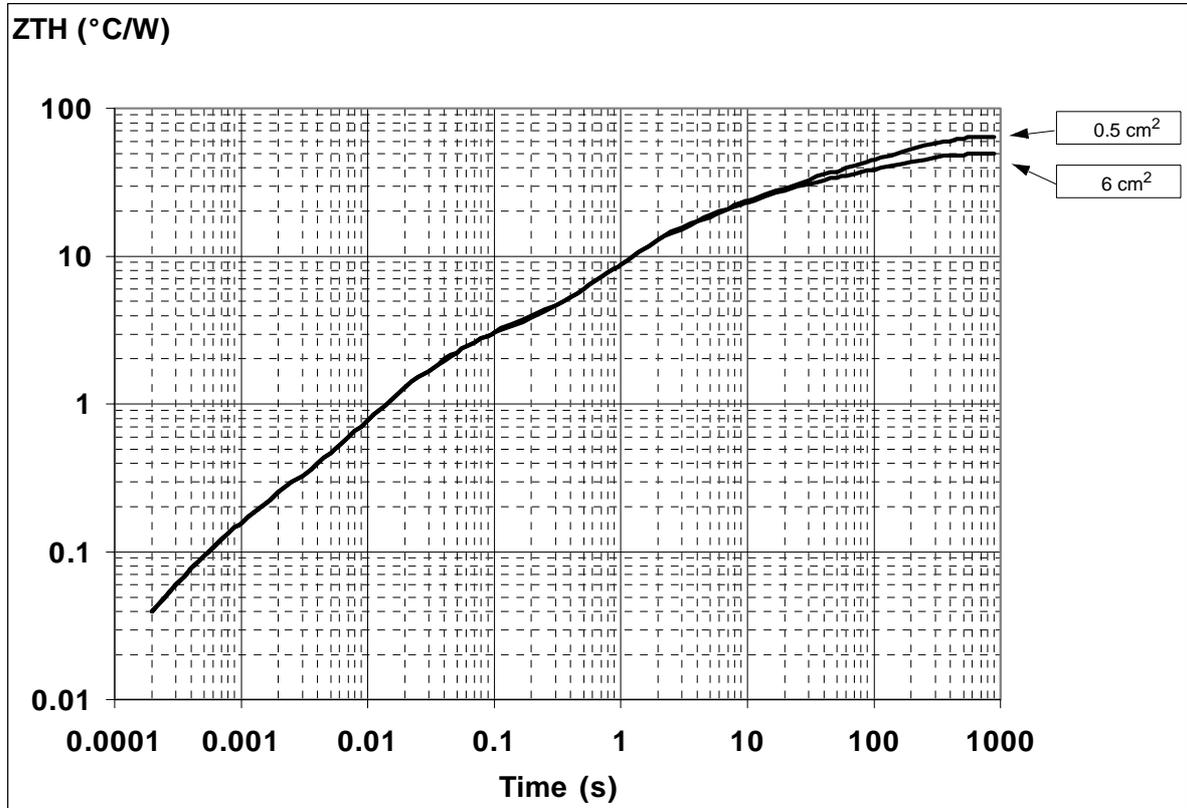
Thermal fitting model of a single channel HSD in SO-16L
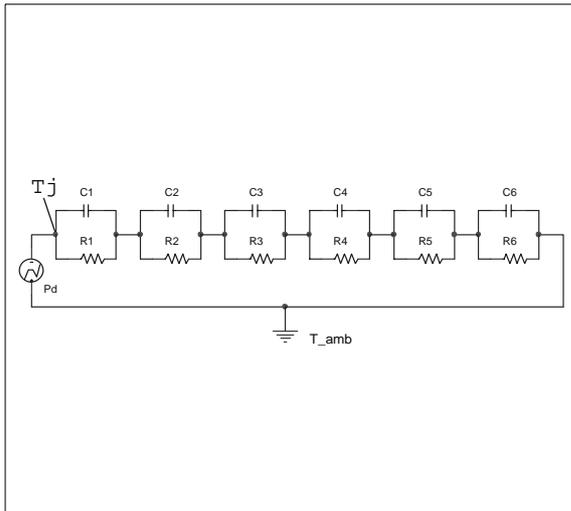

Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\quad \delta = t_p / T$

Thermal Parameter

Area/island (cm²)	0.5	6
R1 (°C/W)	0.02	
R2 (°C/W)	0.1	
R3 (°C/W)	2.2	
R4 (°C/W)	12	
R5 (°C/W)	15	
R6 (°C/W)	35	20
C1 (W.s/°C)	0.0015	
C2 (W.s/°C)	7.00E-03	
C3 (W.s/°C)	1.50E-02	
C4 (W.s/°C)	0.14	
C5 (W.s/°C)	1	
C6 (W.s/°C)	5	8

P^{2}PAK Thermal Impedance Junction Ambient Single Pulse
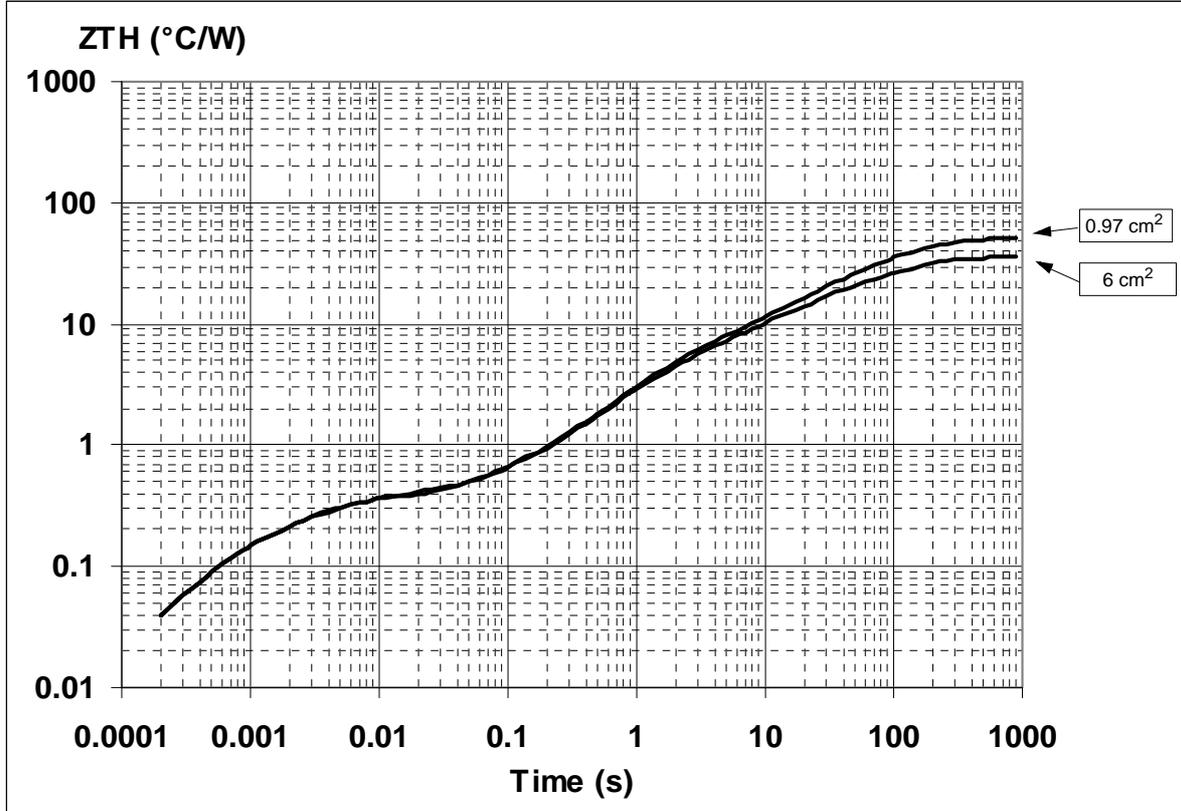
Thermal fitting model of a single channel HSD in P^{2}PAK
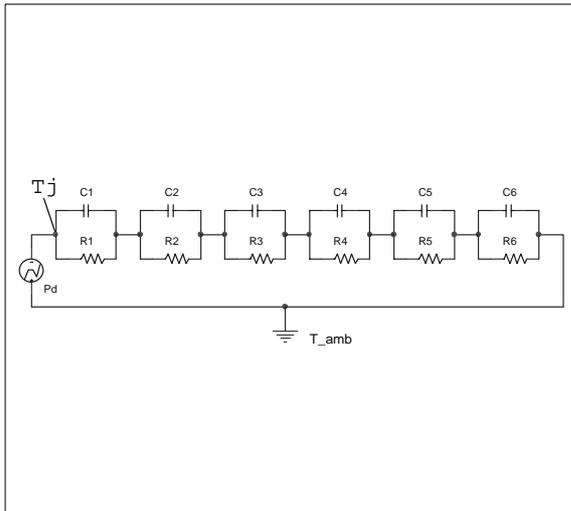
Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\quad \delta = t_p / T$

Thermal Parameter

Area/island (cm^2)	0.97	6
R1 (°C/W)	0.02	
R2 (°C/W)	0.1	
R3 (°C/W)	0.22	
R4 (°C/W)	4	
R5 (°C/W)	9	
R6 (°C/W)	37	22
C1 (W.s/°C)	0.0015	
C2 (W.s/°C)	0.007	
C3 (W.s/°C)	0.015	
C4 (W.s/°C)	0.4	
C5 (W.s/°C)	2	
C6 (W.s/°C)	3	5

SO-16L MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.012
C		0.5			0.020	
c1	45° (typ.)					
D	10.1		10.5	0.397		0.413
E	10.0		10.65	0.393		0.419
e		1.27			0.050	
e3		8.89			0.350	
F	7.4		7.6	0.291		0.300
L	0.5		1.27	0.020		0.050
M			0.75			0.029
S	8° (max.)					
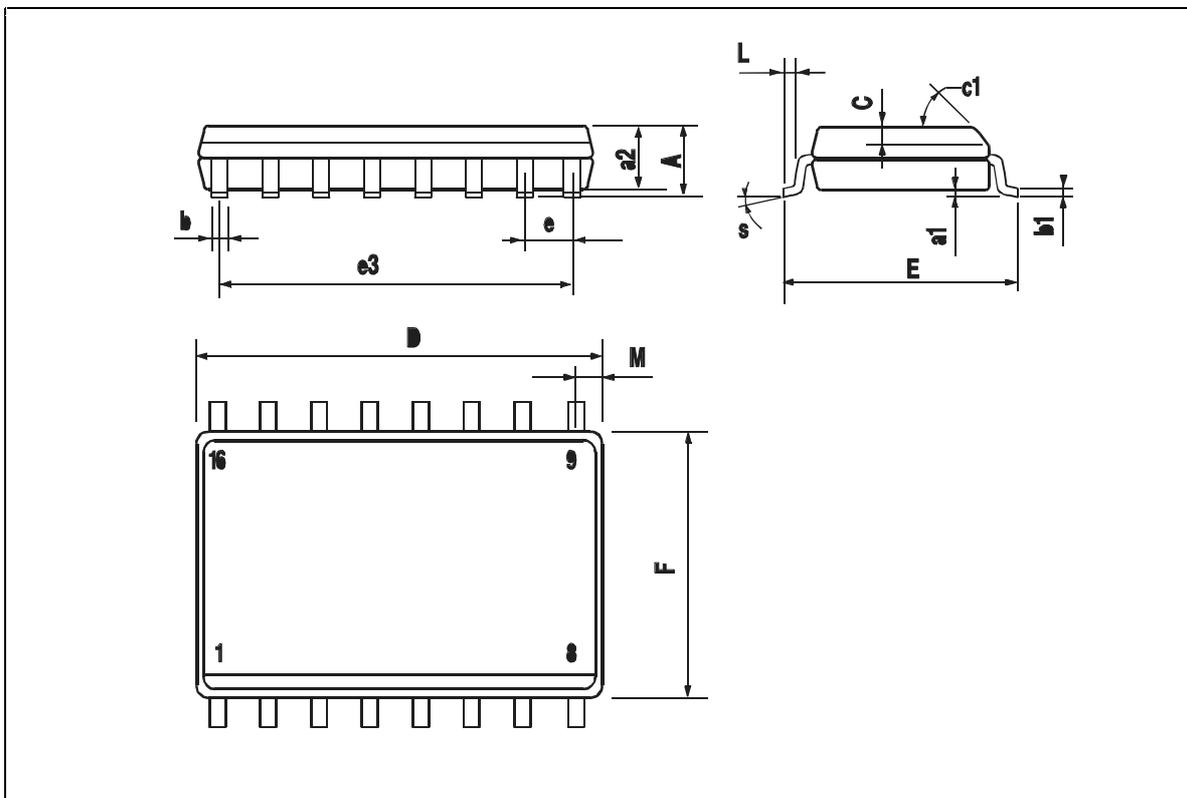
PENTAWATT (VERTICAL) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.8		1.05	0.031		0.041
F1	1		1.4	0.039		0.055
G	3.2	3.4	3.6	0.126	0.134	0.142
G1	6.6	6.8	7	0.260	0.268	0.276
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L		17.85			0.703	
L1		15.75			0.620	
L2		21.4			0.843	
L3		22.5			0.886	
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
M		4.5			0.177	
M1		4			0.157	
Diam.	3.65		3.85	0.144		0.152
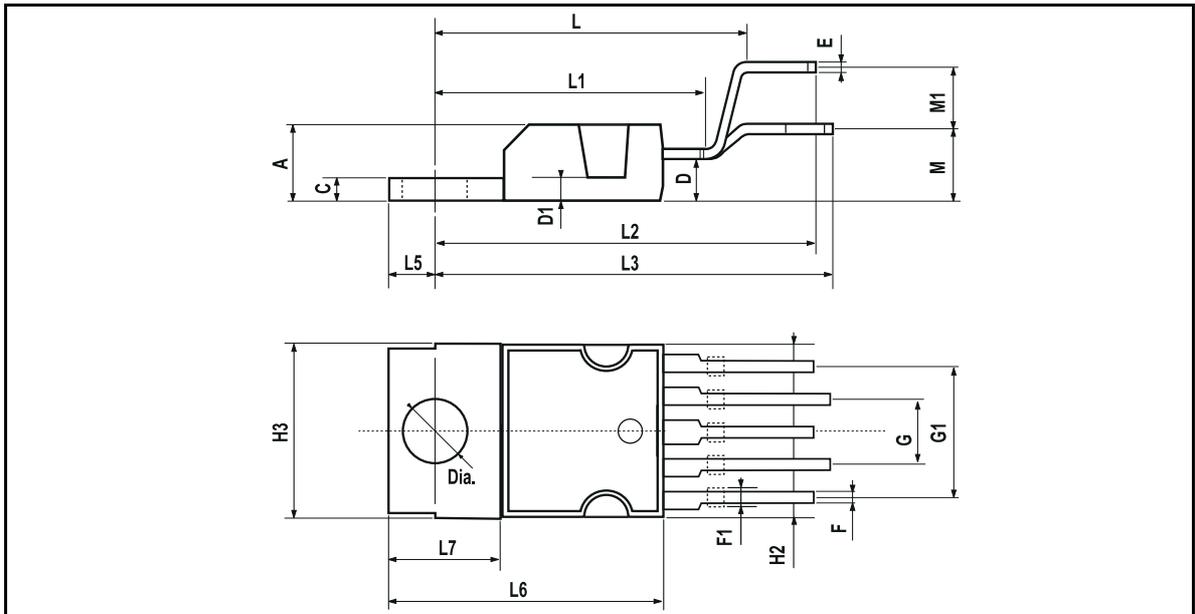
P²PAK MECHANICAL DATA

DIM.	mm.		
	MIN.	TYP	MAX.
A	4.30		4.80
A1	2.40		2.80
A2	0.03		0.23
b	0.80		1.05
c	0.45		0.60
c2	1.17		1.37
D	8.95		9.35
D2		8.00	
E	10.00		10.40
E1		8.50	
e	3.20		3.60
e1	6.60		7.00
L	13.70		14.50
L2	1.25		1.40
L3	0.90		1.70
L5	1.55		2.40
R		0.40	
V2	0º		8º
Package Weight	1.40 Gr (typ)		

COPLANARITY

SCALE 5:1

P010R

* TERMINAL LENGTH FOR SOLDERING NO LESS THAN 1 mm
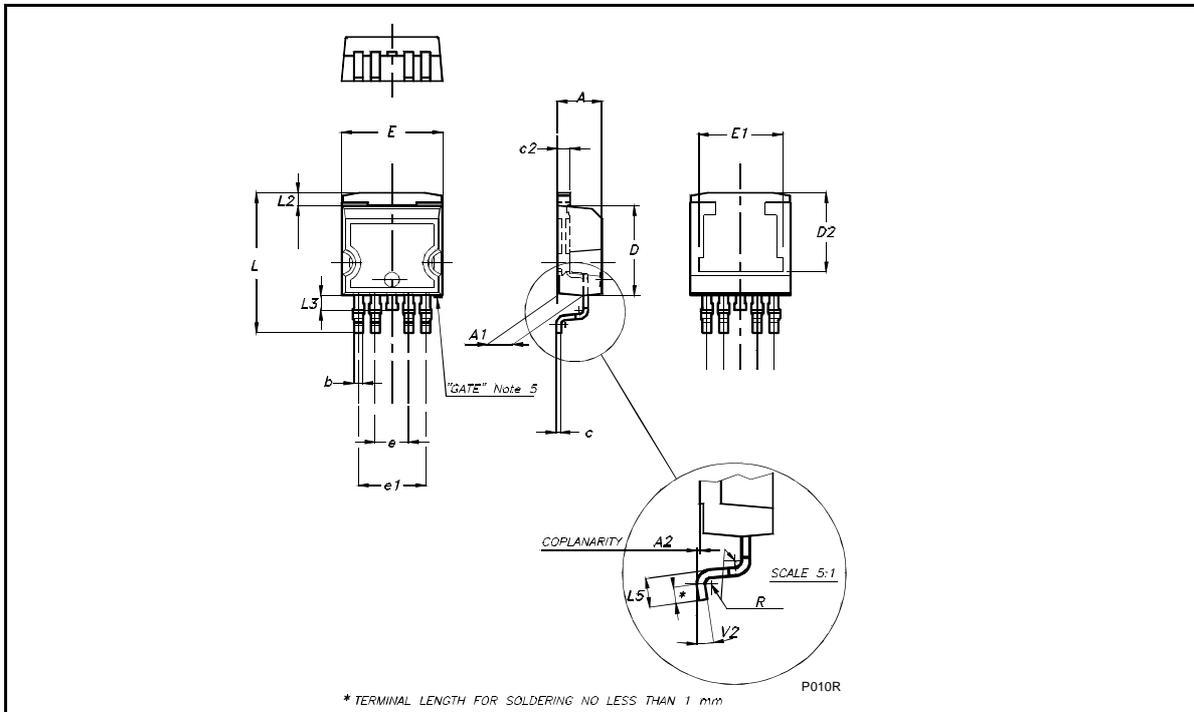
SO-16L TUBE SHIPMENT (no suffix)
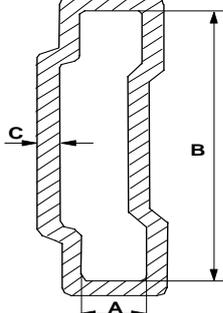
Base Q.ty	50
Bulk Q.ty	1000
Tube length (± 0.5)	532
A	3.5
B	13.8
C (± 0.1)	0.6

All dimensions are in mm.

TAPE AND REEL SHIPMENT (suffix "13TR")
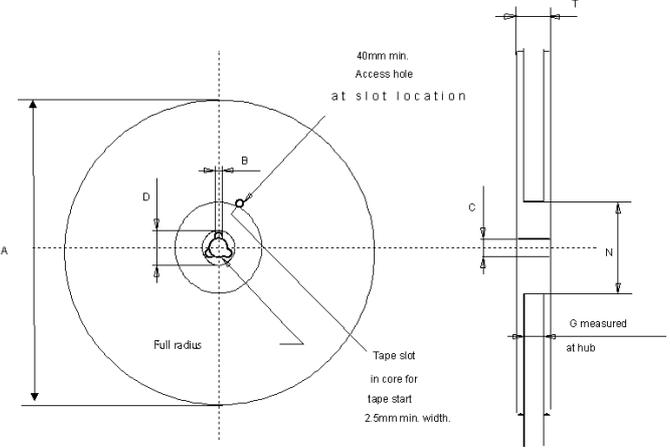
REEL DIMENSIONS

Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	16.4
N (min)	60
T (max)	22.4

TAPE DIMENSIONS

According to Electronic Industries Association
(EIA) Standard 481 rev. A, Feb 1986

Tape width	W	16
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	12
Hole Diameter	D (± 0.1/-0)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.05)	7.5
Compartment Depth	K (max)	6.5
Hole Spacing	P1 (± 0.1)	2
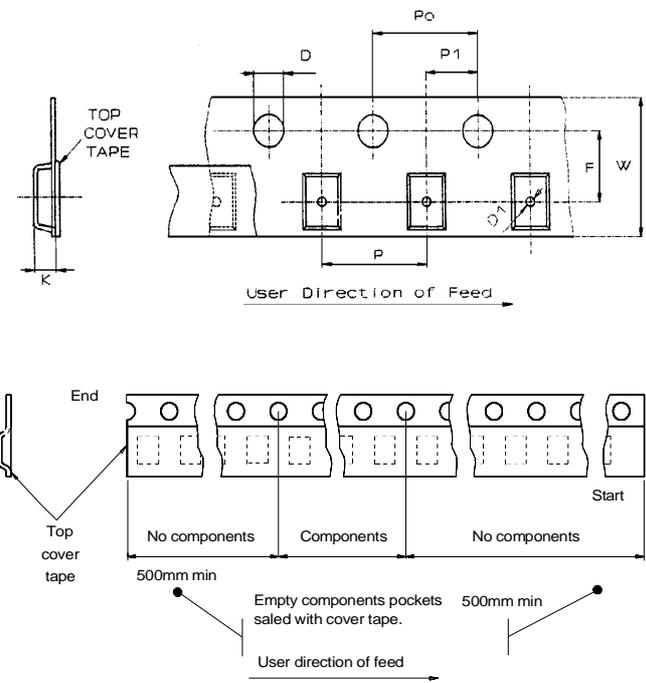
All dimensions are in mm.

PENTAWATT TUBE SHIPMENT (no suffix)

Base Q.ty	50
Bulk Q.ty	1000
Tube length (± 0.5)	532
A	18
B	33.1
C (± 0.1)	1

All dimensions are in mm.

P²PAK TUBE SHIPMENT (no suffix)
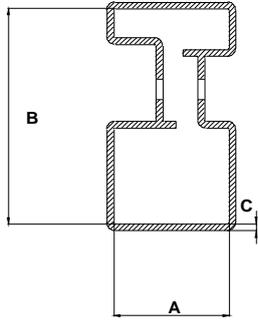
Base Q.ty	50
Bulk Q.ty	1000
Tube length (± 0.5)	532
A	18
B	33.1
C (± 0.1)	1

All dimensions are in mm.

TAPE AND REEL SHIPMENT (suffix "13TR")

40mm min.
Access hole
at slot location

Full radius

Tape slot
in core for
tape start
2.5mm min. width.

G measured
at hub

REEL DIMENSIONS

Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	24.4
N (min)	60
T (max)	30.4

All dimensions are in mm.

TAPE DIMENSIONS

According to Electronic Industries Association
(EIA) Standard 481 rev. A, Feb 1986

Tape width	**W**	24
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	16
Hole Diameter	**D (± 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	11.5
Compartment Depth	**K (max)**	6.5
Hole Spacing	**P1 (± 0.1)**	2

All dimensions are in mm.

TOP
COVER
TAPE
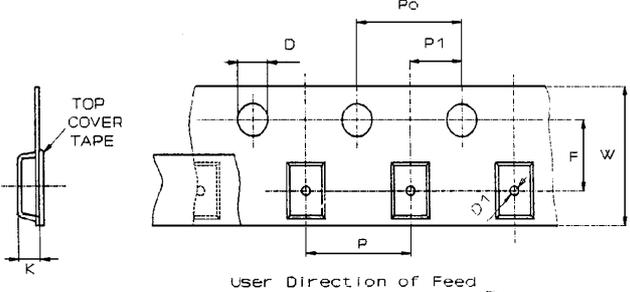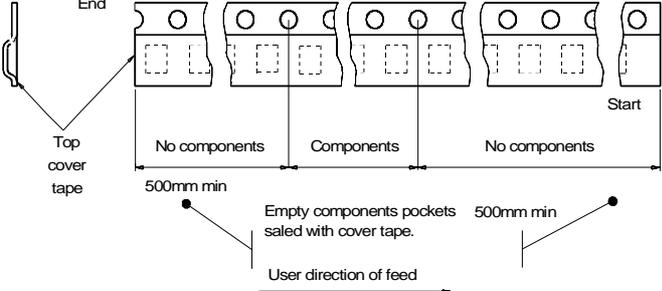
User Direction of Feed

User Direction of Feed

End

Start

Top
cover
tape

No components   Components   No components

500mm min

Empty components pockets
saled with cover tape.

500mm min

User direction of feed

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