

# VCC4A

# **CMOS Crystal Oscillator**

## Features

- Ultra Low Jitter, Fundamental or 3rd OT Crystal Design
- CMOS Output Crystal Oscillator
- Output Frequencies from 1.024 MHz to 160.000 MHz
- +1.8, +2.5, +3.3 or +5.0V Operation
- Output Disable Feature
- Excellent ±25 ppm temperature stability
- -10/70°C or -40/85°C operating temperature
- Small Industry Standard Package, 5 x 3.2 mm
- Product is Compliant to RoHS Directive and Fully Compatible with Lead-Free Assembly (Excluding Solder Dipped, \_SNPB, Option)

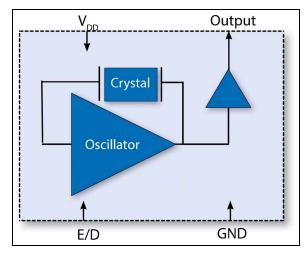
#### **Applications**

- SONET/SDH/DWDM
- Ethernet, GE, SynchE
- Storage Area Networking
- Fiber Channel
- Digital Video
- Broadband Access
- · Base Stations, Picocells
- Driving A/D's, D/A's, FPGA's
- Test and Measurement
- COTS

## **General Description**

Microchip's VCC4A Crystal Oscillator (XO) is a quartz stabilized square wave generator with a CMOS output. The VCC4A uses a fundamental or third overtone crystal, resulting in very low jitter performance, and a monolithic IC, which improves reliability and reduces cost.

#### **Block Diagram**



## 1.0 ELECTRICAL CHARACTERISTICS

## Absolute Maximum Ratings †

Storage Temperature (T <sub>S</sub> )	–55°C to +125°C
Soldering Temperature, 30 seconds (T <sub>LS</sub> )	
ESD Rating (Human Body Model, JES22-A115 Conditions, Note 1)	
ESD Rating (Charged Device Model, JESD22-C101E Conditions, Note 1)	

**† Notice:** Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability. Permanent damage is also possible if Enable/Disable is applied before V<sub>DD</sub>.

**Note 1:** Although ESD protection circuitry has been designed into the VCC4A, proper precautions should be taken when handling and mounting. Microchip employs a human body model (HBM) and a charged device model (CDM) for ESD susceptibility testing and design protection evaluation.

Parameter	Symbol	Min.	Тур.	Max.	Units	Conditions
Supply						·
Voltage (Note 1)	V <sub>DD</sub>	4.5	5.0	5.5	V	—
Max. Supply Voltage	_	-0.5		7.0	V	$-\Delta V_{OUT}/(\Delta V_{OUT} \times \Delta V_{IN})$
Max. Voltage E/D	_	-0.5		V <sub>DD</sub> + 0.5	V	—
			_	5		≤12 MHz
		_	_	13		12.001 MHz to 20 MHz
Current (Note 2)	I <sub>DD</sub>			18	mA	20.001 MHz to 40 MHz
			_	21		40.001 MHz to 65 MHz
				30		65.001 MHz to 100 MHz
Current	I <sub>DD</sub>	—	_	10	μA	Output Disabled
Frequency						·
Nominal Frequency	f <sub>NOM</sub>	1.024	_	100.000	MHz	—
	f <sub>STAB</sub>	—	±25	_		
Frequency Stability (Note 3)			±50		ppm	Ordering option.
			±100	_		
Outputs						·
Output Logic Level High	V <sub>OH</sub>	$0.9 \times V_{DD}$	_	_	V	
Output Logic Level Low	V <sub>OL</sub>	—	_	0.1 × V <sub>DD</sub>	v	Note 2
Load	I <sub>OUT</sub>	—	15	50	pF	—
		—	_	8		≤20 MHz
Output Rise/Fall Time (Note 2)	t <sub>r</sub> /t <sub>f</sub>	_	_	5	ns	20.001 MHz to 50 MHz
(1000 2)		_	_	3		50.001 MHz to 100 MHz
Output Leakage	Ι <sub>Ζ</sub>	—	_	±10	μA	Output disabled
Duty Cycle	DC	45	50	55	%	Note 2, Note 4
Deried litter (Nete 5)	•		2.4		20	100 MHz, RMS
Period Jitter (Note 5)	фJ		23		ps	100 MHz, peak-to-peak
RMS Jitter (Note 6)	фJ	—	65	100	fs	12 kHz to 20 MHz

## **ELECTRICAL CHARACTERISTICS, 5.0V OPTION**

## **ELECTRICAL CHARACTERISTICS, 5.0V OPTION (CONTINUED)**

Parameter	Symbol	Min.	Тур.	Max.	Units	Conditions
Enable/Disable						
Output Enable Voltage	V <sub>IH</sub>	0.7 × V <sub>DD</sub>		_	V	Noto 7
Output Disable Voltage	V <sub>IL</sub>	—	_	0.4	V	Note 7
Disable Time	t <sub>D</sub>	_	_	100	ns	—
Start-Up Time	t <sub>SU</sub>	_	_	10	ms	—
Operating Temperature	т	-10		+70	*0	Ordering option
Range	T <sub>OP</sub>	-40	_	+85	°C	

Note 1: The power supply should have bypass capacitors as close to the supply and to ground as possible. For example, 0.1  $\mu$ F and 0.01  $\mu$ F.

2: Parameters are tested with the test circuit shown in Figure 1-1. Add [(50 pF – 15 pF) × V<sub>DD</sub> × f<sub>OUT</sub>(in MHz) x 0.001] mA for the 50 pF option.

**3:** Includes initial accuracy, operating temperature, supply voltage, shock and vibration (not under operation), and 10 years' aging for ±50 ppm and ±100 ppm options.

- 4: Duty cycle is measured as On-Time/Period. See Figure 1-2.
- **5:** Broadband period jitter measured using a LeCroy Waverunner 610Zi, 100k samples.
- 6: Measured using an Agilent E5052 or equivalent at 100 MHz and +25°C.
- 7: The output is enabled if Enable/Disable is left open. A 10 k $\Omega$  pull-up to V<sub>DD</sub> is recommended.

## **ELECTRICAL CHARACTERISTICS, 3.3V OPTION**

Parameter	Symbol	Min.	Тур.	Max.	Units	Conditions	
Supply							
Voltage (Note 1)	V <sub>DD</sub>	2.97	3.3	3.63	V	—	
Max. Supply Voltage	—	-0.5	_	7.0	V	—	
Max. Voltage E/D	—	-0.5	_	V <sub>DD</sub> + 0.5	V	—	
		—	_	3		≤12 MHz	
		—	_	4		12.001 MHz to 20 MHz	
		—	_	8		20.001 MHz to 40 MHz	
Current (Note 2)	I <sub>DD</sub>	—	_	18	mA	40.001 MHz to 65 MHz	
		—	_	25		65.001 MHz to 100 MHz	
		—	_	30		100.001 MHz to 133 MHz	
		_	_	40		133.001 MHz to 160 MHz	
Current	I <sub>DD</sub>	_	_	10	μA	Output Disabled	
Frequency							
Nominal Frequency	f <sub>NOM</sub>	1.024	_	160.000	MHz	—	
		_	±25	_			
Frequency Stability (Note 3)	f <sub>STAB</sub>		±50	_	ppm	Ordering option.	
		_	±100				
Outputs	·	•	-	-			
Output Logic Level High	V <sub>OH</sub>	$0.9 \times V_{DD}$			V	Noto 2	
Output Logic Level Low	V <sub>OL</sub>	—	_	0.1 × V <sub>DD</sub>	v	Note 2	
Load	I <sub>OUT</sub>		15	50	pF	—	

## **ELECTRICAL CHARACTERISTICS, 3.3V OPTION (CONTINUED)**

Parameter	Symbol	Min.	Тур.	Max.	Units	Conditions
		—	—	8		≤20 MHz
Output Rise/Fall Time (Note 2)	t <sub>r</sub> /t <sub>f</sub>	_	_	5	ns	20.001 MHz to 50 MHz
		—	_	3		50.001 MHz to 160 MHz
Output Leakage	Ι <sub>Ζ</sub>	—	_	±10	μA	Output disabled
Duty Cycle	DC	45	50	55	%	Note 2, Note 4
Deried litter (Note 5)		—	2.8	_	20	100 MHz, RMS
Period Jitter (Note 5)	фJ	_	25	_	ps	100 MHz, peak-to-peak
RMS Jitter (Note 6)	фJ	—	76	115	fs	12 kHz to 20 MHz
Enable/Disable						
Output Enable Voltage	V <sub>IH</sub>	$0.7 \times V_{DD}$	_	_	V	Note 7
Output Disable Voltage	V <sub>IL</sub>	—	_	0.4	v	Note 7
Disable Time	t <sub>D</sub>	_	_	100	ns	—
Start-Up Time	t <sub>SU</sub>	—		10	ms	—
Operating Temperature	т	-10	_	+70	°C	Ordering option
Range	T <sub>OP</sub>	-40	_	+85		Ordering option

Note 1: The power supply should have bypass capacitors as close to the supply and to ground as possible. For example, 0.1  $\mu$ F and 0.01  $\mu$ F.

**2:** Parameters are tested with the test circuit shown in Figure 1-1. Add [(50 pF - 15 pF) ×  $V_{DD}$  ×  $f_{OUT}$  (in MHz) x 0.001] mA for the 50 pF option.

**3:** Includes initial accuracy, operating temperature, supply voltage, shock and vibration (not under operation), and 10 years' aging for ±50 ppm and ±100 ppm options.

- 4: Duty cycle is measured as On-Time/Period. See Figure 1-2.
- **5:** Broadband period jitter measured using a LeCroy Waverunner 610Zi, 100k samples.
- 6: Measured using an Agilent E5052 or equivalent at 100 MHz and +25°C.
- 7: The output is enabled if Enable/Disable is left open. A 10 k $\Omega$  pull-up to V\_{DD} is recommended.

## **ELECTRICAL CHARACTERISTICS, 2.5V OPTION**

Parameter	Symbol	Min.	Тур.	Max.	Units	Conditions		
Supply								
Voltage (Note 1)	V <sub>DD</sub>	2.25	2.5	2.75	V	—		
Max. Supply Voltage	—	-0.5	—	7.0	V	—		
Max. Voltage E/D	—	-0.5	—	V <sub>DD</sub> + 0.5	V	—		
			_	2		≤12 MHz		
			—	3		12.001 MHz to 20 MHz		
		_	—	7		20.001 MHz to 40 MHz		
Current (Note 2)	I <sub>DD</sub>	_	—	12	mA	40.001 MHz to 65 MHz		
		_	_	18		65.001 MHz to 100 MHz		
		_	_	21		100.001 MHz to 133 MHz		
		_		30		133.001 MHz to 160 MHz		
Current	I <sub>DD</sub>	_	_	10	μA	Output Disabled		

## **ELECTRICAL CHARACTERISTICS, 2.5V OPTION (CONTINUED)**

Parameter	Symbol	Min.	Тур.	Max.	Units	Conditions
Frequency						•
Nominal Frequency	f <sub>NOM</sub>	1.024		160.000	MHz	—
			±25	_		
Frequency Stability (Note 3)	f <sub>STAB</sub>	_	±50	—	ppm	Ordering option.
		_	±100	—		
Outputs						
Output Logic Level High	V <sub>OH</sub>	$0.9 \times V_{DD}$		_	V	Note 2
Output Logic Level Low	V <sub>OL</sub>	—		0.1 × V <sub>DD</sub>	v	Note 2
Load	I <sub>OUT</sub>	—	15	50	pF	—
		—		8	ns	≤20 MHz
Output Rise/Fall Time (Note 2)	t <sub>r</sub> /t <sub>f</sub>	—	_	5		20.001 MHz to 50 MHz
		_	_	4		50.001 MHz to 160 MHz
Output Leakage	Ι <sub>Ζ</sub>	—		±10	μA	Output disabled
Duty Cycle	DC	45	50	55	%	Note 2, Note 4
Period Jitter, 100 MHz		—	2.8	—		RMS
(Note 5)	фJ	_	26	—	ps	Peak-to-peak
RMS Jitter (Note 6)	фJ	—	97	145	fs	12 kHz to 20 MHz
Enable/Disable	·					·
Output Enable Voltage	V <sub>IH</sub>	$0.7 \times V_{DD}$		—	V	Note 7
Output Disable Voltage	V <sub>IL</sub>	—		0.4	v	
Disable Time	t <sub>D</sub>	_		100	ns	—
Start-Up Time	t <sub>SU</sub>			10	ms	
Operating Temperature	т	-10		+70	°C	Ordering ention
Range	T <sub>OP</sub>	-40		+85	C	Ordering option

Note 1: The power supply should have bypass capacitors as close to the supply and to ground as possible. For example, 0.1  $\mu$ F and 0.01  $\mu$ F.

- 2: Parameters are tested with the test circuit shown in Figure 1-1. Add [(50 pF 15 pF) ×  $V_{DD}$  ×  $f_{OUT}$ (in MHz) x 0.001] mA for the 50 pF option.
- **3:** Includes initial accuracy, operating temperature, supply voltage, shock and vibration (not under operation), and 10 years' aging for ±50 ppm and ±100 ppm options.
- 4: Duty cycle is measured as On-Time/Period. See Figure 1-2.
- **5:** Broadband period jitter measured using a LeCroy Waverunner 610Zi, 100k samples.
- **6:** Measured using an Agilent E5052 or equivalent at 100 MHz and +25°C.
- 7: The output is enabled if Enable/Disable is left open. A 10 k $\Omega$  pull-up to V<sub>DD</sub> is recommended.

## **ELECTRICAL CHARACTERISTICS, 1.8V OPTION**

Parameter	Symbol	Min.	Тур.	Max.	Units	Conditions
Supply						
Voltage (Note 1)	V <sub>DD</sub>	1.71	1.8	1.89	V	—
Max. Supply Voltage	—	-0.5	—	7.0	V	—
Max. Voltage E/D	_	-0.5	_	V <sub>DD</sub> + 0.5	V	—

## **ELECTRICAL CHARACTERISTICS, 1.8V OPTION (CONTINUED)**

Parameter	Symbol	Min.	Тур.	Max.	Units	Conditions
		_		2		≤12 MHz
		_	_	3		12.001 MHz to 20 MHz
Current (Note 2)	I <sub>DD</sub>	—	_	11	mA	20.001 MHz to 65 MHz
		_	_	18		65.001 MHz to 133 MHz
		_		25		133.001 MHz to 160 MHz
Current	I <sub>DD</sub>	_	_	10	μA	Output Disabled
Frequency						
Nominal Frequency	f <sub>NOM</sub>	1.024	_	160.000	MHz	—
		—	±25	—		
Frequency Stability (Note 3)	f <sub>STAB</sub>	_	±50	—	ppm	Ordering option.
		_	±100	—		
Outputs						
Output Logic Level High	V <sub>OH</sub>	$0.9 \times V_{DD}$		_	V	Note 2
Output Logic Level Low	V <sub>OL</sub>	_	_	0.1 × V <sub>DD</sub>	v	Note 2
Load	I <sub>OUT</sub>	—	15	50	pF	—
	t <sub>r</sub> /t <sub>f</sub>	_		8	ns	≤20 MHz
Output Rise/Fall Time (Note 2)		_		5		20.001 MHz to 50 MHz
		—	_	5		50.001 MHz to 160 MHz
Output Leakage	Ι <sub>Ζ</sub>	_	_	±10	μA	Output disabled
Duty Cycle	DC	45	50	55	%	Note 2, Note 4
Period Jitter, 100 MHz	*	_	3.4	—	<b>n</b> 0	RMS
(Note 5)	фј	_	33	—	ps	Peak-to-peak
RMS Jitter (Note 6)	фJ	_	212	320	fs	12 kHz to 20 MHz
Enable/Disable						
Output Enable Voltage	V <sub>IH</sub>	$0.7 \times V_{DD}$	_	—	V	Note 7
Output Disable Voltage	V <sub>IL</sub>			0.4	v	
Disable Time	t <sub>D</sub>	—		100	ns	—
Start-Up Time	t <sub>SU</sub>			10	ms	—
Operating Temperature Range	T <sub>OP</sub>	-10 -40		+70 +85	°C	Ordering option

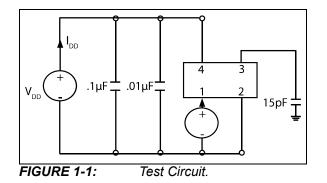
Note 1: The power supply should have bypass capacitors as close to the supply and to ground as possible. For example, 0.1  $\mu$ F and 0.01  $\mu$ F.

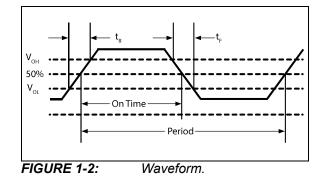
2: Parameters are tested with the test circuit shown in Figure 1-1. Add [(50 pF - 15 pF) ×  $V_{DD}$  ×  $f_{OUT}$ (in MHz) x 0.001] mA for the 50 pF option.

**3:** Includes initial accuracy, operating temperature, supply voltage, shock and vibration (not under operation), and 10 years' aging for ±50 ppm and ±100 ppm options.

4: Duty cycle is measured as On-Time/Period. See Figure 1-2.

- 5: Broadband period jitter measured using a LeCroy Waverunner 610Zi, 100k samples.
- 6: Measured using an Agilent E5052 or equivalent at 100 MHz and +25°C.
- 7: The output is enabled if Enable/Disable is left open. A 10 kΩ pull-up to V<sub>DD</sub> is recommended.





## 2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

#### TABLE 2-1:PIN FUNCTION TABLE

Pin Number	Pin Name	Description	
1	E/D	Enable/Disable.	
2	GND	Case and electrical ground.	
3	Output	Output.	
4	V <sub>DD</sub>	Power supply voltage.	

#### TABLE 2-2: ENABLE/DISABLE FUNCTION

E/D Pin	Output
High	Clock Output
Open	Clock Output
Low	High Impedance

## 3.0 RELIABILITY

Microchip qualification includes aging at various extreme temperatures, shock and vibration, temperature cycling, and IR reflow simulation. The VCC4A family is capable of meeting the following qualification tests:

Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Temperature Cycle	MIL-STD-883, Method 1010
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2015
Moisture Sensitivity Level	MSL 1
Contact Pads	Gold (0.3 µm min. to 1 µm max.) over Nickel
Contact Pads, _SNPB Option	Tinned using solder alloy Sn63Pb37 in accordance with J-STD-006
Weight	62 mg

TABLE 3-1: ENVIRONMENTAL COMPLIANCE

Although ESD protection circuitry has been designed into the VCC4A, proper precautions should be taken when handling and mounting. Microchip employs a human body model (HBM) and a charged device model (CDM) for ESD susceptibility testing and design protection evaluation.

#### TABLE 3-2: ESD RATINGS

Model	Minimum	Conditions		
Human Body Model	400V	JES22-A115		
Charged Device Model	2000V	JESD22-C101		

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability. Permanent damage is also possible if E/D is applied before  $V_{DD}$ .

#### TABLE 3-3: ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Storage Temperature	Τ <sub>S</sub>	-55 to 125	°C
Soldering Temperature / Time	T <sub>LS</sub>	260 / 30	°C / seconds

## 4.0 IR REFLOW

The VCC4A is qualified to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements. The VCC4A device is hermetically sealed so an aqueous wash is not an issue. **Note:** Devices that have been solder dipped (\_SNPB option) will not be Pb-Free.

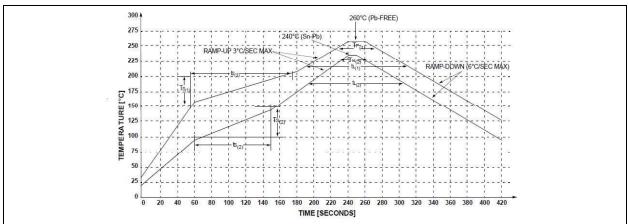


FIGURE 4-1: Reflow Profile.

Symbol	Minimum	Maximum	Conditions		
T <sub>S(1)</sub>	150°C	200°C	Pb-Free		
T <sub>S(2)</sub>	100°C	150°C	_SNPB Option		
t <sub>s(1)</sub>	60 sec.	180 sec.	Pb-Free		
t <sub>s(2)</sub>	60 sec.	120 sec.	_SNPB Option		
t <sub>l(1)</sub>	60 sec.	150 sec.	Pb-Free		
t <sub>l(2)</sub>	60 sec.	150 sec.	_SNPB Option		
T <sub>p(1)</sub>	245°C	260°C	Pb-Free		
T <sub>p(2)</sub>	225°C	240°C	_SNPB Option		

## 5.0 TAPE AND REEL

Tape Dimensions (mm)				Reel Dimensions (mm)								
Dimension	W	F	Do	Po	P1	Α	В	С	D	Ν	W1	W2
Tolerance	Тур.	Тур.	Тур.	Тур.	Тур.	Тур.	Min.	Тур.	Min.	Min.	Тур.	Max.
VCC4A	12	5.5	1.5	4	8	178	1.78	13	20.6	55	12.4	22.4



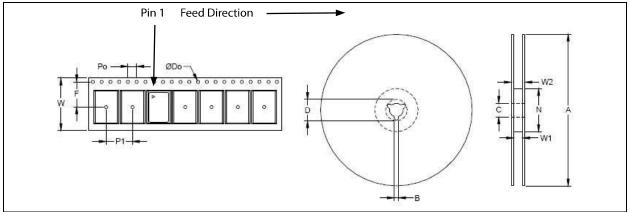
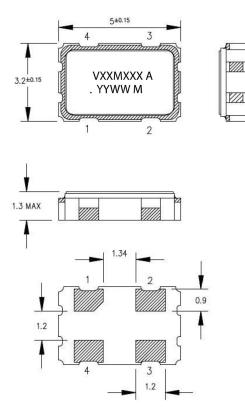


FIGURE 5-1:

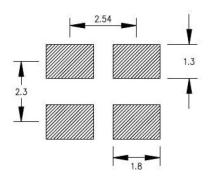
Tape and Reel.

## 6.0 PACKAGING INFORMATION



Dimensions in mm

Recommended Soldering Pad Layout



Marking V = Vectron XXMXXX = Frequency, eg 50M000 = 50.000 MHz A = Product family . = Pin 1 YY = Year WW = Week M = Manufacturing Location, examples C, C3, J1

## APPENDIX A: REVISION HISTORY

## **Revision A (December 2022)**

• Initial release of VCC4A as Microchip data sheet DS20006749A.

NOTES:

## **PRODUCT IDENTIFICATION SYSTEM**

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Part Number		<u>-X</u>	<u>x</u>	<u>x</u>	<u>xxMxxxxx</u>	xx	<u>XX</u>			
Device		Power Supply	Electrical Options	Stability	Frequenc	;y	Media Type			
Device:	VCC4A:		OS Crystal Oscillato mm	r in 5 mm x	Examples:					
Power Supply:	A B C E F G H	$ \begin{array}{rcl} = & +3.3 \\ = & +3.0 \\ = & \pm 5.0 \\ = & \pm 3.3 \\ = & \pm 2.3 \\ \end{array} $	) VDC, 15 pF 3 VDC, 15 pF ) VDC, 15 pF ) VDC, 50 pF 3 VDC, 50 pF 5 VDC, 15 pF 3 VDC, 15 pF		a) VCC4A-B3E 49M1520000T b) VCC4A-F3F 20M0000000:	R:	VCC4A, +3.3VDC Power Supply, Tristate Electrical Option, 45/55% Duty Cycle, -10°C to +70°C Temp. Range, ±50 ppm Stability, 49.152 MHz Frequency, Tape and Reel (1000/Reel). VCC4A, ±3.3 VDC Power Supply, Tristate Electrical Option, 45/55% Duty Cycle, ±25 ppm, -40 to 85°C Temp. Range, 20 MHz Fre- quency, Cut Tape /Non-standard TR Quantities			
Electrical Options: Option 3 recom- mended. All other options not recom- mended for new designs.	3 0 1 2 5 6	= No = Tris = No = Ena	tate, 45/55% Duty C Tristate, 40/60% Dui tate, 40/60% Duty C Tristate, 45/55% Dui ble, 40/60% Duty C ble, 45/55% Duty C	ty Cycle Cycle ty Cycle ycle	c) VCC4A-B3E 24M5760000T		VCC4A, +3.3 VDC Power Supply, Tristate Electrical Option, 45/55% Duty Cycle, ±50 ppm, –40 to 85°C Temp. Range, 24.576 MHz Frequency, Tape and Reel (1000/ Reel)			
Stability:	A C B D E F	$= \pm 10$ $= \pm 50$ $= \pm 50$ $= \pm 25$	0 ppm, -10 to 70°C 0 ppm, -40 to 85°C ppm, -10 to 70°C ppm, -40 to 85°C ppm, -10 to 70°C ppm, -40 to 85°C		part orde pac	number des ering purpos kage. Check	dentifier only appears in the catalog scription. This identifier is used for es and is not printed on the device with your Microchip Sales Office for ility with the Tape and Reel option.			
Frequency:	xxMxxxxxx		quency in MHz character is K if kH	z)						
Media Type:	<blank> TR _SNPB</blank>	= Tap	tape or non-standar e and Reel Lead solder dipped	rd TR quantities						

NOTES:

#### Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
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