TEXAS INSTRUMENTS

SLVS394A – MAY 2002

9-LINE MULTIMODE SCSI TERMINATOR WITH SPI-3 MODE DELAY, DISCONNECT, AND STATUS LINES

FEATURES

- **Auto Selection Single Ended (SE) or Low Voltage Differential (LVD) Termination**
- **Meets SCSI-1, SCSI-2, SCSI-3 SPI, Ultra (Fast-20), Ultra2 (SPI-2 LVD), Ultra3/Ultra160 (SPI-3) and Ultra320 (SPI-4) Standards**
- **2.7-V to 5.25-V TERMPWR Operation**
- **Differential Fail-Safe Bias**
- **Pin Compatible With UCC5630A With Digital SPI-3 Mode Change/Filter Delay**
- **Thermal Packaging for Low Junction Temperature and Better MTBF**

DESCRIPTION

The UCC5670 SCSI multimode terminator, comprises both single-ended (SE) and low-voltage differential (LVD) termination and is intended to bridge the transition from single ended to LVD SCSI parallel interface (SPI-2), (SPI-3), and (SPI-4). The low voltage differential signaling configuration is required to meet the higher SCSI speeds and smaller skew budgets. LVD is specified for Ultra2, (Fast-40), Ultra3/Ultra160 (Fast-80), Ultra320 (Fast-160) and meets the requirements for speeds up to Fast-320. The UCC5670 can not be used with High Power Differential (HIPD)–(EIA485) devices. When it detects high power differential devices, the terminator lines switch to a high impedance state.

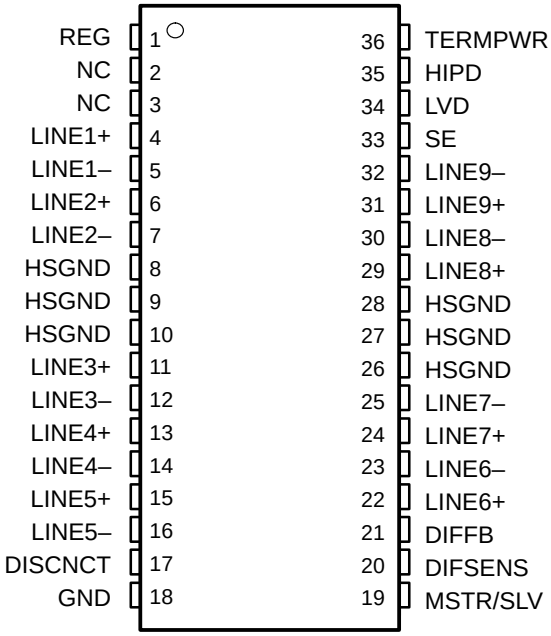
The UCC5670 is offered in a 36-pin MWP package.

AVAILABLE OPTIONS

T_A	Disconnect Status	Packaged Device
		MWP
0°C to 70°C	Regular	UCC5670MWP

† The MWP package is available taped and reeled. Add R suffix to device type (e.g. UCC5670MWPR) to order quantities of 1000 devices per reel.

MWP PACKAGE
(TOP VIEW)



NC – No internal connection

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

TERMPWR voltage . . . . . 6 V
Signal line voltage . . . . . 0 V to 6 V
Package power dissipation . . . . . 2 W
Operating junction temperature, T_J . . . . . –55°C to 150°C
Storage temperature, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal.

electrical characteristics, T_A = 0°C to 70°C, TERMPWR = 2.7 V to 5.25 V, (unless otherwise stated)

supply current (TERMPWR)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
TERMPWR supply current	LVD mode (No Load)		35	50	mA
	SE mode (No Load)		21	35	mA
	Disabled terminator		0.65	1	mA

regulator (REG)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
REG output voltage	LVD mode	1.15	1.25	1.35	V
	Single ended mode	2.5	2.7	3.0	V
Short circuit source current	V_{REG} = 0 V	–800	–420	–225	mA
Short circuit sink current	V_{REG} = 3.3 V	100	180	420	mA

differential sense regulator (DIFSENS)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Output voltage	–5 mA ≤ $I_{DIFSENS}$ ≤ 50 µA	1.2	1.3	1.4	V
1.3-V regulator source current	Differential sense = 0 V	–15	–8	–5	mA
1.3-V regulator sink current	Differential sense = 2.75 V	50	80	200	µA

differential termination (LINE+,LINE–) or (LINE(n)+,LINE(n)–)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Differential impedance		100	105	110	Ω
Common mode impedance	L+ and L– shorted together, See Note 2	110	150	165	Ω
Differential bias voltage		100	113	125	mV
Common mode bias	L+ and L– shorted together	1.15	1.25	1.35	V
Output capacitance	Single ended measurement to ground, See Note 1			3	pF

single ended termination

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Impedance	See Note 3	100	108	116	Ω
Termination current	Signal level 0.2 V	–25.4	–23	–20	mA
	Signal level 0.5 V	–22.4	–20	–17	mA
Output capacitance	Single ended measurement to ground, See Note 1			3	pF
Single ended GND sw impedance	+/– 5 mA		20	60	Ω

NOTES: 1. Ensured by design and engineering test, but not 100% production tested.

2. Common mode impedance = $\frac{(2.0\ V\ -\ 0.5\ V)}{I(at\ 2.0\ V)\ -\ I(at\ 0.5\ V)}$; Short each L+ to its' corresponding L–. Measure the current into each line pair when forced to 2.0–V and then 0.5–V.

3. $Z = \frac{\left(V_{L(X)}\ -\ 0.2\ V\right)}{I_{L(X)}}$; where

$V_{L(X)}$ = Output voltage for each terminator minus output pin (L1– through L9–) with each pin unloaded.
$I_{L(X)}$ = Output current for each terminator minus output pin (L1– through L9–) with the output pin forced to 0.2 V.

electrical characteristics, T_A = 0°C to 70°C, TERMPWR = 2.7 V to 5.25 V, (unless otherwise stated)

disconnected termination (applies to each line pair, 1–9, in DISCNCT or HIPD mode)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Output leakage	Disabled, TERMPWR 0 < 5.25 V			400	nA
Output capacitance	Single ended measurement to ground, See Note 1			3	pF

disconnect & diff sense input

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
DISCNCT threshold		0.8		2.0	V
DISCNCT input current	$V_{DISCNCT}$ = 0 V	–30	–10		µA
DIFFB SE (single ended) to LVD threshold		0.5		0.7	V
DIFFB LVD to HIPD threshold		1.9		2.4	V

time delay/filter

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Mode change delay	A new mode change can start any time after a previous mode has been detected,	100	180	300	ms

status bits (SE, LVD, HIPD)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
I_{SOURCE}	V_{LOAD} = 2.4 V		–8.7	–4	mA
I_{SINK}	V_{LOAD} = 0.5 V	3	6		mA
	V_{LOAD} = 0.4 V	2	5		mA

master/slave (MSTR/SLV) input

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
MSTR/SLV input current	$V_{MSTR/SLV}$ = 0 V to $V_{TERMPWR}$	–1		1	µA
MSTR/SLV threshold	$V_{TERMPWR}$ = 2.7 V	0.8		1.9	V
	$V_{TERMPWR}$ = 3.3 V	1		2.4	V
	$V_{TERMPWR}$ = 5.25 V	1.5		3.7	V

NOTES: 1. Ensured by design and engineering test, but not 100% production tested.

2. Common mode impedance = $\frac{(2.0\ V - 0.5\ V)}{I(\text{at } 2.0\ V) - I(\text{at } 0.5\ V)}$; Short each L+ to its' corresponding L–. Measure the current into each line pair when forced to 2.0–V and then 0.5–V.

3. $Z = \frac{\left(V_{L(X)} - 0.2\ V\right)}{I_{L(X)}}$; where

$V_{L(X)}$ = Output voltage for each terminator minus output pin (L1– through L9–) with each pin unloaded.
$I_{L(X)}$ = Output current for each terminator minus output pin (L1– through L9–) with the output pin forced to 0.2 V.

pin description

TERMPWR

2.7-V to 5.25-V power input pin. TERMPWR must be connected to a 4.7-μF capacitor to ground.

DIFFB

Input pin for the comparators that select SE, LVD, or HIPD modes of operation. This pin should be decoupled with a 0.1-μF capacitor to ground and then connected to the DIFSENS pin through a 20-kΩ resistor.

DIFSENS

Output pin that supplies a regulated, current limited, 1.3 V to the DIFFSENS line of the SCSI bus.

DISCNCT

Input pin used to shut down the terminator if the terminator is not connected at the end of the bus. Connecting this pin to ground on the UCC5670 activates the terminator or open disables the terminator.

REG

Regulator output bypass pin, this pin must be connected to a 4.7-μF capacitor to ground.

MSTR/SLV

If the terminator is enabled, this input pin enables/disables the DIFFSENS driver, when connected to TERMPWR or ground respectively. When the terminator is disabled, the DIFFSENS driver is off, independent of this input.

LINE1– to LINE9–

Termination lines. These are the active lines for SE mode or negative lines for LVD mode. In HIPD mode, these lines are high impedance.

LINE1+ to LINE9+

Termination lines. These lines switch to ground in SE mode, and are the positive lines for LVD mode. In HIPD mode these lines are high impedance.

SE

TTL compatible status line. This output is high in SE mode.

LVD

TTL compatible status line. This output is high in LVD mode.

pin description (continued)

HIPD

TTL compatible status line. This output is high in HIPD mode.

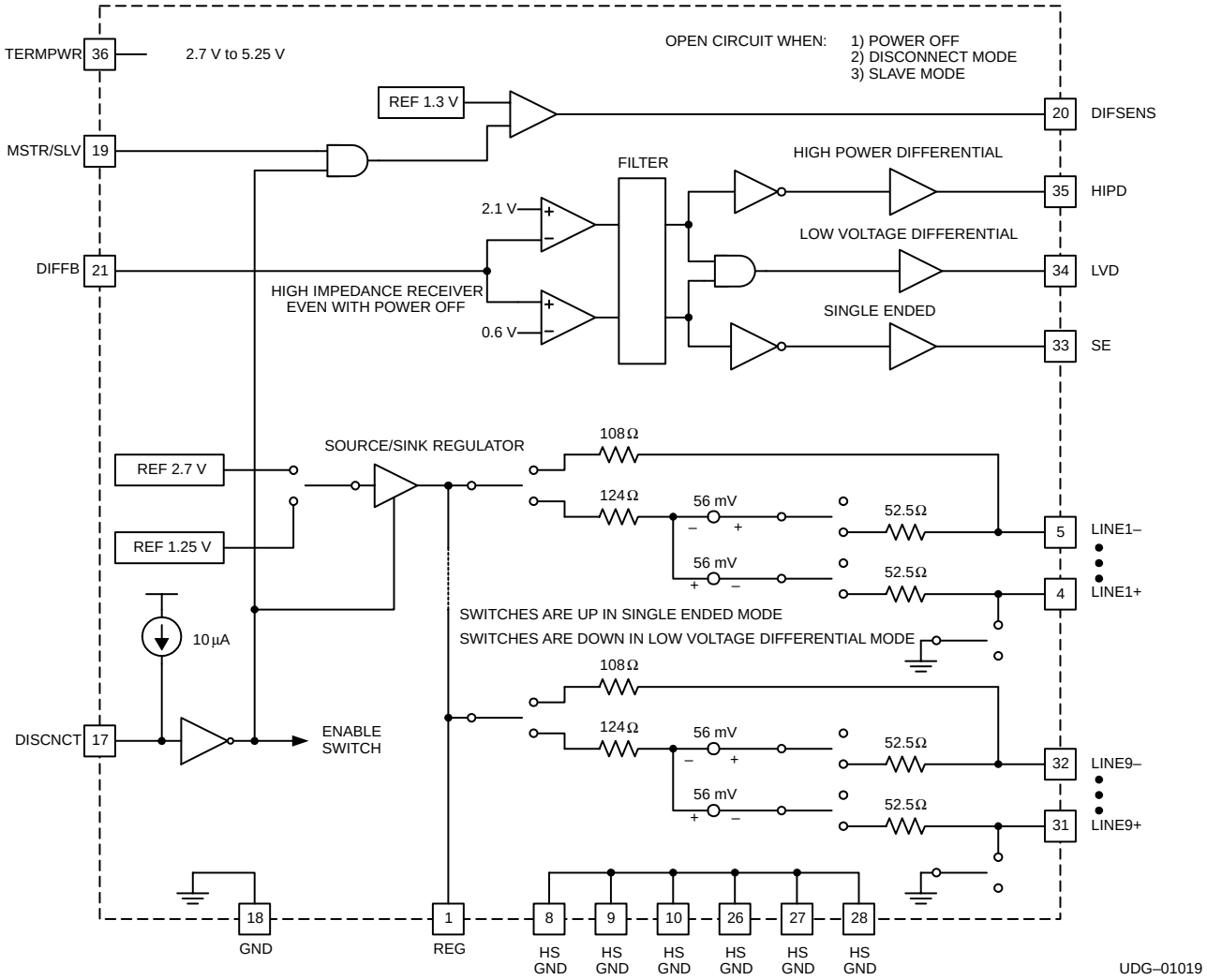
GND

Ground reference.

HSGND

Heat sink ground pins. These should be connected to a large PC board trace to lower the thermal impedance.

block diagram



NOTE: Pinout is for the 36-pin MWP package.

APPLICATION INFORMATION

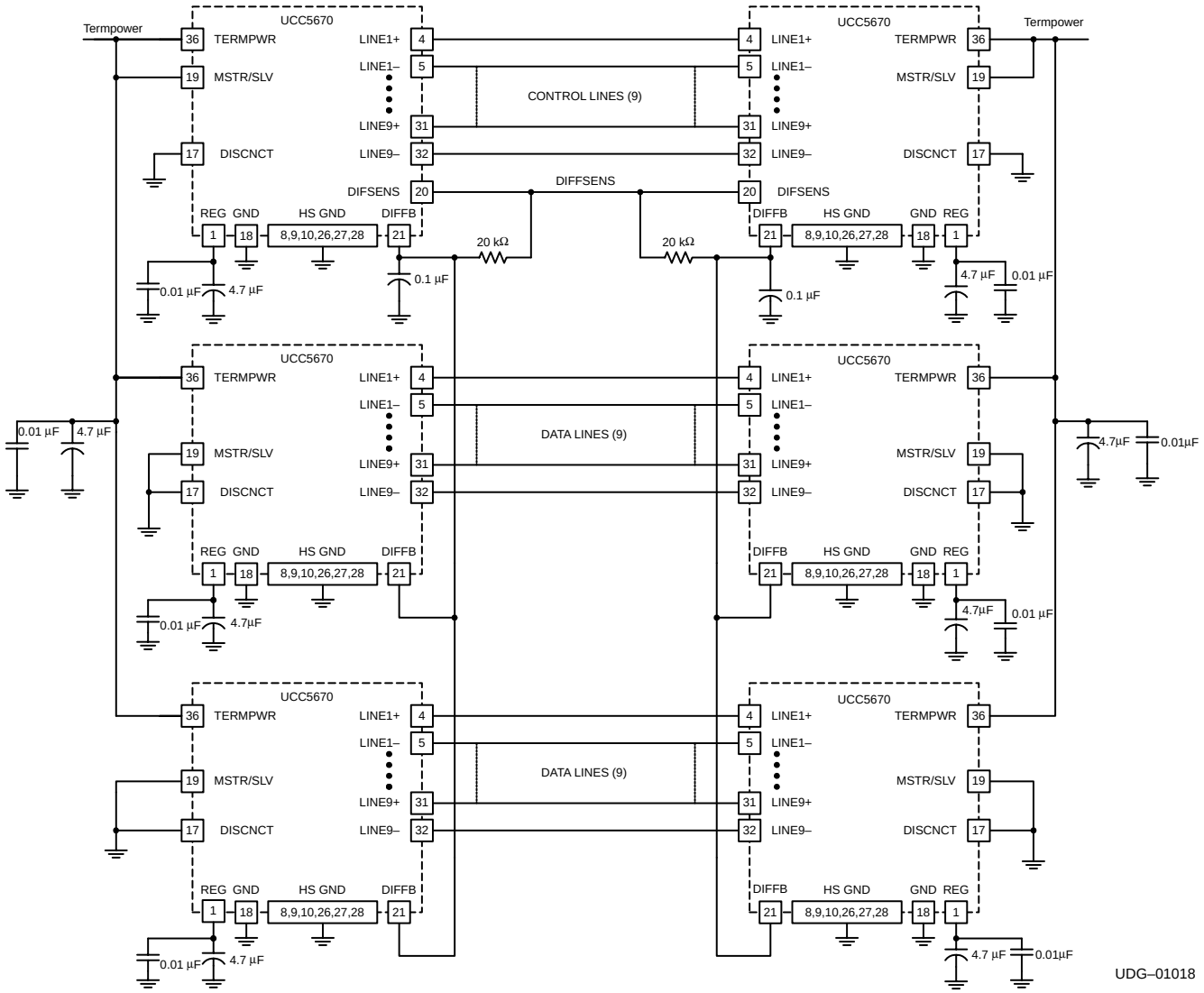


Figure 1. Typical Application

All SCSI buses require a termination network at each end of the bus segment. The UCC5670 is used in multimode active termination applications, where single ended (SE) and low voltage differential (LVD) might coexist. The UCC5670 has both SE and LVD termination networks integrated into a single monolithic component.

The UCC5670 senses what kinds of devices are present on the bus segment by detecting the voltage on the SCSI bus control line, DIFFSENS (See Note 1), which is monitored by the DIFFB input pin. The DIFSENS (See Note 2) output pin on the UCC5670 attempts to drive the DIFFSENS control line to 1.3 V. If only LVD devices are present, the DIFSENS line will be successfully driven to that voltage. If HIPD devices are present, they will pull the DIFFSENS line high. If any single ended devices are present, they will pull the DIFFSENS line to ground.

NOTES: 1 DIFFSENS is the SCSI bus line that is used to signal the bus mode.

NOTES: 2 DIFSENS is the IC pin for driving the SCSI line, DIFFSENS.

APPLICATION INFORMATION

Three UCC5670 ICs are required at each end of the SCSI bus segment to terminate 27 lines (18 data, 9 control). Every UCC5670 contains a DIFFSENS driver, but only one at each end of the bus segment is used to drive the DIFFSENS line. Only the two UCC5670 that are driving the DIFFSENS line are connected to that line.

Only the UCC5670 and the UCC5630A devices that are used to drive the DIFFSENS line have the MSTR/SLV input pin pulled high to termpower. This enables the DIFFSENS driver. All the other terminators have the MSTR/SLV input pins connected to ground. This turns the DIFFSENS driver off.

The DIFFSENS line is monitored by the DIFFB input pin. All the DIFFB inputs at each end of the bus must be connected. Any DIFFSENS signal below 0.5 V is interpreted as single ended, SE. Any DIFFSENS signal between 0.7 V and 1.9 V is interpreted as low voltage differential, LVD. Any DIFFSENS signal above 2.4 V is interpreted as high powered differential, HIPD. Operation of the mode change delay filter is tolerant of noise on the DIFFB input. This is due to a forgiving digital implementation of the delay. Like most digital circuits an anti-aliasing filter is required. The anti-aliasing filter is implemented with a 20-kΩ resistor connecting the DIFFSENS line to the DIFFB input pin, and a 0.1-μF capacitor from the DIFFB input to ground.

On power up, the UCC5670 assumes the HIPD mode. If the voltage on DIFFB indicates another mode the chip will wait between 100-ms to 300-ms before changing the bus terminator mode. If the voltage on the DIFFB input changes later the UCC5670 again waits between 100 ms to 300 ms before changing the bus terminator mode. The time delay is the same when changing between any bus modes, DIFFB input detection, mode change delay, and status outputs are active in all modes.

All Texas Instruments multimode terminators are designed to operate in both 5-V and 3.3-V systems. This means that the terminator operates within SCSI specifications with the termpower voltage as low as 2.7 V and as high as 5.25 V. An on chip termination regulator supplies a stable termination voltage for the terminator networks.

In single ended mode, the UCC5670 termination regulator is set to 2.7 V. The LINE– pins are connected to the regulator through a 108-Ω termination. The LINE+ pins are connected to ground through a low impedance switch.

In low voltage differential mode, the UCC5670 termination regulator is set to 1.25 V. A Y-termination network is presented to each line pair. This provides a common-mode impedance of 150 Ω and a differential impedance of 105-Ω. The lines in each differential pair are biased so that when not driven, LINE(n)+ and LINE(n)– are 56 mV below and 56 mV above the common-modes bias voltage (1.25 V) respectively.

In high power differential mode, the UCC5670 termination regulator is set to 1.25 V. Every LINE+ and LINE– is set to high impedance. The DIFFSENS regulator is on in high power differential mode.

Three status lines are provided by the UCC5670. The SE line is high in single ended mode. The LVD line is high in the low voltage differential mode. The HIPD line is high in high power differential mode.

When the DISCNCT input is pulled to ground the UCC5670 switches to connect mode. When the disconnect input (DISCNCT) is pulled high or left open the UCC5670 switches to the disconnect mode.

In connect mode, the UCC5670 functions as a terminator as described. In disconnect mode the termination regulator and the DIFFSENS drivers are turned off and the lines are switched to high impedance. The DIFFB input, mode change delay, and status outputs are still active. The connect mode is used for terminators that are at the end of the bus. The disconnect mode is used for terminators that are not at the end of the SCSI bus segment.

APPLICATION INFORMATION

The UCC5670 operates down to a TERMPWR voltage of 2.7 V. This accommodates a 3.3-V system with allowance for supply tolerance (±10%), a unidirectional fusing device, and cable drop. The UCC3912 is recommended in place of a fuse and diode implementation, as its lower voltage drop provides additional voltage margin for the system.The UCC3916 is recommended for 5-V systems.

Balanced signal layout is important in all SCSI implementations and even more critical in SPI-3 and SPI-4 systems, which have more stringent requirements on both the absolute value of capacitance on different signal lines, and the balancing of capacitance between the paired lines and from pair to pair.

Feedthroughs, through-hole connections, and etch lengths need to be carefully balanced. Standard multilayer power and ground plane spacing adds about 1 pF to each plane. Each feed-through will add 2.5 pF to 3.5 pF. Enlarging the clearance holes on both power and ground planes reduces capacitance. Opening up the power and ground planes under a through-hole connector reduces added capacitance in those applications. Capacitance is also affected by components in close proximity on both sides of the board.

maximum capacitance

SCSI Class	Trace to GND: REQ, ACK, DATA, Parity, P_CRCA	Trace to Trace: REQ, ACK, DATA, Parity, P_CRCA	Trace to GND: Other signals	Trace to Trace: Other Signals
Ultra1	25 pF	N/A	25 pF	N/A
Ultra2	20 pF	10 pF	25 pF	13 pF
Ultra3/Ultra160	15 pF	8 pF	25 pF	13 pF
Ultra320	13 pF	6.5 pF	21 pF (est.)	10 pF (est.)

TI terminators are designed with very tightly controlled capacitances on their signal lines. Between the positive and negative lines in a differential pair, the difference is typically no more than 0.1 pF, and only 0.3 pF between pairs.

Multilayer boards need to adhere to the 120-Ω impedance standard, including the connector and feedthroughs. Bus traces are normally run on the outer layers of the board with 4-mil etch and 4-mil spacing between the two lines in each differential pair, and a minimum of 8-mil spacing to adjacent pairs to minimize crosstalk. Microstrip technology is normally too low in impedance and should not be used, it is designed for 50 Ω rather than 120-Ω differential systems. Microstrip can only be used with thicker dielectric between layers.

Decoupling capacitors should be installed as close as possible to the following input pins of the UCC5670:

TERMPWR: 4.7-µF capacitor to ground, 0.01-µF capacitor to ground (high-frequency, low ESR)

REG: 4.7-µF capacitor to ground, 0.01-µF capacitor to ground (high-frequency, low ESR)

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