TEXAS INSTRUMENTS

TRF6900

RF Evaluation Kit

User's Guide

May 2001

Mixed-Signal RF Products

SWRU001C

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Read This First

About This Manual

This document is intended to introduce the TRF6900 evaluation module (EVM) and familiarize the reader with setting up and testing the TRF6900 EVM using the evaluation software in a typical laboratory environment.

How to Use This Manual

This document contains the following chapters:

- ❏ Chapter 1 − Overview
- ❏ Chapter 2 − Evaluation Board
- ❏ Chapter 3 − Software User's Guide

Information About Cautions and Warnings

This user's guide may contain cautions and warnings.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

Contents

Figures

Chapter 1

Overview

This chapter provides an overview of the TRF6900 evaluation module (EVM).

Topic **Page**

1.1 Purpose

The TRF6900 evaluation module (EVM) provides a platform for lab prototype evaluation of the Texas Instruments TRF6900.

The TRF6900 EVM board is used to evaluate the RF performance of the TRF6900. It contains a PC parallel port interface and operates from 850 MHz to 950 MHz from 2.2 V to 3.6 V. The TRF6900 EVM contains seven SMA connectors that allow the user to observe transmitted data, LNA output, mixer output, IF output, RSSI output, to test the VCO tuning range, or to feed in an external RF input or mixer signal. The transmitted data can be viewed on a spectrum analyzer as either a single output frequency or in FSK mode at data rates up to 30 kbps. Although higher data rates are achievable with the TRF6900, the TRF6900 EVM is designed to operate at data rates up to 30 kbps at room temperature.

1.2 EVM Setup

The 3.5-inch diskette supplied with the TRF6900 contains the software required to demonstrate the TRF6900. Complete the following steps to set up the TRF6900 for evaluation.

Step 1: Place the 3.5-inch diskette into the floppy disk drive of the computer being used to evaluate the TRF6900.

Step 2: Copy the TRF6900.exe file to the hard drive.

Step 3: Connect a DB25 female to DB25 male cable between the TRF6900 evaluation board and the PC parallel port. The DB25 female end of the cable is connected to the TRF6900. The DB25 male end of the cable is connected to the desired LPT port of the PC (LPT1 or LPT2).

Step 4: Connect a dc power supply capable of 10 V 200 mA between the red power supply pin and ground on the TRF6900 evaluation board.

Step 5: Verify that the power supply output is set to 8 V.

Step 6: Turn the power supply on.

Step 7: If jumper at JP8 is installed, verify that LED3 (the red power-on LED) is illuminated.

Step 8: Run the TRF6900.exe file on the PC.

Step 9: Press the Send Words Now (F12) button on the program screen.

Step 10: Verify that LED1 (the green lock detect LED) is illuminated. When the lock detect LED is illuminated, the PLL is locked on frequency.

Note:

The actual icons/windows on the computer screen may differ from those shown in this user's guide, due to software version upgrades.

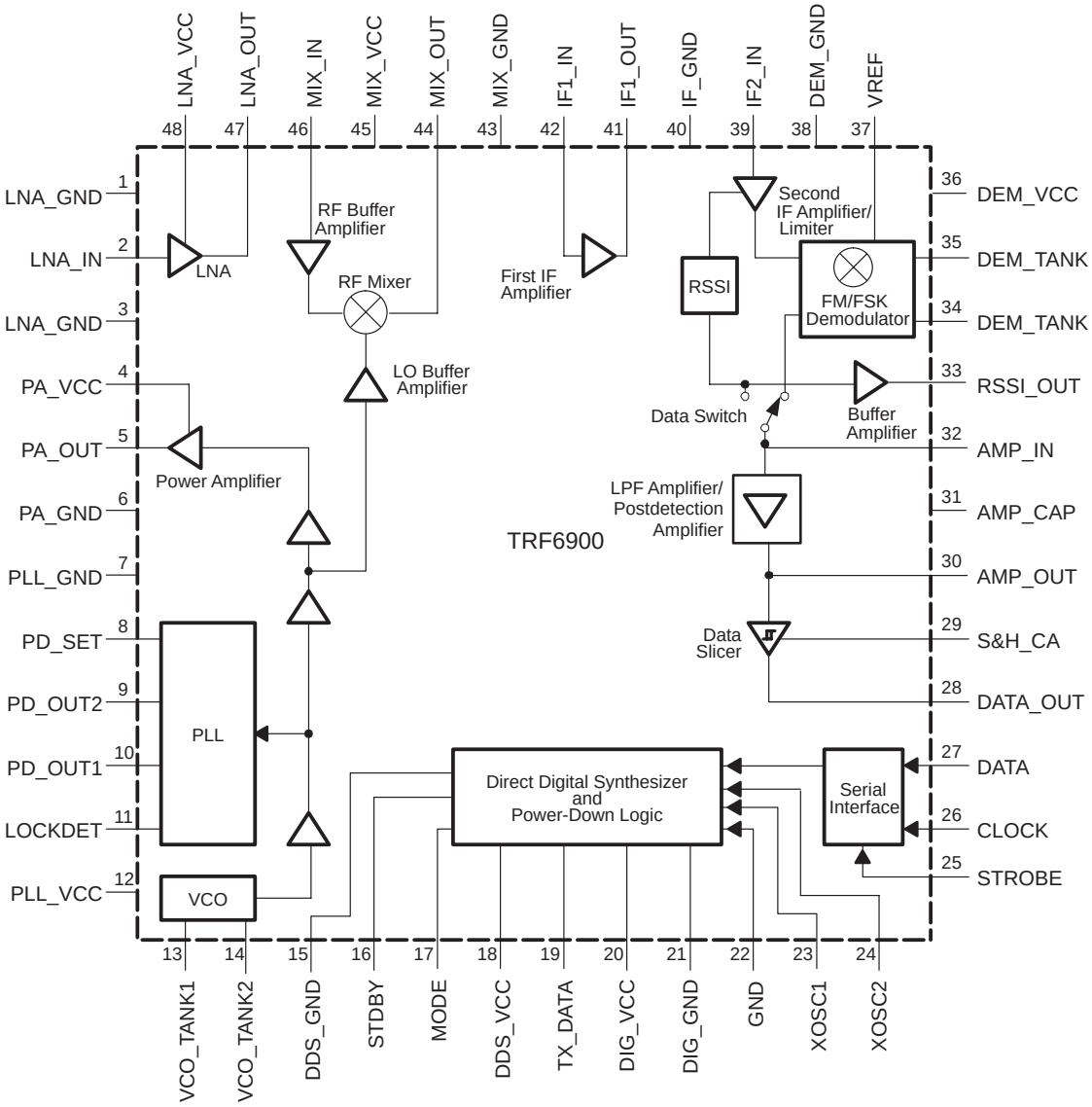
The schematics shown in this user's guide may not match the current revision due to PCB and component upgrades.

Always check the TI website for the latest schematics and software.

1.3 Block Diagram

Figure 1−1 shows the block diagram for the TRF6900.

Figure 1−1. TRF6900 Block Diagram



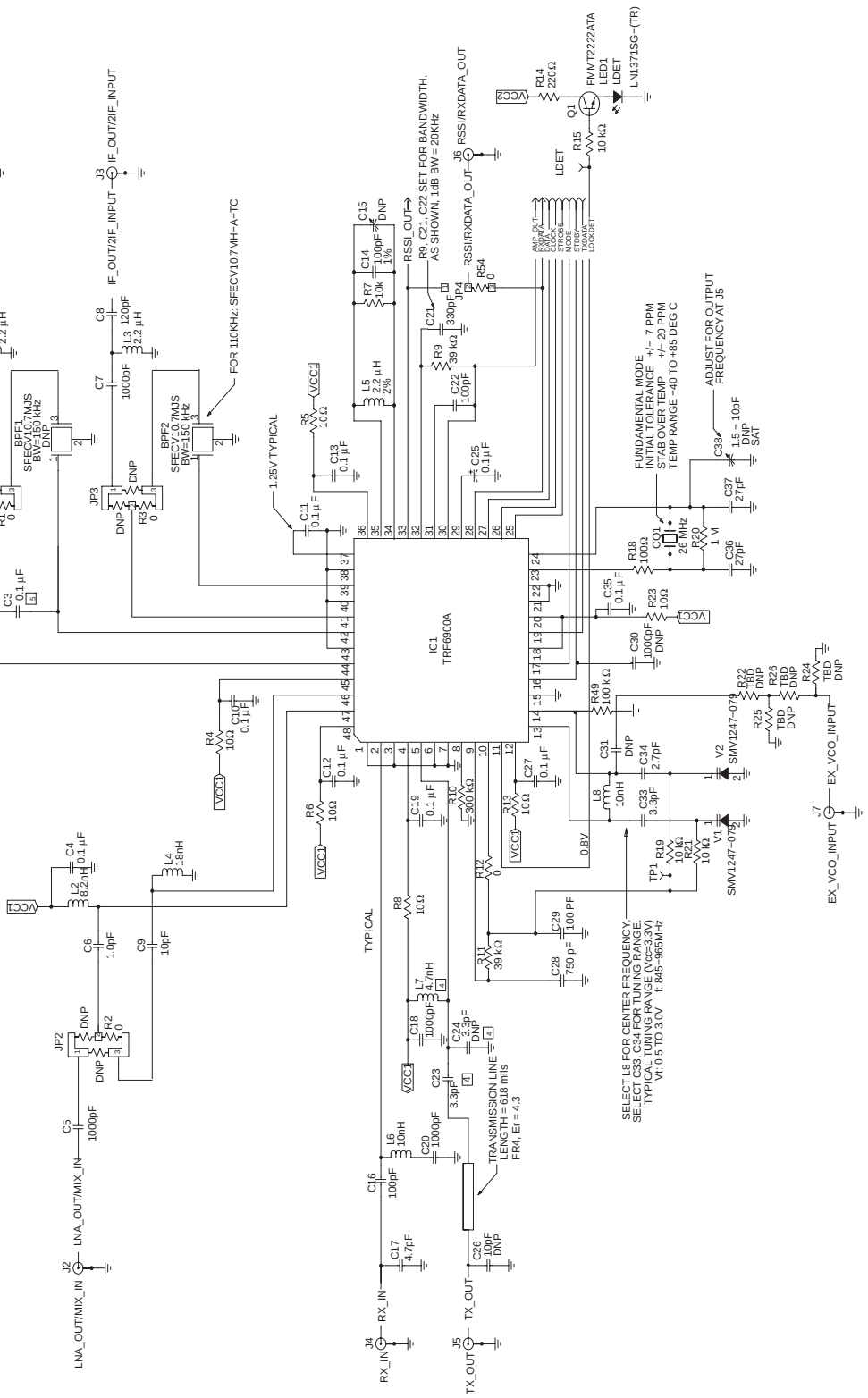
Chapter 2

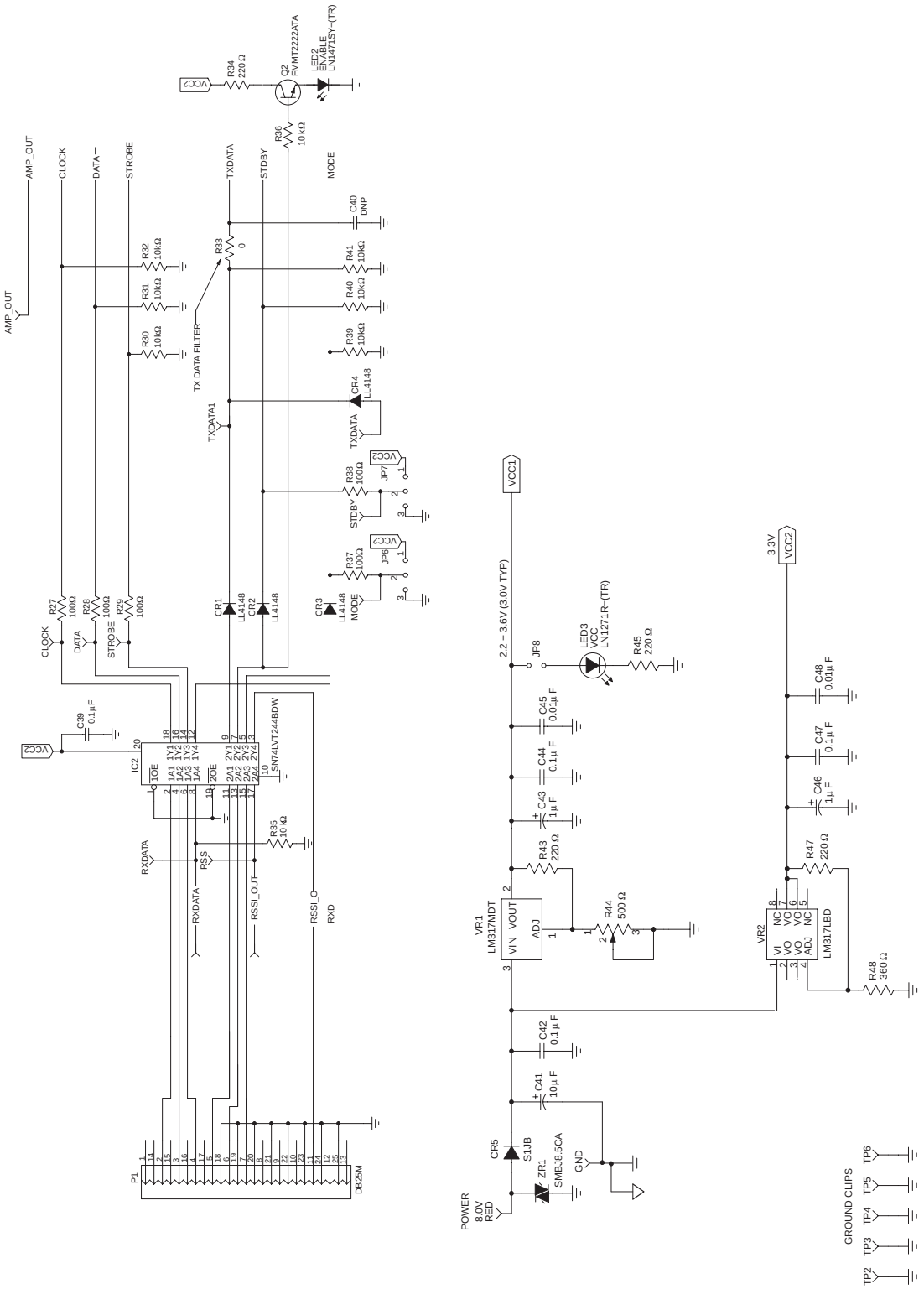
Evaluation Board

This chapter describes the EVM and its operation.

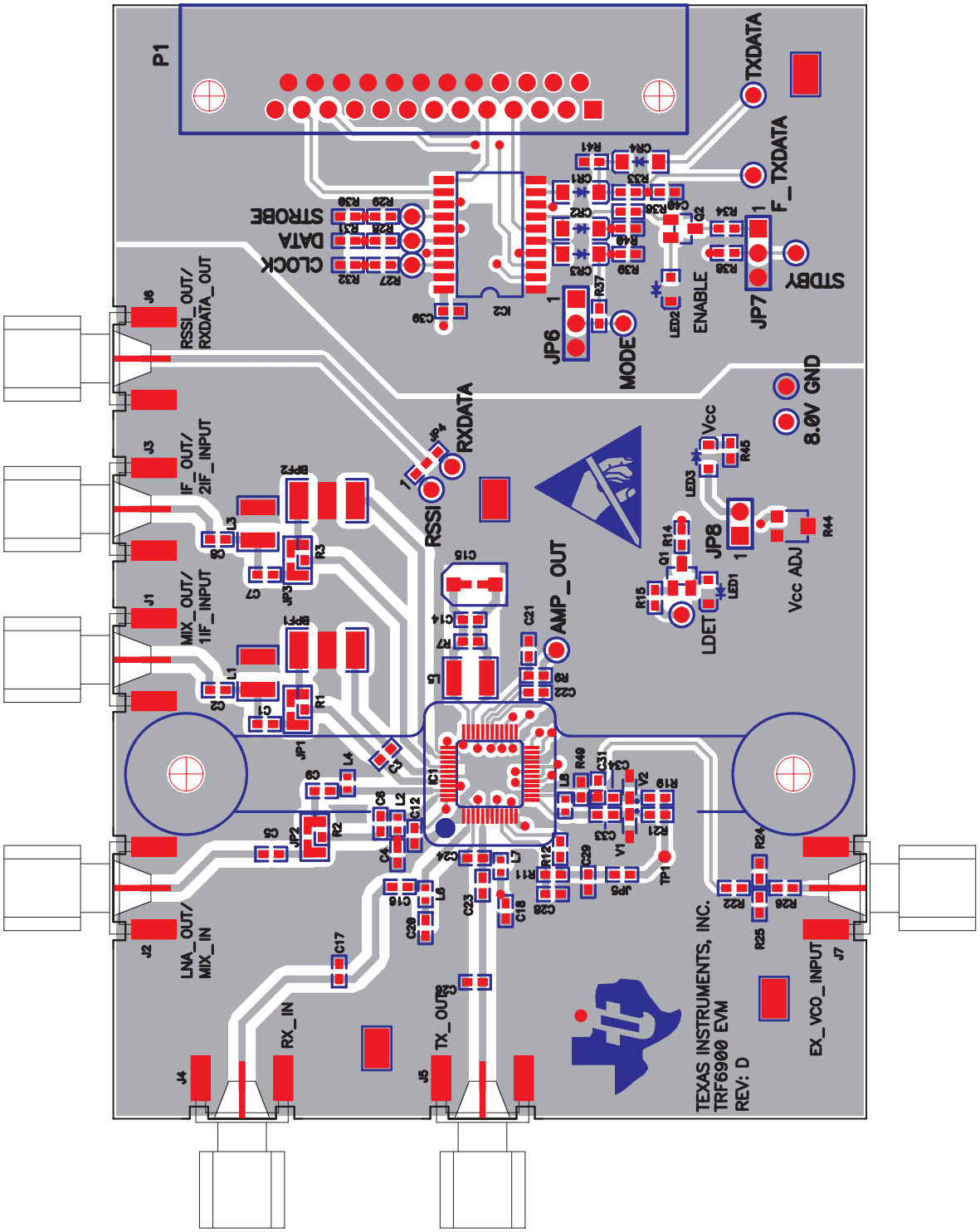
Topic **Page**

2.1 Schematics

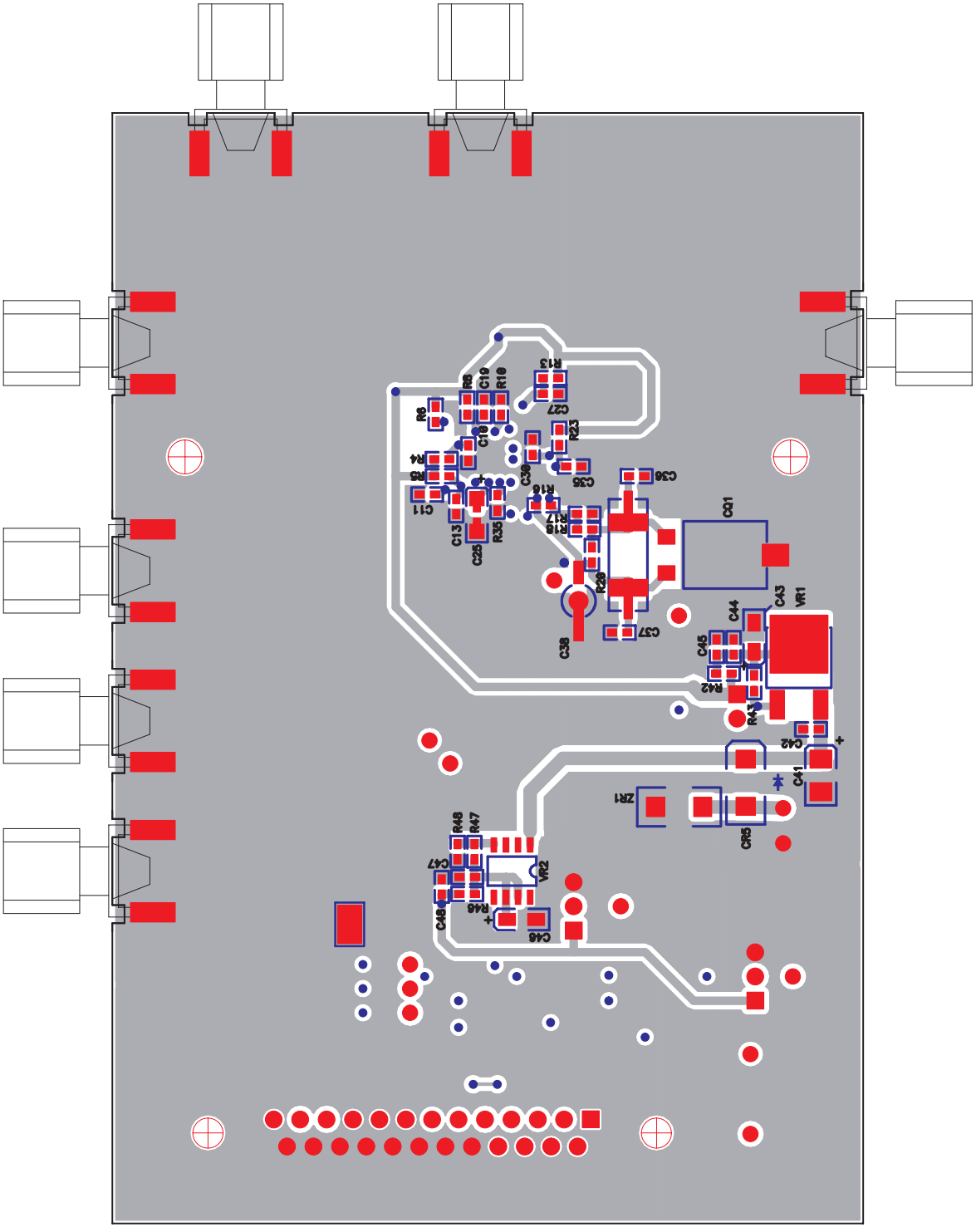



AMP_OUT
CLOCK
DATA
STROBE
TXDATA
STDBY
MODE
RXDATA
RSSI
RSSI_OUT
RSSI_O
RXD
TX DATA FILTER
VCC2
VCC1
3.3V
2.2 – 3.6V (3.0V TYP)
POWER
8.0V
RED
GND
GROUND CLIPS
IC2
SN74LVT244BDW
VR1
LM317MDT
VR2
LM317LBD
P1
DB25M
LED2
ENABLE
LN1471SY–(TR)
LED3
VCC
LN1271R–(TR)
Q2
FMMT2222ATA

2.1.1 Top Side Silkscreen and Drawing



2.1.2 Bottom Side Silkscreen and Drawing



2.2 Parts List

Count	Ref. Designator	Value	Pattern Name	Description	Manufacturer	Part No.	Distributor/Part No.
1	BPF2	BW = 150 kHz	SFECV10.7	Band pass filter	Murata	SFECV10.7MJ-A-TC	
2	C45, C48	0.01 µF	0603				
1	C28	750 pF	0603				
14	C3, C4, C10−C13, C19, C25, C27, C35, C39, C42, C44, C47	0.1 µF	0603				
1	C6	1.0 pF	0603				
2	C43, C46	1 µF	1208 tantalum	Tantalum capacitor			
1	C38	1.5 pF–10 pF, DNP	9341 Series	Trimmer capacitor	Johnson	9341-3SI	Newark−95F9901
1	C9	10 pF	0603				
1	C41	10 µF	1206 tantalum	Tantalum capacitor			
2	C36, C37	27 pF	0603				
2	C23, C33	3.3 pF	0603				
1	C34	2.7 pF	0603				
4	C14, C16, C22, C29	100 pF	0603				
1	C17	4.7 pF	0603				
2	C2, C8	120 pF	0603				
1	C21	330 pF	0603				
5	C1, C5, C7, C18, C20	1000 pF	0603				
1	C15	DNP	AT0300 0603	Surface-mount ceramic trimmer capacitor	Temex	AT0300	
1	CQ1	26 MHz	HC45/U gull wing	Resistance weld miniature crystal	International Crystal Manufacturing	865850	
1	CQ1_A	DNP	CX-1-SM	Surface-mount quartz crystal	CFP (CMAC Frequency Products)		
1	CQ1_B	DNP	ATS-SM series	Crystal	CTS Reeves		Digi-Key
4	CR1, CR2, CR3, CR4		MELF3 (MINIMELF)	Fast switching diode	Diode Inc	LL4148	Digi-Key − LL4148BCT-ND
1	CR5		SMB	Rectifier	Diode Inc	S1JBT	Digi-Key − S1HBDUCT-ND
1	IC1		TQFP48	Single chip transceiver	Texas Instruments	TRF6900A	

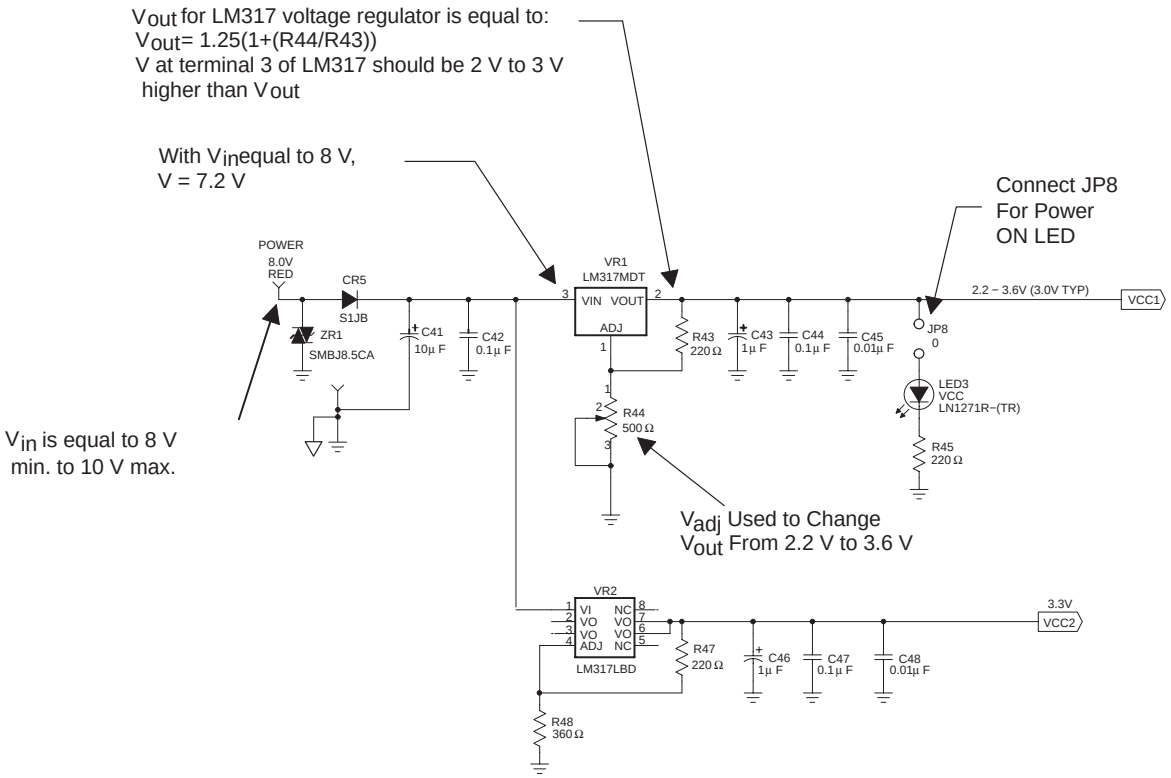
Count	Ref. Designator	Value	Pattern Name	Description	Manufacturer	Part No.	Distributor/Part No.
1	IC2		SO20WB	Octal Buffers and line drivers with 3-state outputs	Texas Instruments	SN74LVT244BDW	Digi-Key − 296-1707-5-ND
7	J1, J2, J3, J4, J5, J6, J7		SMA_H	SMA brass connector − horizontal/PC mount	Johnson Components	142-0701-801	Newark − 90F2624
2	JP6, JP7		Jumper-3 pin	Breakaway headers	AMP	4-103239-0	Newark − 90F7725
1	JP8		Jumper-2 pin	Breakaway headers	AMP	4-103239-0	Newark − 90F7725
3	L1, L3, L5	2.2 µH	1214	Surface-mount inductor	Murata	LQS33N2R2G04M00	
1	L2	8.2 nH	0603	Surface-mount inductor	Murata	LQW1608	
2	L6, L8	10 nH	0603	Surface-mount inductor	Murata	LQW1608	
1	L7	4.7 nH	0603	Surface-mount inductor	Murata	LQW1608	
1	L4	18 nH	0603	Surface-mount inductor	Murata	LQW1608	
1	LED1	LDET	LED, S type	Surface-mount LED-gull wing-S type − green	Panasonic	LN1371SG−(TR)	Digi-Key − P516CT−ND
1	LED2	ENABLE	LED, S type	Surface-mount LED-gull wing-S type − amber	Panasonic	LN1471SY−(TR)	Digi-Key − P517CT−ND
1	LED3	VCC	LED, S type	Surface-mount LED-gull wing-S type − red	Panasonic	LN1271SR−(TR)	Digi-Key − P490CT−ND
1	P1		DB25M	Subminiature D connector	AMP	745783−4	Newark − 90F5485
2	Q1, Q2		SOT23	NPN silicon planar switching transistor − 330 mW	Zetex	FMMT2222A	
6	R1, R2, R3, R12, R33, R54	0	0603				
1	R20	1M	0603				
1	R11	39K	0603				
6	R4−R6, R8, R13, R23	10	0603				
12	R7, R15, R19, R21, R30−R32, R35, R36, R39−R41	10K	0603				
2	R9, R11	39K	0603				
6	R18, R27, R28, R29, R37, R38	100	0603				
1	R49	100K	0603				
5	R14, R34, R43, R45, R47	220	0603				

Count	Ref. Designator	Value	Pattern Name	Description	Manufacturer	Part No.	Distributor/Part No.
1	R10	300K	0603				
1	R48	360	0603				
1	R44	500	P1S Panasonic	Surface mount trimmer potentiometer	Panasonic	EVM-1SSX50BXX	
2	V1, V2	SOD323	Hyperabrupt tuning varactor	Alpha Industries, Inc.	SMV1247-079		
1	VR1		DPAK CADE369A-13	Three-terminal adjustable output positive voltage regulator	ON Semiconductor	LM317MDT	Newark − 06F9320
1	VR2		SO6NB	Three-terminal adjustable output positive voltage regulator	ON Semiconductor	LM317LBD	Newark − 06F9304
1	ZR1		SMBK-BI	Transient voltage suppressor	Vishay/Liteon	SMBJ8.5CA	Digi-Key − SMBJ8.5AGICT-ND
11	AMP_OUT, CLOCK, DATA, F_TXDATA, LDET, MODE, RSSI, RXDATA, STDY, STROBE, TXDATA		PC test point	Color coded PC test point (any color)	Components Corp.		Newark
1	GND	BLK	PC test point	Color coded PC test point (black)	Components Corp.	TP-105-01-00	Newark − 97B3259
1	8.0 V	RED	PC test point	Color coded PC test point (red)	Components Corp.	TP-105-01-02	Newark − 97B3257
5	TP2−TP6		SMD test point	Surface mount test point	Components Corp.	TP-107-01	Newark − 97B2647

2.3 EVM DC Voltage Setup

The evaluation board should be used with a dc power supply voltage of 8 V nominal. Figure 2−1 details the dc voltage supply setup for the TRF6900 EVM.

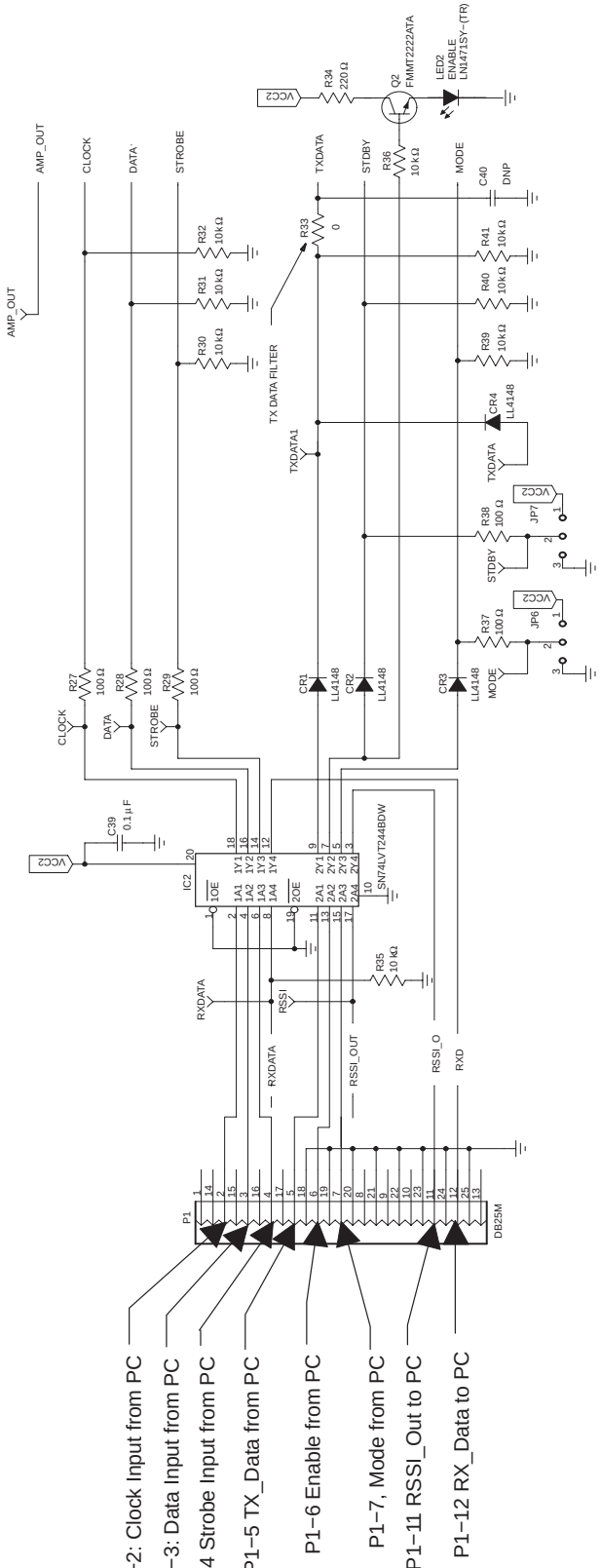
Figure 2−1. TRF6900 EVM DC Voltage Setup



2.4 Serial Interface and PC Port Pin Out

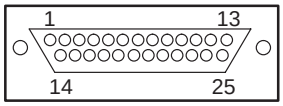
Figure 2−2 details the serial interface portion of the TRF6900 EVM.

Figure 2−2. TRF6900 EVM Serial Interface



2.5 Standard PC Parallel Port

A standard PC parallel port is configured as follows:



View Is Looking at
Connector Side of
DB-25 Male Connector

Pin	Description	
1	$\overline{\text{Strobe}}$	PC Output
2	Data 0	PC Output
3	Data 1	PC Output
4	Data 2	PC Output
5	Data 3	PC Output
6	Data 4	PC Output
7	Data 5	PC Output
8	Data 6	PC Output
9	$\overline{\text{Data}}$ 7	PC Output
10	$\overline{\text{ACK}}$	PC Input
11	Busy	PC Input
12	Paper Empty	PC Input
13	$\overline{\text{Select}}$	PC Input
14	$\overline{\text{Auto}}$ Feed	PC Output
15	$\overline{\text{Error}}$	PC Input
16	$\overline{\text{Initialize Printer}}$	PC Output
17	Select Input	PC Output

Pin Assignments

Note: 8 Data Outputs
4 Misc Other Outputs

5 Data Inputs

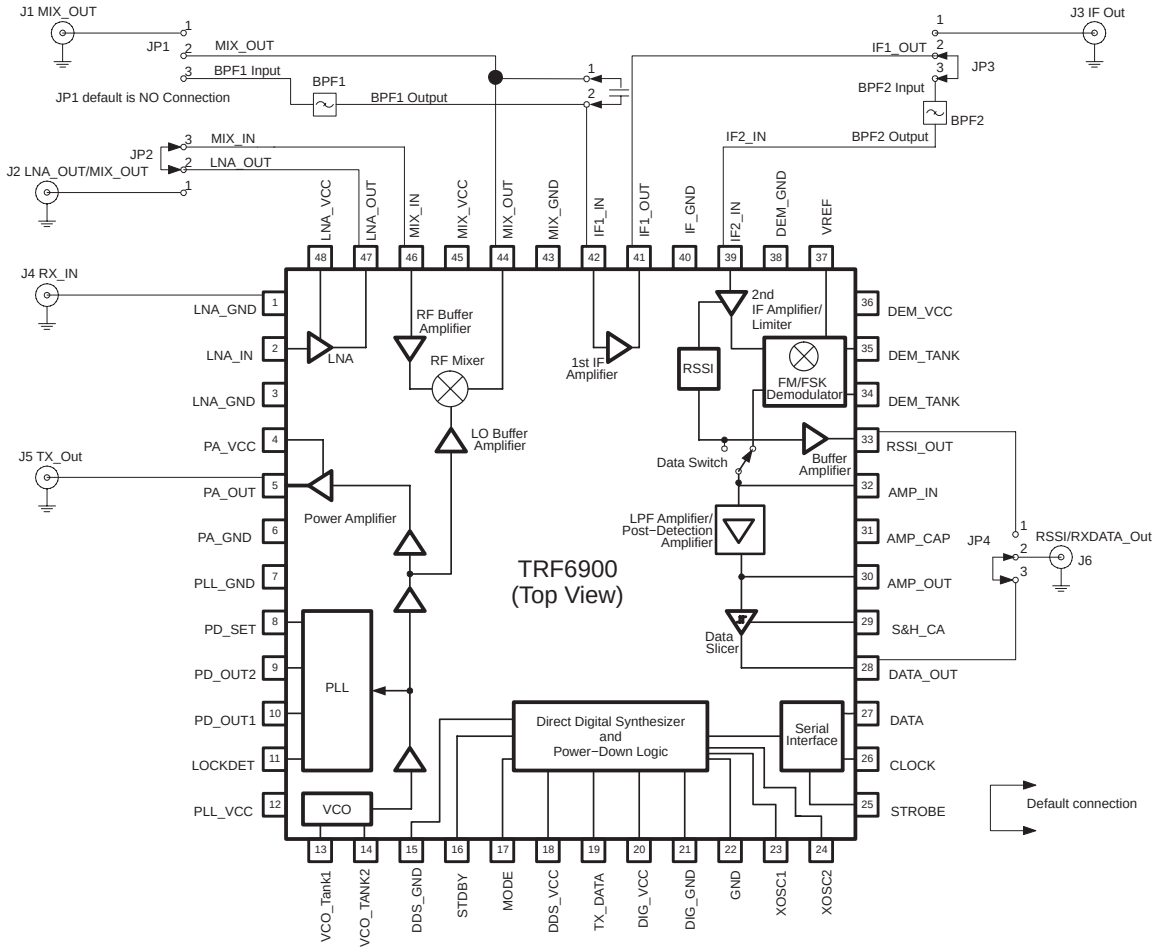
Note: Pins 18−25 Are
Ground

Note: The TRF6900 EVM uses pins 2–7 for signals from the PC to the EVM. Pins 11 and 12 are used for signals from the EVM to the PC.

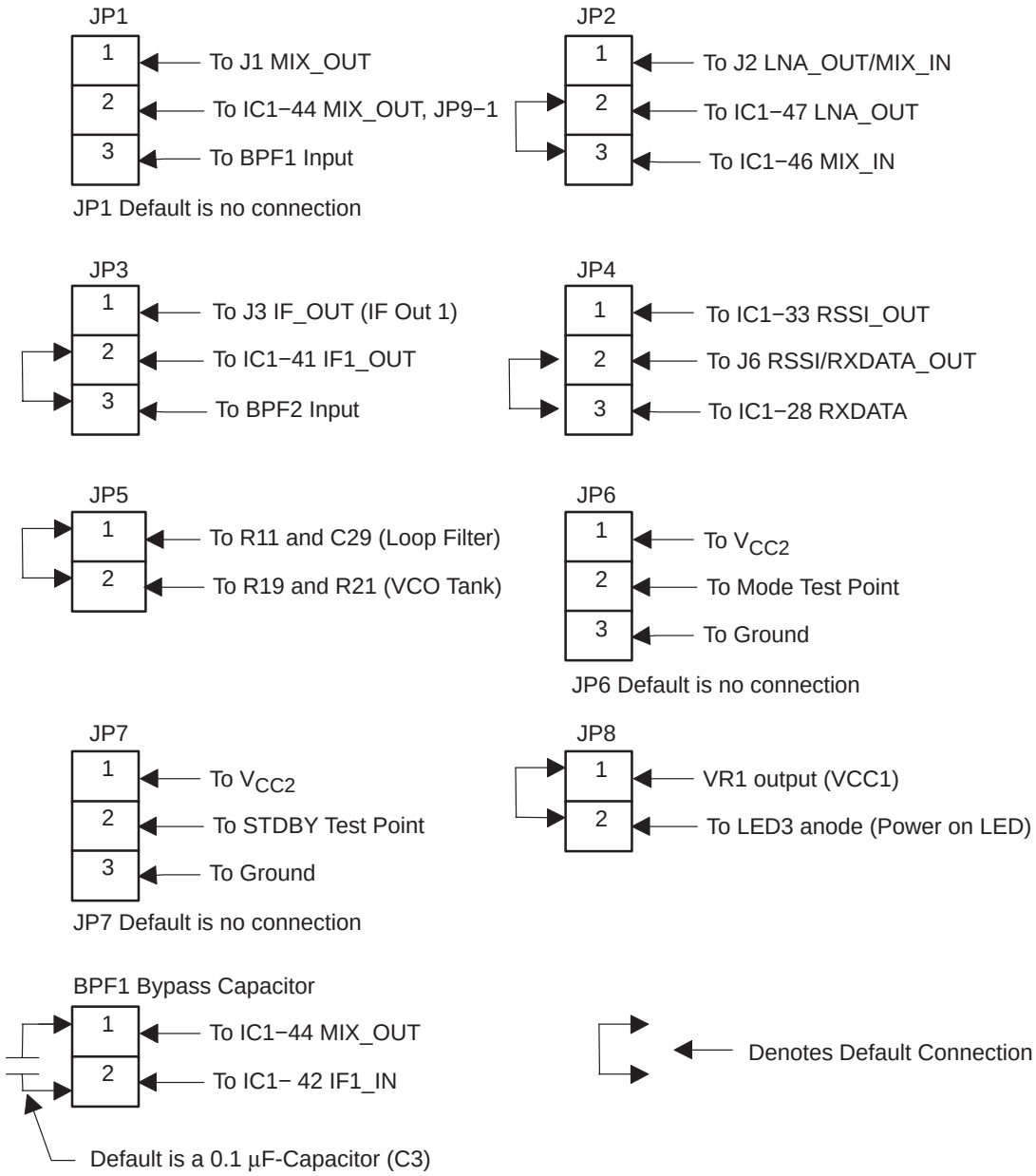
2.6 Jumper Connections

Figure 2−3 shows the default position of the jumpers on the TRF6900 EVM.

Figure 2−3. EVM Jumper Locations and Default Configuration of the EVM



2.6.1 Jumper Connections



2.6.2 Jumper Description

The jumpers on the TRF6900 EVM, as shown in Figure 2−3, are used for the following purposes:

- JP1

  Jumper JP1 is used for testing of the mixer circuit of the TRF6900. Testing of the mixer stage by itself is accomplished by connecting JP1−1 to JP1−2, connecting JP2−1 to JP2−3, and removing the 0.1-µF capacitor (C3) connecting terminal 44 (MIX_OUT) and terminal 42 (IF1_IN). If the BPF1 filter were installed, jumpers JP1−2 and JP1−3 would be connected. The default state for jumper JP1 is no connection.

- JP2
  Jumper JP2 is used for testing of the mixer circuit of the TRF6900. Testing of the mixer stage by itself is accomplished by connecting JP1−1 to JP1−2, JP2−1 to JP2−3, and removing the 0.1-µF capacitor connecting terminal 44 (MIX_OUT) and terminal 42 (IF1_IN). The IF mixer and LNA stages may be tested together by connecting JP1−1 to JP1−2, connecting JP2−2 to JP2−3 (default), and removing the 0.1-µF capacitor (C3) connecting terminal 44 (MIX_OUT) and terminal 42 (IF1_IN). The LNA stage is tested by itself by connecting JP2−1 to JP2−2. The default state for jumper JP2 is JP2−2 to JP2−3.

- JP3
  Jumper JP3 is used to observe the output of IF1, the first IF amplifier, by connecting JP3−1 to JP3−2. The default configuration of JP3−2 to JP3−3 connects the output of the first IF amplifier to the input of the second IF amplifier.

- JP4
  Jumper JP4 is used to monitor RXDATA_OUT when connected as JP4−2 to JP4−3. Jumper JP4 is used to monitor RSSI_OUT when connected as JP4−1 to JP4−2. The default state for jumper JP4 is JP4−2 to JP4−3.

- JP5
  Jumper JP5 is used to connect the VCO tank circuit to the loop filter of the PLL circuit. The only reason to remove jumper JP5 is to test the tuning range of the VCO tank circuit with an external power supply. The default state for jumper JP5 is JP5−1 to JP5−2.

- JP6
  Jumper JP6 can be used to pull the MODE line up to VCC (JP6−1 to JP6−2) or pull down to ground (JP6−2 to JP6−3), if a computer connection is not installed. The primary purpose for JP6 is as a test point to monitor the state of the MODE line. The default state for jumper JP6 is not connected.

- JP7
  Jumper JP7 can be used to pull the STDBY line up to VCC (JP7−1 to JP7−2) or pull down to ground (JP7−2 to JP7−3), if a computer connection is not installed. The primary purpose for JP7 is as a test point to monitor the state of the STDBY line. The default state for jumper JP7 is not connected.

- JP8
  Jumper JP8 is used to connect the Power On LED to the output of the IC1 voltage regulator. The default state for jumper JP8 is JP8−1 to JP8−2.

- BPF1 Bypass Capacitor
  A 0.1-µF capacitor (C3) is used to bypass BPF1 and connect the mixer output directly to the first IF amplifier. BPF1 is not installed on the TRF6900 evaluation board. If the user requires BPF1 to be installed, then remove the capacitor (C3) connecting terminal 44 (MIX_OUT) and terminal 42 (IF1_IN) and connect JP1−2 to JP1−3.

2.7 Connectors and Test Points

The following are descriptions of the TRF6900 EVM connectors and test points.

2.7.1 Connectors

- P1
  P1 is the PC parallel port interface and is a male DB25 connector. P1 is connected to the LPT1 or LPT2 port of the computer on which the TRF6900 software is running.
- J1 MIX_OUT
  MIX_OUT is an SMA female connector used with jumpers JP1 and JP2 to test the mixer circuit of the TRF6900.
- J2 LNA_OUT/MIX IN
  LNA_OUT/MIX_IN is an SMA female connector used with jumpers JP1 and JP2 to test the mixer and LNA circuits of the TRF6900.
- J3 IF_OUT
  IF_OUT is an SMA female connector used with jumper JP3 to monitor the IF output circuit of the TRF6900.
- J4 RX_IN
  RX_IN is an SMA female connector which is connected to the input of the LNA. The LNA is the input to the receiver section of the TRF6900.
- J5 TX_OUT
  TX_OUT is an SMA female connector which is connected to the transmitter output of the TRF6900.
- J6 RSSI/RXDATA_OUT
  RSSI/RXDATA_OUT is an SMA female connector used with jumper JP4 to monitor the RXDATA output or RSSI output of the TRF6900.
- J7 VCO_TANK
  VCO_TANK is an SMA female connector used with resistors R22, R24, R25, R26, and capacitor C31 to directly feed in an external VCO signal. Resistors R22, R24, R25, and R26 are used to form a *T* attenuator. The components for this option are not installed on the EVM.

2.7.2 Test Points (TP)

- TP1
  Test point TP1 is used to monitor the tuning voltage applied to the VCO circuit by the PLL circuit.
- AMP_OUT TP
  The AMP_OUT test point is used to monitor the output of the LPF amplifier/post-detection amplifier.
- LDET TP
  The LDET test point is used to monitor the lock detect line of the TRF6900.

- ❑ RSSI TP
  The RSSI test point is used to monitor the RSSI level from IC1−33 RSSI_OUT.

- ❑ RXDATA TP
  The RXDATA test point is used to monitor the RXDATA from IC1−28 DATA_OUT. This is the demodulated signal.

- ❑ MODE TP
  The MODE test point is used to monitor the MODE line.

- ❑ STDBY TP
  The STDBY test point is used to monitor the STDBY line.

- ❑ CLOCK TP
  The CLOCK test point is used to monitor the CLOCK signal from the PC.

- ❑ DATA TP
  The DATA test point is used to monitor the DATA signal from the PC.

- ❑ STROBE TP
  The STROBE test point is used to monitor the STROBE signal from the PC.

- ❑ TXDATA TP
  The TXDATA test point is used to monitor the transmitted data. Transmit data from an external source can also be applied at this point.

2.7.3 Adjustments

Resistor R44 is varied to adjust the VCC1 voltage applied to IC1 (TRF6900).

2.7.4 LED Indicators

- ❑ VCC LED
  If JP8 is installed, the VCC LED is illuminated when voltage is applied to IC1.

- ❑ LDET LED
  The LDET LED is illuminated when the lock detect line IC1−11 (TRF6900) is high, indicating that the PLL circuit is locked.

- ❑ ENABLE LED
  The ENABLE LED is illuminated when the STDBY line from computer is in the high state.

Chapter 3

Software User's Guide

This chapter describes the Windows-based software application that accompanies the EVM.

Topic **Page**

3.1 Introduction

A Windows-based software application accompanies the evaluation board. The software is intended for use in either a Windows 95/98 or Windows NT environment. If the Windows NT environment is used, the Windows NT driver software must accompany the software. However, if the operating system is Windows 95/98, the software application can run on its own.

Both the Windows NT Driver and the TRF6900 software are provided on diskette. Your system administrator must install the Windows NT Driver if you do not have administrative privileges on your computer. The TRF6900 software can run from the floppy disk by following these steps:

1) Click on the *Start* button on the desktop

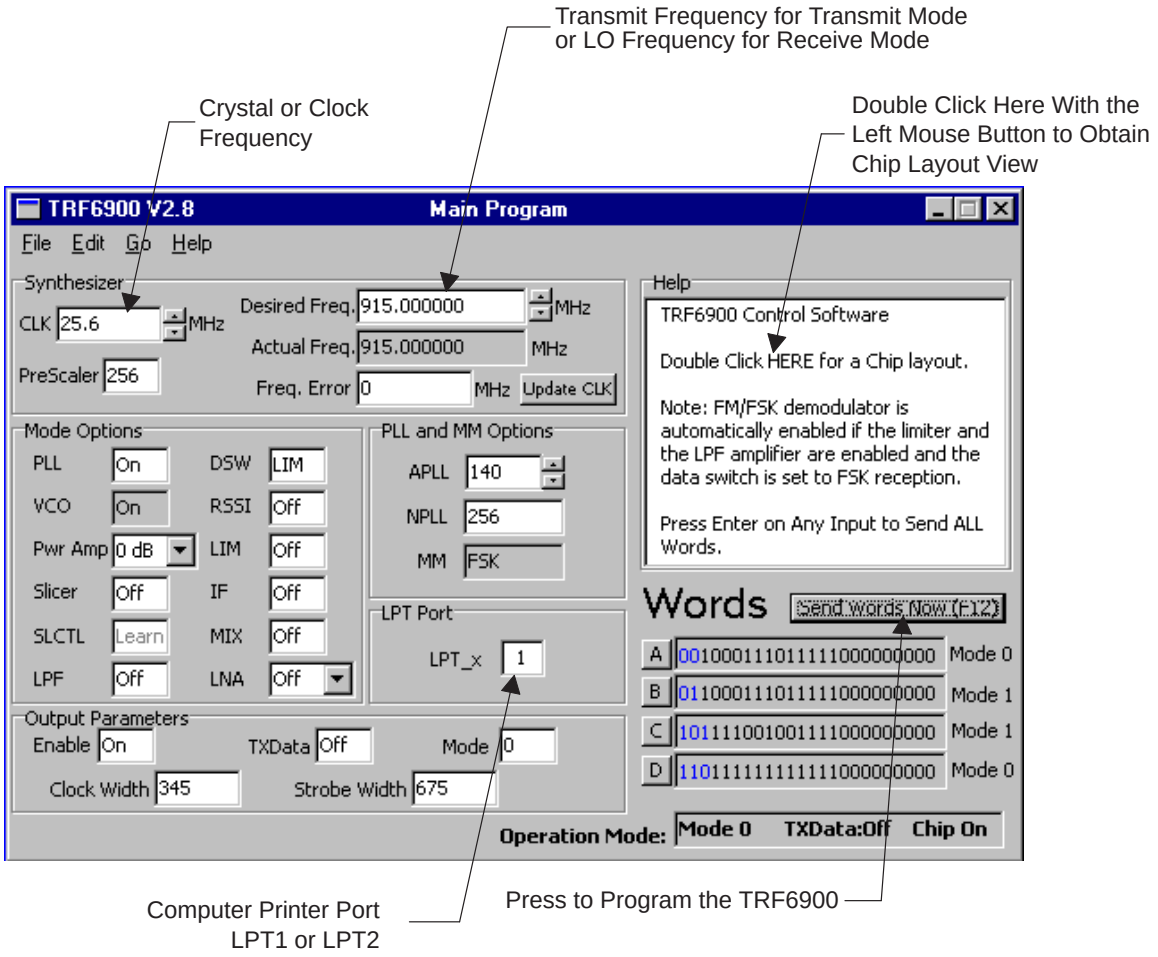
2) Click on the *Run* button

3) Type − A:\ TRF6900.exe and press *OK*

3.2 Main Program Screen

The screen shown in Figure 3−1 appears on your monitor.

Figure 3−1. Main Program Screen



NOTE: When word bits are displayed in RED, the Send Words Now (F12) button on the main program screen, must be pressed for changes to be updated.

The main program screen is divided into eight main sections as follows:

3.2.1 Synthesizer

This section is used to set the crystal/clock (CLK) frequency, the Desired Freq., and the PreScaler value of the divided-by-N of the PLL. From these inputs, the actual frequency and bit values of Words A and B are calculated.

3.2.2 Mode Options

This section allows the user to control various features of the TRF6900. The following is a brief summary of the 12 controls.

1)	PLL	Turns the phase-locked loop on or off
2)	VCO	Turns the voltage controlled oscillator on or off
3)	Pwr Amp	Allows the power amp to be set to off, 20-dB attenuation, 10-dB attenuation, or 0-dB attenuation states
4)	Slicer	Turns the data slicer on or off
5)	SLCTL	If the data slicer is on, this selects either the Learn or Hold mode for the data slicer
6)	LPF	Turns the low pass filter (LPF) on or off
7)	DSW	Data switch. Selecting LIM sets LPF input to the demodulator. Selecting RSSI sets the LPF input to the RSSI
8)	RSSI	Turns the radio strength signal indicator (RSSI) on or off
9)	LIM	Turns the limiter (LIM) on or off
10)	IF	Turns the intermediate frequency (IF) amplifier on or off
11)	MIX	Turns the mixer on or off
12)	LNA	Allows the low-noise amplifier (LNA) to be set to off, low gain, or high gain modes

3.2.3 Output Parameters

This section allows the user to turn the TRF6900 Enable, TXData, and Mode control lines on and off. When the mode control line is off, Mode 0 is defaulted. When the mode control line is on, Mode 1 is defaulted. Mode 0 initializes using Words A and D, Mode 1 initializes using Words B and C.

Clock Width and Strobe Width allow the clock and strobe pulse widths to be increased or decreased.

3.2.4 PLL and MM Options

Allows the change of the APLL value (0, 20, 40...140), the NPLL value (256, 512), and the modulation mode (FSK).

3.2.5 LPT Port

Allows the user to change between the LPT1 and LPT2 ports of the controlling computer.

3.2.6 Help

Gives a brief description of each control box. For example, when the PLL box in the Mode Options section on the main program screen is clicked, the Help box reads:

Phase-Lock Loop
0: Off
1: On
Valid in Mode 0 or 1.

Most of the other control boxes follow this format. The first line indicates what portion of the TRF6900 is being controlled. The next two lines indicate the bit value. If the PLL is off, bit 12 of Words C and D are equal to 0. If it is on, bit 12 is equal to 1. The last line indicates this control works in both Mode 0 and Mode 1.

Double clicking in the Help box on the main program screen, activates the chip layout screen.

3.2.7 Words

This section updates the binary words after changes are made to the control options. Clicking on the box next to the word individually sends each word. Clicking on the *Send Words Now (F12)* button on the main program screen or pressing F12 on the keyboard sends all the words to the TRF6900.

3.2.8 Operation Mode

Operation Mode shows whether the TRF6900 is enabled, which mode (0 or 1) is selected, and whether the transmit (TX) data line is on or off.

3.2.9 Changing Values on the Main Program Screen

❏ Synthesizer Section

CLK	Type the desired clock frequency inside the box or use the arrows located at the right side of the box.
Desired Freq.	Type the desired transmit or LO receive frequency inside the box or use the arrows located at the right side of the box.
PreScaler	Click inside the box to change divide-by-N value between 256 and 512. The value of NPLL under PLL and MM Options changes when the PreScaler value changes.

❏ Mode Options

PLL	Click inside the box to turn the PLL on or off (Turn on for transmit or receive).
VCO	The VCO is always on. Clicking has no effect.
Pwr Amp	Use the arrow at the side of the box to select the desired power amplifier attenuation.

Slicer	Click inside the box to turn the data slicer on or off.
SLCTL	Click inside the box to select between Learn and Hold modes. This will only work when the data slicer is on.
LPF	Click inside the box to turn LPF on or off.
DSW	Click inside the box to select between LIM and RSSI. This changes the position of the data switch inside the TRF6900. The data switch selects between the output of RSSI and FM/FSK demodulator (LIM) as the input to the LPF amplifier. (See block diagram in Figure 1−1)
RSSI	Click inside the box to turn RSSI on or off.
LIM	Click inside the box to turn LIM (second IF amp/limiter) on or off.
IF	Click inside the box to turn the first IF amplifier on or off.
MIX	Click inside the box to turn the RF mixer on or off.
LNA	Click the arrow beside the box to turn LNA off, set to High Gain mode, or set to Low Gain mode.

- Output Parameters

Enable	Click inside the box to turn the TRF6900 on or off.
TXData	Click inside the box to switch the TXData line between high or low.
Mode	Click inside the box to switch the mode line between 0 and 1.
Clock Width	Type inside the box to increase or decrease the clock pulse width (this should not be changed during normal use).
Strobe Width	Type inside the box to increase or decrease the strobe pulse width (this should not be changed during normal use).

- PLL and MM Options

APLL	Use arrows on side of box to select between values of 0, 20, 40, 60, 80, 100, 120, and 140.
NPLL	Click inside of the box to change the divide-by-N value between 256 and 512. The value of PreScaler under Synthesizer changes when the NPLL value changes.
MM	Modulation mode is fixed to FSK modulation mode.

- LPT Port

LPT_x	Click inside the box to chose between PC parallel ports LPT 1 or LPT 2.

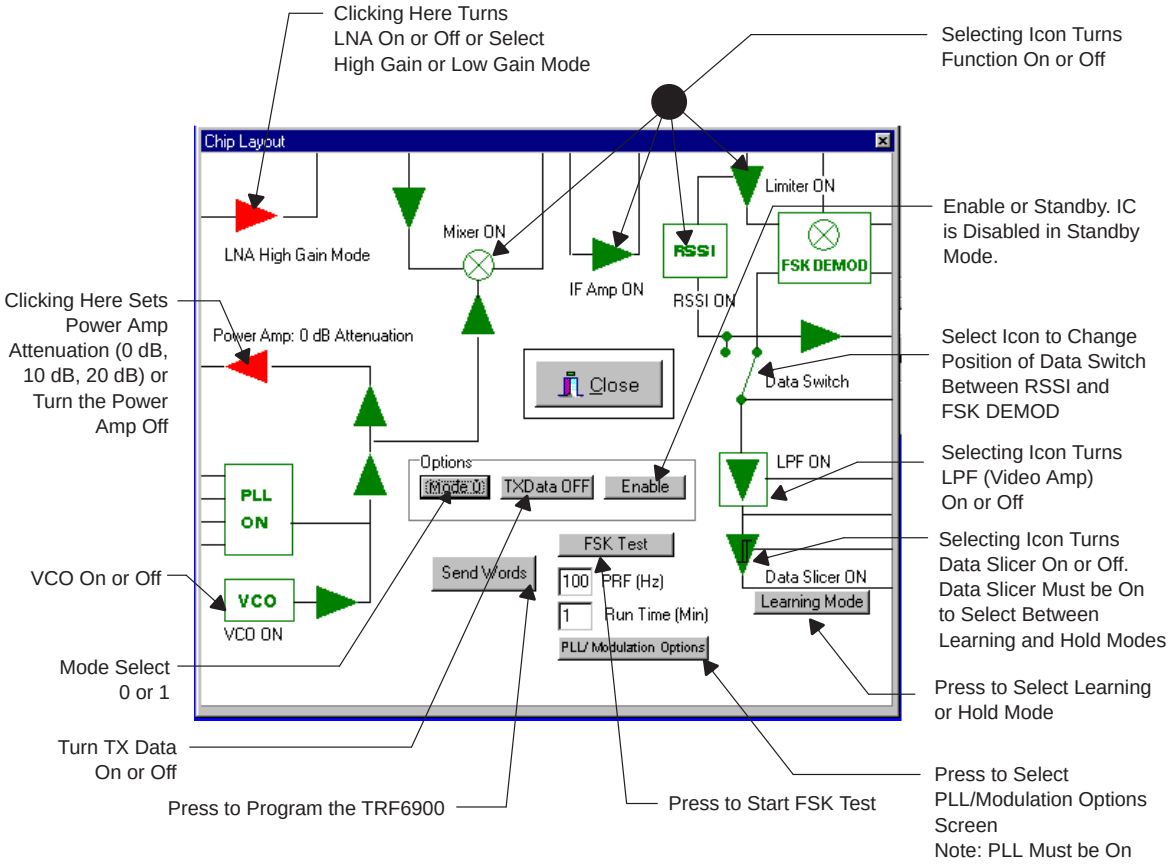
- Help

  Help — When any box on the main program screen is selected, (clicked inside of box with mouse) the Help screen displays the valid selections for that box. Double clicking inside the Help box causes the chip layout screen to be displayed as shown if Figure 3−2.

3.3 Chip Layout Screen

The chip layout screen can be accessed by double clicking on the left mouse button in the Help section of the main program screen. The chip layout screen appears as a simplified internal schematic of the TRF6900 as shown in Figure 3−2.

Figure 3−2. Chip Layout Screen



- The 12 Mode Options (e.g., the PLL, VCO, LNA, etc.) are controlled from the chip layout screen, as well as the main program screen. Changes made in either the main program screen or the chip layout screen simultaneously update both screens. The user can also control the chip enable, TXData, and mode control lines from the chip layout screen.

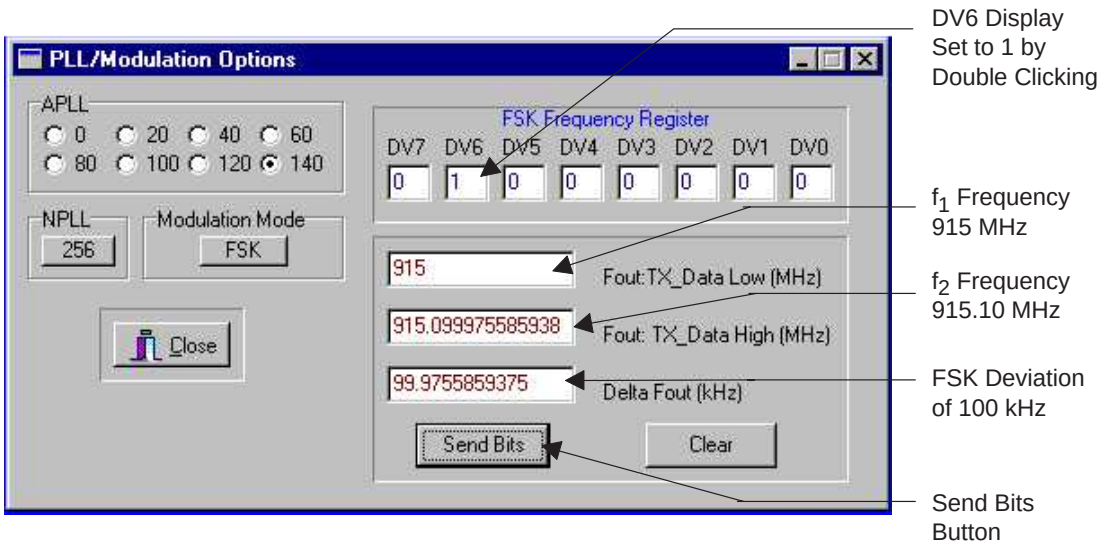
- The user can select FSK Modulation. The FSK Test button, located on the chip layout screen, allows the user to transmit data using the TRF6900. Options for use with the FSK Test button are the pulse repetition frequency (PRF), which is defaulted to 100 Hz, and the Run Time (Min), which can be set in minutes. For example, if you want the test to run for five minutes, set Run Time (Min) to 5.

- The PLL/Modulation Options button brings up the PLL/Modulation Options screen as shown in Figure 3−3. This button is activated only when the PLL is on.

3.4 PLL/Modulation Options Screen

The PLL/Modulation Options screen is accessed by pressing the PLL/Modulation Option button, located on the chip layout screen, and is displayed as shown in Figure 3−3.

Figure 3−3. PLL/Modulation Options Screen



The PLL/Modulations Options screen is divided into four sections:

- APLL

  Controls the acceleration factor for the PLL. The values are 0, 20, 40, 60, 80, 100, 120, and 140. Any changes are automatically updated in the PLL and MM Options section of the main program screen, after pressing the *Send Bits* button located on the PLL screen.

- NPLL

  Controls the N-Divider of the PLL. The NPLL can be set to either 256 or 512. Any changes are automatically updated in the NPLL box on the main program screen, after pressing the *Send Bits* button located on the PLL screen.

- Modulation Mode

  Allows the user to select FSK modulation. Any changes are automatically updated in the MM box on the main program screen, after pressing the *Send Bits* button located on the PLL screen.

- FSK Frequency Register

  This section acts as a calculator, and sets bits 20−13 of Word D to the user defined bits. The bits of the FSK deviation register (DV7−DV0) can be set individually by double clicking inside each *DVx* box. After setting all bits, press the *Send Bits* button located on the PLL screen. The bits of the frequency register will be mapped to Word D on the main program screen and highlighted in green. Furthermore, Fout: TX_Data High (MHz), Fout: TX_Data Low (MHz) frequencies, and their difference (Delta Fout kHz), are calculated and displayed.

Press the *Send Bits* button located on the PLL/Modulation Options screen to program the TRF6900. Press the *Close* button to return to the chip layout screen.

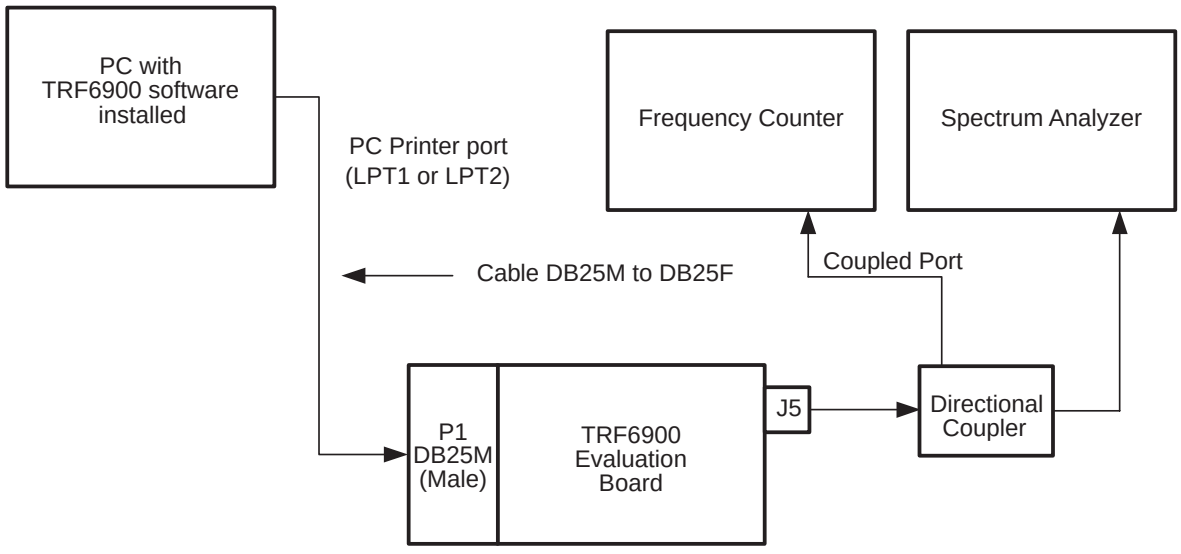
3.5 Testing of Transmitter

To perform tests of the transmitter section of the TRF6900, perform the following steps:

Step 1: Test Setup:

Set up the test bench as shown in Figure 3−4.

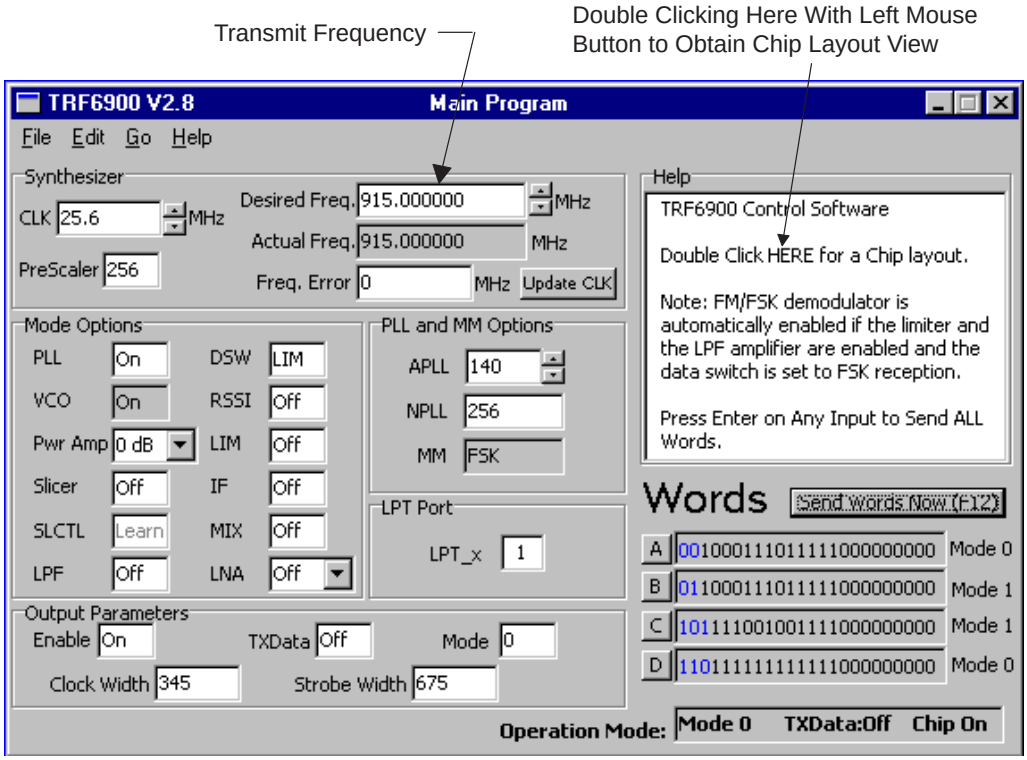
Figure 3−4. Block Diagram for Testing of the TRF6900 EVM Transmitter Section



Step 2: Software Programming:

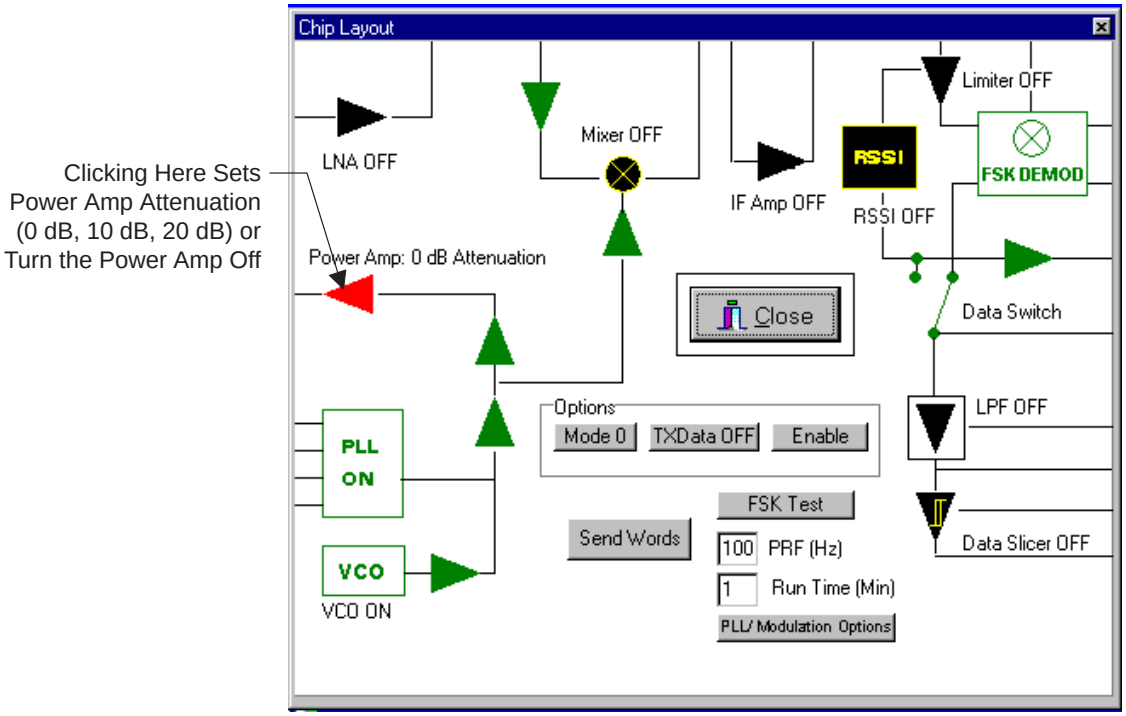
For testing the TRF6900 transmitter section, set the main program screen and the chip layout screen as shown in Figure 3−5 and Figure 3−6.

Figure 3−5. Main Program Screen



Chip Layout Screen of TRF6900 Software for Transmitter Testing

Figure 3−6. Chip Layout Screen

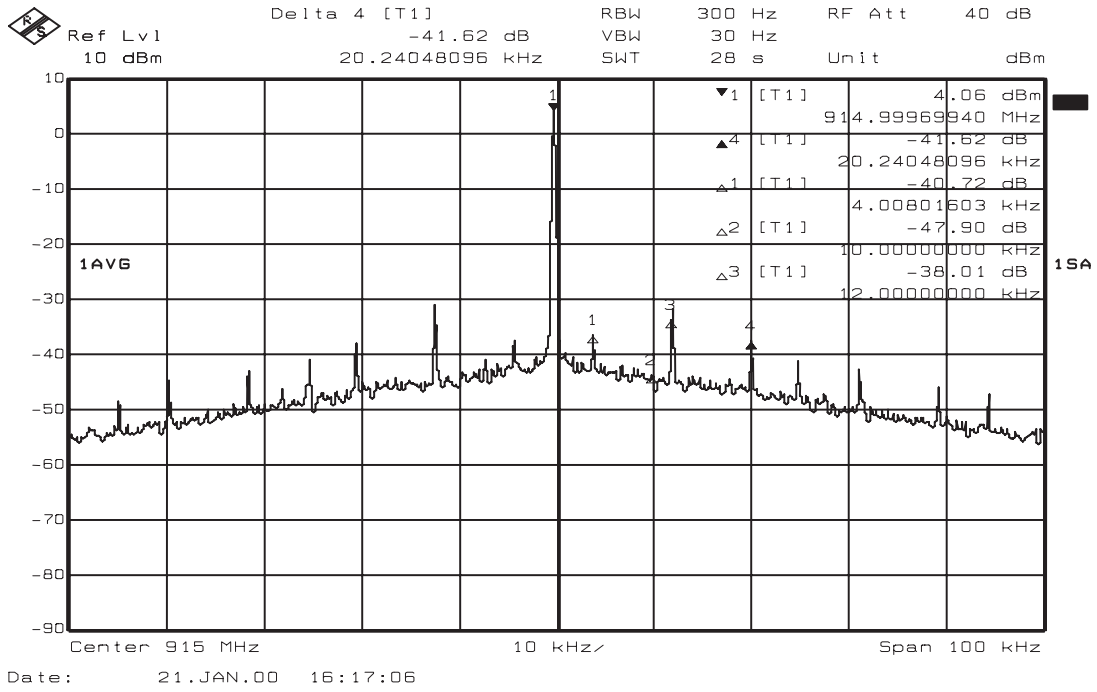


After setup is complete, press the *Send Words* button on the chip layout screen or the *Send Words Now (F12)* button on the main program screen to send the programming words to the TRF6900.

Step 3: Spectrum Analyzer Setup and Clock Offset Procedure

Set up the spectrum analyzer to observe the following:

Figure 3−7. Spectrum Analyzer



Clock Offset Procedure

1) Use the test setup as seen in Figure 3−4 and transmitter software setup as shown in Figure 3−5.

2) Observe the frequency reading on the frequency counter.

3) Subtract 915.000000 MHz from the frequency counter reading.

4) Enter the difference value in the Freq. Error box in the main program screen as shown in Figure 3−8.

5) If difference value is negative, enter – sign, followed by the difference value

   Example: Frequency Counter reading is 914.996000 MHz.
   Subtracting 915.000 MHz from 914.996 MHz yields a difference of –4000 Hz. This difference is entered in the Freq. Error block as −0.004 MHz (see Figure 3−8).

6) Press the Update CLK button on the main program screen.

7) Observe that clock frequency is updated as shown in Figure 3−9.

8) Pressing the Update CLK button twice causes the frequency offset to be cleared.

Figure 3−8. Input of Frequency Error

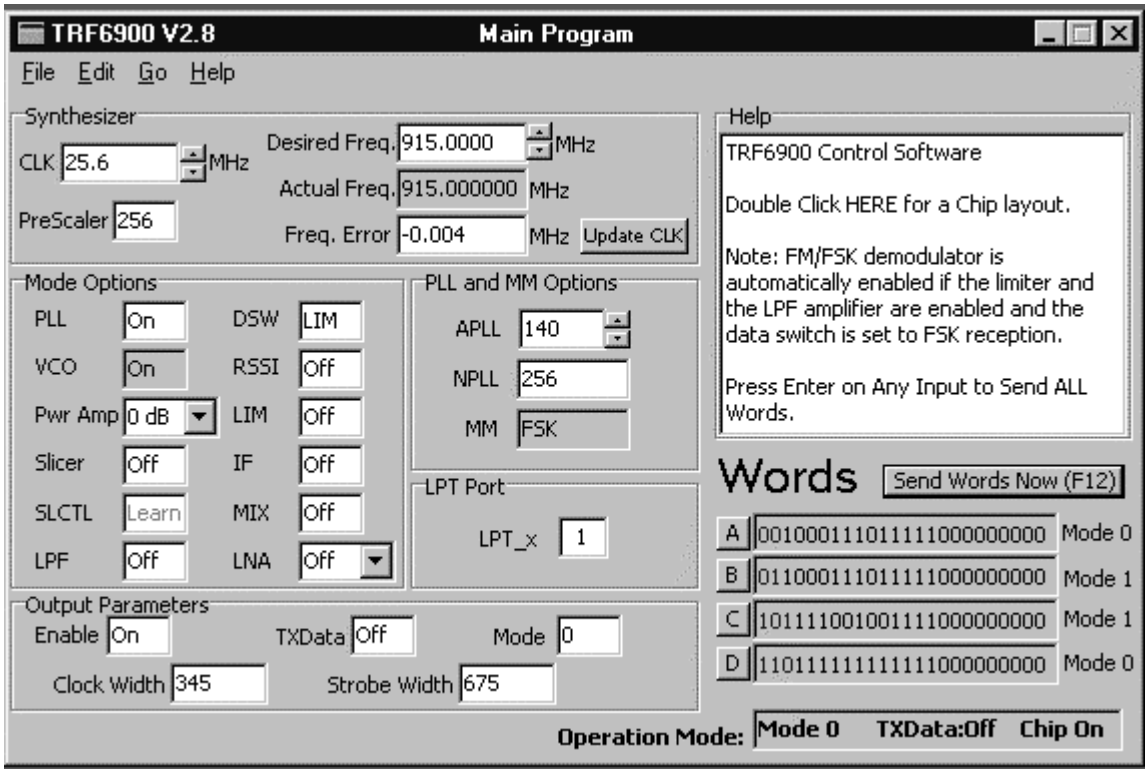
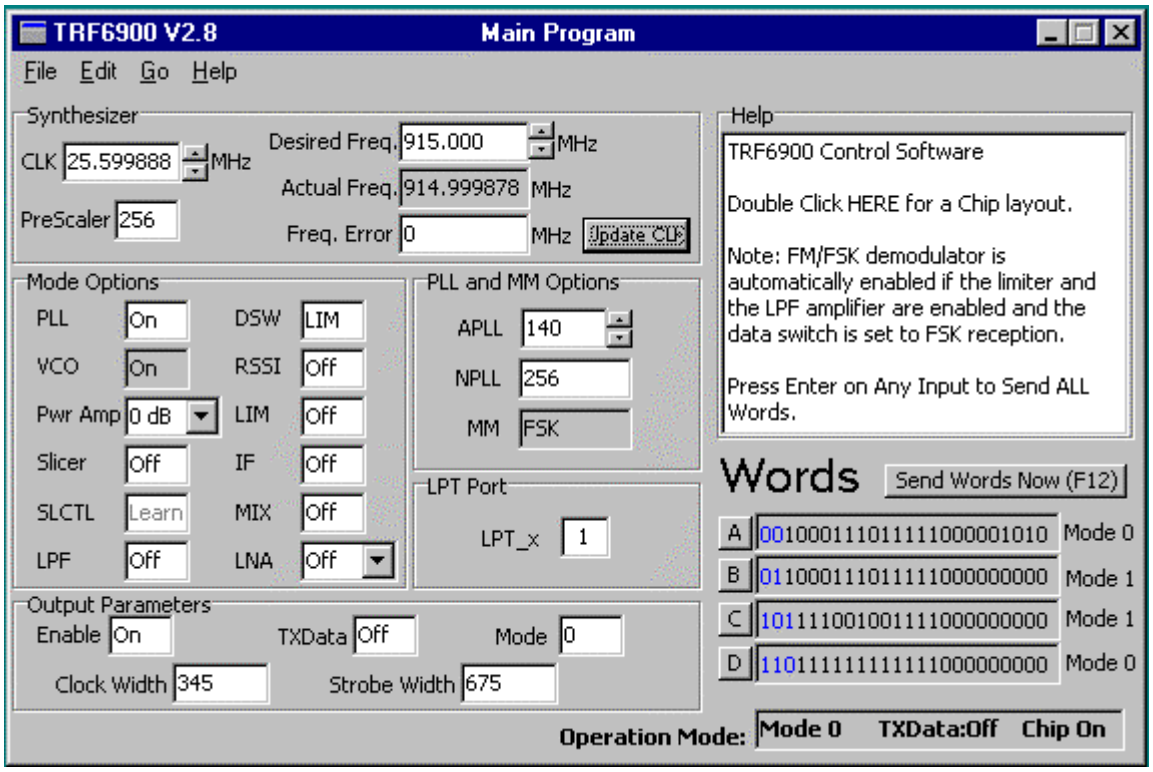


Figure 3−9. Main Panel Display After Clock Offset Is Applied

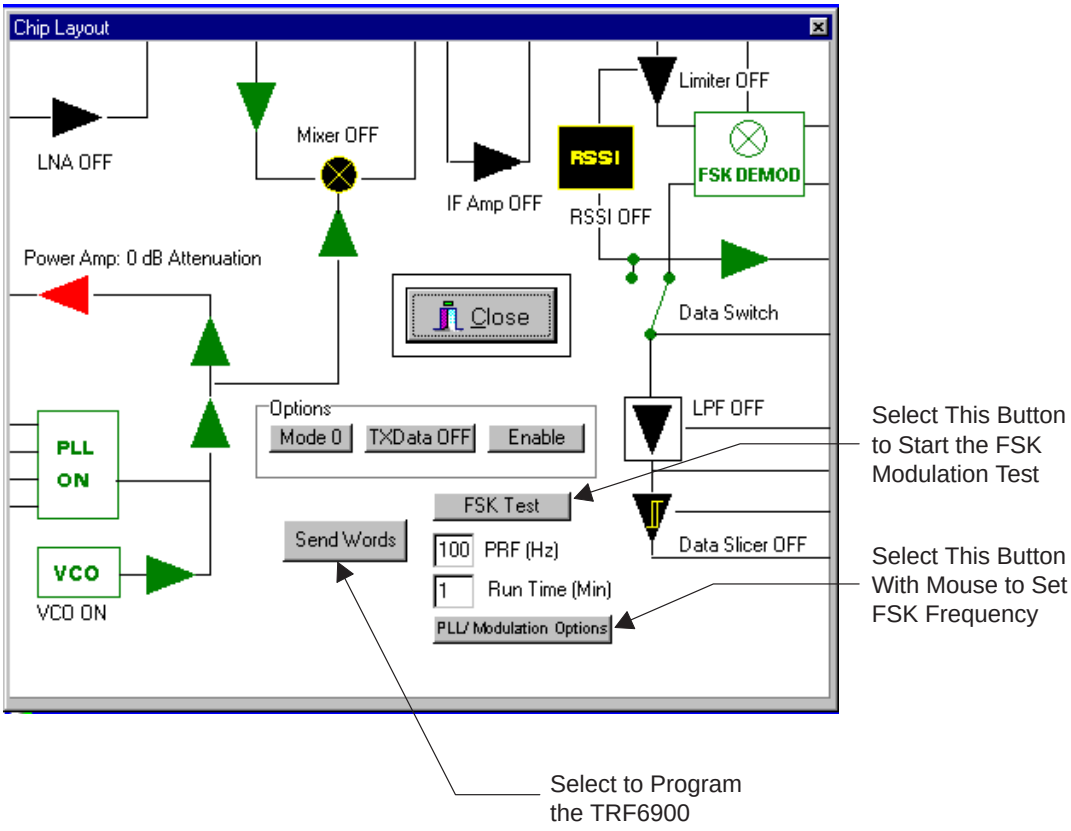


Step 4: FSK Modulation Output Test

On the chip layout screen press the *PLL/Modulation Options* button.

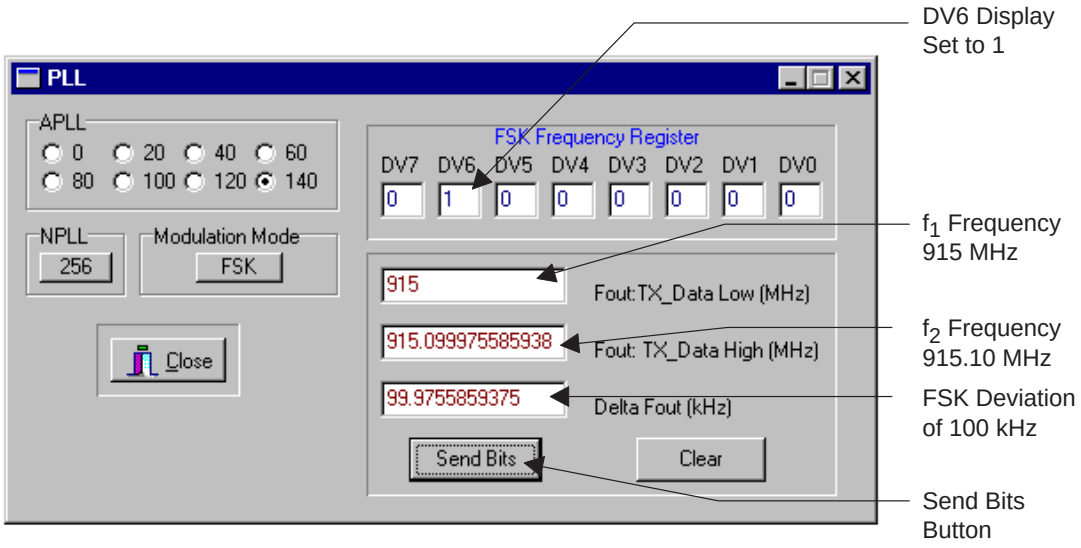
The PLL/Modulation Options View Is Set Up as Shown in Figure 3−10:

Figure 3−10. PLL/Modulation Options View



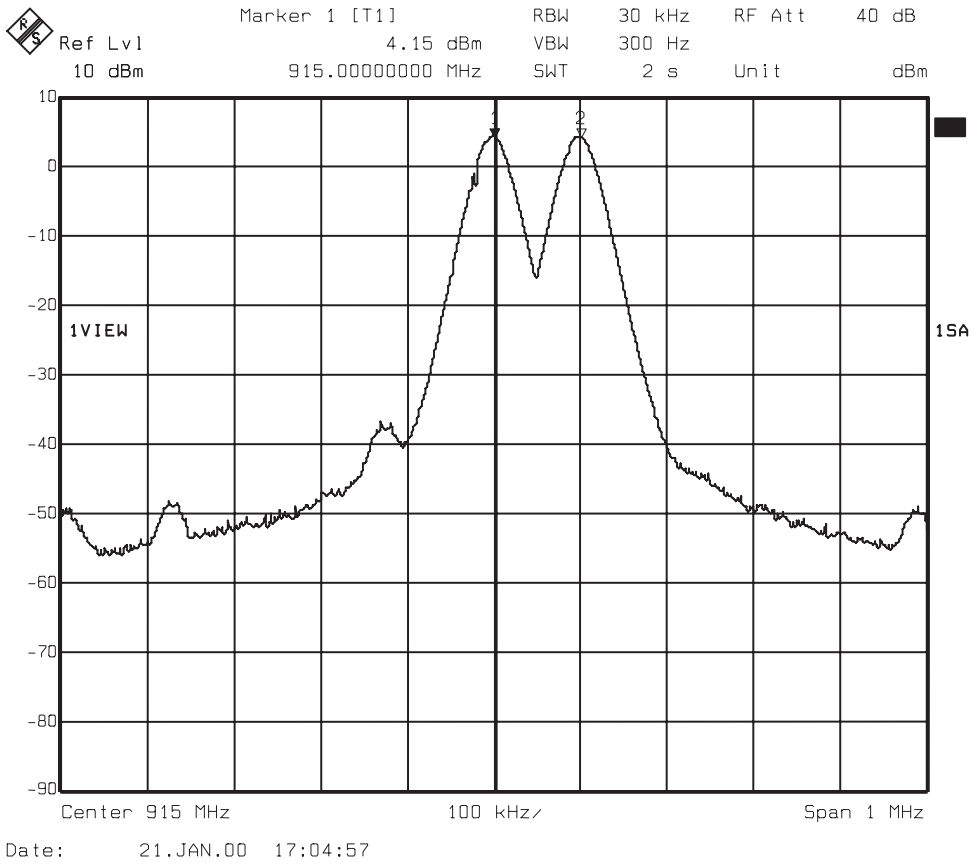
- ❑ Set the *DVx* bits, as shown in Figure 3−11, by double clicking inside each *DVx* box to set the value to either a 1 or 0. For this example only DV6 is set to a 1.
- ❑ Press the *Send Bits* button located on the PLL/Modulations Options screen, to obtain the results shown in Figure 3−11.
- ❑ Press the Close button located on the PLL/Modulations Options screen.

Figure 3−11. PLL/Modulation Options Screen



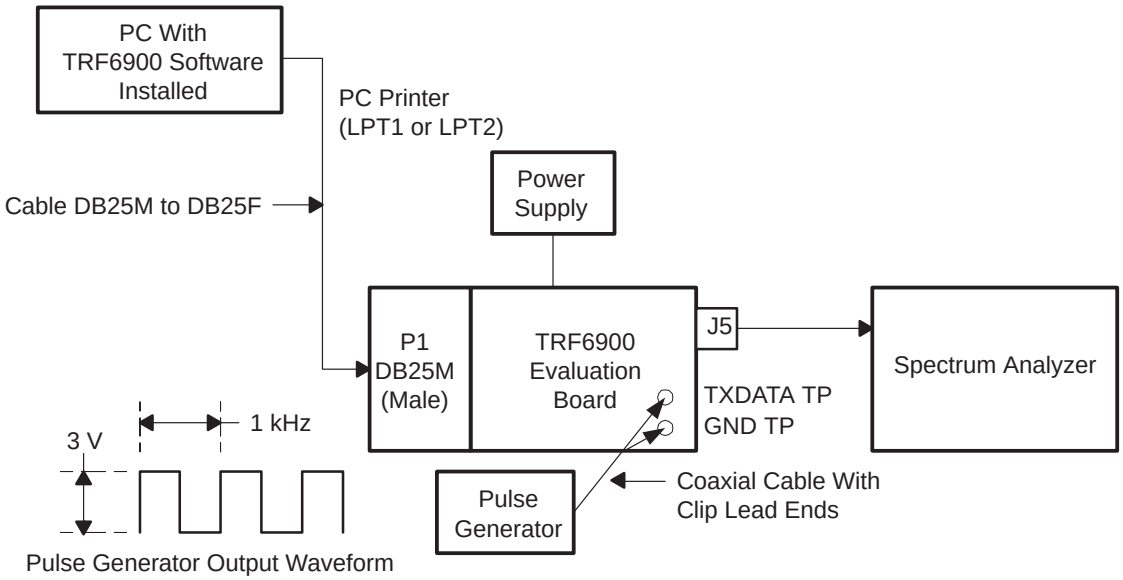
- ❑ Press the *Send Words* button on the chip layout screen or the *Send Words Now (F12)* on the main program screen.
- ❑ Press the *FSK Test* button on the chip layout screen, as shown in Figure 3−10, to start the FSK test.
- ❑ Set up the spectrum analyzer to observe the spectrum analyzer display as shown in Figure 3−12.

Figure 3−12. FSK Output From Transmitter



Note: This is FSK modulation with f_1 equal to 915.0 MHz, f_2 equal to 915.10 MHz and 100 Hz data rate. The f_1 frequency is the 0 frequency. The f_2 frequency is the 1 frequency.

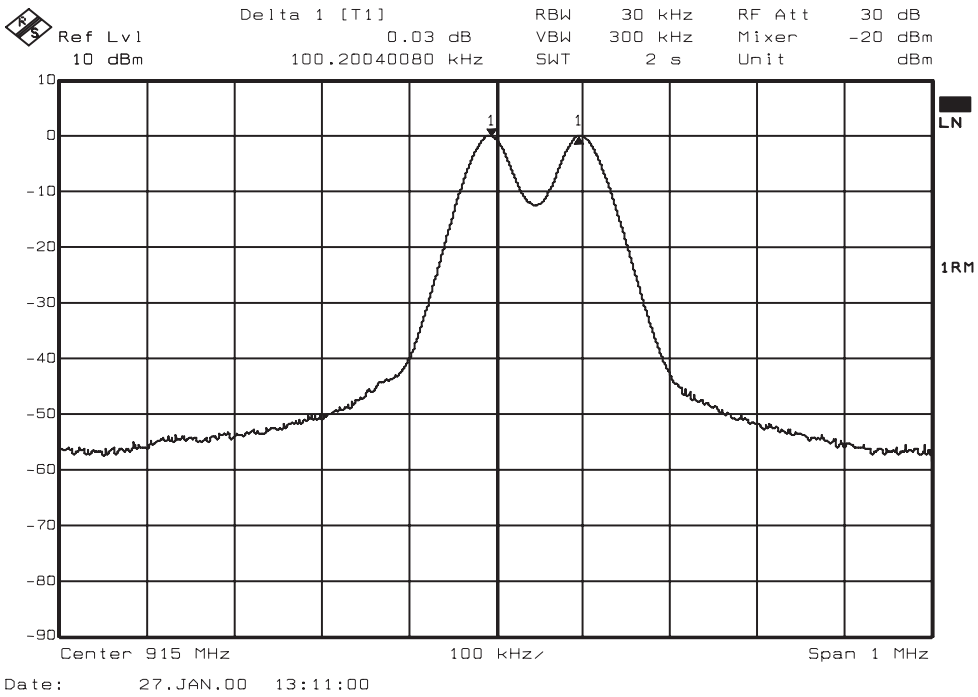
Figure 3−13. Block Diagram for Testing of the TRF6900 EVM Transmitter Section With an External Pulse Generator



To use an external pulse generator to supply transmit data, set up the test bench as shown in Figure 3−13.

❑ Perform the FSK modulation output test as described in the previous section. In this new setup, an external pulse generator provides the modulation. The *FSK Test* button on the chip layout screen does not need to be pressed to start the FSK test.

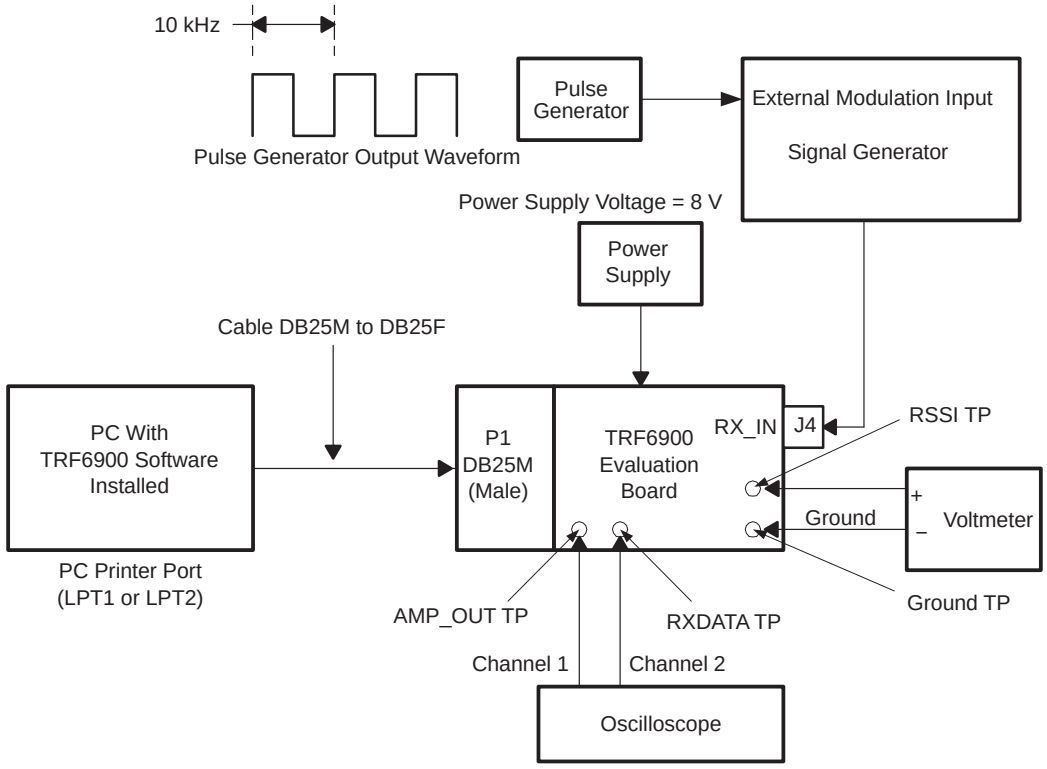
Figure 3−14. FSK Output From Transmitter With an External Modulation



Note: This is FSK modulation with f_1 equal to 915.0 MHz, f_2 equal to 915.10-MHz and 1000-Hz data rate. The f_1 frequency is the 0 frequency. The f_2 frequency is the 1 frequency.

3.6 Testing of the Receiver

Figure 3−15. Test Setup for TRF6900 Receiver Testing



3.6.1 Test Equipment Setup

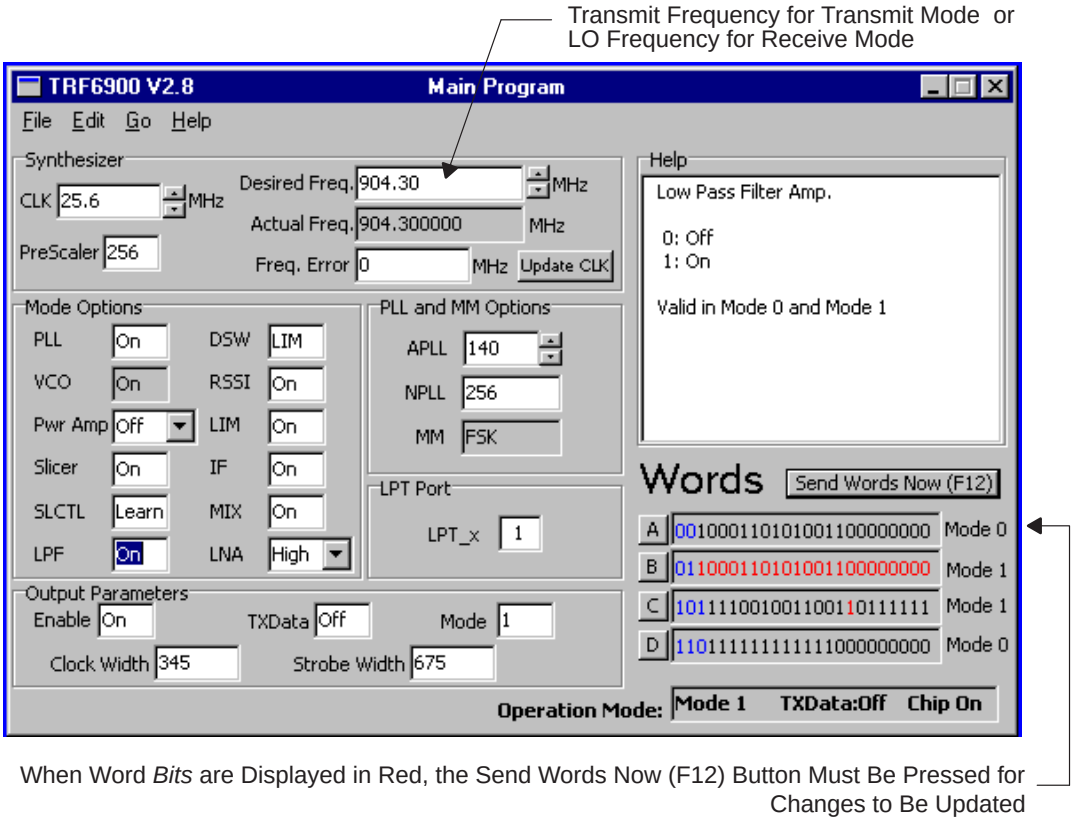
Set the external signal generator and oscilloscope according to the following:

Signal Generator		Oscilloscope		
Center frequency	915.000 MHz	Channel	Volts/Division	Time/Division
FM frequency deviation from carrier	50 kHz	1	1	20 µs
External modulation input	10 kHz	2	2	20 µs

3.6.2 Software Programming for Receiver Testing

Set up the main program screen and the chip layout screen as shown in Figure 3−16 and Figure 3−17.

Figure 3−16. Main Program Screen



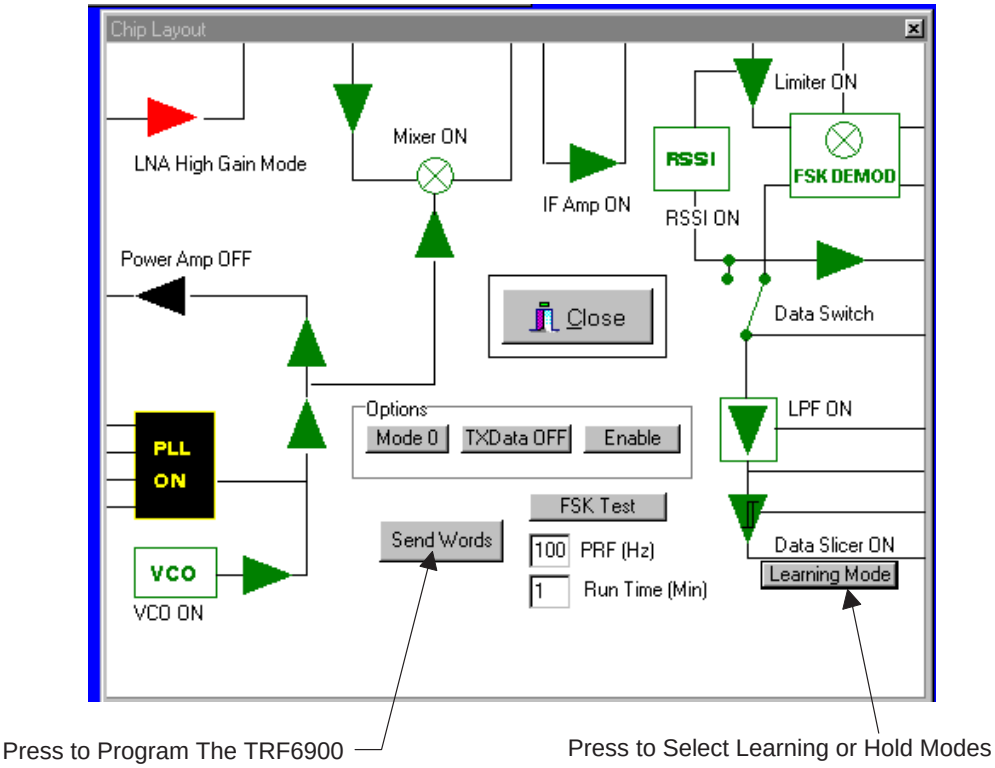
Note:

The receiver frequency of the TRF6900 is 915.000 MHz. The TRF6900 is using a 10.7-MHz IF frequency. Therefore, the local oscillator (LO) is set to a frequency of 904.30 MHz.

LO frequency = RF frequency – IF Frequency (904.30 = 915.000 – 10.7)

The desired frequency block of the TRF6900 software control program is used to set the internal VCO frequency of the TRF6900. (See block diagram)

Figure 3−17. Chip Layout Screen for Receiver Testing



3.6.3 Learning and Hold Modes

During the Learning Mode, the data slicer is constantly integrating the incoming signal and charging capacitor C25 (see schematic diagram) to a dc voltage level (V_{ref}) that is proportional to the average demodulation dc level. Capacitor C25 is connected to terminal 29 of the TRF6900 (*S&H_CA* terminal).

During the Hold Mode, the data slicer stops integrating and uses the dc voltage level stored on capacitor C25 as the decision threshold between a logic 1 and logic 0 as measured on terminal 28 *DATA_OUT*. For receiver measurements, the output of terminal 28 *DATA_OUT* is measured at the RXDATA test point.

3.6.4 Measured Receive Data

The data plots in Figure 3−18 and Figure 3−19, show the measured receive data at the AMP_OUT and RXDATA test points for input signals at −50 dBm and −90 dBm, respectively.

Figure 3−18. Measured Data With −50 dBm Input Signal at AMP_OUT and RXDATA Test Points

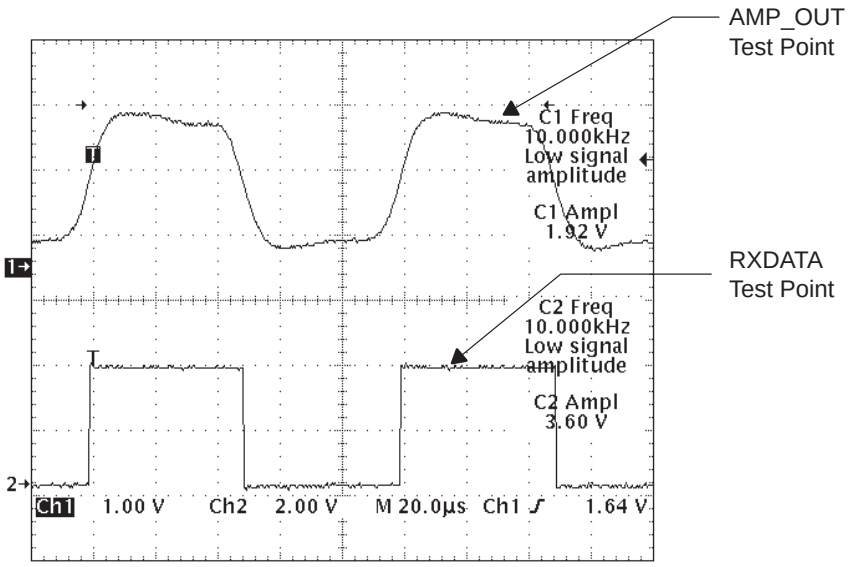


Figure 3−19. Measured Data With −90 dBm Input Signal at AMP_OUT and RXDATA Test Points