TP3076 COMBO® II Programmable PCM CODEC/Filter for ISDN and Digital Phone Applications

Check for Samples: TP3076

FEATURES

- **Complete CODEC and Filter System Including:**
  - **Transmit and Receive PCM Channel Filters**
  - **μ-law or A-law Companding Coder and Decoder**
  - **Receive Power Amplifier Drives 300Ω**
  - **4.096 MHz Serial PCM Data (max)**
- **Programmable Functions:**
  - **Transmit Gain: 25.4 dB Range, 0.1 dB Steps**
  - **Receive Gain: 25.4 dB Range, 0.1 dB Steps**
  - **Time-slot Assignment; to 64 Slots/frame**
  - **4 Interface Latches**
  - **A or μ-law**
  - **Analog Loopback**
  - **Digital Loopback**
- **Direct Interface to Solid-state SLICs**
- **Standard Serial Control Interface**
- **80 mW Operating Power (typ)**
- **1.5 mW Standby Power (typ)**
- **Designed for CCITT and LSSGR Specifications**
- **TTL and CMOS Compatible Digital Interfaces**

DESCRIPTION

The TP3076 is a second-generation combined PCM CODEC and Filter devices optimized for digital switching applications on subscriber line and trunk cards and digital phone applications. Using advanced switched capacitor techniques, COMBO II combines transmit bandpass and receive lowpass channel filters with a companding PCM encoder and decoder. The devices are A-law and μ-law selectable and employ a conventional serial PCM interface capable of being clocked up to 4.096 MHz. A number of programmable functions may be controlled via a serial control port.

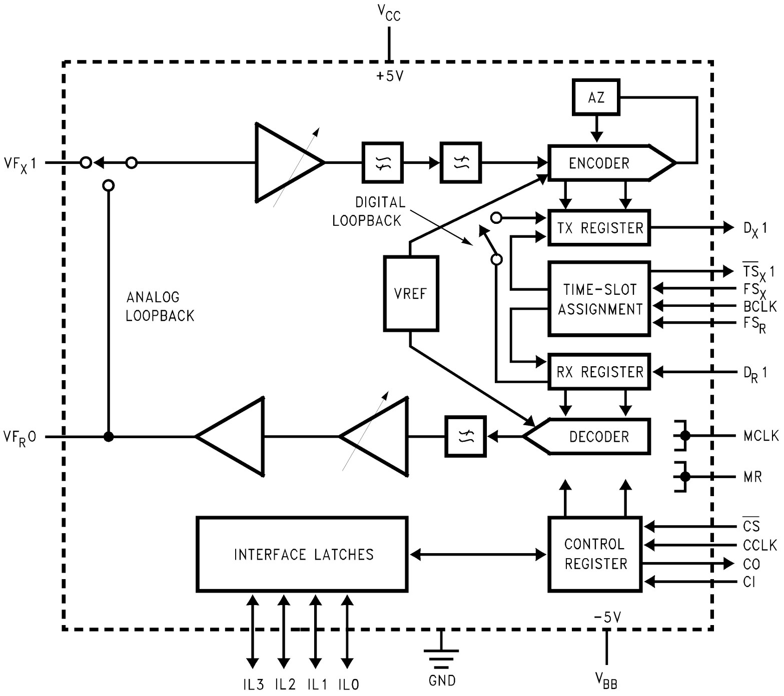
Channel gains are programmable over a 25.4 dB range in each direction.

To enable COMBO II to interface to the SLIC control leads, a number of programmable latches are included; each may be configured as either an input or an output. The TP3076 provides 4 latches.

NOTE

See also AN-614 COMBO II application guide.

Block Diagram



Connection Diagram

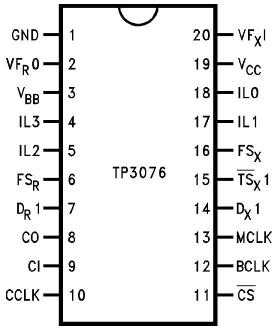


Figure 1. See Package PDIP (NFH)

PIN DESCRIPTIONS

Pin	Description
V_{CC}	+5V ±5% power supply.
V_{BB}	−5V ±5% power supply.
GND	Ground. All analog and digital signals are referenced to this pin.
FS_X	Transmit Frame Sync input. Normally a pulse or squarewave with an 8 kHz repetition rate is applied to this input to define the start of the transmit time slot assigned to this device (non-delayed data timing mode), or the start of the transmit frame (delayed data timing mode using the internal time-slot assignment counter).
FS_R	Receive Frame Sync input. Normally a pulse or squarewave with an 8 kHz repetition rate is applied to this input to define the start of the receive time slot assigned to this device (non-delayed data timing mode), or the start of the receive frame (delayed data timing mode using the internal time-slot assignment counter).
BCLK	Bit clock input used to shift PCM data into and out of the D_R and D_X pins. BCLK may vary from 64 kHz to 4.096 MHz in 8 kHz increments, and must be synchronous with MCLK.
MCLK	Master clock input used by the switched capacitor filters and the encoder and decoder sequencing logic. Must be 512 kHz, 1.536/1.544 MHz, 2.048 MHz or 4.096 MHz and synchronous with BCLK.

PIN DESCRIPTIONS (continued)

Pin	Description
VF_XI	The Transmit analog high-impedance input. Voice frequency signals present on this input are encoded as an A-law or μ-law PCM bit stream and shifted out on the selected D_X pin.
VF_RO	The Receive analog power amplifier output, capable of driving load impedances as low as 300Ω (depending on the peak overload level required). PCM data received on the assigned D_R pin is decoded and appears at this output as voice frequency signals.
D_X1	This transmit data TRI-STATE® output remains in the high impedance state except during the assigned transmit time slot on the assigned port, during which the transmit PCM data byte is shifted out on the rising edges of BCLK.
$\overline{TS}_X1$	Normally this open drain output is floating in a high impedance state except when a time-slot is active on the D_X output, when the $\overline{TS}_X1$ output pulls low to enable a backplane line-driver.
D_R1	This receive data input is inactive except during the assigned receive time slot of the assigned port when the receive PCM data is shifted in on the falling edges of BCLK.
CCLK	Control Clock input. This clock shifts serial control information into CI or out from CO when the $\overline{CS}$ input is low, depending on the current instruction. CCLK may be asynchronous with the other system clocks.
CI	Control Data Input pin. Serial control information is shifted into COMBO II on this pin when $\overline{CS}$ is low. Byte 1 of control information is always written into COMBO II, while the direction of byte 2 data is determined by bit 2 of byte 1, as defined in Table 1
CO	Control Data Output pin. Serial control or status information is shifted out of COMBO II on this pin when $\overline{CS}$ is low.
$\overline{CS}$	Chip Select input. When this pin is low, control information can be written to or read from COMBO II via CI or CO.
IL3–IL0	Each Interface Latch I/O pin may be individually programmed as an input or an output determined by the state of the corresponding bit in the Latch Direction Register (LDR). For pins configured as inputs, the logic state sensed on each input is latched into the Interface Latch Register (ILR) whenever control data is written to COMBO II, while $\overline{CS}$ is low, and the information is shifted out on the CO pin. When configured as outputs, control data written into the ILR appears at the corresponding IL pins.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

V_{CC} to GND	7V
Voltage at VF_XI	V_{CC} +0.5V to V_{BB} −0.5V
Voltage at Any Digital Input	V_{CC} +0.5V to GND −0.5V
Storage Temperature Range	−65°C to +150°C
V_{BB} to GND	−7V
Current at VF_R0	±100 mA
Current at Any Digital Output	±50 mA
Lead Temperature (Soldering, 10 sec.)	300°C

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

Electrical Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are ensured for V_{CC} = +5V ±5%, V_{BB} = −5V ±5%; T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL INTERFACES						
V_{IL}	Input Low Voltage(1)	All Digital Inputs (DC Meas.)			**0.7**	V
V_{IH}	Input High Voltage(1)	All Digital Inputs (DC Meas.)(2)	**2.0**			V
V_{OL}	Output Low Voltage	D_X1, $\overline{TS}_X1$, and CO, I_L = 3.2 mA, All Other Digital Outputs, I_L = 1 mA			**0.4**	V
V_{OH}	Output High Voltage	D_X1 and CO, I_L = −3.2 mA, All Other Digital Outputs (except $\overline{TS}_X$), I_L = −1 mA	**2.4**			V
		All Digital Outputs, I_L = −100 µA	V_{CC} − 0.5			V
I_{IL}	Input Low Current	Any Digital Input, GND < V_{IN} < V_{IL}	**−10**		**10**	µA
I_{IH}	Input High Current	Any Digital Input, except MR, V_{IH} < V_{IN} < V_{CC}	**−10**		**10**	µA
		MR Only	**−10**		**100**	
I_{OZ}	Output Current in High Impedance State (TRI-STATE®)	D_X1, $\overline{TS}_{X1}$ and CO IL3–IL0 when Selected as Inputs GND < V_{OUT} < V_{CC}	**−10**		**10**	µA
ANALOG INTERFACES						
I_{VFXI}	Input Current, VF_XI	−3.3V < VF_XI < 3.3V	**−1.0**		**1.0**	µA
R_{VFXI}	Input Resistance	−3.3V < VF_XI < 3.3V	**1.0**			MΩ
VOS_X	Input Offset Voltage Applied at VF_XI	Transmit Gain = 0 dB			200	mV
		Transmit Gain = 25.40 dB			10	mV
RL_{VFRO}	Load Resistance	Receive Gain = 0 dB	15k			Ω
		Receive Gain = −0.5 dB	600			
		Receive Gain = −1.2 dB	**300**			
CL_{VFRO}	Load Capacitance	RL_{VFRO} ≥ 300Ω CL_{VFRO} from VF_RO to GND			**200**	pF
RO_{VFRO}	Output Resistance	Steady Zero PCM Code Applied to D_R1		1.0	3.0	Ω
VOS_R	Output Offset Voltage at V_{FRO}	Alternating ± Zero PCM Code Applied D_R1, Maximum Receive Gain	**−200**		**200**	mV

(1) A signal is Valid if it is above V_{IH}or below V_{IL} and Invalid if it is between V_{IL} and V_{IH}. For the purposes of this specification the following conditions apply: a) All input signals are defined as: V_{IL} = 0.4V, V_{IH} = 2.7V, t_R < 10 ns, t_F < 10 ns. b) t_R is measured from V_{IL} to V_{IH}. t_F is measured from V_{IH} to V_{IL}. c) Delay Times are measured from the input signal Valid to the output signal Valid. d) Setup Times are measured from the data input Valid to the clock input Invalid. e) Hold Times are measured from the clock signal Valid to the data input Invalid. f) Pulse widths are measured from V_{IL} to V_{IL} or from V_{IH} to V_{IH}.

(2) See definitions and timing conventions section.

Electrical Characteristics (continued)

Unless otherwise noted, limits printed in **BOLD** characters are ensured for V_{CC} = +5V ±5%, V_{BB} = −5V ±5%; T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER DISSIPATION						
$I_{CC}0$	Power Down Current	CCLK, CI, CO = 0.4V, $\overline{CS}$ = 2.4V Interface Latches Set as Outputs with No Load, All Other Inputs Active, Power Amp Disabled		0.1	**0.6**	mA
$I_{BB}0$	Power Down Current	As Above		−0.1	**−0.3**	mA
$I_{CC}1$	Power Up Current	CCLK, CI, CO = 0.4V, $\overline{CS}$ = 2.4V No Load on Power Amp Interface Latches Set as Outputs with No Load		8.0	**11.0**	mA
$I_{BB}1$	Power Up Current	As Above		−8.0	**−11.0**	mA
$I_{CC}2$	Power Down Current	As Above, Power Amp Enabled		2.0	**3.0**	mA
$I_{BB}2$	Power Down Current	As Above, Power Amp Enabled		−2.0	**−3.0**	mA

Timing Specifications

Unless otherwise noted, limits printed in **BOLD** characters are ensured for V_{CC} = +5V ±5%; V_{BB} = −5V ±5%; T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C.

All timing parameters are measured at V_{OH} = 2.0V and V_{OL} = 0.7V.

See Definitions and Timing Conventions section for test methods information.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
MASTER CLOCK TIMING						
f_{MCLK}	Frequency of MCLK	Selection of Frequency is Programmable (See Table 5)		512 1536 1544 2048 **4096**		kHz kHz kHz kHz kHz
t_{WMH}	Period of MCLK High	Measured from V_{IH} to V_{IH} (1)	**80**			ns
t_{WML}	Period of MCLK Low	Measured from V_{IL} to V_{IL} (1)	**80**			ns
t_{RM}	Rise Time of MCLK	Measured from V_{IL} to V_{IH}			30	ns
t_{FM}	Fall Time of MCLK	Measured from V_{IH} to V_{IL}			30	ns
t_{HBM}	HOLD Time, BCLK LOW to MCLK HIGH		**50**			ns
t_{WFL}	Period of FS_X or FS_R Low	Measured from V_{IL} to V_{IL}	1			MCLK Period
PCM INTERFACE TIMING						
f_{BCLK}	Frequency of BCLK	May Vary from 64 kHz to 4096 kHz in 8 kHz Increments	**64**		**4096**	kHz
t_{WBH}	Period of BCLK High	Measured from V_{IH} to V_{IH}	**80**			ns
t_{WBL}	Period of BCLK Low	Measured from V_{IL} to V_{IL}	**80**			ns
t_{RB}	Rise Time of BCLK	Measured from V_{IL} to V_{IH}			30	ns
t_{FB}	Fall Time of BCLK	Measured from V_{IH} to V_{IL}			30	ns
t_{HBF}	Hold Time, BCLK Low to $FS_{X/R}$ High or Low		**30**			ns
t_{SFB}	Setup Time, $FS_{X/R}$ High to BCLK Low		**30**			ns
t_{DBD}	Delay Time, BCLK High to Data Valid	Load = 100 pF Plus 2 LSTTL Loads			**80**	ns

(1) Applies only to MCLK Frequencies ≥ 1.536 MHz. At 512 kHz a 50:50 ±2% Duty Cycle must be used.

Timing Specifications (continued)

Unless otherwise noted, limits printed in **BOLD** characters are ensured for V_{CC} = +5V ±5%; V_{BB} = −5V ±5%; T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C.
All timing parameters are measured at V_{OH} = 2.0V and V_{OL} = 0.7V.
See Definitions and Timing Conventions section for test methods information.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{DBZ}	Delay Time, BCLK Low to D_X1 Disabled if FS_X Low, FS_X Low to D_X1 disabled if 8th BCLK Low, or BCLK High to D_X1 Disabled if FS_X High	D_X1 disabled is measured at V_{OL} or V_{OH} according to Figure 4	**15**		**80**	ns
t_{DBT}	Delay Time, BCLK High to $\overline{TS}_X$ Low if FS_X High, or FS_X High to $\overline{TS}_X$ Low if BCLK High (Nondelayed mode); BCLK High to $\overline{TS}_X$ Low (delayed data mode)	Load = 100 pF Plus 2 LSTTL Loads			60	ns
t_{ZBT}	TRI-STATE Time, BCLK Low to $\overline{TS}_X$ High if FS_X Low, FS_X Low to $\overline{TS}_X$ High if 8th BCLK Low, or BCLK High to $\overline{TS}_X$ High if FS_X High		15		60	ns
t_{DFD}	Delay Time, $FS_{X/R}$ High to Data Valid	Load = 100 pF Plus 2 LSTTL Loads, Applies if $FS_{X/R}$ Rises Later Than BCLK Rising Edge in Non-Delayed Data Mode Only			**80**	ns
t_{SDB}	Setup Time, D_R1 Valid to BCLK Low		**30**			ns
t_{HBD}	Hold Time, BCLK Low to D_R1 Invalid		**15**			ns
SERIAL CONTROL PORT TIMING						
f_{CCLK}	Frequency of CCLK				**2048**	kHz
t_{WCH}	Period of CCLK High	Measured from V_{IH} to V_{IH}	**160**			ns
t_{WCL}	Period of CCLK Low	Measured from V_{IL} to V_{IH}	**160**			ns
t_{RC}	Rise Time of CCLK	Measured from V_{IL} to V_{IH}			50	ns
t_{FC}	Fall Time of CCLK	Measured of V_{IH} to V_{IL}			50	ns
t_{HCS}	Hold Time, CCLK Low to $\overline{CS}$ Low	CCLK1	**10**			ns
t_{HSC}	Hold Time, CCLK Low to $\overline{CS}$ High	CCLK8	**100**			ns
t_{SSC}	Setup Time, $\overline{CS}$ Transition to CCLK Low		**60**			ns
t_{SSC0}	Setup Time, $\overline{CS}$ Transition to CCLK High	To Insure CO is Not Enabled for Single Byte	60			ns
t_{SDC}	Setup Time, CI Data In to CCLK Low		**50**			ns
t_{HCD}	Hold Time, CCLK Low to CO Invalid		50			ns
t_{DCD}	Delay Time, CCLK High to CO Data Out Valid	Load = 100 pF Plus 2 LSTTL Loads			**80**	ns

Timing Specifications (continued)

Unless otherwise noted, limits printed in **BOLD** characters are ensured for V_{CC} = +5V ±5%; V_{BB} = −5V ±5%; T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C.
All timing parameters are measured at V_{OH} = 2.0V and V_{OL} = 0.7V.
See Definitions and Timing Conventions section for test methods information.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{DSD}	Delay Time, $\overline{CS}$ Low to CO Valid	Applies Only if Separate $\overline{CS}$ Used for Byte 2			**80**	ns
t_{DDZ}	Delay Time, $\overline{CS}$ or 9th CCLK High to CO High Impedance	Applies to Earlier of $\overline{CS}$ High or 9th CCLK High	15		80	ns
INTERFACE LATCH TIMING						
t_{SLC}	Setup Time, IL to CCLK 8 of Byte 1	Interface Latch Inputs Only	**100**			ns
t_{HCL}	Hold Tme, IL Valid from 8th CCLK Low (Byte 1)		50			ns
t_{DCL}	Delay Time CCLK8 of Byte 2 to IL	Interface Latch Outputs Only C_L = 50 pF			200	ns

Timing Diagrams

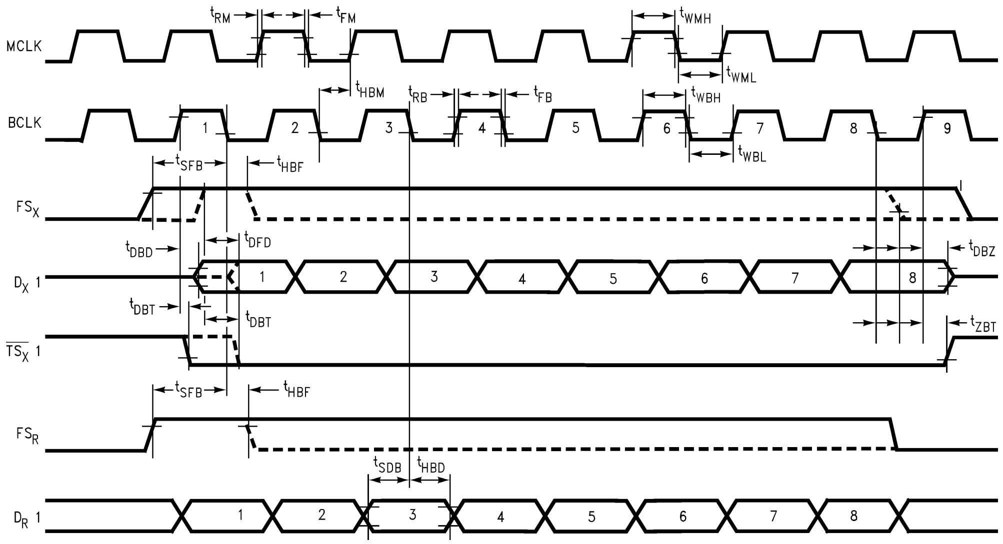


Figure 2. Non-Delayed Data Timing Mode

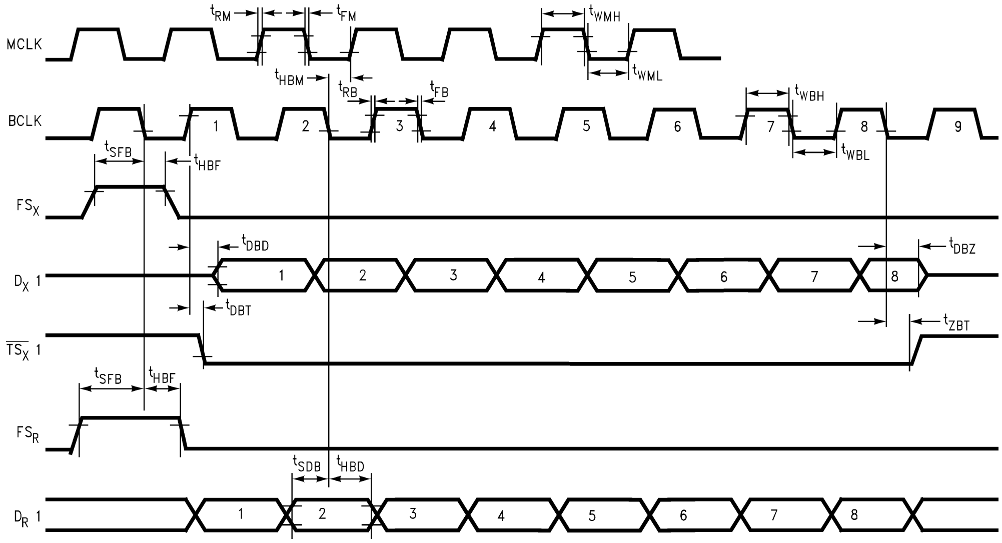


Figure 3. Delayed Data Timing Mode

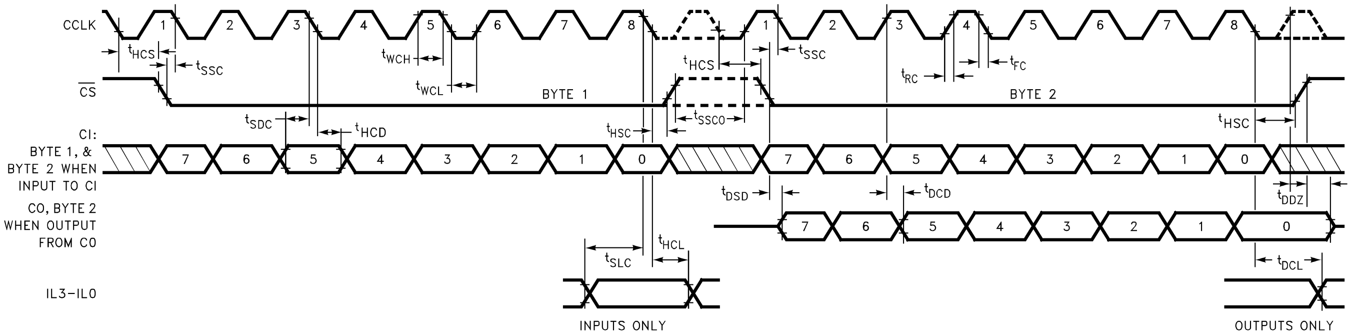


Figure 4. Control Port Timing

Transmission Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are ensured for V_{CC} = +5V ±5%, V_{BB} = −5V ±5%; T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. f = 1015.625 Hz, VF_XI = 0 dBm0, D_R1 = 0 dBm0 PCM code. Transmit and receive gains programmed for maximum 0 dBm0 test levels (0 dB Gain). All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AMPLITUDE RESPONSE						
	Absolute Levels	The Maximum 0 dBm0 Levels Are:				
		VF_XI		1.375		Vrms
		VF_RO (15 kΩ Load)		1.964		Vrms
		The Minimum 0 dBm0 Levels are:				
		VF_XI		73.8		mVrms
		VF_RO (Any Load ≥ 300Ω)		105.0		mVrms
G_{XA}	Transmit Gain Absolute Accuracy	Transmit Gain Programmed for Maximum 0 dBm0 Test Level. Measure Deviation of Digital Code from Ideal 0 dBm0 PCM Code at D_X1.				
		T_A = 25°C	**−0.15**		**0.15**	dB

Transmission Characteristics (continued)

Unless otherwise noted, limits printed in **BOLD** characters are ensured for V_{CC} = +5V ±5%, V_{BB} = −5V ±5%; T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. f = 1015.625 Hz, VF_XI = 0 dBm0, D_R1 = 0 dBm0 PCM code. Transmit and receive gains programmed for maximum 0 dBm0 test levels (0 dB Gain). All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
G_{XAG}	Transmit Gain Variation with Programmed Gain	T_A = 25°C, V_{CC} = 5V, V_{BB} = 5V				
		Programmed Gain from 0 dB to 19 dB				
		(0 dBm0 Levels of 1.619 Vrms to 0.182 Vrms)	**−0.1**		**0.1**	dB
		Programmed Gain from 19.1 dB to 25.4 dB				
		(0 dBm0 Levels of 0.180 Vrms to 0.087 Vrms)	**−0.3**		**0.3**	dB
		NOTE: ±0.1 dB Min/Max is Available as a Selected Part				
G_{XAF}	Transmit Gain Variation with	Relative to 1015.625 Hz(1)				
		Minimum Gain < G_X < Maximum Gain				
	Frequency	f = 60 Hz			−26	dB
		f = 200 Hz	−1.8		−0.1	dB
		f = 300 Hz to 3000 Hz	−0.15		0.15	dB
		f = 3400 Hz	−0.7		0.0	dB
		f = 400 Hz			−14	dB
		f ≥ 4600 Hz. Measure Response			−32	dB
		at Alias Frequency from 0 kHz to 4 kHz				
		G_X = 0.0 dB, VF_XI = 1.375 Vrms				
		Relative to 1015.625 Hz				
		f = 62.5 Hz			**−24.9**	dB
		f = 203.125 Hz	**−1.7**		**−0.1**	dB
		f = 343.75 Hz	**−0.15**		**0.15**	dB
		f = 515.625 Hz	**−0.15**		**0.15**	dB
		f = 2140.625 Hz	**−0.15**		**0.15**	dB
		f = 3156.25 Hz	**−0.15**		**0.15**	dB
		f = 3406.250 Hz	**−0.74**		**0.0**	dB
		f = 3984.375 Hz			**−13.5**	dB
		Relative to 1062.5 Hz(1)				
		f = 5250 Hz, Measure 2750 Hz			**−32**	dB
		f = 11750 Hz, Measure 3750 Hz			**−32**	dB
		f = 49750 Hz, Measure 1750 Hz			**−32**	dB
G_{XAT}	Transmit Gain Variation with Temperature	Measured Relative to G_{XA}, V_{CC} = 5V,				
		V_{BB} = −5V,	−0.1		0.1	dB
		Minimum gain < G_X < Maximum Gain				
G_{XAL}	Transmit Gain Variation with Signal Level	Sinusoidal Test Method.				
		Reference Level = 0 dBm0				
		VF_XI = −40 dBm0 to +3 dBm0	**−0.2**		**0.2**	dB
		VF_XI = −50 dBm0 to −40 dBm0	**−0.4**		**0.4**	dB
		VF_XI = −55 dBm0 to −50 dBm0	**−1.2**		**1.2**	dB
G_{RA}	Receive Gain Absolute Accuracy	Receive Gain Programmed for Maximum				
		0 dBm0 Test Level. Apply 0 dBm0	**−0.15**		**0.15**	dB
		PCM Code to D_R1. Measure VF_R0.				
		T_A = 25°C				

(1) A multi-tone test technique is used.

Transmission Characteristics (continued)

Unless otherwise noted, limits printed in **BOLD** characters are ensured for V_{CC} = +5V ±5%, V_{BB} = −5V ±5%; T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. f = 1015.625 Hz, VF_XI = 0 dBm0, D_R1 = 0 dBm0 PCM code. Transmit and receive gains programmed for maximum 0 dBm0 test levels (0 dB Gain). All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
G_{RAG}	Receive Gain Variation with Programmed Gain	T_A = 25°C, V_{CC} = 5V, V_{BB} = −5V				
		Programmed Gain from 0 dB to 19 dB				
		(0 dBm0 Levels of 1.964 Vrms to 0.220 Vrms)	**−0.1**		**0.1**	dB
		Programmed Gain from 19.1 dB to 25.4 dB				
		(0 dBm0 Levels of 0.218 Vrms to 0.105 Vrms)	**−0.3**		**0.3**	dB
		NOTE: ±0.1 dB Min/Max is Available as a Selected Part				
G_{RAT}	Receive Gain Variation with Temperature	Measured Relative to G_{RA}.				
		V_{CC} = 5V, V_{BB} = −5V.	−0.1		0.1	dB
		Minimum Gain < G_R < Maximum Gain				
G_{RAF}	Receive Gain Variation with Frequency	Relative to 1015.625 Hz (2)				
		D_R1 = 0 dBm0 Code.				
		Minimum Gain < G_R < Maximum Gain				
		f = 200 Hz	−0.25		0.15	dB
		f = 300 Hz to 3000 Hz	−0.15		0.15	dB
		f = 3400 Hz	−0.7		0.0	dB
		f = 4000 Hz			−14	dB
		G_R = 0 dB, D_R1 = 0 dBm0 Code,				
		G_X = 0 dB (2)				
		f = 296.875 Hz	**−0.15**		**0.15**	dB
		f = 1875.00 Hz	**−0.15**		**0.15**	dB
		f = 2906.25 Hz	**−0.15**		**0.15**	dB
		f = 2984.375 Hz	**−0.15**		**0.15**	dB
		f = 3406.250 Hz	**−0.74**		**0.0**	dB
		f = 3984.375 Hz			**−13.5**	dB
G_{RAL}	Receive Gain Variation with Signal Level	Sinusoidal Test Method.				
		Reference Level = 0 dBm0.				
		D_R1 = −40 dBm0 to +3 dBm0	**−0.2**		**0.2**	dB
		D_R1 = −50 dBm0 to −40 dBm0	**−0.4**		**0.4**	dB
		D_R1 = −55 dBm0 to −50 dBm0	**−1.2**		**1.2**	dB
		DR_1 = 3.1 dBm0 −0.5				
		R_L = 600Ω, G_R = −0.5 dB	−0.2		0.2	dB
		R_L = 300Ω, G_R = 1.2 dB	−0.2		0.2	dB
ENVELOPE DELAY DISTORTION WITH FREQUENCY						
D_{XA}	Tx Delay, Absolute	f = 1600 Hz			315	µs
D_{XR}	Tx Delay, Relative to DXA	f = 500 Hz–600 Hz			220	µs
		f = 600 Hz–800 Hz			145	µs
		f = 800 Hz–1000 Hz			75	µs
		f = 1000 Hz–1600 Hz			40	µs
		f = 1600 Hz–2600 Hz			75	µs
		f = 2600 Hz–2800 Hz			105	µs
		f = 2800 Hz–3000 Hz			155	µs

(2) A multi-tone test technique is used.

Transmission Characteristics (continued)

Unless otherwise noted, limits printed in **BOLD** characters are ensured for V_{CC} = +5V ±5%, V_{BB} = −5V ±5%; T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. f = 1015.625 Hz, VF_XI = 0 dBm0, D_R1 = 0 dBm0 PCM code. Transmit and receive gains programmed for maximum 0 dBm0 test levels (0 dB Gain). All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
D_{RA}	Rx Delay, Absolute	f = 1600 Hz			200	µs
D_{RR}	Rx Delay, Relative to DRA	f = 500 Hz–1000 Hz	−40			µs
		f = 1000 Hz–1600 Hz	−30			µs
		f = 1600 Hz–2600 Hz			90	µs
		f = 2600 Hz–2800 Hz			125	µs
		f = 2800 Hz–3000 Hz			175	µs
NOISE						
N_{XC}	Transmit Noise, C Message Weighted, µ-Law Selected	See(3). 11111111 in Gain Register		12	**15**	dBrnC0
N_{XP}	Transmit Noise, P Message Weighted, A-Law Selected	See(3). 11111111 in Gain Register		−74	**−67**	dBm0p
N_{RC}	Receive Noise, C Message Weighted, µ-Law Selected	PCM Code is Alternating Positive		8	**11**	dBrnC0
N_{RP}	Receive Noise, P Message Weighted, A-Law Selected	PCM Code Equals Positive Zero		−82	**−79**	dBm0p
N_{RS}	Noise, Single Frequency	f = 0 kHz to 100 kHz, Loop Around Measurement, VF_XI = 0 Vrms			−53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit	V_{CC} = 5.0 V_{DC} + 100 mVrms				
		f = 0 kHz–4 kHz (4)	**36**			dBC
		f = 4 kHz–50 kHz	30			dBC
$NPSR_X$	Negative Power Supply Rejection, Transmit	V_{BB} = −5.0 V_{DC} +100 mVrms				
		f = 0 kHz–4 kHz (4)	**36**			dBC
		f = 4 kHz–50 kHz	30			dBC
$PPSR_R$	Positive Power Supply Rejection, Receive	PCM Code Equals Positive Zero				
		V_{CC} = 5.0 V_{DC} + 100 mVrms				
		Measure VF_RO				
		f = 0 Hz–4000 Hz	**36**			dBC
		f = 4 kHz–25 kHz	40			dB
		f = 25 kHz–50 kHz	36			dB
$NPSR_R$	Negative Power Supply Rejection, Receive	PCM Code Equals Positive Zero				
		V_{BB} = −5.0 V_{DC} + 100 mVrms				
		Measure VF_RO				
		f = 0 Hz–4000 Hz	**36**			dBC
		f = 4 kHz–25 kHz	40			dB
		f = 25 kHz–50 kHz	36			dB
SOS	Spurous Out-of-Band Signals Applied at the Channel Output	0 dBm0 300 Hz to 3400 Hz Input PCM Code at D_R1				
		4600 Hz–7600 Hz			**−30**	dB
		7600 Hz–8400 Hz			**−40**	dB
		8400 Hz–50,000 Hz			**−30**	dB
DISTORTION						

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(3) Measured by grounded input at V_{FXI}.

(4) $PPSR_X$, $NPSR_X$, and CT_{R-X} are measured with a −50 dBm0 activation signal applied to VF_XI.

Transmission Characteristics (continued)

Unless otherwise noted, limits printed in **BOLD** characters are ensured for V_{CC} = +5V ±5%, V_{BB} = −5V ±5%; T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. f = 1015.625 Hz, VF_XI = 0 dBm0, D_R1 = 0 dBm0 PCM code. Transmit and receive gains programmed for maximum 0 dBm0 test levels (0 dB Gain). All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STD_X	Signal to Total Distortion	Sinusoidal Test Method				
STD_R	Transmit or Receive Half-Channel, μ-Law Selected	Level = 3.0 dBm0	**33**			dBC
		= 0 dBm0 to −30 dBm0	**36**			dBC
		= −40 dBm0	**30**			dBC
		= −45 dBm0	**25**			dBC
STD_{RL}	Single to Total Distortion Receive with Resistive Load	Sinusoidal Test Method				
		Level = +3.1 dBm0				
		R_L = 600Ω, G_R = −0.5 dB	**33**			dBC
		R_L = 300Ω, G_R = −1.2 dB	**33**			dBC
SFD_X	Single Frequency Distortion, Transmit				**−46**	dB
SFD_R	Single Frequency Distortion, Receive				**−46**	dB
IMD	Intermodulation Distortion	Transmit or Receive Two Frequencies in the Range 300 Hz–3400 Hz			**−41**	dB
CROSSTALK						
$CT_{X\text{-}R}$	Transmit to Receive Crosstalk, 0 dBm0 Transmit Level	f = 300 Hz–3400 Hz D_R = Idle Code		−90	**−75**	dB
$CT_{R\text{-}X}$	Receive to Transmit Crosstalk, 0 dBm0 Receive Level	f = 300 Hz–3400 Hz (4)		−90	**−70**	dB

FUNCTIONAL DESCRIPTION

POWER-ON INITIALIZATION

When power is first applied, power-on reset circuitry initializes the COMBO II and puts it into the power-down state. The gain control registers for the transmit and receive gain sections are programmed for no output, the power amp is disabled and the device is in the non-delayed timing mode. The Latch Direction Register (LDR) is pre-set with all IL pins programmed as inputs, placing the SLIC interface pins in a high impedance state. The CO pin is in TRI-STATE condition. Other initial states in the Control Register are indicated in CONTROL REGISTER INSTRUCTION.

The desired modes for all programmable functions may be initialized via the control port prior to a Power-up command.

POWER-DOWN STATE

Following a period of activity in the powered-up state the power-down state may be re-entered by writing any of the control instructions into the serial control port with the “P” bit set to “1” as indicated in Table 1. It is recommended that the chip be powered down before writing any additional instructions. In the power-down state, all non-essential circuitry is de-activated and the D_X1 output is in the high impedance TRI-STATE condition.

The data stored in the Gain Control registers, the LDR and ILR, and all control bits remain unchanged in the power-down state unless changed by writing new data via the serial control port, which remains active. The outputs of the Interface Latches also remain active, maintaining the ability to monitor and control the SLIC.

TRANSMIT FILTER AND ENCODER

The Transmit section input, VF_XI, is a high impedance input. No external components are necessary to set the gain. Following this is a programmable gain/attenuation amplifier which is controlled by the contents of the Transmit Gain Register (see PROGRAMMABLE FUNCTIONS section). An active pre-filter then precedes the 3rd order high-pass and 5th order low-pass switched capacitor filters. The A/D converter has a compressing characteristic according to the standard CCITT A or μ255 coding laws, which must be selected by a control instruction during initialization (see Table 1 and Table 2). A precision on-chip voltage reference ensures accurate and highly stable transmission levels. Any offset voltage arising in the gain-set amplifier, the filters or the comparator is canceled by an internal auto-zero circuit.

Each encode cycle begins immediately following the assigned Transmit time-slot. The total signal delay referenced to the start of the time-slot is approximately 165 μs (due to the Transmit Filter) plus 125 μs (due to encoding delay), which totals 290 μs. Data is shifted out on D_X1 during the selected time slot on eight rising edges of BCLK.

DECODER AND RECEIVER FILTER

PCM data is shifted into the Decoder's Receive PCM Register via the D_R1 pin during the selected time-slot on the 8 falling edges of BCLK. The Decoder consists of an expanding DAC with either A or μ255 law decoding characteristic, which is selected by the same control instruction used to select the Encode law during initialization. Following the Decoder is a 5th order low-pass switched capacitor filter with integral Sin x/x correction for the 8 kHz sample and hold. A programmable gain amplifier, which must be set by writing to the Receive Gain Register, is included, and finally a Power Amplifier capable of driving a 300Ω load to ±3.5V, a 600Ω load to ±3.8V or a 15 kΩ load to ±4.0V at peak overload.

Table 1. Programmable Register Instructions

Function	Byte 1 (1)(2)(3)								Byte 2 (1)							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Single Byte Power-Up/Down	P	X	X	X	X	X	0	X	None							
Write Control Register	P	0	0	0	0	0	1	X	See Table 2							
Read-Back Control Register	P	0	0	0	0	1	1	X	See Table 2							
Write to Interface Latch Register	P	0	0	0	1	0	1	X	See Table 4							

(1) Bit 7 of bytes 1 and 2 is always the first bit clocked into or out from the CI or CO pin. X = don't care.
(2) “P” is the power-up/down control bit, see POWER-UP/DOWN CONTROL section. (“0” = Power Up, “1” = Power Down)
(3) Other register address codes are invalid and should not be used.

Table 1. Programmable Register Instructions (continued)

Function	Byte 1(1)(2)(3)								Byte 2(1)							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Read Interface Latch Register	P	0	0	0	1	1	1	X	See Table 4							
Write Latch Direction Register	P	0	0	1	0	0	1	X	See Table 3							
Read Latch Direction Register	P	0	0	1	0	1	1	X	See Table 3							
Write Receive Gain Register	P	0	1	0	0	0	1	X	See Table 8							
Read Receive Gain Register	P	0	1	0	0	1	1	X	See Table 8							
Write Transmit Gain Register	P	0	1	0	1	0	1	X	See Table 7							
Read Transmit Gain Register	P	0	1	0	1	1	1	X	See Table 7							
Write Receive Time-Slot/Port	P	1	0	0	1	0	1	X	See Table 6							
Read-Back Receive Time-Slot/Port	P	1	0	0	1	1	1	X	See Table 6							
Write Transmit Time-Slot/Port	P	1	0	1	0	0	1	X	See Table 6							
Read-Back Transmit Time-Slot/Port	P	1	0	1	0	1	1	X	See Table 6							

A decode cycle begins immediately after the assigned receive timeslot, and 10 μs later the Decoder DAC output is updated. The total signal delay is 10 μs plus 120 μs (filter delay) plus 62.5 μs (½ frame) which gives approximately 190 μs.

PCM INTERFACE

The FS_X and FS_R frame sync inputs determine the beginning of the 8-bit transmit and receive time-slots respectively. They may have any duration from a single cycle of BCLK HIGH to one MCLK period LOW. Two different relationships may be established between the frame sync inputs and the actual time-slots on the PCM busses by setting bit 3 in the Control Register (see Table 2). Non-delayed data mode is similar to long-frame timing on the TP3050/60 series of devices (COMBO); time-slots begin nominally coincident with the rising edge of the appropriate FS input. The alternative is to use Delayed Data mode, which is similar to shortframe sync timing on COMBO, in which each FS input must be high at least a half-cycle of BCLK earlier than the timeslot. The Time-Slot Assignment circuit on the device can only be used with Delayed Data timing.

When using Time-Slot Assignment, the beginning of the first time-slot in a frame is identified by the appropriate FS input. The actual transmit and receive time-slots are then determined by the internal Time-Slot Assignment counters.

Transmit and Receive frames and time-slots may be skewed from each other by any number of BCLK cycles. During each assigned Transmit time-slot, the D_X1 output shifts data out from the PCM register on the rising edges of BCLK. $\overline{TS_X}1$ also pulls low for the first 7½ bit times of the time-slot to control the TRI-STATE Enable of a backplane line-driver. Serial PCM data is shifted into the D_R1 input during each assigned Receive time-slot on the falling edges of BCLK.

SERIAL CONTROL PORT

Control information and data are written into or read-back from COMBO II via the serial control port consisting of the control clock CCLK, the serial data input, CI, and output, CO, and the Chip Select input, $\overline{CS}$. All control instructions require 2 bytes, as listed Table 1, with the exception of a single byte power-up/down command. The Byte 1 bits are used as follows: bit 7 specifies power up or power down; bits 6, 5, 4 and 3 specify the register address, bit 2 specifies whether the instruction is read or write; bit 1 specifies a one or two byte instruction; and bit 0 is not used.

To shift control data into COMBO II, CCLK must be pulsed high 8 times while $\overline{CS}$ is low. Data on the CI input is shifted into the serial input register on the falling edge of each CCLK pulse. After all data is shifted in, the contents of the input shift register are decoded, and may indicate that a 2nd byte of control data will follow. This second byte may either be defined by a second byte-wide $\overline{CS}$ pulse or may follow the first contiguously, i.e, it is not mandatory for $\overline{CS}$ to return high between the first and second control bytes. At the end of CCLK8 in the 2nd control byte the data is loaded into the appropriate programmable register. $\overline{CS}$ may remain low continuously when programming successive registers, if desired. However, $\overline{CS}$ must be set high when no data transfers are in progress.

To readback Interface Latch data or status information from COMBO II, the first byte of the appropriate instruction is strobed while $\overline{\text{CS}}$ is low, as defined in Table 1. $\overline{\text{CS}}$ must be kept low, or be taken low again for a further 8 CCLK cycles, during which the data is shifted onto the CO pin on the rising edges of CCLK. When $\overline{\text{CS}}$ is high the CO pin is in the high-impedance TRI-STATE, enabling the CI and CO pins of many devices to be multiplexed together.

If $\overline{\text{CS}}$ returns high during either byte 1 or byte 2 before all eight CCLK pulses of that byte occur, both the bit count and byte count are reset and register contents are not affected. This prevents loss of synchronization in the control interface as well as corruption of register data due to processor interrupt or other problem. When $\overline{\text{CS}}$ returns low again, the device will be ready to accept bit 1 of byte 1 of a new instruction.

PROGRAMMABLE FUNCTIONS

POWER-UP/DOWN CONTROL

Following power-on initialization, power-up and power-down control may be accomplished by writing any of the control instructions listed in Table 1 into COMBO II with the “P” bit set to “0” for power-up or “1” for power-down. Normally it is recommended that all programmable functions be initially programmed while the device is powered down. Power state control can then be included with the last programming instruction or the separate single-byte instruction. Any of the programmable registers may also be modified while the device is powered-up or down by setting the “P” bit as indicated. When the power-up or down control is entered as a single byte instruction, bit one (1) must be reset to a 0.

When a power-up command is given, all de-activated circuits are activated, but the TRI-STATE PCM output(s), D_X1 will remain in the high impedance state until the second FS_X pulse after power-up.

CONTROL REGISTER INSTRUCTION

The first byte of a READ or WRITE instruction to the Control Register is as shown in Table 1. The second byte has the following bit functions:

Table 2. Control Register Byte 2 Functions

Bit Number and Name								
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Function**
F_1	**F_0**	**MA**	**IA**	**DN**	**DL**	**AL**	**PP**	
0	0							MCLK = 512 kHz
0	1							MCLK = 1.536 MHz or 1.544 MHz
1	0							MCLK = 2.048 MHz (1)
1	1							MCLK = 4.096 MHz
		0	X					Select µ255 Law (1)
		1	0					A-Law, Including Even Bit Inversion
		1	1					A-Law, No Even Bit Inversion
				0				Delay Data Timing
				1				Non-Delayed Data Timing (1)
					0	0		Normal Operation (1)
					1	X		Digital Loopback
					0	1		Analog Loopback
							0	Power Amp Enabled in PDN
							1	Power Amp Disabled in PDN (1)

(1) state at power-on initialization.

Master Clock Frequency Selection

A Master clock must be provided to COMBO II for operation of the filter and coding/decoding functions. The MCLK frequency must be either 512 kHz, 1.536 MHz, 1.544 MHz, 2.048 MHz, or 4.096 MHz and must be synchronous with BCLK. Bits F_1 and F_0 (see Table 2) must be set during initialization to select the correct internal divider.

Coding Law Selection

Bits “MA” and “IA” in Table 2 permit the selection of µ255 coding or A-law coding, with or without even bit inversion.

Analog Loopback

Analog Loopback mode is entered by setting the “AL” and “DL” bits in the Control Register as shown in Table 2. In the analog loopback mode, the Transmit input VF_XI is isolated from the input pin and internally connected to the VF_RO output, forming a loop from the Receive PCM Register back to the Transmit PCM Register. The VF_RO pin remains active, and the programmed settings of the Transmit and Receive gains remain unchanged, thus care must be taken to ensure that overload levels are not exceeded anywhere in the loop.

Digital Loopback

Digital Loopback mode is entered by setting the “AL” and “DL” bits in the Control Register as shown in Table 2. This mode provides another stage of path verification by enabling data written into the Receive PCM Register to be read back from that register in any Transmit time-slot at D_X1. PCM decoding continues and analog output appears at VF_R0. The output can be disabled by programming ‘No Output' in the Receive Gain Register (see Table 8).

INTERFACE LATCH DIRECTIONS

Immediately following power-on, all Interface Latches assume they are inputs, and therefore all IL pins are in a high impedance state. Each IL pin may be individually programmed as a logic input or output by writing the appropriate instruction to the LDR, see Table 1 and Table 3. For minimum power dissipation, unconnected latch pins should be programmed as outputs. For the TP3076, bits 2 and 3 should always be programmed as “1” (outputs).

Bits L_3–L_0 must be set by writing the specific instruction to the LDR with the L bits in the second byte set as follows:

Table 3. Byte 2 Functions of Latch Direction Register(1)

Byte 2 Bit Number							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
L_0	**L_1**	**L_2**	**L_3**	**1**	**1**	**X**	**X**

L_n Bit	IL Direction
0	Input
1	Output

(1) X = Don't Care

INTERFACE LATCH STATES

Interface Latches configured as outputs assume the state determined by the appropriate data bit in the 2-byte instruction written to the Interface Latch Register (ILR) as shown in Table 1 and Table 4. Latches configured as inputs will sense the state applied by an external source, such as the Off-Hook detect output of a SLIC. All bits of the ILR, i.e. sensed inputs and the programmed state of outputs, can be read back in the 2nd byte of a READ from the ILR.

It is recommended that during initialization, the state of IL pins to be configured as outputs should be programmed first followed immediately by the Latch Direction Register.

Table 4. Interface Latch Data Bit Order

Bit Number							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
D_0	D_1	D_2	D_3	D_4	D_5	X	X

Table 5. Coding Law Conventions(1)

	μ255 Law MSB LSB	True A-Law with Even Bit Inversion MSB LSB	A-Law without Even Bit Inversion MSB LSB
V_{IN} = +Full Scale	1 0 0 0 0 0 0 0	1 0 1 0 1 0 1 0	1 1 1 1 1 1 1 1 1
V_{IN} = 0V	1 1 1 1 1 1 1 1	1 1 0 1 0 1 0 1	1 0 0 0 0 0 0 0 0
	1 1 1 1 1 1 1 1	0 1 0 1 0 1 0 1	0 0 0 0 0 0 0 0 0
V_{IN} = −Full Scale	0 0 0 0 0 0 0 0	0 0 1 0 1 0 1 0	0 1 1 1 1 1 1 1 1

(1) The MSB is always the first PCM bit shifted in or out of COMBO II.

Table 6. Time-Slot and Port Assignment Instruction

Bit Number and Name								Function
7 EN	6 PS(1)	5 T_5(2)	4 T_4	3 T_3	2 T_2	1 T_1	0 T_0	
0	1	X	X	X	X	X	X	Disable D_X1 Output (Transmit Instruction) Disable D_R1 Input (Receive Instruction)
1	1	Assign One Binary Coded Time-Slot from 0–63 Assign One Binary Coded Time-Slot from 0–63						Enable D_X1 Output (Transmit Instruction) Enable D_R1 Input (Transmit Instruction)

(1) The “PS” bit MUST be set to “1” for both transmit and receive for the TP3076.

(2) T5 is the MSB of the time-slot assignment bit field. Time-slot bits should be set to “000000” for both transmit and receive when operating in non-delayed data timing mode.

TIME-SLOT ASSIGNMENT

COMBO II can operate in either fixed time-slot or time-slot assignment mode for selecting the Transmit and Receive PCM time-slots. Following power-on, the device is automatically in Non-Delayed Timing mode, in which the time-slot always begins with the leading (rising) edge of frame sync inputs FS_X and FS_R. Time-Slot Assignment may only be used with Delay Data timing; see Figure 3. FS_X and FS_R may have any phase relationship with each other in BCLK period increments.

Alternatively, the internal time-slot assignment counters and comparators can be used to access any time-slot in a frame, using the frame sync inputs as marker pulses for the beginning of transmit and receive time-slot 0. In this mode, a frame may consist of up to 64 time-slots of 8 bits each. A time-slot is assigned by a 2-byte instruction as shown in Table 1 and Table 6. The last 6 bits of the second byte indicate the selected time-slot from 0–63 using straight binary notation. When writing a time-slot and port assignment register, if the PCM interface is currently active, it is immediately deactivated to prevent possible bus clashes. A new assignment becomes active on the second frame following the end of the Chip-Select for the second control byte. Rewriting of the register contents should not be performed during the talking period of a connection to prevent waveform distortion caused by loss of a sample which will occur with each register write. The “EN” bit allows the PCM input, D_R1, or output, D_X1, as appropriate, to be enabled or disabled.

Time-Slot Assignment mode requires that the FS_X and FS_R pulses conform to the delayed data timing format shown in Figure 3.

PORT SELECTION

On the TP3076, the “PS” bit MUST always be set to 1.

Table 6 shows the format for the second byte of both transmit and receive time-slot and port assignment instructions.

TRANSMIT GAIN INSTRUCTION BYTE 2

The transmit gain can be programmed in 0.1 dB steps by writing to the Transmit Gain Register as defined in Table 1 and Table 7. This corresponds to a range of 0 dBm0 levels at VF_XI between 1.375 Vrms and 0.074 Vrms (equivalent to +5.0 dBm to −20.4 dBm in 600Ω).

To calculate the binary code for byte 2 of this instruction for any desired input 0 dBm0 level in Vrms, take the nearest integer to the decimal number given by:

$$200 \times \log_{10} (V/0.07299) \tag{1}$$

and convert to the binary equivalent. Some examples are given in Table 7. A complete tabulation is given in Appendix I of AN-614.

It should be noted that the Transmit (idle channel) Noise and Transmit Signal to Total Distortion are both specified with transmit gain set to 0 dB (gain register set to all ones). At high transmit gains there will be some degradation in noise performance for these parameters. See Application Note AN-614 for more information on this subject.

Table 7. Byte 2 of Transmit Gain Instruction

Bit Number **7 6 5 4 3 2 1 0**	**0 dBm0 Test Level (Vrms)** **at $VF_X I$**
0 0 0 0 0 0 0 0	No Output[1]
0 0 0 0 0 0 0 1	0.074
0 0 0 0 0 0 1 0	0.075
—	—
1 1 1 1 1 1 1 0	1.359
1 1 1 1 1 1 1 1	1.375

(1) Analog signal path is cut off, but D_X remains active and will output codes representing idle noise.

RECEIVE GAIN INSTRUCTION BYTE 2

The receive gain can be programmed in 0.1 dB steps by writing to the Receive Gain Register as defined in Table 1 and Table 8. Note the following restrictions on output drive capability:

1. 0 dBm0 levels ≤ 1.96 Vrms at $VF_R O$ may be driven into a load of ≥ 15 kΩ to GND; Receive Gain set to 0 dB (gain register set to all ones).
2. 0 dBm0 levels ≤ 1.85 Vrms at $VF_R O$ may be driven into a load of ≥ 600Ω to GND; Receive Gain set to 0.5 dB.
3. 0 dBm0 levels ≤ 1.71 Vrms at $VF_R O$ may be driven into a load of ≥ 300 Ω to GND. Receive Gain set to −1.2 dB.

To calculate the binary code for byte 2 of this instruction for any desired output 0 dBm0 level in Vrms, take the nearest integer to the decimal number given by:

$$200 \times \log_{10} (V/0.1043) \tag{2}$$

and convert to the binary equivalent. Some examples are given in Table 8. A complete tabulation is given in Appendix I or AN-614.

Table 8. Byte 2 of Receive Gain Instruction

Bit Number **7 6 5 4 3 2 1 0**	**0 dBm0 Test Level (Vrms)** **at $VF_R O$**
0 0 0 0 0 0 0 0	No Output (Low Z to GND)
0 0 0 0 0 0 0 1	0.105
0 0 0 0 0 0 1 0	0.107
—	—
1 1 1 1 1 1 1 0	1.941
1 1 1 1 1 1 1 1	1.964

APPLICATIONS INFORMATION

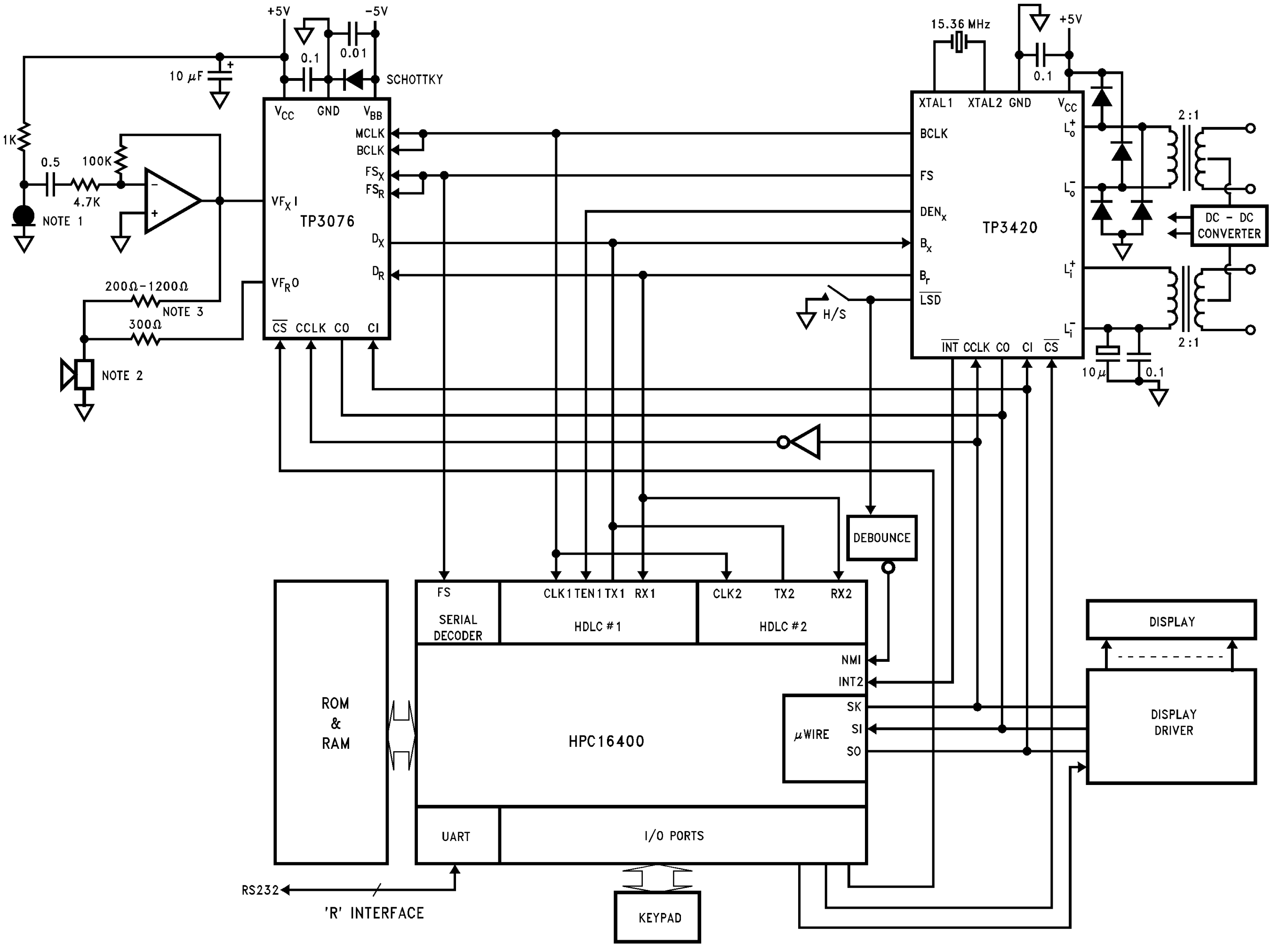
Figure 5 shows a typical ISDN phone application of the TP3076 together with a TP3420 ISDN Transceiver "S" Interface Device and HPC16400 High-Performance Microcontroller with HDLC Controller. The TP3076 device is programmed over its serial control interface via the HPC16400 MICROWIRE/PLUS™ serial I/O port.

POWER SUPPLIES

While the pins of the TP3076 COMBO II device are well protected against electrical misuse, it is recommended that the standard CMOS practice of applying GND to the device before any other connections are made should always be followed. In applications where the printed circuit card may be plugged into a hot socket with power and clocks already present, an extra long ground pin on the connector should be used and a Schottky diode connected between V_{BB} and GND.

To minimize noise sources all ground connections to each device should meet at a common point as close as possible to the GND pin in order to prevent the interaction of ground return currents flowing through a common bus impedance. Power supply decoupling capacitors of 0.1 μF should be connected from this common point to V_{CC} and V_{BB} as close to the device pins as possible.

Further guidelines on PCB layout techniques are provided in Application Note AN-614, “ COMBO II™ Programmable PCM CODEC/Filter Family Application Guide”.



(1) Primo type EM80–PMI2 or similar.

(2) Primo type DH31 or similar.

(3) Sidetone ≃ −9.2 dB for 200Ω,Sidetone ≃ −21.5 dB for 1200Ω.

Figure 5. Typical Application in an ISDN Phone

REVISION HISTORY

Changes from Revision C (April 2013) to Revision D	**Page**
• Changed layout of National Data Sheet to TI format	19

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