TEXAS INSTRUMENTS

TLV5619-5639 12-Bit Parallel DAC Evaluation Module

User's Guide

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Advanced Analog Applications

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Preface

Read This First

About This Manual

This users guide describes the characteristics, operation, and use of the TLV5619-5639 12-bit parallel digital-to-analog converter evaluation module (EVM). A complete circuit description as well as schematic diagram and bill of materials are included.

How to Use This Manual

This document contains the following chapters:

- ❏ Chapter 1 – Overview
- ❏ Chapter 2 – Physical Description
- ❏ Chapter 3 – EVM Operation
- ❏ Appendix A – Schematics

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This book may contain cautions and warnings.

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Data Sheets:	Literature Number:
❑ TLV5619	SLAS172
❑ TLV5639	SLAS189
❑ TPS6734	SLVS127
❑ SN74AHC1G32	SCLS317
❑ SN74AHC1G04	SCLS318
❑ REF1004	SBVS002
❑ SN74AHC32	SCLS247
❑ SN74AHC139	SCLS259
❑ SN74HC163	SCLS298
❑ SN74AHC245	SCLS230
❑ TLV2772	SLOS209

Application Report:

❑ TMS320 Cross-Platform Daughtercard Specification, literature number SPRA711

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Contents

Figures

Tables

Chapter 1

EVM OVERVIEW

This chapter gives an overview of the TLV5619-5639 parallel DAC EVM.

The EVM is shipped with the following devices installed:

- TLV5619DW
- TLV5639DW

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1.1 Features

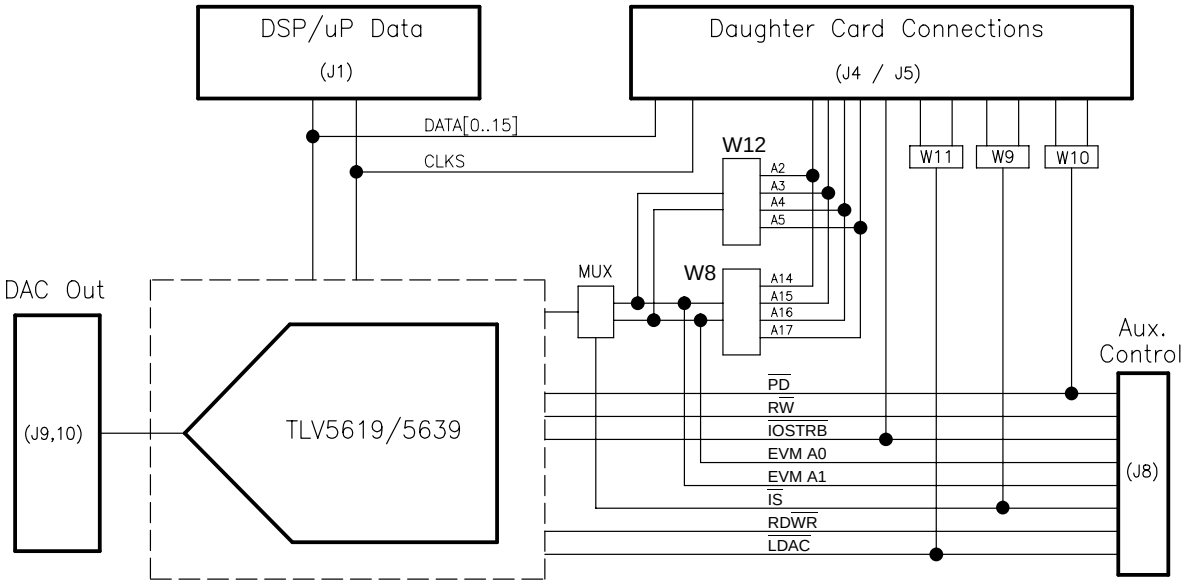
This EVM features two independent digital to analog converters on one convenient evaluation platform.

Both the TLV5619 and TLV5639 are 12-bit parallel, voltage output, digital-to-analog converters. The TLV5619 requires an external reference and features a 1 μS settling time. The TLV5639 features programmable settling time (1 or 3 μS) and programmable internal reference (1.024 V or 2.048 V). Both devices support a powerdown mode through a hardware pin (TLV5619), or through software register (TLV5639).

The EVM contains a precision reference for the DACs, as well as terminals for connection of an independent external reference. Each DAC is address selectable through hardware or user-supplied software. The EVM has a built-in functional test mode that supplies a staircase ramp to the DACs.

1.2 EVM Basic Functions

Figure 1–1. EVM Block Diagram



1.2.1 Stand-Alone Testing

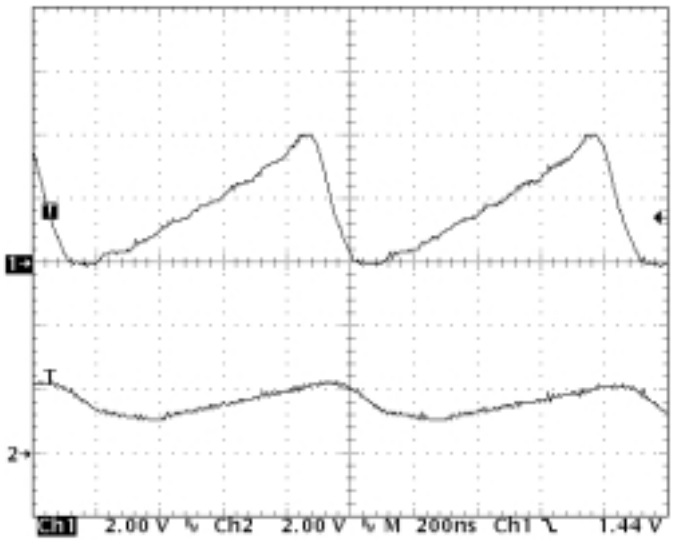
Opening W2 activates an onboard 5 MHz clock. This puts the EVM in self-test mode. The onboard oscillator provides the $\overline{WE}$ signal to the data converters and a clock to the test circuitry.

Hardware jumpers W3 and W4 allow the EVM user to select which DAC to evaluate. Opening these jumpers brings the chip select signal to each data converter low. Either one or both of the DACs can be operated at the same time.

The onboard clock is fed through a 4-bit binary counter. The counter output is used to generate a staircase ramp, via buffers U5 and U8, to verify that the

DACs are operational. The output from the DACs should look similar to Figure 1-2. Channel 1, available on J9, is the test mode output from the TLV5619. Channel 2, available on J10, is the test output from the TLV5639.

Figure 1–2. DAC Output



1.2.2 Testing With a Processor

When operated outside of the test mode (W2 closed), the DACs expect to receive their control signals and parallel data input from a host processor. The EVM is designed to work with TI's DSK series of digital signal processor evaluation boards that support the common connector interface described in tables 15 and 16 of the *TMS320 Cross–Platform Daughtercard Specification* (No. SPRA711). Connectors J4 and J5, which are located on the underside of the EVM, provide the daughtercard interface.

Connectors J3 and J8 allow the EVM user to define a custom control interface. The shorting bar on J3 can be removed, allowing the EVM user to interface to older DSKs, microcontrollers or pattern generators. Parallel data input to the DACs is supplied via J1. Pins 1 through 31 (odd) provide data bits D0 through D15. The DACs are MSB aligned to the host, which means the lowest data bits (D0 through D3) are unused on this EVM.

1.2.2.1 Clock Source

The SMA connector at location J2 allows the user to attach an external clock source to the EVM. This clock can be used to synchronize the host processor or data generator via J1 pin 33, or J8 pin 19. When the EVM is used as a daughtercard in a DSP system, the clock source can be supplied from the DSP via J5 pin 78 by closing W13.

1.2.2.2 EVM Address Bus

Address decoder U7 determines access to each data converter. A two-bit address bus on the EVM can be directly accessed via J8. The address bus can

also be accessed through daughtercard connector J4 and two jumper blocks, W8 and W12. The jumper blocks allow the EVM user to select any two of the upper four or lower four address bits from the TMS320C6X series DSPs.

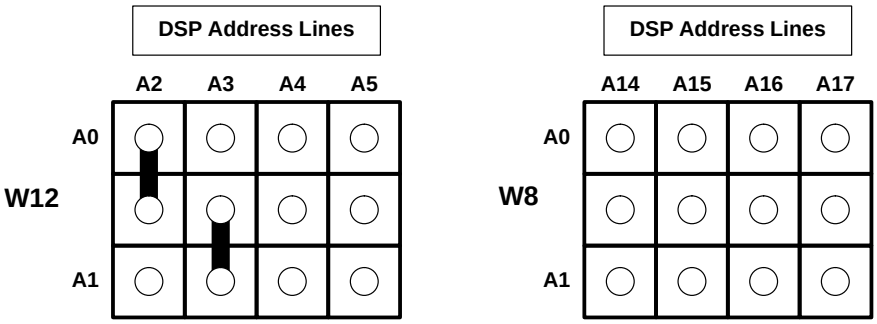
Note:

Address lines may vary depending on the DSP being used. Check your DSP EVM documentation for the specific address line mapping.

Jumper block W8 and W12 are configured as follows:

Note:

Rows A0 and A1 are common to the EVM address bus. The center row is connected to the DSP address bus via J4 pins 7 through 10, and 23 through 26. The following diagram shows the C6000 address lines A2 and A3 connected to EVM A0 and A1 respectively.



1.2.2.3 Address Function

Selection of the DACs at U2 or U3 places the respective chip select in a low state.

Table 1–1. Address Function

Address	Function
00	No selection (default)
01	Selects U2 to receive chip select
10	Selects U3 to receive chip select
11	Selects U3 to receive chip select and activates the configuration register (enable DAC configuration register write)

1.3 Power Requirements

1.3.1 Supply Voltage

The DAC EVM is designed to operate from 3.3 V to 5.5 VDC. The EVM requires 170 mA at 3.3V, and 150 mA at 5.5 V. Power to the EVM can be applied via J6 from an external supply, or can be directed through the common connector interface via J4. Jumper W1 allows the EVM user to select either the 3.3 or 5 V bus from the DSP.

Supply Voltage

When using an external power supply via J6, remove jumper W1 to avoid potential damage to the DSP circuitry.

1.3.2 Reference Voltage

W5 controls the reference source to the DACs. Placing a shunt jumper on pins 1–2 selects the onboard reference circuit. Placing a shunt jumper on pins 2–3, allows an external reference source to be applied via TP6 and TP7. Variable resistor R28 can be used to adjust the reference voltages to U2 and U3. Before using either of the external reference voltage sources, the TLV5639 should be configured through software for external reference (default condition). Refer to section 3.1.2 for the TLV5639 configuration.

When using the internal reference of the TLV5639, place a shunt jumper on W5, pins 2–3. This allows the EVM user to monitor the internal reference at TP6. The internal reference of the TLV5639 will also be applied to the TLV5619 when operating in this mode.

Chapter 2

Physical Description

This chapter describes the PCB layers and provides a bill of materials for the EVM.

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2.1 PCB Layout

The EVM is constructed on a four-layer, 134,6-mm (5.30 inch) x 86-mm (3.39 inch). 1,57-mm (0.062 inch) thick printed circuit board using FR-4 material. Figures 2–1 through 2–5 show the assembly silkscreen and individual layers.

Figure 2–1. Assembly Silkscreen

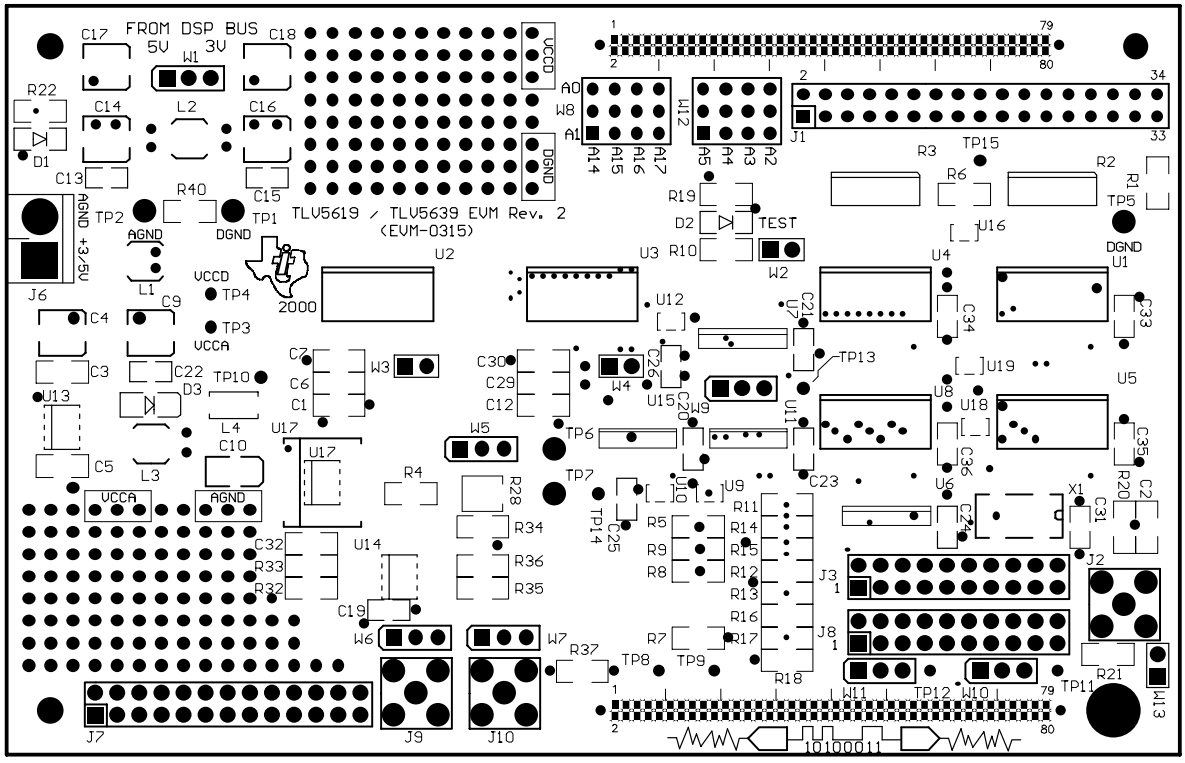


Figure 2–2. Top Layer

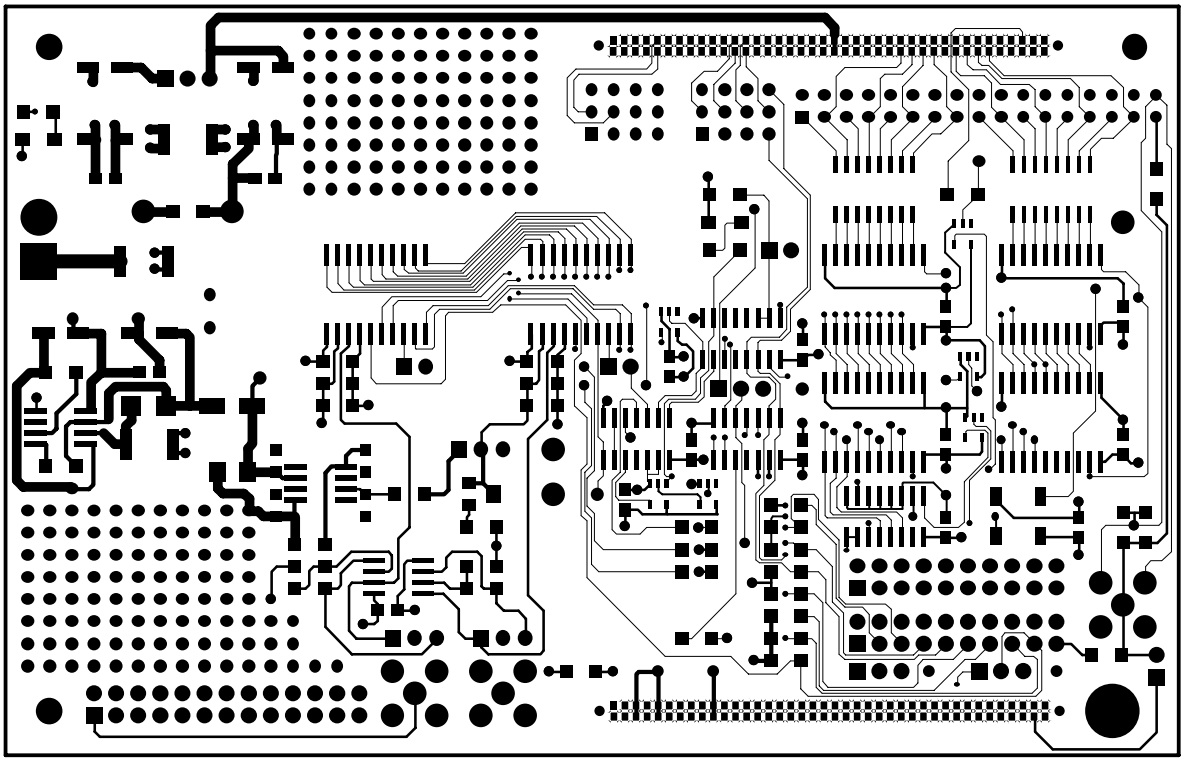


Figure 2–3. Layer 2

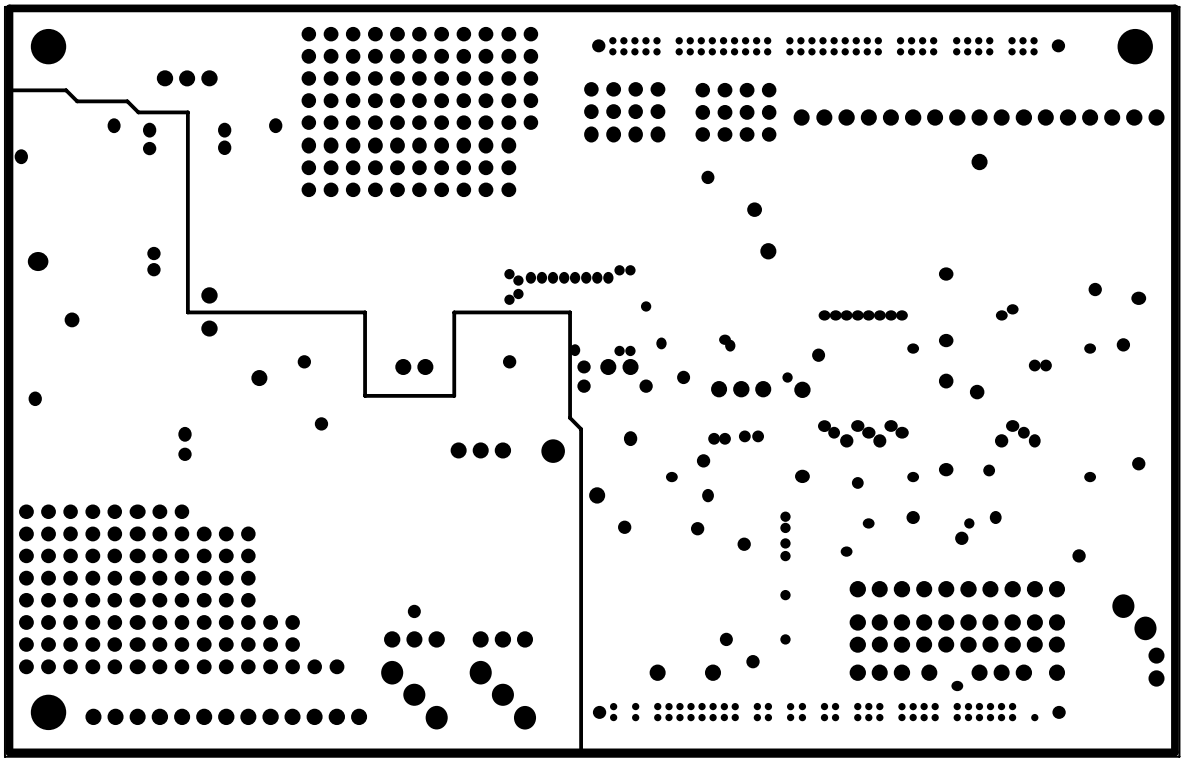


Figure 2–4. Layer 3

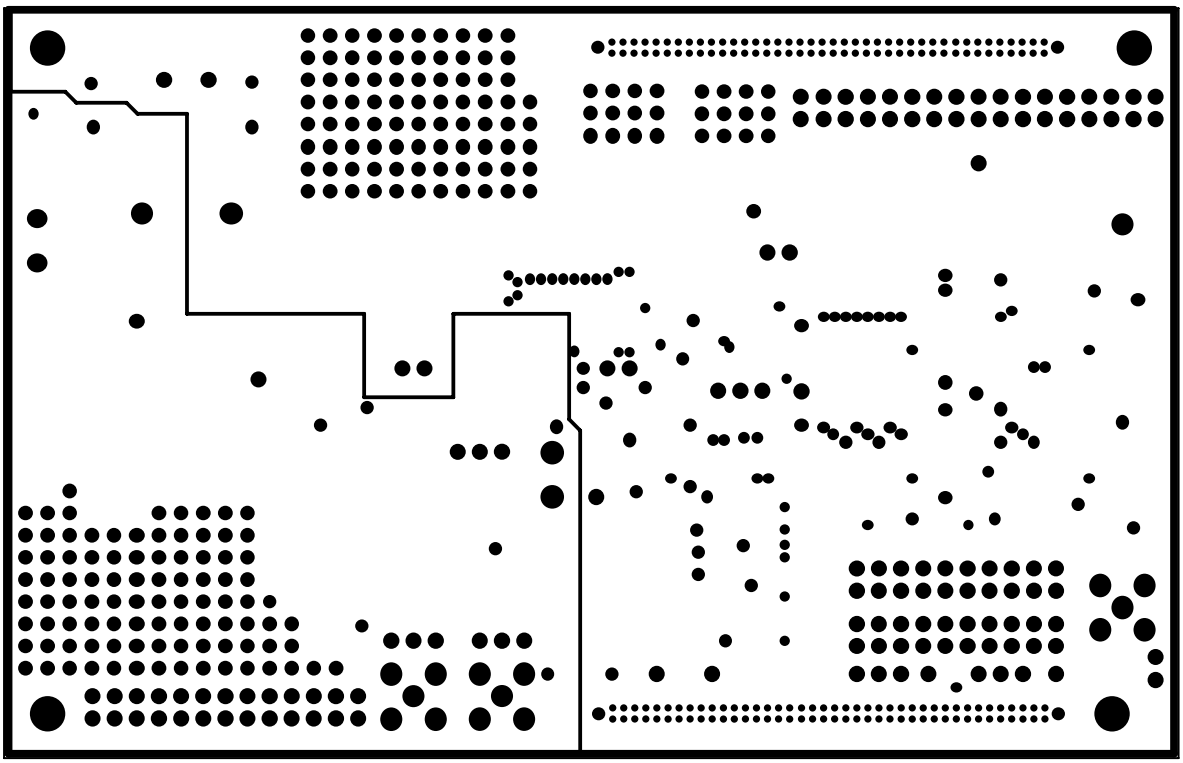
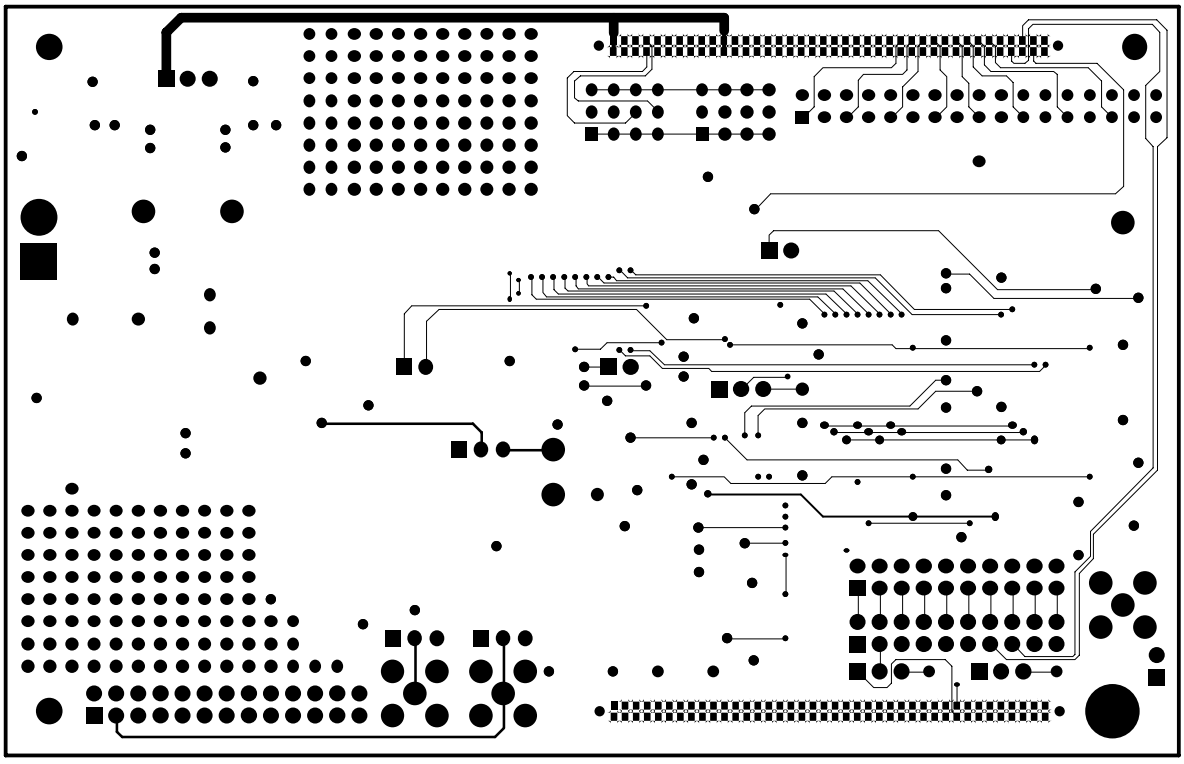


Figure 2–5. Bottom Layer



2.2 Parts List

Table 2–1. EVM Parts List

Qty.	Reference Designator	Value	Supplier	Part No.
3	C1 C3 C12	0.01 µF	Digi-Key	1206PHCT–ND
4	C4 C9 C14 C16	33 µF	Panasonic	ECEV1AA330SR
2	C5 C32	1 nF	Digi-Key	PCC102CCT–ND
4	C6 C7 C29 C30	0.1 µF	Digi-Key	PCC104BCT–ND
1	C10	10 µF, 10 V, Tant.	Any	
15	C13 C15 C19 C20 C21 C22 C23 C24 C25 C26 C31 C33 C34 C35 C36	0.1 µF	Digi-Key	PCC103BNCT–ND
2	C17 C18	10 µF	Panasonic	ECEV1CA100SR
1	D1	Green	Digi-Key	L62205CT–ND
1	D2	Amber	Digi-Key	L62007CT–ND
1	D3	1N5817	Digi-Key	1N5817MCT–ND
1	J1	34PIN_IDC	Samtec	TWS–117–07–L–D
3	J2 J9 J10	SMA_JACK	Lighthorse Technologies	LTI–SASF54GT
2	J3 J8	20PIN_IDC	Samtec	TWS–110–07–L–D
2	J4 J5	TFM–140	Samtec	TFM–140–31–S–D–A
1	J6	KRMZ2	Lumberg	KRMZ2
1	J7	26PIN_IDC	Samtec	TWS–113–07–L–D
2	L1 L2	4.7 µH	Coil Craft	DO1608C–472
1	L3	16 µH	Coil Craft	DO1608C–163
1	L4	Ferrite bead	FAIR–RITE	2744044447
5	R1 R4 R5 R6 R7	33 Ω	Digi-Key	P33ECT–ND
2	R2 R3	33 Ω	Bourns	2NBS16TJ1331
11	R8 R9 R11 R12 R13 R14 R15 R16 R17 R18 R19	10 kΩ	Digi-Key	P10.0KFCT–ND
2	R10 R22	1 kΩ	Digi-Key	P1.0KECT–ND
1	R20	49.9 Ω		
1	R28 Potentiometer	10 kΩ	Digi-Key	3214W–103ETR–ND
1	R34	332 Ω		
4	R32 R35 R37 R40	0 Ω	Digi-Key	P0.0ECT–ND
5	TP1 TP2 TP5 TP6 TP7	Turrent type test points	Cambion	180–7337–02–05
10	TP3 TP4 TP8 TP9 TP10 TP11 TP12 TP13 TP14 TP15	Test points	Digi-Key	5000K–ND
4	U1 U4 U5 U8	SN74AHC245	Texas Instruments	SN74AHC245DW
1	U2	TLV5619DW	Texas Instruments	TLV5619CDW / IDW
1	U3	TLV5639DW	Texas Instruments	TLV5639CDW / IDW
1	U6	SN74AHC163	Texas Instruments	SN74HC163D
1	U7	SN74HC139	Texas Instruments	SN74AHC139D
5	U9 U12 U16 U18 U19	SN74HC1G04	Texas Instruments	SN74AHC1G04DBV
1	U10	SN74HC1G32	Texas Instruments	SN74AHC1G32DBV
1	U11	SN74AHC32	Texas Instruments	SN74AHC32D
1	U13	TPS6734ID	Texas Instruments	TPS6734ID
1	U14	TLV2772	Texas Instruments	TLV2772AID / CD
1	U15	SN74AHC08	Texas Instruments	SN74AHC08D

Table 2–1. EVM Parts List (Continued)

Qty.	Reference Designator	Value	Supplier	Part No.
1	U17	REF1004	TI	REF1004
4	W2 W3 W4 W13	Shunt jumper	Samtec	TSW–102–07–LS
7	W1 W5 W6 W7 W9 W10 W11	2 Position jumper	Samtec	TSW–103–07–LS
2	W8 W12	3 Row, 2 position jumper	Samtec	TSW–104–07–LT
1	X1	5 MHz	Norvel	SG–8002JC5.0M–PHBS

Chapter 3

EVM Operation

This chapter describes the operation of the TLV5619-5639 EVM.

The EVM is factory tested and, with a few simple connections, is configured for immediate operation.

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3.1 Power Supply

Connect a positive dc source of 3–5 V to the EVM at connector J6-1 referenced to J6-2. D1 (LED) should illuminate, indicating that power is applied to the board. D2 should also illuminate if the EVM is in test mode (W2 jumper is not installed).

3.1.1 Test Mode—Factory Defaults

Jumpers W3 and W4 are open, placing the chip select pin on U2 and U3 in a low state. W2 is open, enabling the on-board 5 MHz oscillator. Trim potentiometer R28 is set to provide the DACs with 2.048V as a reference voltage. The reference voltage is supplied via U17. W5, W6 and W7 pins 1–2 are shorted.

At power up, U3 defaults to slow settling time while U2 defaults to fast settling time. The voltage output waveform will look like the one shown in Figure 1–2.

3.1.2 Configuring the TLV5639

TLV5639 register configuration:

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	REF1	REF0	X	PWR	SPD

X: Don't Care

SPD: Speed Control Bit 1 = fast mode (1 μS) 0 = slow mode (3 μS) (default)

PWR: Power Control BIt 1 = power down 0 = normal operation (default)

Table 3–1. Reference Selection

D4 – REF1	D3 – REF0	Function
0	0	External reference
0	1	Internal reference at 1.024 V
1	0	Internal reference at 2.048 V
1	1	External reference

3.2 Processor Controlled Testing

The operation of the EVM through a host processor such as a DSP or microcontroller is described in the following subsections. Daughtercard connectors J4 and J5 are designed for direct plug-in to a DSP development board that complies with the *TMS320 Cross–Platform Daughtercard Specification*. Connectors J1, J3 and J8 however, can be used to develop a custom interface to suit most any situation. Each subsection gives the EVM user the necessary information required to successfully operate the data converters.

3.2.1 Address Selection

When testing the EVM with a host processor, several options are available. Closing jumpers W3 and W4 allow the user to access the data converters via address decoder U7. Address selecting U2 or U3 causes a logic low to be applied to the chip select pin of the chosen device.

Table 3–2. EVM Address Bus

A0†	A1†	Reference	Selection Results	Device
0	0	N/A	None	None
0	1	U2	$\overline{CS}$ low	TLV5619
1	0	U3	$\overline{CS}$ low	TLV5639
1	1	U3	$\overline{CS}$ low, REG high	TLV5639 (write cycle)

† Additional information on DSP address mapping can be found in Chapter 1 of this manual.

The output enable pin for the address decoder can be controlled through the DSP interface via W9. When W9 is in position 1–2, a low level on the DSP's DC_$\overline{CSa}$ line enables the address decoder. Position 2–3 connects this line to TP13. TP13 can be tied to any available GPIO in the event the DSP chip select *address* signal is unavailable. The output enable pin can also be tied low by inserting a shorting jumper across pins 7–8 of J8.

3.2.2 Write Enable

The write enable pin of the devices included with this EVM can be controlled in several ways. When using this EVM as a daughtercard with the TMS320C5000/6000 platform, the DC_$\overline{WE}$ signal on J4 pin 74 is used in combination with the DC_$\overline{OE}$ signal on J4 pin 75. These signals are also available on J8 pins 15 and 13, respectively.

Microcontroller users can access the $\overline{WE}$ pin directly through J8 via pin 5.

3.2.3 Parallel Input Data

When using this EVM with a host processor, parallel data can be applied to the DACs via J1 or the 80 pin connector at location J4. It is important to remember that the most significant bit of the DAC is aligned with the 16th bit of the DSP to maintain compatibility across the various EVM platforms.

3.2.4 Load DAC

The *load DAC* ($\overline{LDAC}$) pin is designed to simultaneously update all of the DAC outputs with the current conversion data. This is an asynchronous signal that can be held low permanently if simultaneous updates are not required. This pin is held at a low state by default on the EVM via pulldown resistor R27. The signal can be controlled through J8-3. DSP users can select to control $\overline{LDAC}$ from DC_CNTL0 at J5-64 or TP12 through jumper W11. TP12 can be wired to any available GPIO if the DSP platform does not provide the DC_CNTL0 signal.

3.2.5 Power Down

The TLV5619 device at U2 has a power-down pin that can be accessed from J8-17. A low level on this pin will send the device into power down mode. DSP users can select either DC_CNTRL1 at J5-63 or TP11 via W10 as the source of this control. TP11 can be tied to any available GPIO if the DSP platform does not provide the DC_CNTL1 signal.

3.3 Jumper Settings

The Table 3–3 shows the function of each jumper on the EVM.

Table 3–3. Jumper Settings

Reference	Setting	Function
W1	Pin 1–2 Closed	Provides EVM with 5 V from the DSP
	Pin 2–3 Closed	Provides EVM with 3.3 V from the DSP
W2	Open	EVM in test mode
	Closed	EVM in host mode
W3	Open	TLV5619 hardware selected
	Closed	TLV5619 software selected
W4	Open	TLV5639 hardware selected
	Closed	TLV5639 software selected
W5	Pin 1–2 Closed	Applies onboard reference to data converters
	Pin 2–3 Closed	Applies external (or Internal TLV5639) reference to data converters
W6	Pin 1–2 Closed	TLV5619 output to J9 and J7-1
	Pin 2–3 Closed	TLV5619 output to J9 and J7-1 through U14 buffer circuit.
W7	Pin 1–2 Closed	TLV5639 output to J10 and J7-3
	Pin 2–3 Closed	TLV5639 output to J10 and J7-3 through U14 buffer circuit.
W8	See Section 1.2.2.2	Upper address selection block
W9	Pin 1–2 Closed	Applies DC_CSa# signal to mux. output enable
	Pin 2–3 Closed	Ties TP13 to mux. output enable for user configurable I/O
W10	Pin 1–2 Closed	Applies DC_CNTL1 signal to TLV5619 $\overline{PD}$ pin
	Pin 2–3 Closed	Ties TP11 to TLV5619 $\overline{PD}$ pin for user configurable I/O
W11	Pin 1–2 Closed	Applies DC_CNTL0 signal to TLV5619 and TLV5639 $\overline{LDAC}$ pin
	Pin 2–3 Closed	Ties TP12 to TLV5619 and TLV5639 /LDAC pin for user configurable I/O
W12	See Section 1.2.2.2	Lower address selection block
W13	Open	CLKOUT source from J2
	Closed	CLKOUT source from DSP via J5

3.4 I/O Connector Signals

The following tables show the signal pins available to the EVM from the input/output connectors.

Table 3–4. Daughtercard Connector J4 (unused pins omitted for clarity)

Signal	Pin	Pin	Signal
+5V	1	2	+5V
DC_A17	7	8	DC_A16
DC_A15	9	10	DC_A14
GROUND	11	12	GROUND
+5V	21	22	+5V
DC_A5	23	24	DC_A4
DC_A3	25	26	DC_A2
GROUND	31	32	GROUND
+3.3V	41	42	+3.3V
GROUND	51	52	GROUND
DSP_15	53	54	DSP_14
DSP_13	55	56	DSP_12
DSP_11	57	58	DSP_10
DSP_9	59	60	DSP_8
GROUND	61	62	GROUND
DSP_7	63	64	DSP_6
DSP_5	65	66	DSP_4
DSP_3	67	68	DSP_2
DSP_1	69	70	DSP_0
GROUND	71	72	GROUND
N/C	73	74	DC_$\overline{WE}$
DC_A$\overline{OE}$	75	76	N/C
N/C	77	78	DC_$\overline{CSa}$
GROUND	79	80	GROUND

Table 3–5. Daughtercard Connector J5 (unused pins omitted for clarity)

Signal	Pin	Pin	Signal
GROUND	3	4	Ground
+5V (TP8)	5	6	+5V (TP8)
GROUND	7	8	GROUND
+5V (TP8)	9	10	+5V (TP8)
+3.3V (TP9)	19	20	+3.3V (TP9)
GROUND	25	26	GROUND
GROUND	31	32	GROUND
GROUND	37	38	GROUND
GROUND	43	44	GROUND
GROUND	51	52	GROUND
GROUND	61	62	GROUND
DC_CNTL1	63	64	DC_CNTL0
GROUND	75	76	GROUND
GROUND	77	78	DC_CLKOUT
GROUND	79	80	GROUND

Table 3–6. DSP/Micro Data Input Connector J1

Signal	Pin	Pin	Signal
DSP_15	1	2	DGND
DSP_14	3	4	DGND
DSP_13	5	6	DGND
DSP_12	7	8	DGND
DSP_11	9	10	DGND
DSP_10	11	12	DGND
DSP_9	13	14	DGND
DSP_8	15	16	DGND
DSP_7	17	18	DGND
DSP_6	19	20	DGND
DSP_5	21	22	DGND
DSP_4	23	24	DGND
DSP_3	25	26	DGND
DSP_2	27	28	DGND
DSP_1	29	30	DGND
DSP_0	31	32	DGND
CLKOUT	33	34	DGND

Table 3–7. DSP/Micro Control Connector J8

Signal	Pin	Pin	Signal
SPARE	1	2	DGND
$\overline{\text{LDAC}}$	3	4	DGND
RD/WR	5	6	DGND
$\overline{\text{IS}}$	7	8	DGND
A1	9	10	DGND
A0	11	12	DGND
DC_$\overline{\text{OE}}$	13	14	DGND
DC_$\overline{\text{WE}}$	15	16	DGND
$\overline{\text{PD}}$	17	18	DGND
CLKOUT	19	20	DGND

3.5 DAC Output Connectors

The following tables show the signal pins of the data converter output connectors.

Table 3–8. Data Converter Output J7

Signal	Pin	Pin	Signal
TLV5619	1	2	AGND
TLV5639	3	4	AGND
SPARE	5–25	6–26	AGND

Table 3–9. SMA Output J9

Signal	Pin	Pin	Signal
TLV5619	Center	Shell	AGND

Table 3–10. SMA Output J10

Signal	Pin	Pin	Signal
TLV5639	Center	Shell	AGND

Appendix A

Schematics

The following pages show a complete schematic diagram of the EVM.

Revision History		
REV	ECN Number	Approved

J2 R20 49.9 C2 SIT CLKOUT

R1 33

J1 CLKOUT DSP_0 DSP_1 DSP_2 DSP_3 DSP_4 DSP_5 DSP_6 DSP_7 DSP_8 DSP_9 DSP_10 DSP_11 DSP_12 DSP_13 DSP_14 DSP_15

U1 SN74AHC245 — /OE, /TEST, DIR, VCC, GND; A1–A8 ← D0–D7 via R2A–R2H 33; B1–B8 → D0–D7; C33 0.1uF

U4 SN74AHC245 — /OE, /TEST, DIR, VCC, GND; A1–A8 ← D8–D15 via R3A–R3H 33; B1–B8 → D8–D15; C34 0.1uF

U5 SN74AHC245 — /OE ← /TEST, DIR, VCC, GND; B1–B8 → TD0–TD7; A1–A8 → D0–D7; C35 0.1uF

U8 SN74AHC245 — /OE ← /TEST, DIR, VCC, GND; B1–B8 → TD1, TD2, TD0, TD1, TD2, TD0, TD1, TD2; A1–A8 → D8–D15; C36 0.1uF

U18 SN74X1G04 — CLR

U6 SN74AHC163 — CLR, LOAD, ENT, ENP, CLK, A, B, C, D; RCO; QA–QD → TD0–TD2, CLR

U7A SN74HC139 — A, B, G; Y0–Y3; W2; R19 10K; R10 1K; D2 Amber (On = Test); /TEST

X1 5MHz — OE, VCC, OUT, GND; C31 0.1uF

U9 SN74HC1G04

U10 SN74HC1G32

U2 TLV5619DW — D0–D11 ← D4–D15; /PD; /CS_5619; /WE; /LDAC; OUT → 5619_OUT; VDD, REFIN, GND; C1 0.01uF, C6 0.1uF, C7 0.1uF; REF; VCCA

U3 TLV5639DW — D0–D11 ← D4–D15; REG ← CR_WR; /CS_5639; /WE; /LDAC; OUT → 5639_OUT; VDD, REFIN, GND; C12 0.01uF, C29 0.1uF, C30 0.1uF; REF; VCCA

U7B SN74HC139 — A ← A0, B ← A1, G ← /IS; Y0–Y3

W3 → /CS_5619; R8 10K

U15A SN74AHC08 — W4 → /CS_5639; R9 10K

U12 SN74HC1G04 → CR_WR

U11A SN74AHC32 — A0, A1

U19 SN74X1G04

U11B SN74AHC32 — /IS → /OE

U15B SN74AHC08 — RD/WR, R5 33

U11C SN74AHC32 — DC_OE, DC_WE#, R7 33

U15C SN74AHC08 — TP14 → /WE

CONTROL

U14A TLV2772 — 5619_OUT; R32 10K; R33 SIT; W6; J9

U14B TLV2772 — 5639_OUT; R35 10K; R36 SIT; W7; J10

J7

Engineer:	
Drawn By:	
FILE:	

12500 TI Boulevard. Dallas, Texas 75243

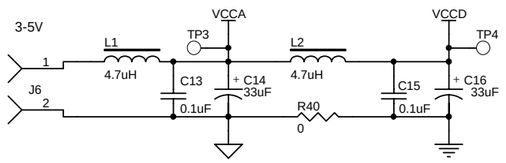
Title: TLV5619/5639 DAC EVM Schematic

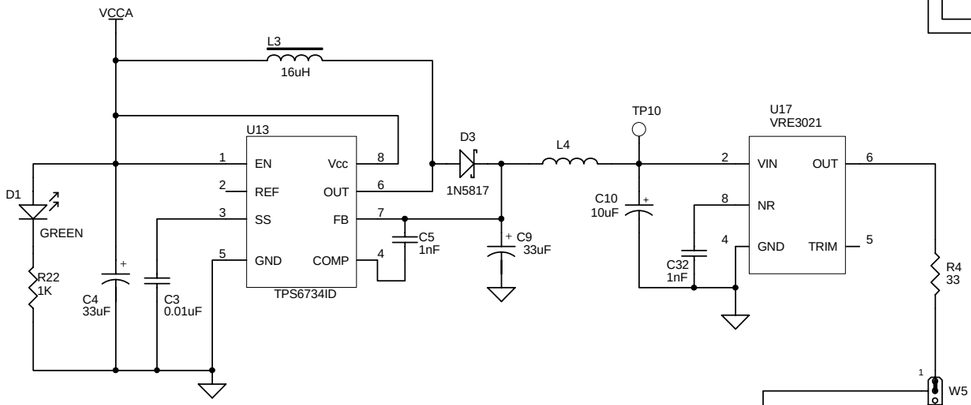
SIZE: | DATE: 15-Nov-2000 | REV: 2

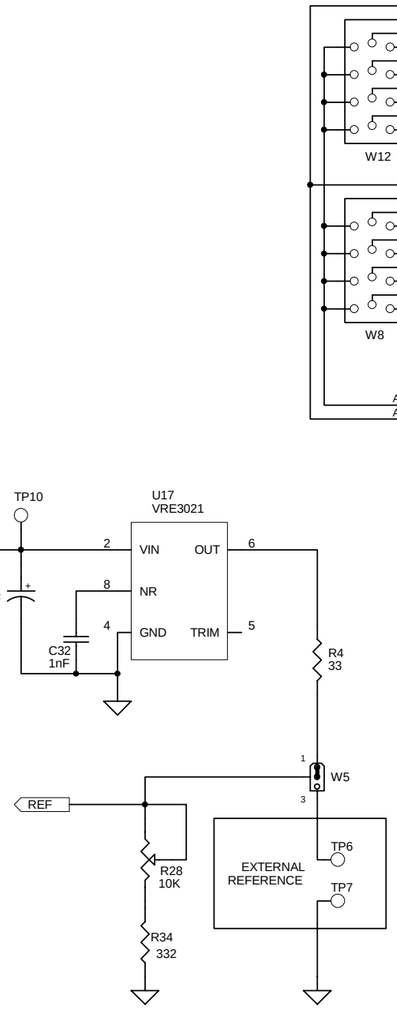
SHEET: 1 OF: 2

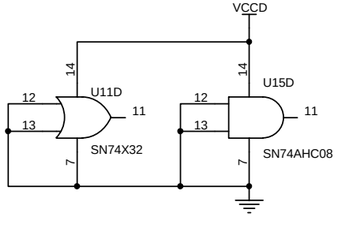
Revision History		
REV	ECN Number	Approved

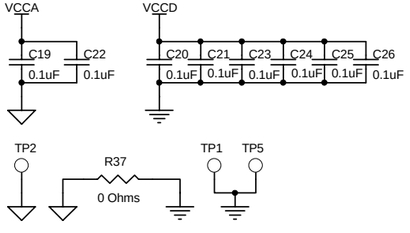
TMS320 Common Connector Interface

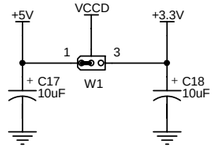


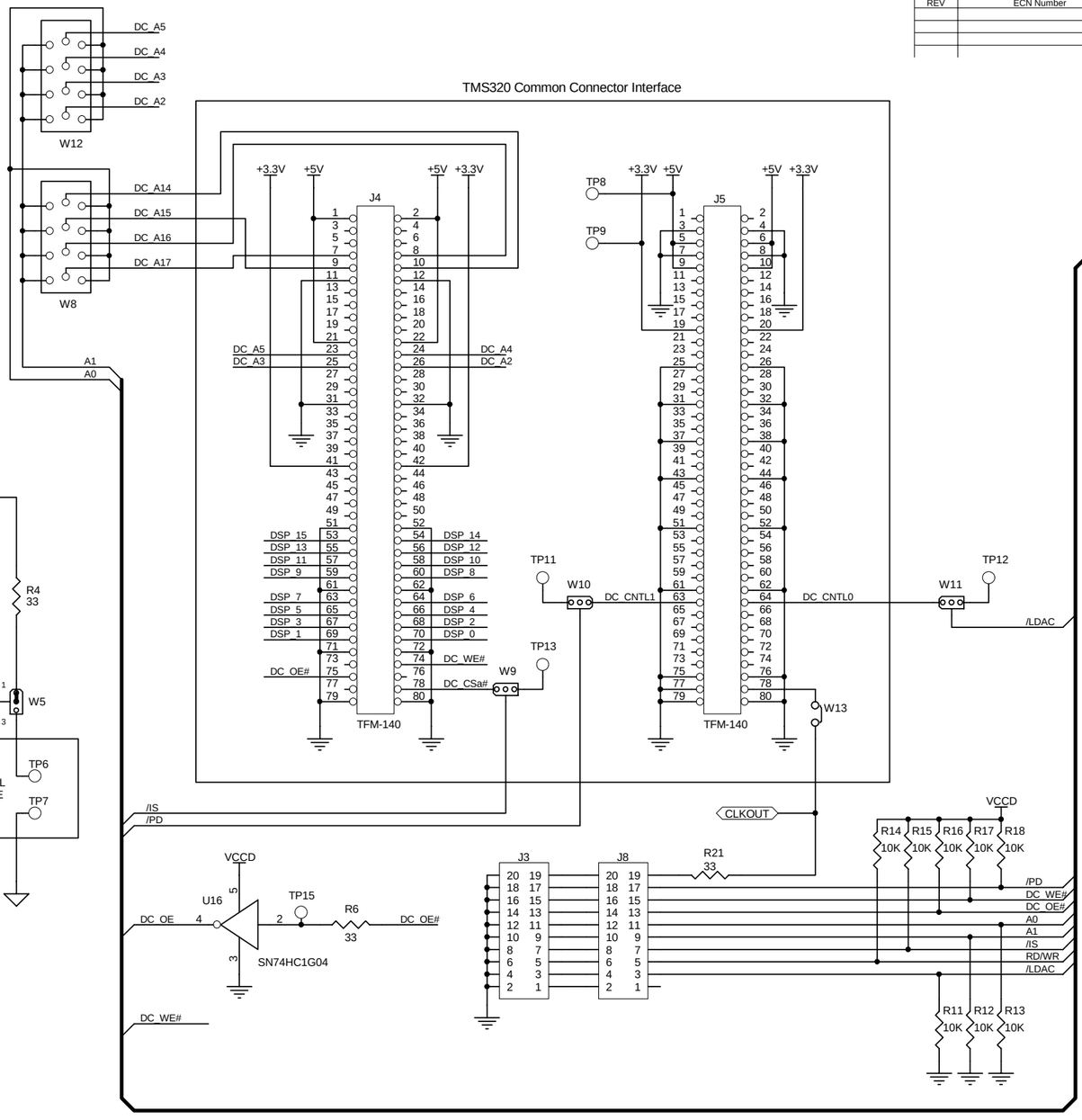












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