

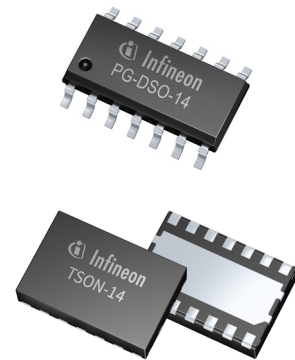
# TLE9254V

## High speed dual CAN transceiver with bus wake-up



### Features

- Compliant to ISO 11898-2:2016
- Dual channel CAN FD transceiver with very low quiescent current in stand-by mode
- Wide common mode range for electromagnetic immunity (EMI)
- Very low electromagnetic emission (EME) allows the use without additional common mode choke
- Excellent ESD robustness
- Very high CAN FD symmetry to support CAN FD data frames up to 5 MBit/s
- $V_{IO}$  input for voltage adaption to the microcontroller supply
- Extended supply range on  $V_{CC}$  and  $V_{IO}$
- CAN short circuit proof to ground, to battery and to  $V_{CC}$
- TxD timeout function
- Low CAN bus leakage current in power-down state
- Overtemperature protection
- Protected against automotive transients according to ISO 7637 and SAE J2962-2
- Stand-by mode with bus wake-up pattern function
- Wake-up indication on the RxD output
- Transmitter supply  $V_{CC}$  can be turned off in stand-by mode
- Green Product (RoHS compliant)



### Potential applications

- Gateway modules
- Body Control Modules (BCMs)
- Electric Power Steering
- Battery Management Systems
- Cluster and Lighting Control Modules

### Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

### Description

The TLE9254V is part of Infineon's high speed CAN transceiver generation, used in HS CAN for automotive applications as well as in industrial applications. It is designed to fulfill the requirements of the following standards:

- ISO 11898-2 (2016) physical layer specification

# TLE9254V

## High speed dual CAN transceiver with bus wake-up



### Description

- SAE J1939
- SAE J2284

The TLE9254V is available in a PG-DSO-14 package and in a small, leadless PG-TSON-14 package. Both packages are RoHS compliant and halogen free. Additionally the PG-TSON-14 package supports the solder joint requirements for automated optical inspection (AOI).

As an interface between the physical bus layer and the HS CAN protocol controller, the TLE9254V is designed to protect the microcontroller against interference generated inside the network. A very high ESD robustness and the very high RF immunity allow the use in automotive applications without additional protection devices, such as suppressor diodes.

The very high transmitter symmetry combined with the optimized delay symmetry of the receiver enables the TLE9254V to support CAN FD data frames up to 5 Mbit/s. Based on the high symmetry of the CANH and CANL output signals, the TLE9254V provides a very low level of electromagnetic emission (EME) within a wide frequency range. The TLE9254V fulfills even stringent EMC test limits without external components, such as a common mode choke.

TLE9254V offers low-power management using the stand-by mode with an optimized, very low quiescent current. In stand-by mode the typical quiescent current for one channel of the TLE9254V is below 10  $\mu$ A, while the CAN channel can still wake up on a signal on the HS CAN bus.

Fail-safe features such as overtemperature protection, output current limitation or the TxD timeout feature are designed to protect the TLE9254V and the external circuitry from irreparable damage.

While the transceiver TLE9254V is not supplied, the bus is switched off and exhibits an ideal passive behavior with the lowest possible load to all other subscribers of the HS CAN network.

TLE9254V supports 3.3 V as well as 5 V supplied microcontrollers with the  $V_{IO}$ .

Type	Package	Marking
TLE9254VSK	PG-DSO-14	9254V
TLE9254VLC	PG-TSON-14	9254V

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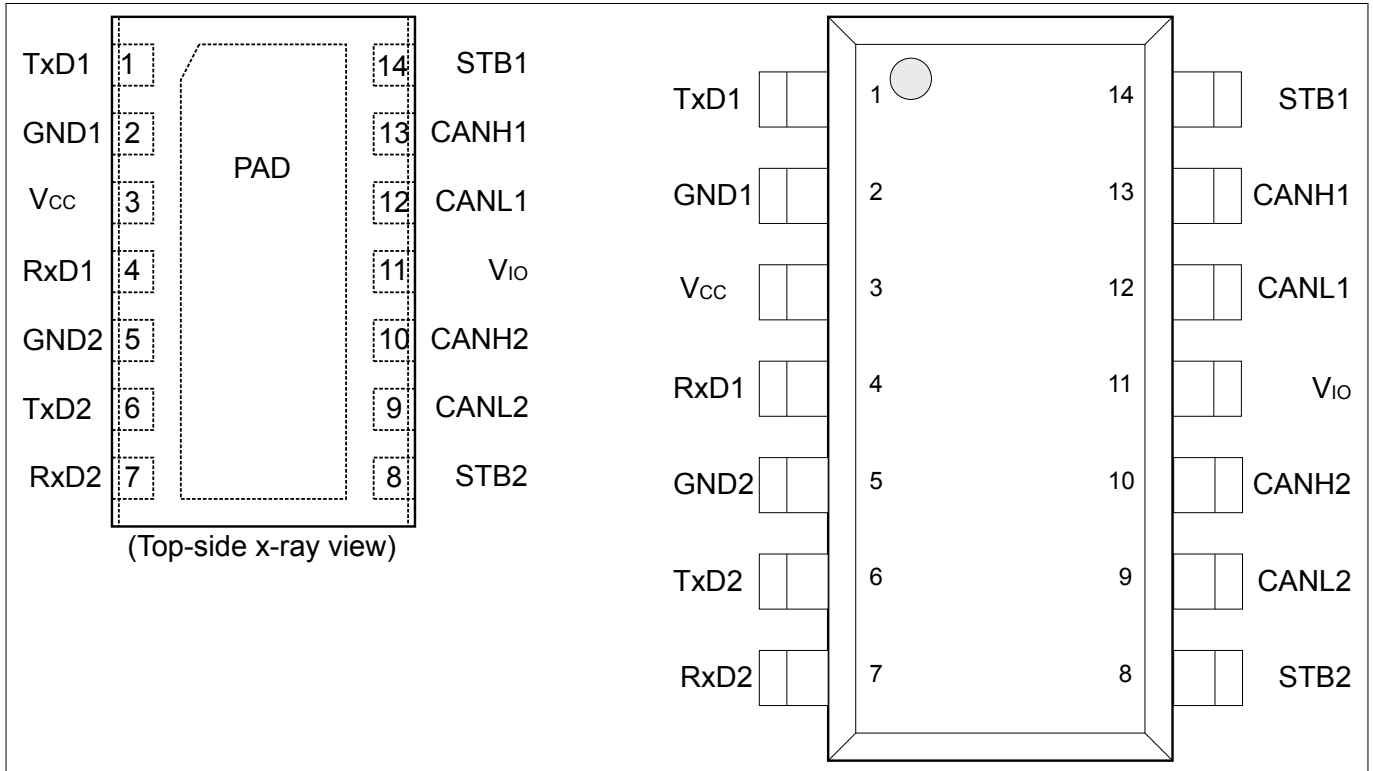
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**Pin configuration**

**2 Pin configuration**

**2.1 Pin assignment**



**Figure 2 Pin configuration**

**2.2 Pin definitions**

**Table 1 Pin definitions and functions**

Pin No.	Symbol	Function
1	TxD1	Transmit Data input for HS CAN channel 1; Internal pull-up current source to $V_{CC}$ , "low" for dominant state.
2	GND1	Ground for HS CAN channel 1; GND1 and GND2 must be connected to the same ground of the PCB.
3	$V_{CC}$	Transmitter supply voltage; 100 nF decoupling capacitor to GND required.
4	RxD1	Receive Data output for HS CAN channel 1; "low" in dominant state.
5	GND2	Ground for HS CAN channel 2; GND1 and GND2 must be connected to the same ground of the PCB.
6	TxD2	Transmit Data input for HS CAN channel 2;

**Pin configuration**

**Table 1 Pin definitions and functions (continued)**

Pin No.	Symbol	Function
		Internal pull-up current source to $V_{CC}$ , "low" for dominant state.
7	RxD2	Receive Data output for HS CAN channel 2; "low" in dominant state.
8	STB2	Stand-by control input for HS CAN channel 2; Internal pull-up current source to $V_{CC}$ , "high" to select stand-by mode.
9	CANL2	CAN bus Low level I/O for HS CAN channel 2; "low" in dominant state.
10	CANH2	CAN bus High level I/O for HS CAN channel 2; "high" in dominant state.
11	$V_{IO}$	Digital supply voltage; Supply voltage input of internal state machine. Used to adapt the levels of logical input voltage and output voltage of the transceiver to the microcontroller supply. 100 nF decoupling capacitor to GND required.
12	CANL1	CAN bus Low level I/O for HS CAN channel 1; "low" in dominant state.
13	CANH1	CAN bus High level I/O for HS CAN channel 1; "high" in dominant state.
14	STB1	Stand-by control input for HS CAN channel 1; Internal pull-up current source to $V_{CC}$ , "high" to select stand-by mode.
PAD	–	Connect to PCB heat sink area. Do not connect to other potential than GND.

**General product characteristics**

### 3 General product characteristics

Electrical parameters described within this chapter apply for each channel of TLE9254V, respectively.

#### 3.1 Absolute maximum ratings

**Table 2 Absolute maximum ratings voltages, currents and temperatures<sup>1)</sup>**

All voltages with respect to ground; positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
<b>Voltages</b>							
Transmitter supply voltage	$V_{CC}$	-0.3	–	6.0	V	–	P_7.1.1
Digital supply voltage	$V_{IO}$	-0.3	–	6.0	V	–	P_7.1.9
CANH DC voltage versus GND	$V_{CANH}$	-40	–	40	V	–	P_7.1.2
CANL DC voltage versus GND	$V_{CANL}$	-40	–	40	V	–	P_7.1.14
Differential voltage between CANH and CANL	$V_{CAN\_Diff}$	-40	–	40	V	–	P_7.1.3
Voltages at pins: STB, TxD, RxD	$V_{MAX\_IO1}$	-0.3	–	6	V	–	P_7.1.4
Voltages at pin: STB, TxD, RxD	$V_{MAX\_IO2}$	-0.3	–	$V_{IO} + 0.3$	V	–	P_7.1.5
<b>Currents</b>							
RxD output current	$I_{RxD}$	-20	–	20	mA	–	P_7.1.6
<b>Temperatures</b>							
Junction temperature	$T_j$	-40	–	150	°C	–	P_7.1.7
Storage temperature	$T_S$	-55	–	150	°C	–	P_7.1.8
<b>ESD resistivity</b>							
ESD immunity at CANH, CANL versus GND	$V_{ESD\_HBM\_CAN}$	-10	–	10	kV	<sup>2)</sup> HBM (100 pF via 1.5 kΩ)	P_7.1.10
ESD immunity at all other pins	$V_{ESD\_HBM\_ALL}$	-3	–	3	kV	<sup>2)</sup> HBM (100 pF via 1.5 kΩ)	P_7.1.11
ESD immunity at corner pins	$V_{ESD\_CDM\_CP}$	-750	–	750	V	<sup>3)</sup> CDM	P_7.1.12
ESD immunity at any pin	$V_{ESD\_CDM\_OP}$	-500	–	500	V	<sup>3)</sup> CDM	P_7.1.13

Notes:

- 1 Not subject to production test, specified by design.
- 2 ESD susceptibility, Human Body Model (HBM) according to ANSI/ESDA/JEDEC JS-001.
- 3 ESD susceptibility, Charged Device Model (CDM) according to EIA/JESD22-C101 or ESDA STM5.3.1.



**General product characteristics**

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as outside the normal operating range. Protection functions are not designed for continuous repetitive operation.*

**General product characteristics**

**3.2 Functional range**

**Table 3 Functional range**

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
<b>Supply voltages</b>							
Transmitter supply voltage	$V_{CC}$	4.5	–	5.5	V	–	P_7.2.1
Digital supply voltage	$V_{IO}$	3.0	–	5.5	V	–	P_7.2.3
<b>Thermal parameters</b>							
Junction temperature	$T_j$	-40	–	150	°C	–	P_7.2.2

*Note:* Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the electrical characteristics table.

**3.3 Thermal resistance**

*Note:* This thermal data was generated in accordance with JEDEC JESD51 standards. For more information visit [www.jedec.org](http://www.jedec.org).

**Table 4 Thermal resistance<sup>4)</sup>**

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
<b>Thermal resistance</b>							
Junction to ambient PG-TSON-14	$R_{thJA\_TSON14}$	–	65	–	K/W	<sup>5)</sup>	P_7.3.1
Junction to ambient PG-DSO-14	$R_{thJA\_DSO14}$	–	120	–	K/W	<sup>5)</sup>	P_7.3.2
<b>Thermal shutdown (junction temperature)</b>							
Thermal shutdown temperature	$T_{JSD}$	170	180	190	°C	–	P_7.3.3
Thermal shutdown hysteresis	$\Delta T$	5	8	20	K	–	P_7.3.4

<sup>4</sup> Not subject to production test, specified by design.

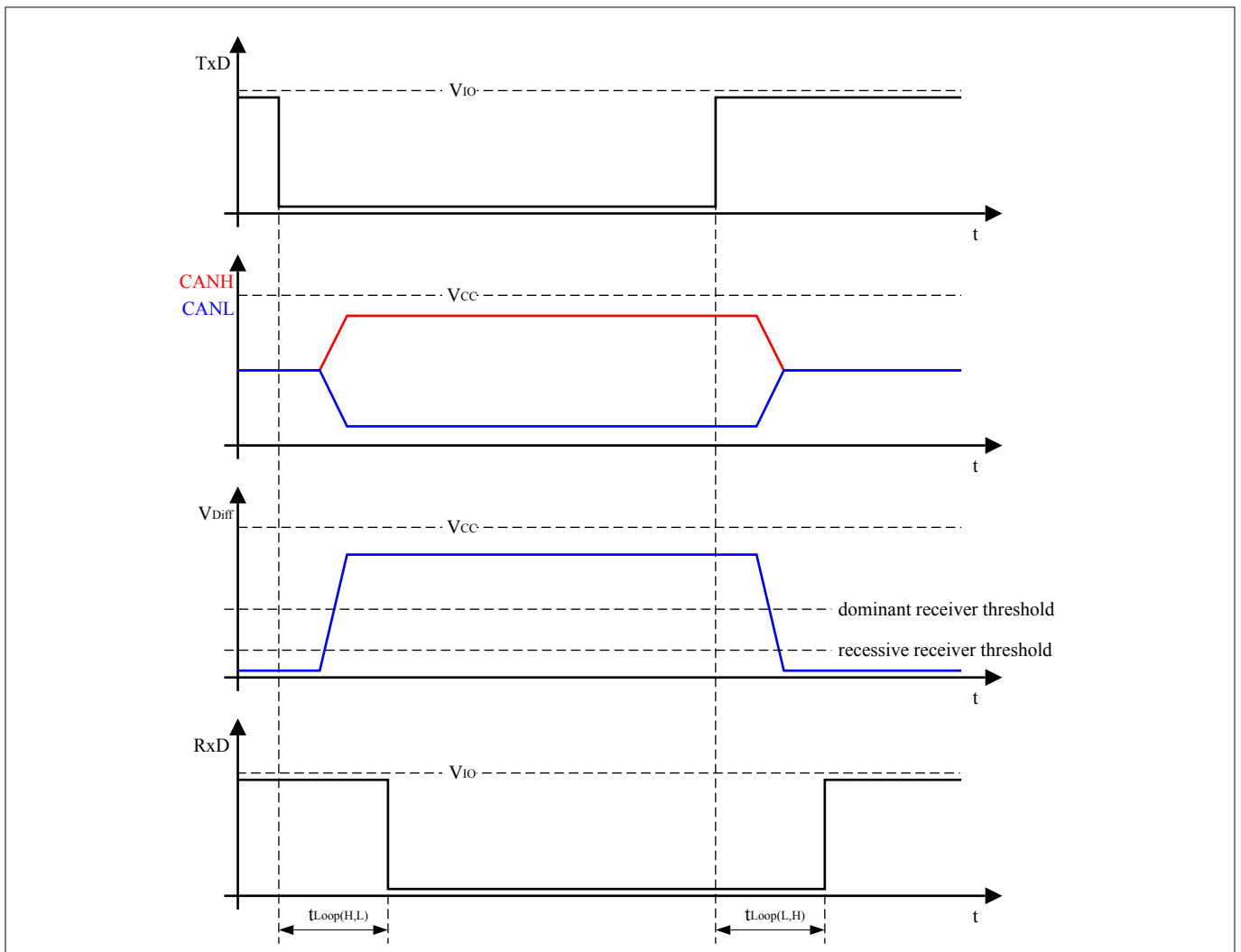
<sup>5</sup> Specified  $R_{thJA}$  value is according to JEDEC JESD51-2,-7 at natural convection on FR4 2s2p board; the product (chip and package) was simulated on a 76.2 × 114.3 × 1.5 mm<sup>3</sup> board with two inner copper layers (2 × 70 μm Cu, 2 × 35 μm Cu).

**High speed CAN functional description**

**4 High speed CAN functional description**

HS CAN is a serial bus system that connects microcontrollers, sensors and actuators for real-time control applications. ISO 11898 describes the use of the Controller Area Network (CAN) within road vehicles. According to the 7-layer OSI reference model, the physical layer of an HS CAN bus system specifies the data transmission from one CAN node to all other available CAN nodes within the network. The physical layer specification of a CAN bus system includes all electrical specifications of a CAN network. The CAN transceiver is part of the physical layer specification. The TLE9254V is a high speed CAN transceiver with a dedicated bus wake-up function as defined in the latest ISO 11898-2 HS CAN standard.

**4.1 High speed CAN physical layer**



**Figure 3 High speed CAN bus signals and logic signals**

---

## High speed CAN functional description

The TLE9254V is a high speed CAN transceiver, operating as an interface between the CAN controller and the physical bus medium. An HS CAN network is a two wire, differential network which allows data transmission rates up to 5 MBit/s. HS CAN signals can have the following states on the CAN bus: dominant and recessive (see [Figure 3](#)).

The CANH and CANL pins are the interface to the CAN bus and both pins operate as input and output simultaneously. The RxD and TxD pins are the interface to the microcontroller. The TxD pin is the serial data input from the CAN controller, the RxD pin is the serial data output to the CAN controller. The TLE9254V includes a receiver and a transmitter unit, allowing the transceiver to send data to the bus medium and monitor the data from the bus medium at the same time, see [Figure 1](#). The TLE9254V converts the serial data stream, which is available on the transmit data input TxD, into a differential output signal on the CAN bus, provided by the CANH and CANL pins. The receiver stage of the TLE9254V monitors the data on the CAN bus and converts them to a serial, single-ended signal on the RxD output pin. A "low" signal on the TxD pin creates a dominant signal on the CAN bus, followed by a logical "low" signal on the RxD pin (see [Figure 3](#)). The feature of broadcasting data to the CAN bus and listening to the data traffic on the CAN bus simultaneously is essential to support the bit-to-bit arbitration within CAN.

ISO 11898-2 specifies the voltage levels for HS CAN transceivers. Whether a data bit is dominant or recessive depends on the voltage difference between the CANH and CANL pins:

$$V_{\text{Diff}} = V_{\text{CANH}} - V_{\text{CANL}}$$

To transmit a dominant signal to the CAN bus, the amplitude of the differential signal  $V_{\text{Diff}}$  is higher than or equal to 1.5 V. To receive a recessive signal from the CAN bus, the amplitude of the differential  $V_{\text{Diff}}$  is lower than or equal to 0.5 V.

In partially-supplied high speed CAN the bus nodes of one common network have different power supply conditions. Some nodes are connected to the common power supply, while other nodes are disconnected from the power supply and in power-down state. Regardless of whether the CAN bus subscriber is supplied or not, each subscriber connected to the common bus media must not interfere with the communication. The TLE9254V is designed to support partially-supplied networks. In power-down state, the receiver input resistors are switched off and the transceiver input has a high resistance.

For permanently supplied ECUs, the TLE9254V provides a stand-by mode. In stand-by mode, the power consumption of the TLE9254V is optimized to a minimum, while the device can still recognize wake-up patterns on the CAN bus and signal the wake-up event to the external microcontroller.

The voltage level on the digital input TxD and the digital output RxD is determined by the power supply level at the  $V_{\text{IO}}$  pin.

**Modes of operation**

## 5 Modes of operation

The description within this chapter applies for each of the two HS CAN channels of TLE9254V. The HS CAN channels are independent from each other. Both HS CAN channels have equal functionality.

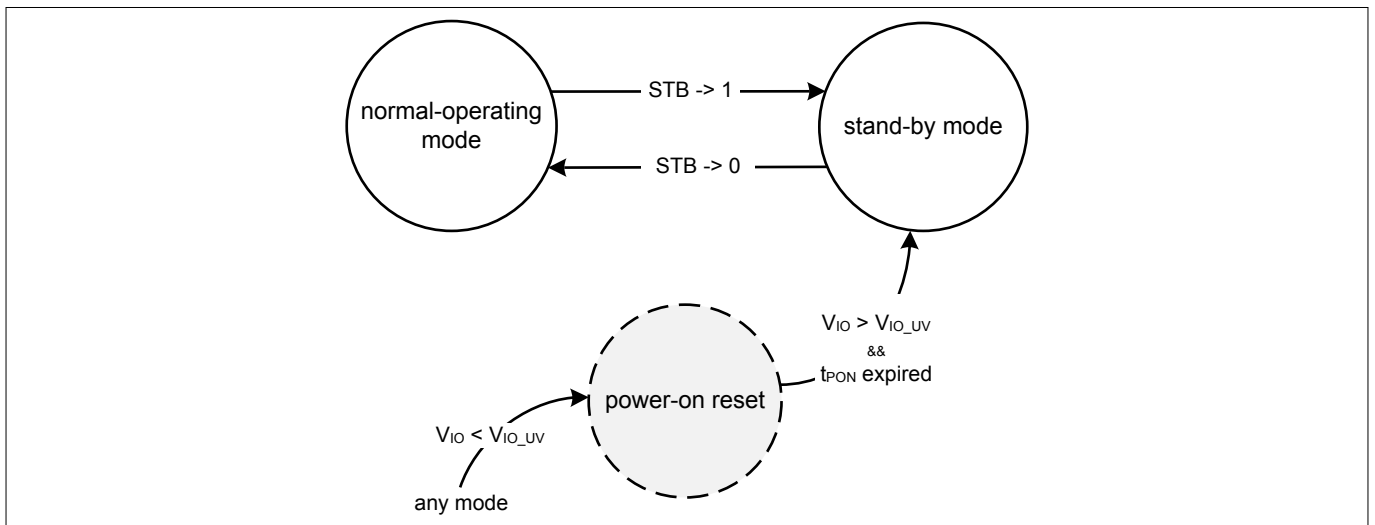
The TLE9254V supports two different modes of operation for each HS CAN channel (see **Figure 4**):

- Normal-operating mode (see **Normal-operating mode**)
- Stand-by mode (see **Stand-by mode**)

The mode selection input pin STB triggers mode changes. If a wake-up event occurs on the HS CAN bus, then the TLE9254V indicates that on the RxD output pin in stand-by mode, but it does not trigger a mode change. The transceiver channels work independently from each other. Both channels are supplied by  $V_{IO}$  supply.

Transmitter output stage of channel 1 is supplied by  $V_{CC}$  and the mode of operation is selected by STB1.

Transmitter output stage of channel 2 is supplied by  $V_{CC}$  and the mode of operation is selected by STB2.



**Figure 4** Mode state diagram

**Modes of operation**

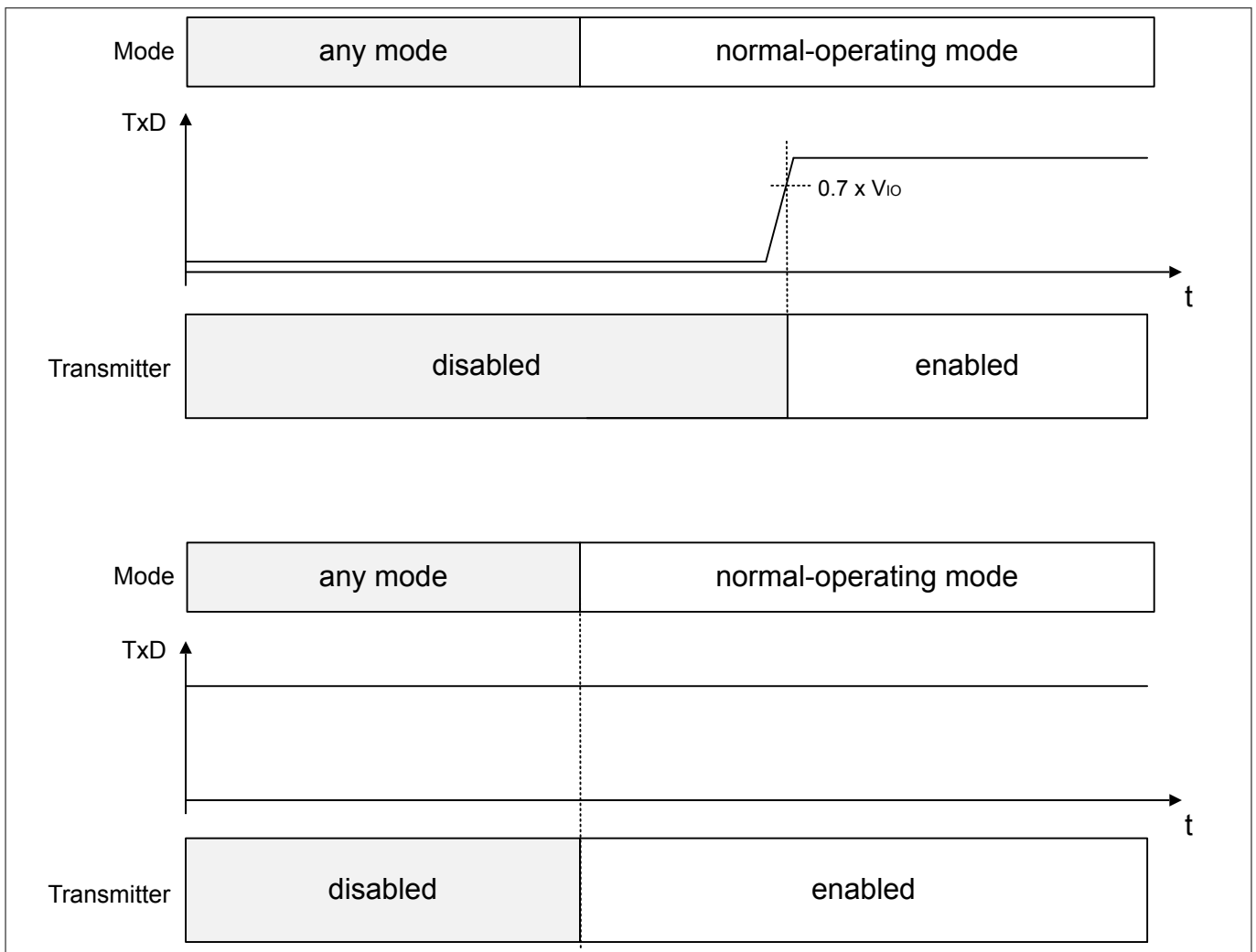
**5.1 Normal-operating mode**

In normal-operating mode the TLE9254V sends and receives data from the HS CAN bus. All functions are active (see [Figure 4](#)):

- The transmitter is enabled and drives the serial data stream on the TxD input pin to the bus pins CANH and CANL.
- The receiver is enabled and converts the signal from the bus to a serial data stream on the RxD output pin.
- The bus biasing is connected to  $V_{CC}/2$ .
- The STB input pin drives the mode of operation and can change the mode of operation.
- The TxD timeout function is enabled (see [TxD timeout feature](#)).
- The overtemperature protection is enabled (see [Overtemperature protection](#)).
- The undervoltage detection on  $V_{CC}$  is enabled (see [Undervoltage detection on  \$V\_{CC}\$](#) ).
- The undervoltage detection on  $V_{IO}$  is enabled (see [Undervoltage detection on  \$V\_{IO}\$](#) ).

Conditions for entering the normal-operation mode for one channel of TLE9254V:

- One channel of TLE9254V enters normal-operating mode after  $t_{Mode}$ , by setting the respective mode selection pin STB to "low" (see [Figure 4](#)).



**Figure 5 Mode change to normal-operating mode with dominant signal on TxD**

If a recessive signal on TxD input pin is applied after a mode change from any mode to normal-operating mode, then the TLE9254V enables the transmitter path. If a dominant signal is on TxD input pin after a mode change, then the TLE9254V keeps the transmitter path disabled and blocks the dominant signal in order not to disturb the bus communication (see [Figure 5](#)).

---

**Modes of operation**

## **5.2 Stand-by mode**

The stand-by mode is the low-power mode of the TLE9254V. In stand-by mode most of the functions are disabled and each channel of TLE9254V monitors the respective bus for a valid wake-up pattern (WUP), see [Bus Wake-up pattern \(WUP\) detection](#). The following functions are available in stand-by mode:

- The transmitter is disabled and the data available on the TxD input is blocked.
- The TLE9254V monitors the bus for a valid wake-up pattern (WUP).
- The RxD output pin indicates a wake-up (see [RxD pin wake-up behavior](#)).
- The bus biasing is connected to GND.
- The TxD timeout function is disabled.
- The overtemperature protection is disabled.
- The undervoltage detection on  $V_{CC}$  is disabled (see [Undervoltage detection on  \$V\_{CC}\$](#) ).
- The undervoltage detection on  $V_{IO}$  is enabled (see [Undervoltage detection on  \$V\_{IO}\$](#) ).

Conditions for entering the stand-by mode for one channel of TLE9254V:

- If  $V_{IO} > V_{IO\_UV}$  for at least  $t_{PON}$  after power-on reset, then the TLE9254V enters stand-by mode.
- If STB is set to "high" in normal-operating mode, then the TLE9254V enters stand-by mode.

**Modes of operation**

**5.3 Power-on reset**

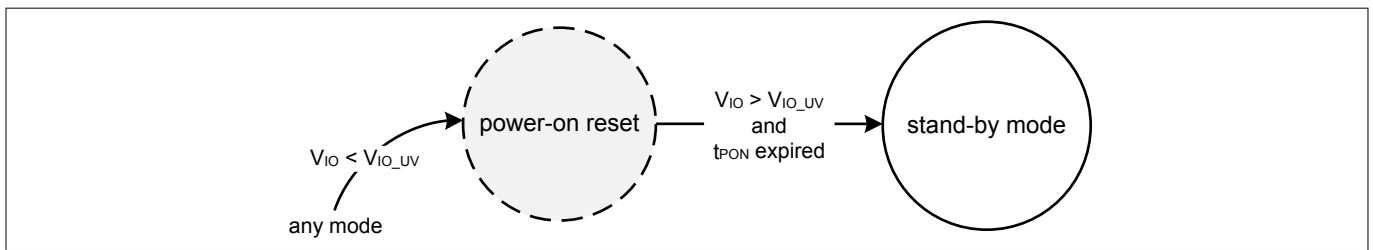
In power-on reset the CANH and CANL bus interface of the TLE9254V acts as a high-impedance input with a very low leakage current. The highly-resistive input does not influence the recessive level of the CAN network and allows an optimized EME performance of the entire HS CAN.

In power-on reset all functions of the TLE9254V are disabled and all channels are switched off:

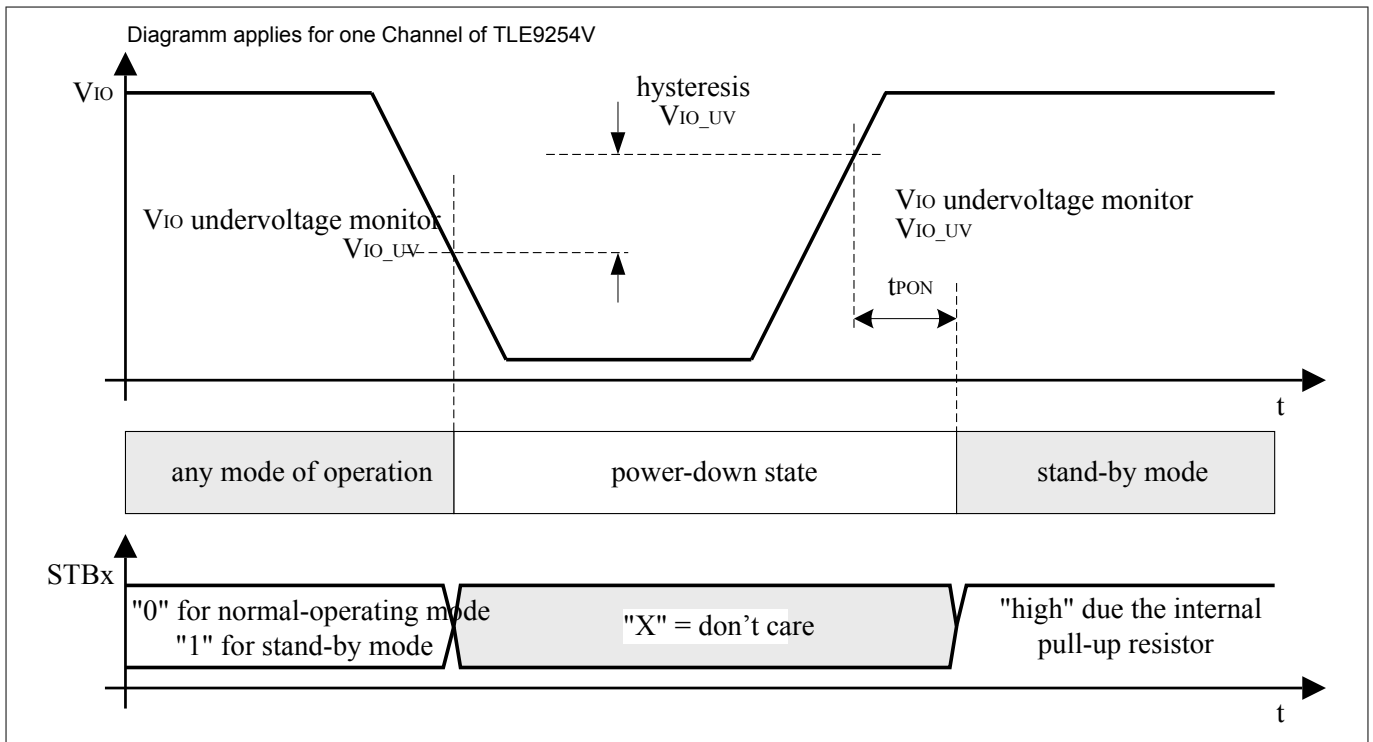
- The transmitter and receiver are disabled.
- The bus biasing is connected to high impedance.
- The TxD timeout function is disabled.
- The overtemperature protection is disabled.
- The undervoltage detection on  $V_{CC}$  is disabled.
- The undervoltage detection on  $V_{IO}$  is disabled.
- The logical input pins are blocked.
- RxD is connected to high impedance.

Conditions for entering the power-on reset:

- $V_{IO}$  is below the  $V_{IO\_UV}$  threshold (see [Figure 6](#)).



**Figure 6 Power-up and power-down**



**Figure 7 Power-up and power-down timings**



**Modes of operation**

**5.4 Bus Wake-up pattern (WUP) detection**

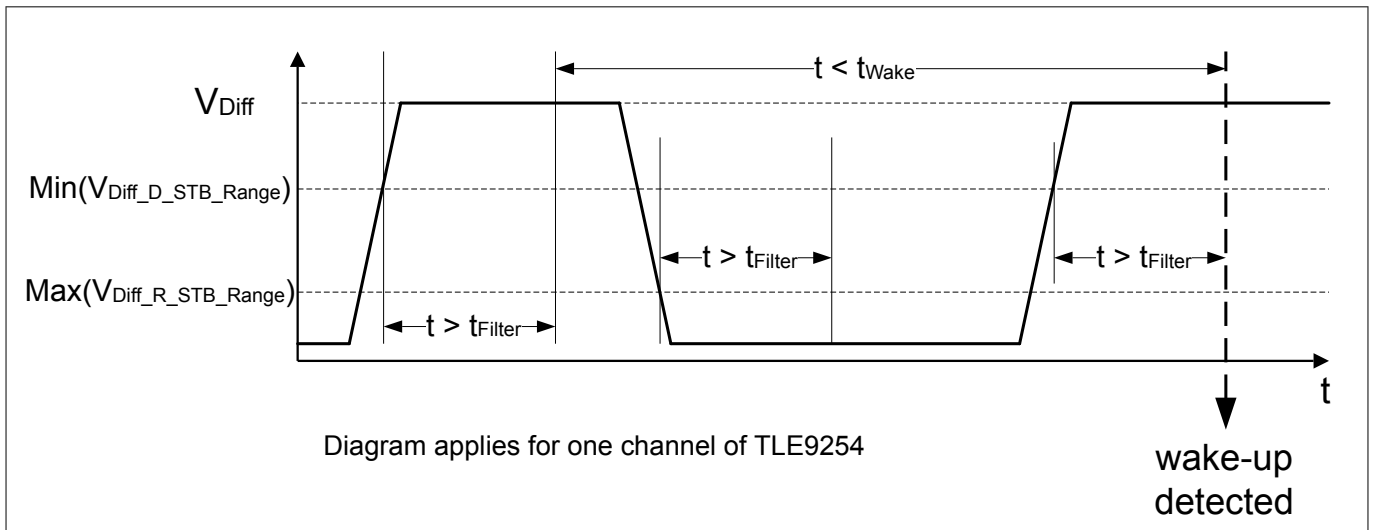
Each channel of TLE9254V has a separate remote wake-up feature called bus wake-up feature according to ISO 11898-2:2016. In stand-by mode the low-power receiver monitors the activity on the CAN bus. If it detects a wake-up pattern, then the device indicates the wake-up signal on the RxD output pin of the dedicated channel. A wake-up event does not trigger a mode change of the respective channel. The TLE9254V remains in stand-by mode until the microcontroller requests a mode change to normal-operating mode. A valid wake-up pattern triggers a wake-up of the dedicated bus.

**5.4.1 Bus Wake-up pattern (WUP)**

The wake-up pattern contains the following sequence of signals:

- dominant with pulse width  $> t_{Filter}$
- recessive with pulse width  $> t_{Filter}$
- dominant with pulse width  $> t_{Filter}$

The  $t_{Wake}$  starts with the first valid dominant pulse (pulse width  $> t_{Filter}$ ). The subsequent recessive and dominant pulses must occur within  $t_{Wake}$  to fulfill a wake-up pattern, see [Figure 8](#). As long as the TLE9254V does not detect a wake-up event, the RxD output remains "high".

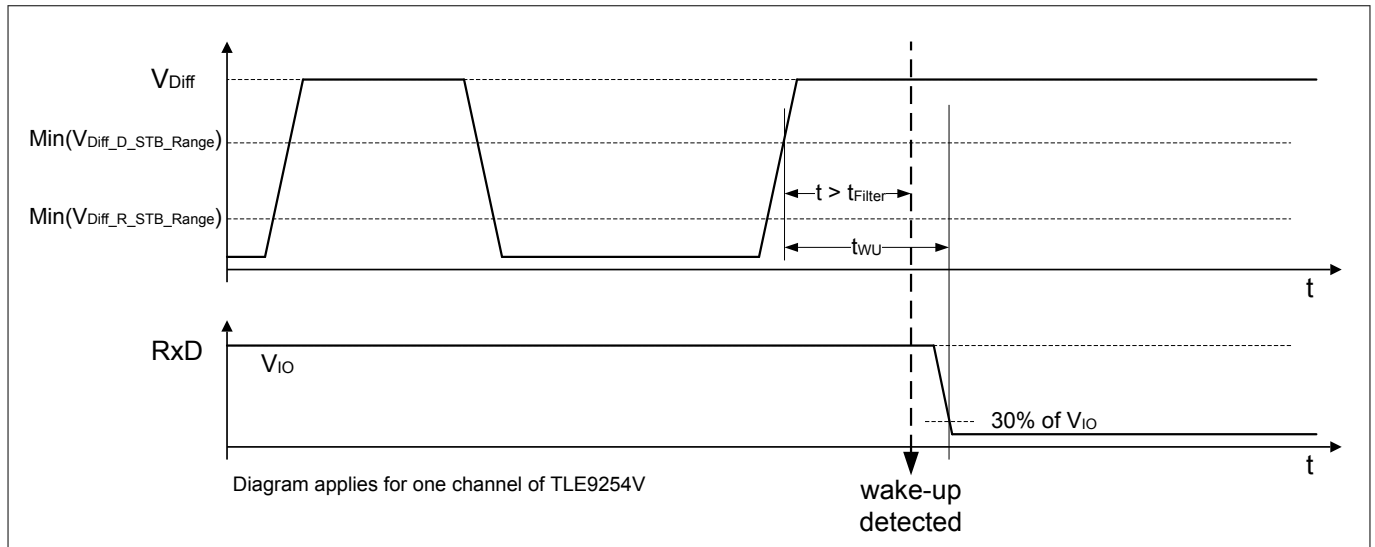


**Figure 8 Remote wake-up signal**

**5.4.2 RxD pin wake-up behavior**

If TLE9254V detects a wake-up event, then it sets the RxD output to "low" (see [Figure 9](#)).

**Modes of operation**



**Figure 9 RxD signal after wake-up detection**

The TLE9254V disables the RxD pin wake-up behavior under each of the following conditions:

- A mode change to normal-operating mode is applied during the wake-up pattern.
- A power-down event occurs on the voltage supply  $V_{IO} < V_{IO\_UV}$ .

Fail-safe functions

## 6 Fail-safe functions

### 6.1 Short circuit protection

The CANH and CANL bus outputs are short circuit proof to GND and short circuit proof to a positive supply voltage. A current limiting circuit is designed to protect the transceiver against damage.

### 6.2 Unconnected logic pins

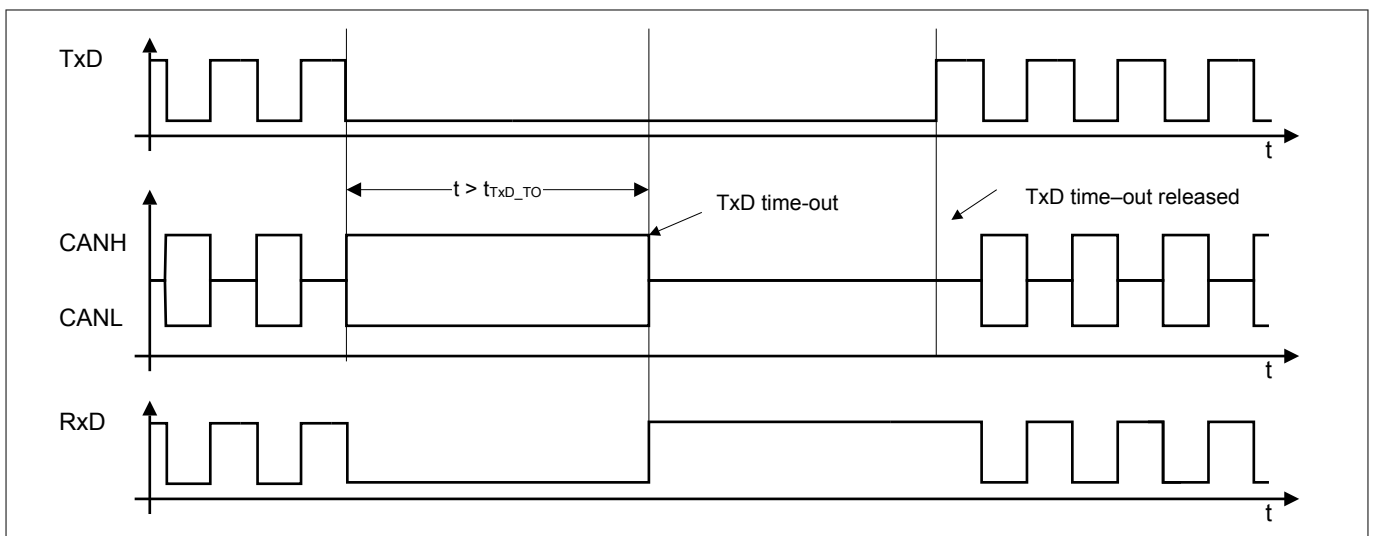
If the input pins are not connected and floating, then this forces the TLE9254V into fail-safe behavior (see [Table 5](#)).

**Table 5** Logical inputs when unconnected

Input signal	Default state	Comment
TxD	"high"	pull-up current source to $V_{IO}$
STB	"high"	pull-up current source to $V_{IO}$

### 6.3 TxD timeout feature

The TxD timeout feature protects the CAN bus from permanently blocking in case the logical signal on the TxD pin is continuously "low". A continuous "low" signal on the TxD pin might have its root cause in a locked-up microcontroller or in a short circuit on the printed circuit board, for example. In normal-operating mode, a logical "low" signal on the TxD pin for the time  $t > t_{TxD\_TO}$  enables the TxD timeout feature and the TLE9254V disables the transmitter (see [Figure 10](#)). The receiver is still active. It monitors the CAN bus communication on the CANH and CANL pins and reflects it on the RxD pin. The TxD timeout feature works for each CAN channel independently.



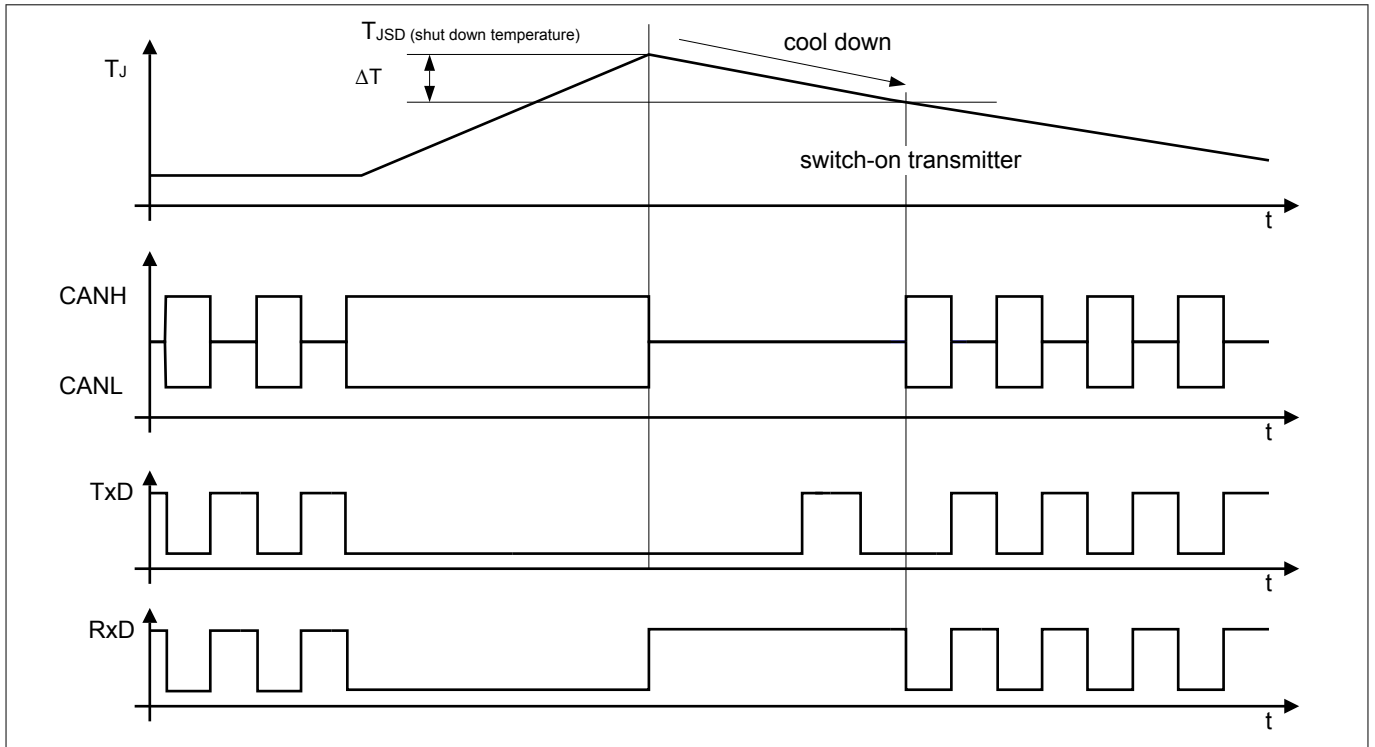
**Figure 10** TxD timeout function

[Figure 10](#) shows how the transmitter is disabled and enabled again. A permanent "low" signal on the TxD input pin activates the TxD timeout function and disables the transmitter. To release the transmitter after a TxD timeout event, the TLE9254V requires a signal change from "low" to "high" on the TxD input pin.

**Fail-safe functions**

**6.4 Overtemperature protection**

The integrated overtemperature detection is designed to protect the TLE9254V from thermal overstress of the transmitter. If the temperature exceeds the threshold  $T_{JSD}$ , then the TLE9254V disables the transmitter. After the device cools down, the TLE9254V enables the transmitter again (see [Figure 11](#)). A hysteresis is implemented within the temperature sensor.

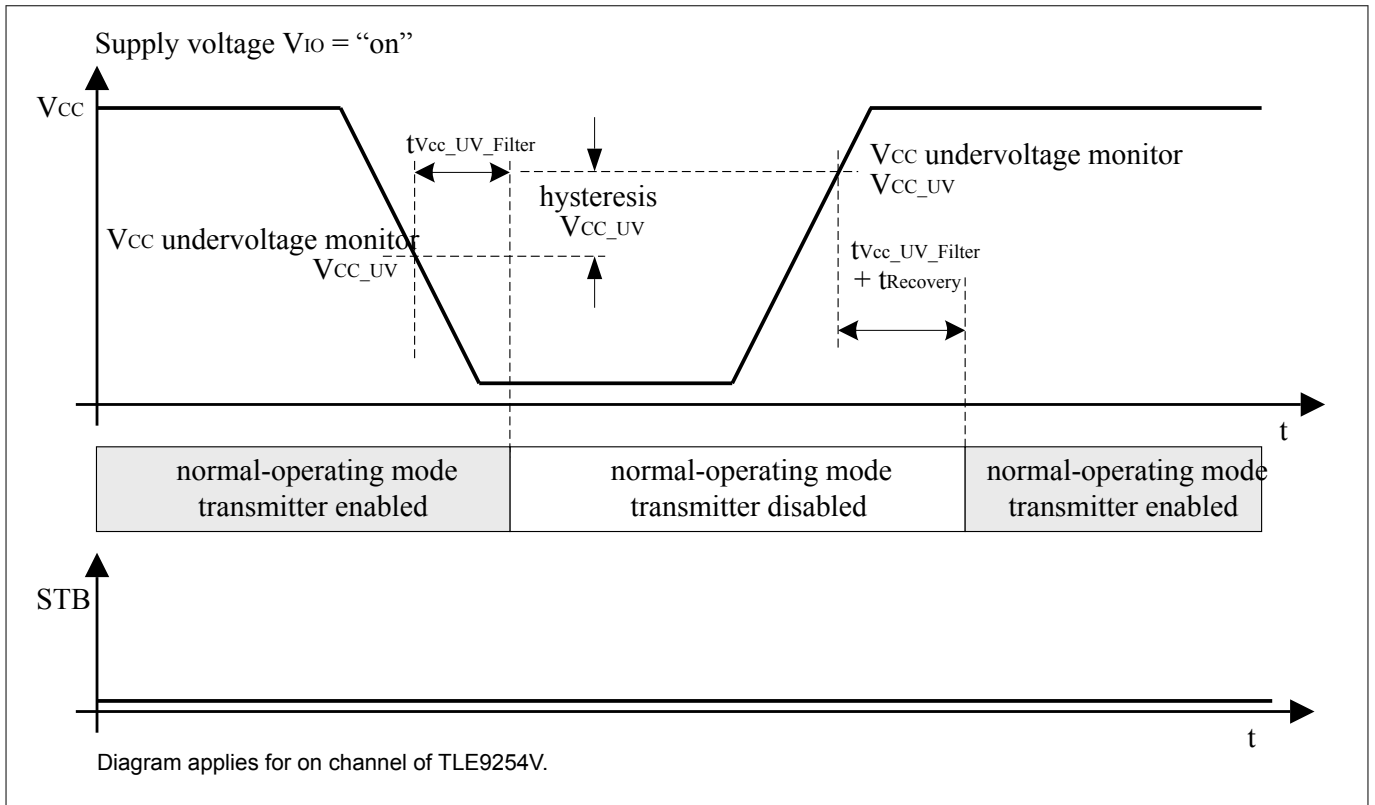


**Figure 11** Overtemperature protection

**6.5 Undervoltage detection on  $V_{CC}$**

If  $V_{CC} < V_{CC\_UV}$ , then the affected channel might not be able to provide the correct bus levels on the CANH and CANL output pins. To avoid any interference with the network the TLE9254V disables the transmitter of the affected channel (see [Figure 12](#)). If  $V_{CC}$  has recovered ( $V_{CC} > V_{CC\_UV}$ ) for more than the glitch filter time  $t_{Filter}$  AND if the  $t_{Recovery}$  time has expired, then the TLE9254V enables the transmitter.

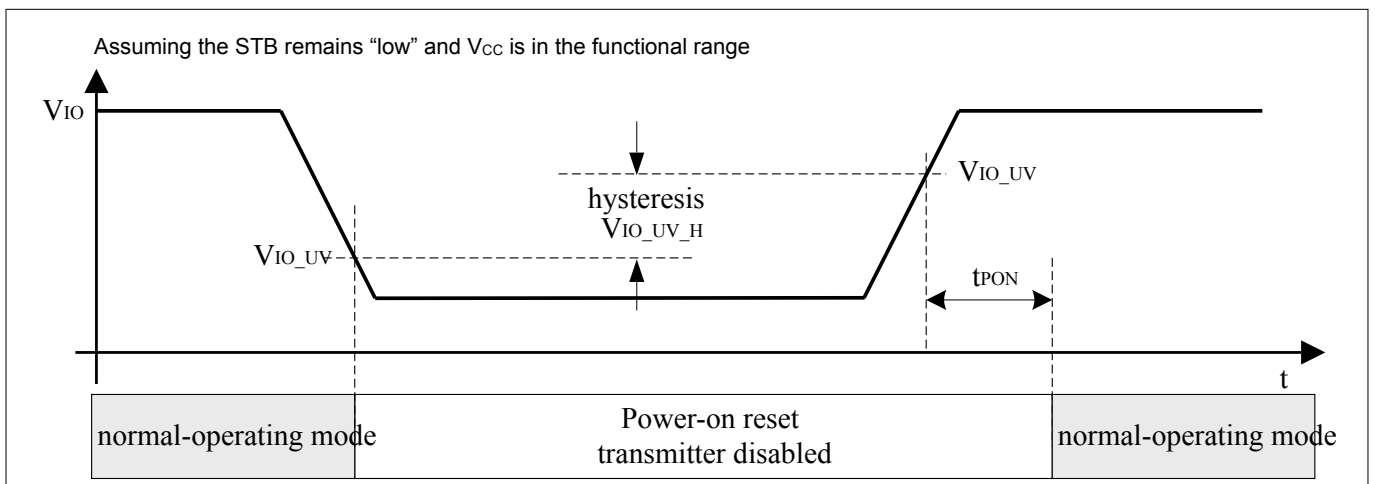
**Fail-safe functions**



**Figure 12** **V<sub>CC</sub> undervoltage**

**6.6 Undervoltage detection on V<sub>IO</sub>**

If  $V_{IO} < V_{IO\_UV}$ , the TLE9254V is not supplied anymore. The TLE9254V reacts as described in [Power-on reset](#) (see [Power-on reset](#)). If  $V_{IO}$  has recovered ( $V_{IO} > V_{IO\_UV}$ ) and  $t_{PON}$  time has expired, then the TLE9254V is fully functional. [Figure 13](#) shows the undervoltage detection for  $V_{IO}$ .



**Figure 13** **V<sub>IO</sub> undervoltage**

## **6.7 Delay time for mode change**

The HS CAN transceiver TLE9254V changes the mode of operation within the time window  $t_{Mode}$ . During the mode change the TLE9254V sets the RxD output pin permanently to "high", so RxD does not reflect the status on the CANH and CANL input pins then. After the mode change is completed, the TLE9254V releases the RxD output pin.

**Electrical characteristics**

**7 Electrical characteristics**

Electrical parameters described within this chapter apply for each channel of TLE9254V.

**7.1 Electrical characteristics general timing parameters**

**Table 6 Electrical characteristics general timing parameters**

$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ;  $V_{IO} = 3.0\text{ V to }5.5\text{ V}$ ;  $R_L = 60\ \Omega$ ;  $T_j = -40^\circ\text{C to }150^\circ\text{C}$ ;  
 all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Power up delay time	$t_{PON}$	–	–	110	$\mu\text{s}$	–	P_8.1.2
Delay time for mode change	$t_{Mode}$	–	–	20	$\mu\text{s}$	–	P_8.1.3
TxD permanent dominant timeout	$t_{TxD\_TO}$	1	–	4	ms	Normal-operating mode, see <b>TxD timeout feature</b>	P_8.1.4

**7.2 Electrical characteristics power supply interface**

**7.2.1 Electrical characteristics current consumption**

**Table 7 Electrical characteristics current consumption**

$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ;  $V_{IO} = 3.0\text{ V to }5.5\text{ V}$ ;  $R_L = 60\ \Omega$ ;  $T_j = -40^\circ\text{C to }150^\circ\text{C}$ ;  
 all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
<b>Normal-operating mode</b>							
$V_{CC}$ supply current dominant bus signal	$I_{CC\_NM\_D}$	–	33	48	mA	dominant state, $V_{TxD} = V_{STB} = 0\text{ V}$ <sup>6)</sup>	P_8.2.1
$V_{CC}$ supply current recessive bus signal	$I_{CC\_NM\_R}$	–	2.0	2.5	mA	recessive state, $V_{TxD} = V_{IO}$ $V_{STB} = 0\text{ V}$ <sup>6)</sup>	P_8.2.2
$V_{IO}$ supply current (both transceivers together)	$I_{IO\_NM\_R}$	–	–	2.2	mA	$V_{STB} = 0\text{ V}$ , recessive state	P_8.2.3

**Stand-by Mode**

<sup>6)</sup> Applies for one channel of TLE9254V.

**Electrical characteristics**

**Table 7 Electrical characteristics current consumption (continued)**

$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ;  $V_{IO} = 3.0\text{ V to }5.5\text{ V}$ ;  $R_L = 60\ \Omega$ ;  $T_j = -40^\circ\text{C to }150^\circ\text{C}$ ;  
 all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
$V_{IO}$ supply current (both transceivers together)	$I_{IO\_STB}$	–	10	22	$\mu\text{A}$	$V_{TxD} = V_{STB} = V_{IO}$	P_8.2.6
$V_{IO}$ supply current (both transceivers together)	$I_{IO\_STB}$	–	8	12	$\mu\text{A}$	$V_{TxD} = V_{STB} = V_{IO}$ ; $T_J < 105^\circ\text{C}^{7)}$	P_8.2.7
$V_{CC}$ leakage current (both transceivers together)	$I_{CC\_STB}$	–	–	5	$\mu\text{A}$	$V_{TxD} = V_{STB} = V_{IO}$	P_8.2.8

**7.2.2 Electrical characteristics undervoltage detection**

**Table 8 Electrical characteristics undervoltage detection**

$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ;  $V_{IO} = 3.0\text{ V to }5.5\text{ V}$ ;  $R_L = 60\ \Omega$ ;  $T_j = -40^\circ\text{C to }150^\circ\text{C}$ ;  
 all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
<b>Undervoltage detection</b>							
Undervoltage detection threshold	$V_{CC\_UV}$	3.8	4.25	4.5	V	–	P_8.2.9
Undervoltage detection threshold	$V_{IO\_UV}$	2.0	2.6	3.0	V	–	P_8.2.11
Undervoltage glitch filter	$t_{VCC\_UV\_Filter}$	–	–	10	$\mu\text{s}$	see <a href="#">Figure 12</a>	P_8.2.13
Undervoltage recovery time	$t_{Recovery}$	10	17	25	$\mu\text{s}$	see <a href="#">Figure 12</a>	P_8.2.14

**7.3 Electrical characteristics CAN controller interface**

**Table 9 Electrical characteristics CAN controller interface**

$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ;  $V_{IO} = 3.0\text{ V to }5.5\text{ V}$ ;  $R_L = 60\ \Omega$ ;  $T_j = -40^\circ\text{C to }150^\circ\text{C}$ ;  
 all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			

**Input pins: STB, TxD**

<sup>7</sup> Not subject to production test, specified by design.



**Electrical characteristics**

**Table 9 Electrical characteristics CAN controller interface (continued)**

$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ;  $V_{IO} = 3.0\text{ V to }5.5\text{ V}$ ;  $R_L = 60\ \Omega$ ;  $T_j = -40^\circ\text{C to }150^\circ\text{C}$ ;  
 all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
"High" level input range	$V_{IP\_H}$	$0.7 \times V_{IO}$	–	$V_{IO} + 0.3\text{V}$	V	–	P_8.3.1
"Low" level input range	$V_{IP\_L}$	-0.3V	–	$0.3 \times V_{IO}$	V	–	P_8.3.2
"High" level input current	$I_{IP\_H}$	-2.0	–	2.0	$\mu\text{A}$	$V_{IP} = V_{IO}$	P_8.3.3
"Low" level input current	$I_{IP\_L}$	-200	–	-20.0	$\mu\text{A}$	$V_{IP} = 0\text{ V}$	P_8.3.4
Input capacitance	$C_{IP}$	–	–	10	pF	<sup>8)</sup>	P_8.3.7

**Receiver output RxD**

"High" level output current	$I_{RXD\_H}$	–	-1.8	-1.0	mA	$V_{RXD} = V_{IO} - 0.4\text{ V}$ $V_{DIFF} < 0.5\text{ V}$	P_8.3.8
"Low" level output current	$I_{RXD\_L}$	1.0	2.0	–	mA	$V_{RXD} = 0.4\text{ V}$ $V_{DIFF} > 0.9\text{ V}$	P_8.3.9

**7.4 Electrical characteristics transmitter**

**Table 10 Electrical characteristics transmitter**

$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ;  $V_{IO} = 3.0\text{ V to }5.5\text{ V}$ ;  $R_L = 60\ \Omega$ ;  $T_j = -40^\circ\text{C to }150^\circ\text{C}$ ;  
 all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			

**Bus transmitter**

CANH, CANL recessive output voltage	$V_{CANL/H}$	2.0	2.4	3.0	V	Normal-operating mode, $V_{TXD} = V_{IO}$ no load	P_8.4.1
CANH, CANL recessive output voltage difference	$V_{Diff\_R\_NM} = V_{CANH} - V_{CANL}$	-50	–	50	mV	$V_{TXD} = V_{IO}$ no load	P_8.4.2
CANH dominant output voltage normal-operating mode	$V_{CANH}$	2.75	–	4.5	V	$V_{TXD} = 0\text{ V}$ , $50\ \Omega < R_L < 65\ \Omega$ ; $4.75\text{ V} < V_{CC} < 5.25\text{ V}$	P_8.4.3

<sup>8)</sup> Not subject to production test, specified by design.

**Electrical characteristics**

**Table 10 Electrical characteristics transmitter (continued)**

$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ;  $V_{IO} = 3.0\text{ V to }5.5\text{ V}$ ;  $R_L = 60\ \Omega$ ;  $T_j = -40^\circ\text{C to }150^\circ\text{C}$ ;

all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
CANL dominant output voltage normal-operating mode	$V_{CANL}$	0.5	–	2.25	V	$V_{TXD} = 0\text{ V}$ , $50\ \Omega < R_L < 65\ \Omega$ ; $4.75\text{ V} < V_{CC} < 5.25\text{ V}$	P_8.4.4
CANH dominant output voltage difference: $V_{Diff\_D} = V_{CANH} - V_{CANL}$ normal-operating mode	$V_{Diff\_D}$	1.5	1.8	2.5	V	$V_{TXD} = 0\text{ V}$ , $50\ \Omega < R_L < 65\ \Omega$ ; $4.75\text{ V} < V_{CC} < 5.25\text{ V}$	P_8.4.5
CANH dominant output voltage difference extended bus load $V_{Diff\_D} = V_{CANH} - V_{CANL}$ normal-operating mode	$V_{Diff\_D\_EXT\_BL}$	1.4	–	3.3	V	$V_{TXD} = 0\text{ V}$ , $R_L = 45\ \Omega < R_L < 70\ \Omega$ ; $4.75\text{ V} < V_{CC} < 5.25\text{ V}$	P_8.4.6
CANH, CANL dominant output voltage difference high extended bus load normal-operating mode $V_{Diff} = V_{CANH} - V_{CANL}$	$V_{Diff\_D\_HEXT\_BL}$	1.5	–	5.0	V	<sup>9)</sup> $V_{TXD} = 0\text{ V}$ , $R_L = 2240\ \Omega$ ; $4.75\text{ V} < V_{CC} < 5.25\text{ V}$ ; static behavior	P_8.4.7
CANH, CANL recessive output voltage stand-by mode	$V_{CANL\_H}$	-0.1	–	0.1	V	no load	P_8.4.8
CANH, CANL recessive output voltage difference stand-by mode	$V_{Diff\_STB}$	-0.2	–	0.2	V	no load	P_8.4.9
Driver symmetry $V_{SYM} = V_{CANH} + V_{CANL}$	$V_{SYM}$	$0.9 \times V_{CC}$	$1.0 \times V_{CC}$	$1.1 \times V_{CC}$	V	<sup>9) 10)</sup> $C_1 = 4.7\text{ nF}$	P_8.4.10
CANH short circuit current	$I_{CANHSC}$	-115	-80	5	mA	$-3\text{ V} < V_{CANHshort} < 18\text{ V}$ ; $t < t_{TXD\_TO}$ ; $V_{TXD} = 0\text{ V}$	P_8.4.11

<sup>9</sup> Not subject to production test, specified by design.

<sup>10</sup>  $V_{SYM}$  is observed during dominant and recessive state and also during the transition from dominant to recessive and vice versa, while TxD is stimulated by a square wave signal with a frequency of 1 MHz.

**Electrical characteristics**

**Table 10 Electrical characteristics transmitter (continued)**

$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ;  $V_{IO} = 3.0\text{ V to }5.5\text{ V}$ ;  $R_L = 60\ \Omega$ ;  $T_j = -40^\circ\text{C to }150^\circ\text{C}$ ;  
 all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
CANL short circuit current	$I_{CANLSC}$	-5	80	115	mA	$-3\text{ V} < V_{CANLshort} < 18\text{ V}$ ; $t < t_{TXD\_TO}$ ; $V_{TXD} = 0\text{ V}$	P_8.4.12
CANH leakage current	$I_{CANH\_Ik}$	-3	-	3	$\mu\text{A}$	$V_{CC} = 0\text{ V}$ ; $0\text{ V} < V_{CANH} < 5\text{ V}$ ; $V_{CANH} = V_{CANL}$	P_8.4.14
CANL leakage current	$I_{CANL\_Ik}$	-3	-	3	$\mu\text{A}$	$V_{CC} = 0\text{ V}$ ; $0\text{ V} < V_{CANL} < 5\text{ V}$ ; $V_{CANH} = V_{CANL}$	P_8.4.15
CANH, CANL output voltage difference slope, recessive to dominant	$V_{diff\_slope\_rd}$	-	-	70	V/ $\mu\text{s}$	30% to 70% of measured differential bus voltage; $C_L = 100\text{ pF}$ ; $R_L = 60\ \Omega$ ; $4.75\text{ V} < V_{CC} < 5.25\text{ V}$ <sup>9)</sup>	P_8.4.16
CANH, CANL output voltage difference slope, dominant to recessive	$V_{diff\_slope\_dr}$	-	-	70	V/ $\mu\text{s}$	30% to 70% of measured differential bus voltage; $C_L = 100\text{ pF}$ ; $R_L = 60\ \Omega$ ; $4.75\text{ V} < V_{CC} < 5.25\text{ V}$ <sup>9)</sup>	P_8.4.17

**7.5 Electrical characteristics receiver**

**Table 11 Electrical characteristics receiver**

$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ;  $V_{IO} = 3.0\text{ V to }5.5\text{ V}$ ;  $R_L = 60\ \Omega$ ;  $T_j = -40^\circ\text{C to }150^\circ\text{C}$ ;  
 all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			

**Bus receiver**

<sup>9)</sup> Not subject to production test, specified by design.

**Electrical characteristics**

**Table 11 Electrical characteristics receiver (continued)**

$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ;  $V_{IO} = 3.0\text{ V to }5.5\text{ V}$ ;  $R_L = 60\ \Omega$ ;  $T_j = -40^\circ\text{C to }150^\circ\text{C}$ ;  
 all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Common mode Voltage Range	$V_{CMR}$	-12	-	12	V	-	P_8.5.1
Differential range dominant normal-operating mode	$V_{Diff\_D\_Range}$	0.9	-	8.0	V	<sup>11)</sup> $V_{CMR}$	P_8.5.3
Differential range recessive normal-operating mode	$V_{Diff\_R\_Range}$	-3.0	-	0.5	V	<sup>11)</sup> $V_{CMR}$	P_8.5.5
Single ended internal resistance	$R_{CAN\_H}$ , $R_{CAN\_L}$	6	-	50	k $\Omega$	recessive state, $-2\text{ V} < V_{CANH} < 7\text{ V}$ ; $-2\text{ V} < V_{CANL} < 7\text{ V}$	P_8.5.7
Differential internal resistance	$R_{Diff}$	12	-	100	k $\Omega$	recessive state, $-2\text{ V} < V_{CANH} < 7\text{ V}$ ; $-2\text{ V} < V_{CANL} < 7\text{ V}$	P_8.5.8
Input resistance deviation between CANH and CANL	$\Delta R_i$	-3.0	-	3.0	%	<sup>11)</sup> recessive state, $V_{CANH} = V_{CANL} = 5\text{ V}$	P_8.5.9
Input capacitance CANH, CANL versus GND	$C_{In}$	-	30	40	pF	recessive state <sup>12)</sup>	P_8.5.10
Differential input capacitance	$C_{InDiff}$	-	2	8	pF	recessive state <sup>12)</sup>	P_8.5.11

**7.6 Electrical characteristics dynamic transceiver parameters**

**Table 12 Electrical characteristics propagation delay**

$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ;  $V_{IO} = 3.0\text{ V to }5.5\text{ V}$ ;  $R_L = 60\ \Omega$ ;  $T_j = -40^\circ\text{C to }150^\circ\text{C}$ ;  
 all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
<b>Propagation delay</b>							
Propagation delay, TxD to RxD	$t_{Loop}$	80	200	235	ns	$C_L = 100\text{ pF}$ ; $C_{RxD} = 15\text{ pF}$	P_8.6.1

<sup>11</sup> Not subject to production test, specified by design.

<sup>12</sup> Not subject to production test, specified by design, S2P -Method;  $f = 10\text{ MHz}$ .

**Electrical characteristics**

**Table 12 Electrical characteristics propagation delay (continued)**

$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ;  $V_{IO} = 3.0\text{ V to }5.5\text{ V}$ ;  $R_L = 60\ \Omega$ ;  $T_j = -40^\circ\text{C to }150^\circ\text{C}$ ;

all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Propagation delay, TxD to bus ("low" to dominant)	$t_{d(L),T}$	30	110	140	ns	$C_L = 100\text{ pF}$ ; $C_{RxD} = 15\text{ pF}$	P_8.6.2
Propagation delay, TxD to bus ("high" to recessive)	$t_{d(H),T}$	30	110	140	ns	$C_L = 100\text{ pF}$ ; $C_{RxD} = 15\text{ pF}$	P_8.6.3
Propagation delay, bus to RxD (dominant to "low")	$t_{d(L),R}$	30	90	140	ns	$C_L = 100\text{ pF}$ ; $C_{RxD} = 15\text{ pF}$	P_8.6.4
Propagation delay, bus to RxD (recessive to "high")	$t_{d(H),R}$	30	90	140	ns	$C_L = 100\text{ pF}$ ; $C_{RxD} = 15\text{ pF}$	P_8.6.5

**Electrical characteristics**

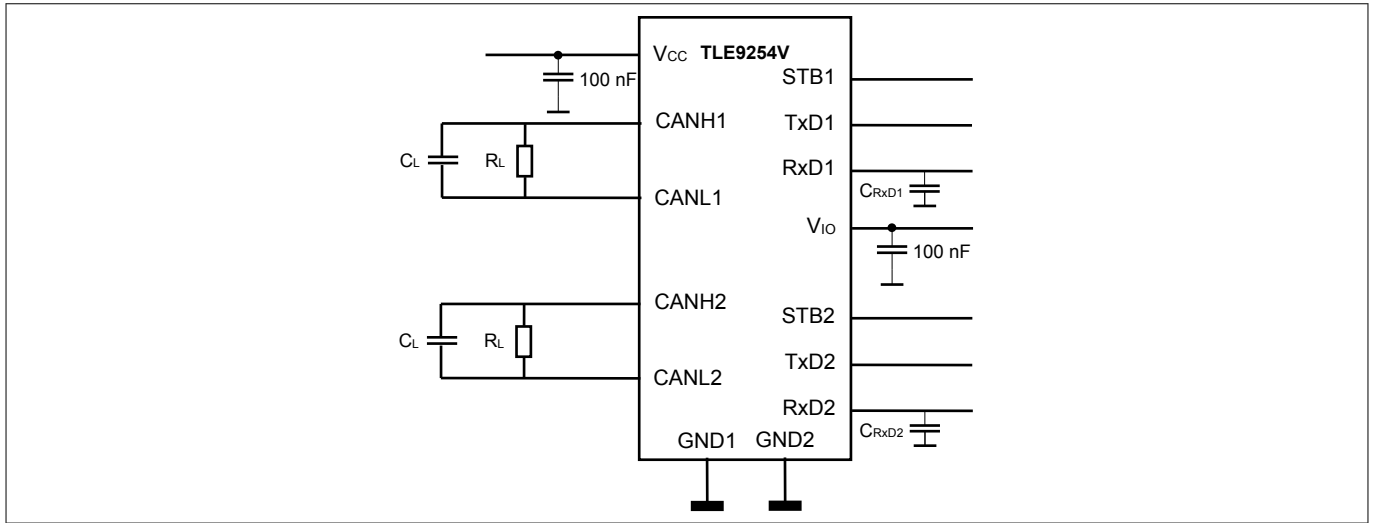
**Table 13 Electrical characteristics CAN FD**

$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ;  $V_{IO} = 3.0\text{ V to }5.5\text{ V}$   $R_L = 60\ \Omega$ ;  $T_j = -40^\circ\text{C to }150^\circ\text{C}$ ;

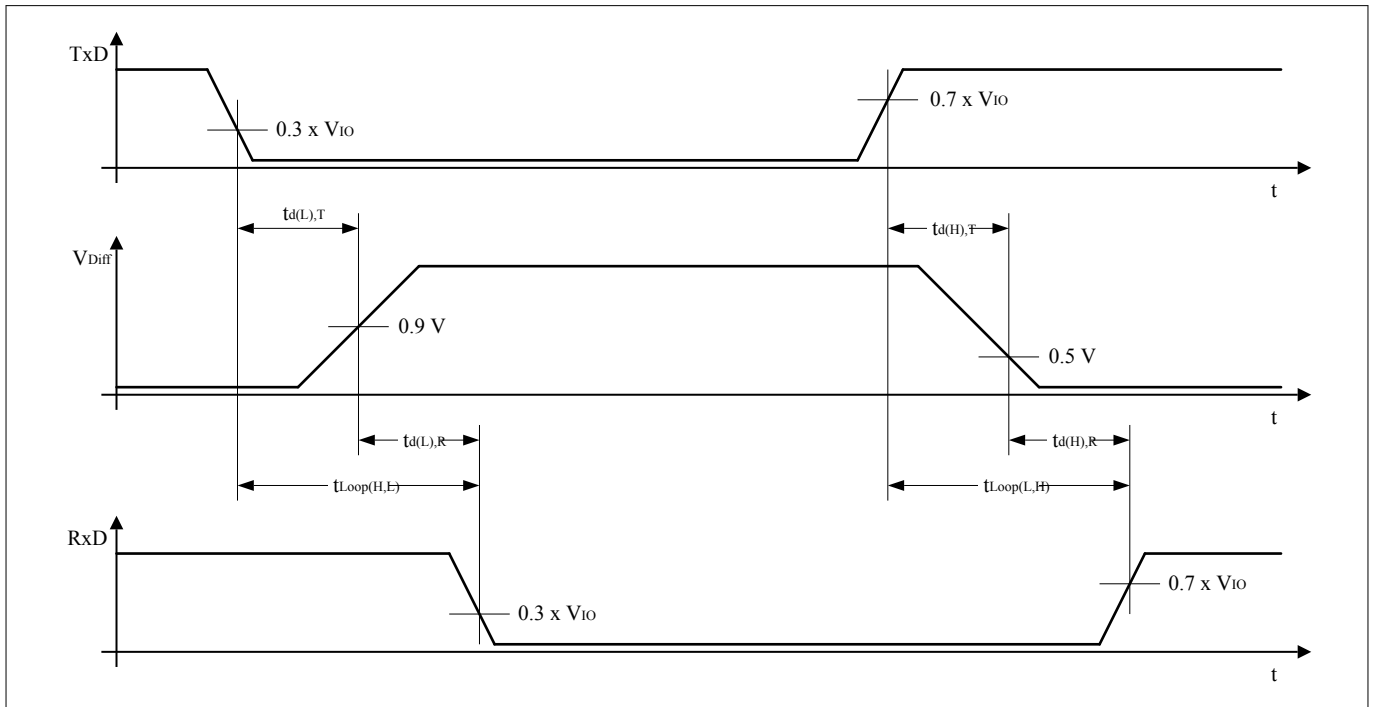
all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
<b>CAN FD</b>							
Received recessive bit width at 2 MBit/s	$t_{\text{Bit(RxD)}\_2\text{M}}$	400	500	550	ns	$C_L = 100\text{ pF}$ ; $C_{\text{RxD}} = 15\text{ pF}$ ; $t_{\text{Bit}} = 500\text{ ns}$ (see <a href="#">Figure 16</a> )	P_8.6.6
Transmitted recessive bit width at 2 MBit/s	$t_{\text{Bit(Bus)}\_2\text{M}}$	435	500	530	ns	$C_L = 100\text{ pF}$ ; $C_{\text{RxD}} = 15\text{ pF}$ ; $t_{\text{Bit}} = 500\text{ ns}$ (see <a href="#">Figure 16</a> )	P_8.6.7
Receiver timing symmetry at 2 MBit/s $\Delta t_{\text{Rec}_2\text{M}} = t_{\text{Bit(RxD)}\_2\text{M}} - t_{\text{Bit(Bus)}\_2\text{M}}$	$\Delta t_{\text{Rec}_2\text{M}}$	-65	-	40	ns	$C_L = 100\text{ pF}$ ; $C_{\text{RxD}} = 15\text{ pF}$ ; $t_{\text{Bit}} = 500\text{ ns}$ (see <a href="#">Figure 16</a> )	P_8.6.8
Received recessive bit width at 5 MBit/s	$t_{\text{Bit(RxD)}\_5\text{M}}$	120	200	220	ns	$C_L = 100\text{ pF}$ ; $C_{\text{RxD}} = 15\text{ pF}$ ; $t_{\text{Bit}} = 200\text{ ns}$ $4.75\text{ V} < V_{CC} < 5.5\text{ V}$ (see <a href="#">Figure 16</a> )	P_8.6.9
Received recessive bit width at 5 MBit/s	$t_{\text{Bit(Bus)}\_5\text{M}}$	155	200	210	ns	$C_L = 100\text{ pF}$ ; $C_{\text{RxD}} = 15\text{ pF}$ ; $t_{\text{Bit}} = 200\text{ ns}$ $4.75\text{ V} < V_{CC} < 5.5\text{ V}$ (see <a href="#">Figure 16</a> )	P_8.6.10
Receiver timing symmetry at 5 MBit/s $\Delta t_{\text{Rec}_5\text{M}} = t_{\text{Bit(RxD)}\_5\text{M}} - t_{\text{Bit(Bus)}\_5\text{M}}$	$\Delta t_{\text{Rec}_5\text{M}}$	-45	-	15	ns	$C_L = 100\text{ pF}$ ; $C_{\text{RxD}} = 15\text{ pF}$ ; $t_{\text{Bit}} = 200\text{ ns}$ $4.75\text{ V} < V_{CC} < 5.5\text{ V}$ (see <a href="#">Figure 16</a> )	P_8.6.11

**Electrical characteristics**

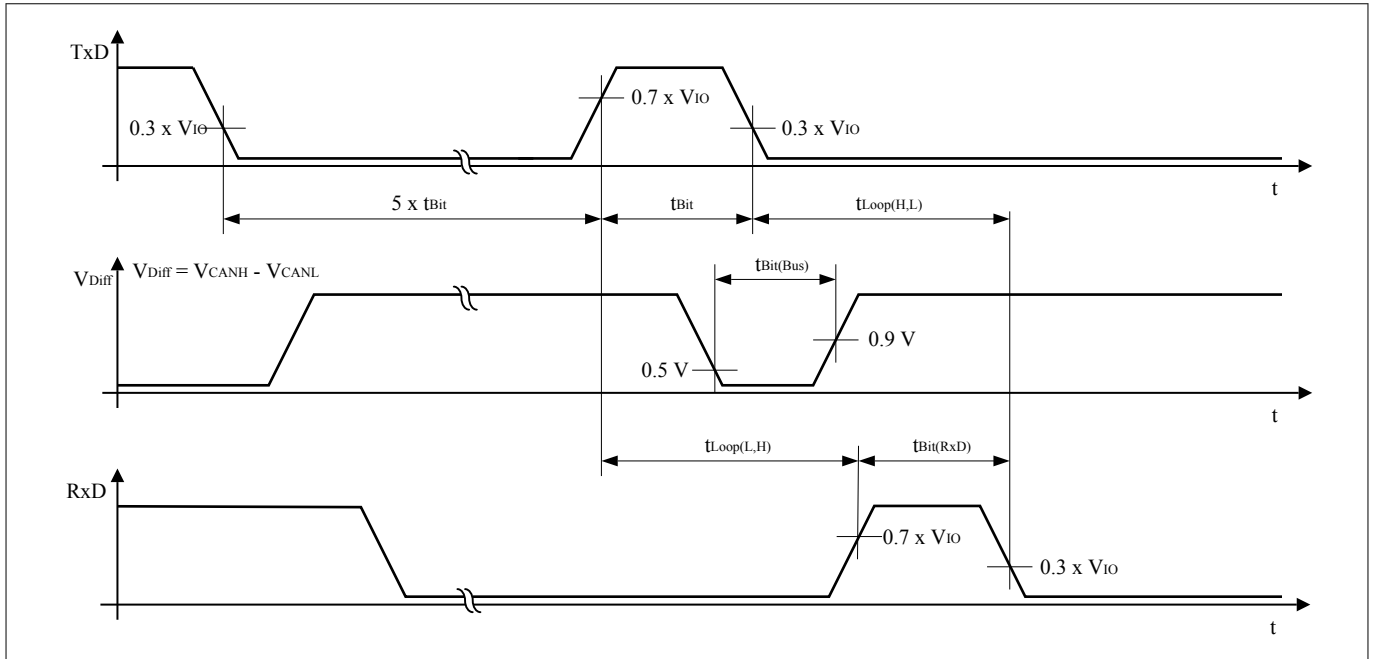


**Figure 14** Test circuit for dynamic characteristics



**Figure 15** Timing diagram for dynamic characteristics

**Electrical characteristics**



**Figure 16** Recessive bit time for five dominant bits followed by one recessive bit

**7.7 Electrical characteristics wake-up pattern detection**

**Table 14** Electrical characteristics wake-up pattern detection

$V_{CC} = 4.75\text{ V to }5.25\text{ V}$ ;  $V_{IO} = 3.0\text{ V to }5.5\text{ V}$ ;  $R_L = 60\ \Omega$ ;  $T_j = -40^\circ\text{C to }150^\circ\text{C}$ ;  
 all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Differential range dominant low power modes	$V_{Diff\_D\_STB\_Range}$	1.15	–	8.0	V	<sup>13)</sup> $V_{CMR}$	P_8.7.1
Differential range recessive low power modes	$V_{Diff\_R\_STB\_Range}$	-3.0	–	0.4	V	<sup>13)</sup> $V_{CMR}$	P_8.7.3
CAN activity filter time	$t_{Filter}$	0.5	–	1.8	$\mu\text{s}$	Figure 8	P_8.7.6
Bus wake-up timeout	$t_{WAKE}$	0.8	–	10.0	ms	Figure 8	P_8.7.7
Bus wake-up delay time	$t_{WU}$	–	–	5.0	$\mu\text{s}$	stand-by mode, Figure 9	P_8.7.8

<sup>13)</sup> Not subject to production test, specified by design.



## 8 Application information

### 8.1 ESD robustness according to IEC 61000-4-2

Tests for ESD robustness according to IEC 61000-4-2 "Gun test" (150 pF, 330  $\Omega$ ) have been performed. The results and test conditions are available in a separate test report.

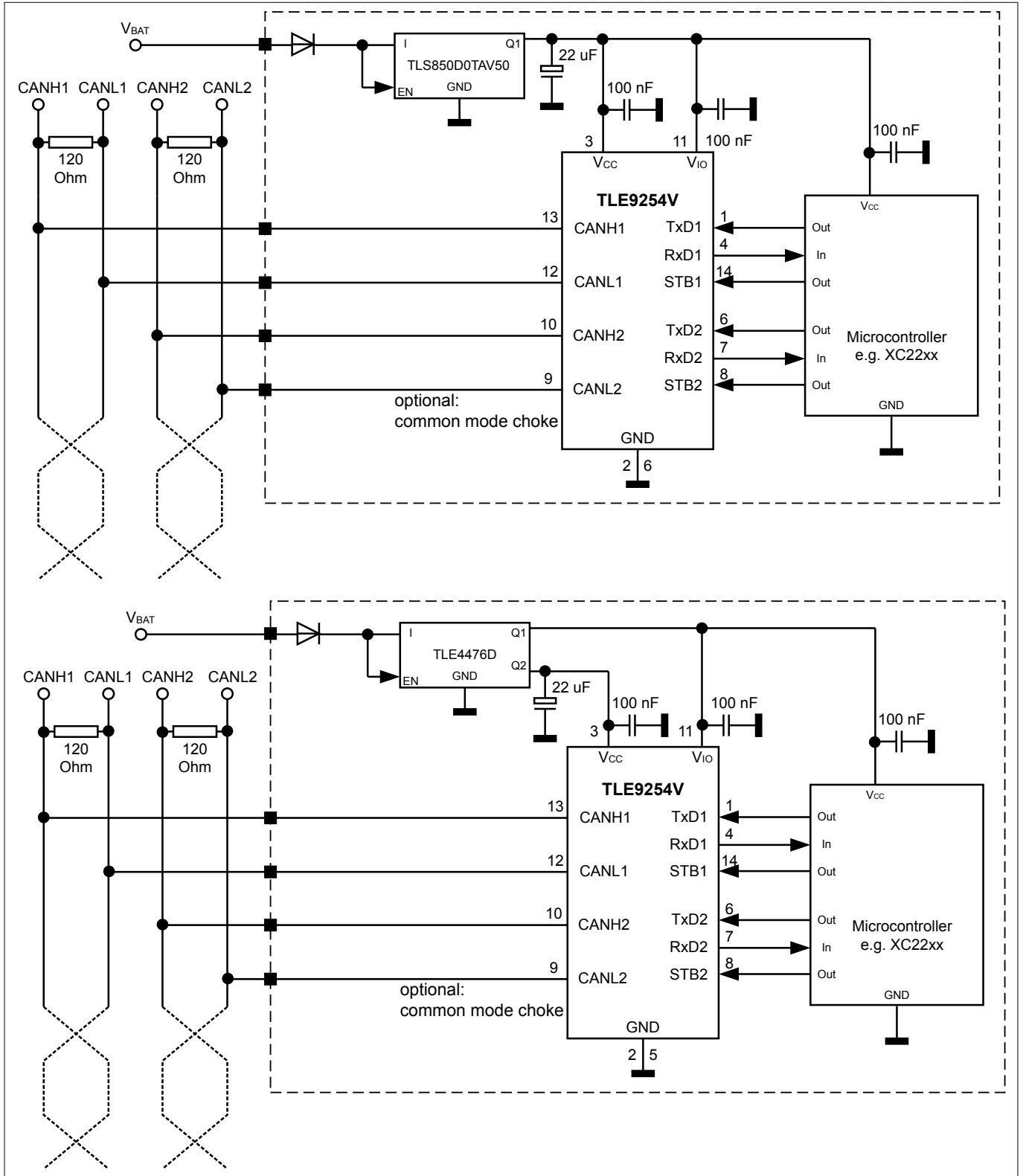
**Table 15 ESD robustness according to IEC61000-4-2**

Performed Test	Result	Unit	Remarks
Electrostatic discharge voltage at pin CANH and CANL versus GND	$\geq +8$	kV	<sup>14)</sup> Positive pulse
Electrostatic discharge voltage at pin CANH and CANL versus GND	$\leq -8$	kV	<sup>14)</sup> Negative pulse

<sup>14</sup> ESD susceptibility "ESD GUN" according to GIFT / ICT paper: "EMC Evaluation of CAN Transceivers, version 03/02/IEC TS62228", section 4.3. (DIN EN 61000-4-2), Tested by external facility IBEE Zwickau.

**Application information**

**8.2 Application example**



**Figure 17 Application circuit**

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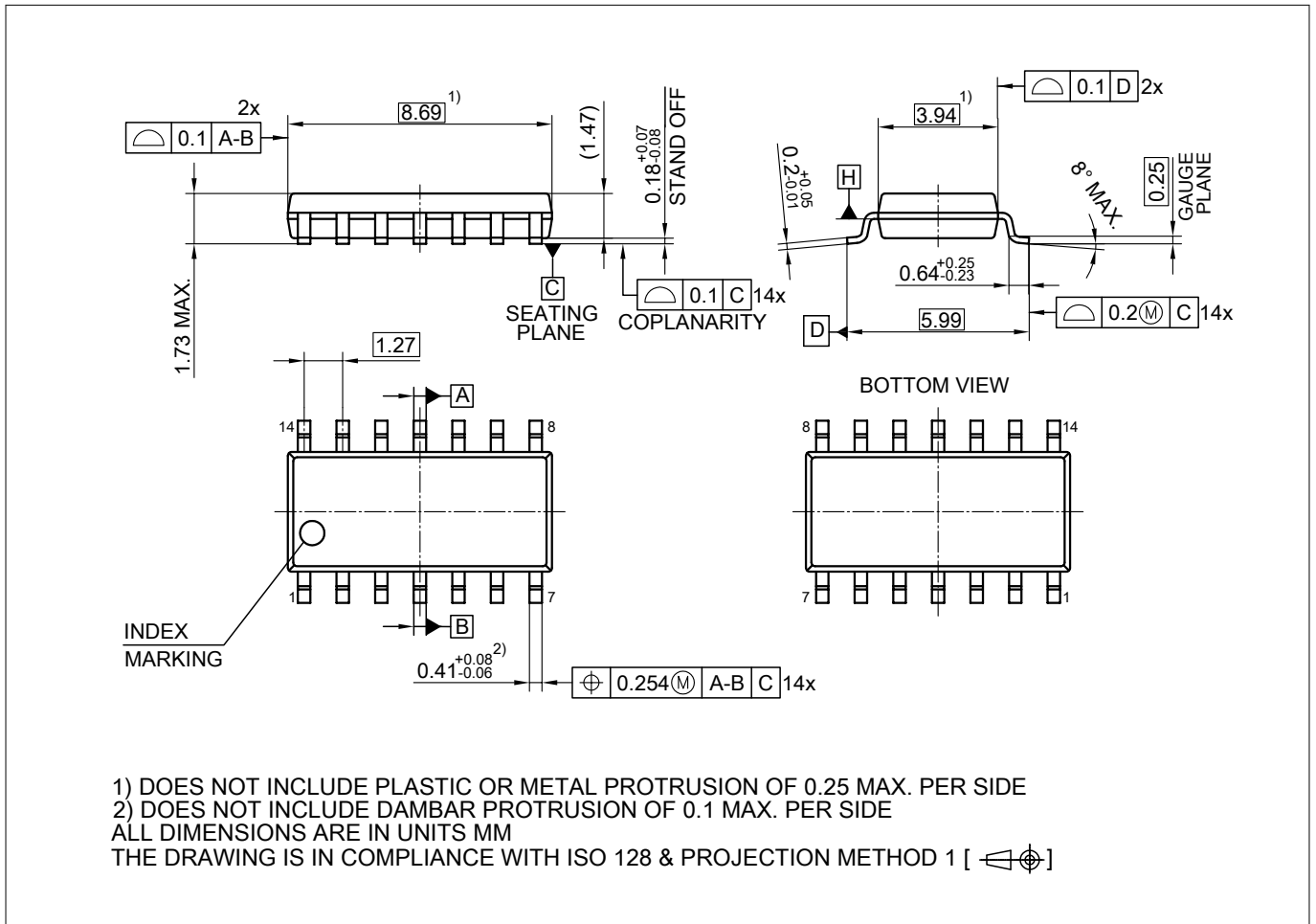
**Application information**

### **8.3 Further application information**

- Please contact us for information regarding the pin FMEA.
- For further information please visit: [www.infineon.com/transceiver](http://www.infineon.com/transceiver)

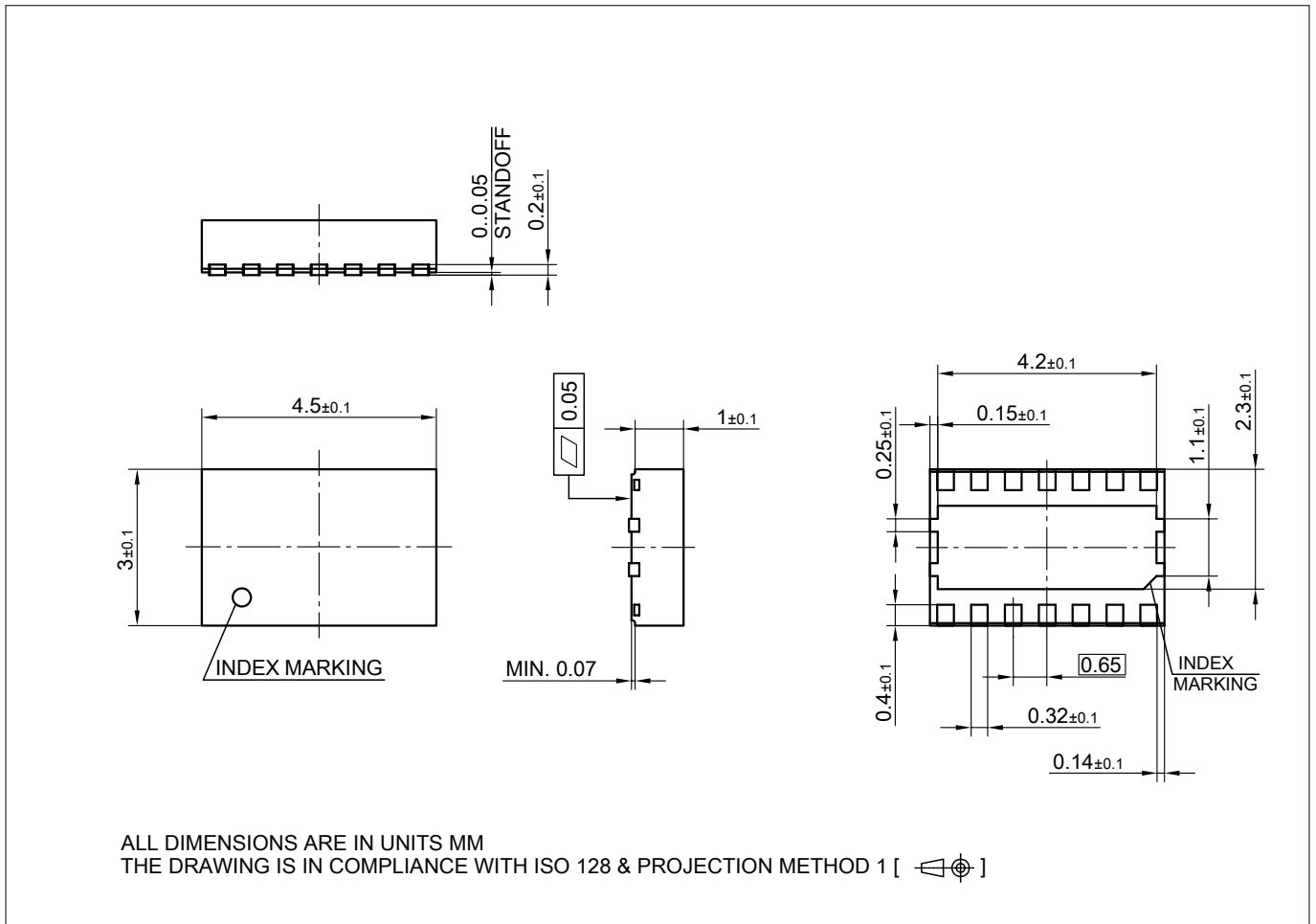
**Package information**

**9 Package information**



**Figure 18 PG-DSO-14**

**Package information**



**Figure 19**      **PG-TSON-14**

**Green Product (RoHS compliant)**

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

**Information on alternative packages**

Please visit [www.infineon.com/packages](http://www.infineon.com/packages).

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**Revision history**

**Revision history**

<b>Revision</b>	<b>Date</b>	<b>Changes</b>
1.0	2019-10-16	Datasheet created

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