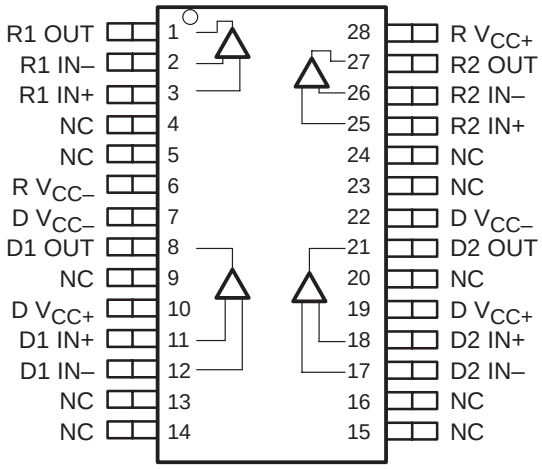
- **ADSL Differential Line Driver and Receiver**
- **Driver Features**
  - **140 MHz Bandwidth (–3dB) With 25-Ω Load**
  - **1300 V/μs Slew Rate, G = 5**
  - **400 mA Output Current Minimum Into 25-Ω Load**
  - **–72 dBc 3rd Order Harmonic Distortion at f = 1 MHz, 25-Ω Load, and 20 $V_{O(PP)}$**
- **Receiver Features**
  - **175 MHz Bandwidth (–3dB)**
  - **230 V/μs Slew Rate**
  - **–79 dBc Total Harmonic Distortion at f = 1 MHz, R_L 1 kΩ**
  - **Quiescent Current = 3.4 mA Per Channel**
- **Wide Supply Range ±4.5 V to ±16 V**
- **Available in the PowerPAD™ Package**

PWP PACKAGE
(TOP VIEW)



NC – No internal connection

description

The THS6007 contains two high-current, high-speed drivers and two low-power, high-speed receivers. These drivers and receivers can be configured differentially for driving and receiving signals over low-impedance lines. The THS6007 is ideally suited for asymmetrical digital subscriber line (ADSL) applications where it supports the high-peak voltage and current requirements of that application. The drivers are current feedback amplifiers designed for the high slew rates necessary to support low total harmonic distortion (THD) in ADSL applications. The receivers are traditional voltage feedback amplifiers designed for maximum flexibility while consuming only 3.4 mA per channel quiescent current. Separate power supply connections for each driver and both receivers are provided to minimize crosstalk.

The THS6007 is packaged in the patented PowerPAD™ package. This package provides outstanding thermal characteristics in a small footprint package, which is fully compatible with automated surface-mount assembly procedures. The exposed thermal pad on the underside of the package is in direct contact with the die. By simply soldering the pad to the PWB copper and using other thermal outlets, the heat is conducted away from the junction.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICE	EVALUATION MODULE
	PowerPAD™ TSSOP† (PWP)	
0°C to 70°C	THS6007CPWP	THS6007EVM
–40°C to 85°C	THS6007IPWP	

† The PWP packages are available taped and reeled. Add an R suffix to the device type (i.e., THS6007PWPR)

CAUTION: The THS6007 provides ESD protection circuitry. However, permanent damage can still occur if this device is subjected to high-energy electrostatic discharges. Proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC+} to V_{CC-} . . . . . 33 V
Input voltage, V_I (driver and receiver) . . . . . $\pm V_{CC}$
Output current, I_O (driver) (see Note 1) . . . . . 800 mA
Output current, I_O (receiver) (see Note 1) . . . . . 150 mA
Differential input voltage, V_{ID} (driver and receiver) . . . . . ±4 V
Maximum junction temperature, T_J . . . . . 150°C
Continuous total power dissipation at (or below) T_A = 25°C (see Note 1) . . . . . 4.48 W
Operating free air temperature, T_A . . . . . –40°C to 85°C
Storage temperature, T_{stg} . . . . . –65°C to 125°C
Lead temperature, 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 300°C

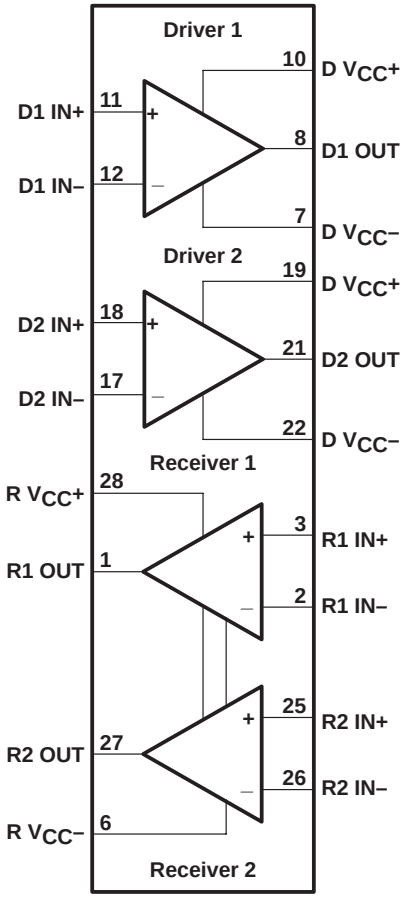
† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The THS6007 incorporates a PowerPad™ on the underside of the chip. This acts as a heatsink and must be connected to a thermal dissipation plane for proper power dissipation. Failure to do so can result in exceeding the maximum junction temperature, which could permanently damage the device. See the *Thermal Information* section of this document for more information about PowerPad™ technology.

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC+} and V_{CC-}	Split supply	±4.5		±16	V
	Single supply	9		32	
Operating free-air temperature, T_A		–40		85	°C

functional block diagram



DRIVER

electrical characteristics, V_{CC} = ±15 V, R_L = 25 Ω, R_F = 1 kΩ, T_A = 25°C (unless otherwise noted)

dynamic performance

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
BW	Small-signal bandwidth (–3 dB)	V_I = 200 mV, R_F = 680 Ω,	G = 1, R_L = 25 Ω	V_{CC} = ±15 V		140		MHz
		V_I = 200 mV, R_F = 1 kΩ,	G = 1, R_L = 25 Ω	V_{CC} = ±5 V		100		
		V_I = 200 mV, R_F = 620 Ω,	G = 2, R_L = 25 Ω	V_{CC} = ±15 V		120		
		V_I = 200 mV, R_L = 25 Ω,	G = 2, R_F = 820 Ω	V_{CC} = ±5 V		100		
		V_I = 200 mV, R_F = 820 Ω,	G = 1, R_L = 100 Ω	V_{CC} = ±15 V		315		
		V_I = 200 mV, R_F = 560 Ω,	G = 2, R_L = 100 Ω	V_{CC} = ±15 V		265		
	Bandwidth for 0.1 dB flatness	V_I = 200 mV,	G = 1	V_{CC} = ±5 V, R_F = 820 Ω		30		MHz
				V_{CC} = ±15 V, R_F = 680 Ω		40		
	Full power bandwidth†	V_{CC} = ±15 V,	$V_{O(PP)}$ = 20 V			20		MHz
		V_{CC} = ±5 V,	$V_{O(PP)}$ = 4 V			35		
SR	Slew rate‡	V_{CC} = ±15 V,	V_O = 20 $V_{(PP)}$,	G = 5		1300		V/μs
		V_{CC} = ±5 V,	V_O = 5 $V_{(PP)}$,	G = 2		900		
t_S	Settling time to 0.1%	0 V to 10 V Step,		G = 2		70		ns

† Full power bandwidth = slew rate/2π $V_{O(Peak)}$.
‡ Slew rate is measured from an output level range of 25% to 75%.

noise/distortion performance

PARAMETER			TEST CONDITIONS			MIN	TYP	MAX	UNIT
THD	Total harmonic distortion		V_{CC} = ±15 V, G = 2,	R_F = 680 Ω, f = 1 MHz	$V_{O(PP)}$ = 20 V		–65		dBc
					$V_{O(PP)}$ = 2 V		–79		
			V_{CC} = ±5 V, G = 2,	R_F = 680 Ω, f = 1 MHz	$V_{O(PP)}$ = 2 V		–76		
V_n	Input voltage noise		V_{CC} = ±5 V or ±15 V, G = 2,		f = 10 kHz, Single-ended		1.7		nV/√Hz
I_n	Input noise current	Positive (IN+)	V_{CC} = ±5 V or ±15 V, G = 2		f = 10 kHz,		11.5		pA/√Hz
		Negative (IN–)					16		
A_D	Differential gain error		G = 2, R_L = 150 Ω,	NTSC, 40 IRE Modulation	V_{CC} = ±5 V		0.04%		
					V_{CC} = ±15 V		0.05%		
ϕ_D	Differential phase error		G = 2, R_L = 150 Ω,	NTSC, 40 IRE Modulation	V_{CC} = ±5 V		0.07°		
					V_{CC} = ±15 V		0.08°		
	Crosstalk	Driver to driver	V_I = 200 mV,		f = 1 MHz		–62		dB

DRIVER

electrical characteristics, V_{CC} = ±15 V, R_L = 25 Ω, R_F = 1 kΩ, T_A = 25°C (unless otherwise noted) (continued)

dc performance

PARAMETER			TEST CONDITIONS†		MIN	TYP	MAX	UNIT
	Open loop transresistance		V_{CC} = ±5 V			1.5		MΩ
			V_{CC} = ±15 V			5		
V_{IO}	Input offset voltage		V_{CC} = ±5 V or ±15 V	T_A = 25°C		2	5	mV
				T_A = full range			7	
	Input offset voltage drift		V_{CC} = ±5 V or ±15 V,	T_A = full range		20		µV/°C
	Differential input offset voltage		V_{CC} = ±5 V or ±15 V	T_A = 25°C		1.5	4	mV
				T_A = full range			5	
I_{IB}	Input bias current	Negative	V_{CC} = ±5 V or ±15 V	T_A = 25°C		3	9	µA
				T_A = full range			12	
		Positive		T_A = 25°C		4	10	µA
				T_A = full range			12	
		Differential		T_A = 25°C		1.5	8	µA
				T_A = full range			11	
	Differential input offset voltage drift		V_{CC} = ±5 V or ±15 V,	T_A = full range		10		µV/°C

NOTE: Full range = –40°C to 85°C

input characteristics

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{ICR}	Common-mode input voltage range	V_{CC} = ±5 V		±3.6	±3.7		V
		V_{CC} = ±15 V		±13.4	±13.5		
CMRR	Common-mode rejection ratio	V_{CC} = ±5 V or ±15 V,	T_A = full range	62	70		dB
	Differential common-mode rejection ratio				100		
R_I	Input resistance				300		kΩ
C_I	Differential input capacitance				1.4		pF

NOTE: Full range = –40°C to 85°C

DRIVER

electrical characteristics, V_{CC} = ±15 V, R_L = 25 Ω, R_F = 1 kΩ, T_A = 25°C (unless otherwise noted) (continued)

output characteristics

PARAMETER			TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_O	Output voltage swing	Single ended	R_L = 25 Ω	V_{CC} = ±5 V	3 to −2.8	3.2 to −3		V
				V_{CC} = ±15 V	11.8 to −11.5	12.5 to −12.2		
		Differential	R_L = 50 Ω	V_{CC} = ±5 V	6 to −5.6	6.4 to −6		V
				V_{CC} = ±15 V	23.6 to −23	25 to −24.4		
I_O	Output current (see Note 2)		V_{CC} = ±5 V,	R_L = 5 Ω		500		mA
			V_{CC} = ±15 V,	R_L = 25 Ω	400	500		
I_{OS}	Short-circuit output current (see Note 2)					800		mA
R_O	Output resistance		Open loop			13		Ω

NOTE 2: A heat sink is required to keep the junction temperature below absolute maximum when an output is heavily loaded or shorted. See absolute maximum ratings and *Thermal Information* section.

power supply

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{CC}	Power supply operating range	Split supply		±4.5		±16.5	V
		Single supply		9		33	
I_{CC}	Quiescent current (each driver)	V_{CC} = ±5 V	T_A = full range			12	mA
		V_{CC} = ±15 V	T_A = 25°C		11.5	13	
			T_A = full range			15	
PSRR	Power supply rejection ratio	V_{CC} = ±5 V	T_A = 25°C	−68	−74		dB
			T_A = full range	−65			
		V_{CC} = ±15 V	T_A = 25°C	−64	−72		dB
			T_A = full range	−62			

NOTE: Full range = −40°C to 85°C

RECEIVER

electrical characteristics at T_A = 25°C, V_{CC} = ±15 V, R_L = 150 Ω (unless otherwise noted)

dynamic performance

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
BW	Small-signal bandwidth (–3 dB)	V_{CC} = ±15 V		Gain = 1		175		MHz
		V_{CC} = ±5 V				160		
		V_{CC} = ±15 V		Gain = –1		70		MHz
		V_{CC} = ±5 V				65		
	Bandwidth for 0.1 dB flatness	V_{CC} = ±15 V		Gain = 1		35		MHz
		V_{CC} = ±5 V				35		
	Full power bandwidth†	$V_{O(pp)}$ = 20 V,	V_{CC} = ±15 V			2.7		MHz
		$V_{O(pp)}$ = 5 V,	V_{CC} = ±5 V			7.1		
SR	Slew rate‡	V_{CC} = ±15 V,	20-V step	Gain = 5		230		V/µs
		V_{CC} = ±5 V,	5-V step	Gain = 1		170		
t_s	Settling time to 0.1%	V_{CC} = ±15 V,	5-V step	Gain = –1		43		ns
		V_{CC} = ±5 V,	2-V step			30		
	Settling time to 0.01%	V_{CC} = ±15 V,	5-V step	Gain = –1		233		ns
		V_{CC} = ±5 V,	2-V step			280		

† Full power bandwidth = slew rate/2π $V_{O(Peak)}$.
‡ Slew rate is measured from an output level range of 25% to 75%.

noise/distortion performance

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
THD	Total harmonic distortion	$V_{O(pp)}$ = 2 V, f = 1 MHz, Gain = 2	V_{CC} = ±15 V	R_L = 1 kΩ		–79		dBc
			V_{CC} = ±5 V	R_L = 1 kΩ		–77		
V_n	Input voltage noise	V_{CC} = ±5 V or ±15 V,	f = 10 kHz			10		nV/√Hz
I_n	Input current noise	V_{CC} = ±5 V or ±15 V,	f = 10 kHz			0.7		pA/√Hz
X_T	Receiver-to-receiver crosstalk	V_{CC} = ±5 V or ±15 V,	f = 1 MHz			–75		dB

dc performance

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Open loop gain	V_{CC} = ±15 V, V_O = ±10 V, R_L = 1 kΩ	T_A = 25°C	10	19		V/mV
			T_A = full range	9			
		V_{CC} = ±5 V, V_O = ±2.5 V, R_L = 250 Ω	T_A = 25°C	8	16		V/mV
			T_A = full range	7			
V_{OS}	Input offset voltage	V_{CC} = ±5 V or ±15 V	T_A = 25°C		1	7	mV
			T_A = full range			8	
	Offset voltage drift		T_A = full range		15		µV/°C
I_{IB}	Input bias current		T_A = 25°C		1.2	6	µA
			T_A = full range			8	
I_{OS}	Input offset current		T_A = 25°C		20	250	nA
			T_A = full range			400	
	Offset current drift	T_A = full range			0.3		nA/°C

NOTE: Full range = –40°C to 85°C

RECEIVER

electrical characteristics at T_A = 25°C, V_{CC} = ±15 V, R_L = 150 Ω (unless otherwise noted) (continued)

input characteristics

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{ICR}	Common-mode input voltage range	V_{CC} = ±15 V			±13.8	±14.1		V
		V_{CC} = ±5 V			±3.8	±3.9		
CMRR	Common mode rejection ratio	V_{CC} = ±15 V,	V_{ICR} = ±12 V,	T_A = full range	78	93		dB
		V_{CC} = ±5 V,	V_{ICR} = ±2 V,	T_A = full range	84	90		dB
R_I	Input resistance					1		MΩ
C_I	Input capacitance					1.5		pF

NOTE: Full range = –40°C to 85°C

output characteristics

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Output voltage swing	V_{CC} = ±15 V	R_L = 250 Ω	±12	±13.6		V
		V_{CC} = ±5 V	R_L = 150 Ω	±3.4	±3.8		
		V_{CC} = ±15 V	R_L = 1 kΩ	±13	±13.8		V
		V_{CC} = ±5 V		±3.5	±3.9		
I_O	Output current†	V_{CC} = ±15 V	R_L = 20 Ω	65	85		mA
		V_{CC} = ±5 V		50	70		
I_{SC}	Short-circuit current†	V_{CC} = ±15 V			100		mA
R_O	Output resistance	Open loop			13		Ω

† Observe power dissipation ratings to keep the junction temperature below the absolute maximum rating when the output is heavily loaded or shorted. See the absolute maximum ratings section of this data sheet for more information.

power supply

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage operating range	Dual supply		±4.5		±16.5	V
		Single supply		9		33	
I_{CC}	Supply current (per amplifier)	V_{CC} = ±15 V	T_A = 25°C		3.4	4.2	mA
			T_A = full range			5	
		V_{CC} = ±5 V	T_A = 25°C		2.9	3.7	
			T_A = full range			4.5	
PSRR	Power supply rejection ratio	V_{CC} = ±5 V or ±15 V	T_A = full range	79	90		dB

NOTE: Full range = –40°C to 85°C

PARAMETER MEASUREMENT INFORMATION

Figure 1. Driver Input-to-Output Crosstalk Test Circuit

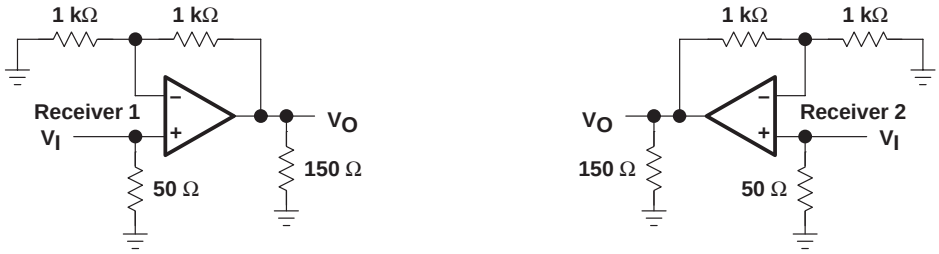


Figure 2. Receiver Input-to-Output Crosstalk Test Circuit

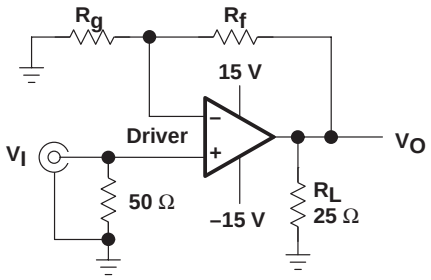


Figure 3. Driver Test Circuit, Gain = 1 + (R_f/R_g)

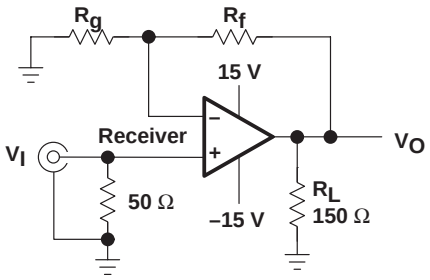


Figure 4. Receiver Test Circuit, Gain = 1 + (R_f/R_g)

TYPICAL CHARACTERISTICS

Table of Graphs

				FIGURE
	Peak-to-peak output voltage	Driver	vs Supply voltage	5
			vs Load resistance	6
V_{IO}	Input offset voltage	Driver	vs Free-air temperature	7
I_{IB}	Input bias current	Driver	vs Free-air temperature	8
CMMR	Common-mode rejection ratio	Driver	vs Free-air temperature	9
	Driver-to-driver crosstalk	Driver	vs Frequency	10
PSSR	Power supply rejection ratio	Driver	vs Free-air temperature	11
	Closed-loop output impedance	Driver	vs Frequency	12
I_{CC}	Supply current	Driver	vs Supply voltage	13
			vs Free-air temperature	14
SR	Slew rate	Driver	vs Output step	15, 16
V_n	Input voltage and current noise	Driver	vs Frequency	17
	Normalized frequency response	Driver	vs Frequency	18, 19
	Output amplitude	Driver	vs Frequency	20 – 23
	Normalized output response	Driver	vs Frequency	24 – 27
	Small and large signal frequency response	Driver		28, 29
	Single-ended harmonic distortion	Driver	vs Frequency	30, 31
		Driver	vs Output voltage	32, 33
	Differential gain and phase	Driver	vs DC input offset voltage	34, 35
			vs Number of 150-Ω loads	36, 37
	400-mV step response	Driver		38
	10-V step response	Driver		39
	20-V step response	Driver		40
	Driver-to-receiver crosstalk	Receiver	vs Frequency	41
	Receiver-to-driver crosstalk	Receiver	vs Frequency	42
	Power supply rejection ratio	Receiver	vs Frequency	43
	Open loop gain and phase response	Receiver	vs Frequency	44
	Receiver-to-receiver crosstalk	Receiver	vs Frequency	45
THD	Total harmonic distortion	Receiver	vs Frequency	46, 47
	Settling	Receiver	vs Output step	48
PSSR	Power supply rejection ratio	Receiver	vs Frequency	49
	Distortion	Receiver	vs Output voltage	50, 51
			vs Frequency	52 – 55
	Output amplitude	Receiver	vs Frequency	56 – 67
	2-V step response	Receiver		68, 70
	5-V step response	Receiver		69
	20-V step response	Receiver		71
V_{IO}	Input offset voltage	Receiver	vs Free-air temperature	72
I_{IB}	Input bias current	Receiver	vs Free-air temperature	73
V_O	Output voltage	Receiver	vs Supply voltage	74
			vs Free-air temperature	75
V_{ICR}	Common-mode input voltage	Receiver	vs Supply voltage	76
I_{CC}	Supply current	Receiver	vs Supply voltage	77
V_n, I_n	Voltage and current noise	Receiver	vs Frequency	78

TYPICAL CHARACTERISTICS (DRIVER)

PEAK-TO-PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

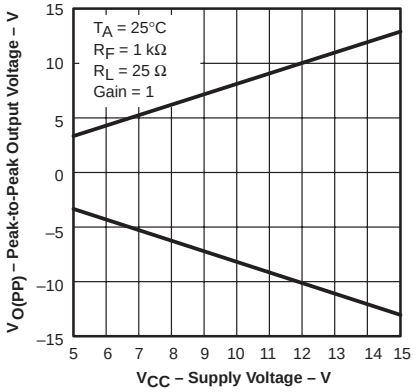


Figure 5

PEAK-TO-PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

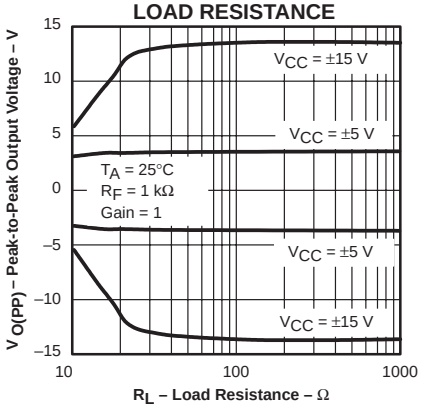


Figure 6

INPUT OFFSET VOLTAGE vs FREE-AIR TEMPERATURE

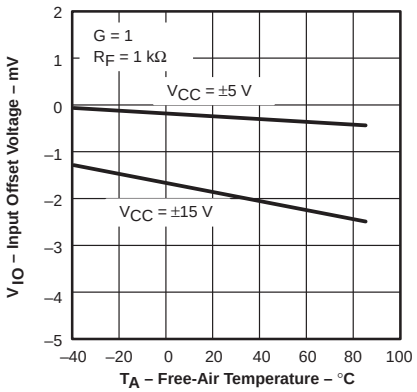


Figure 7

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

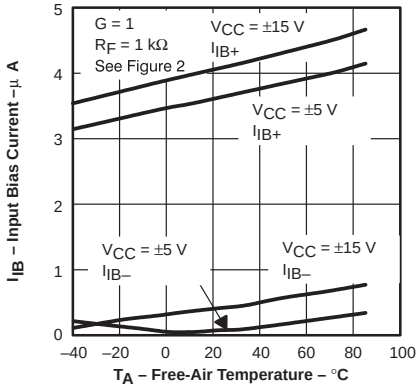


Figure 8

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

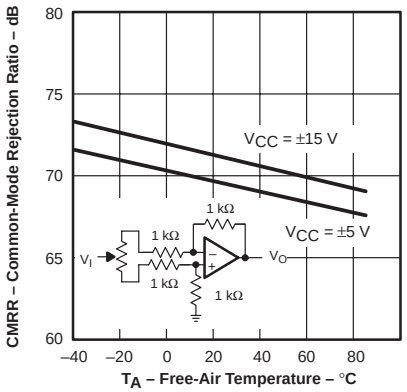


Figure 9

DRIVER-TO-DRIVER CROSSTALK vs FREQUENCY

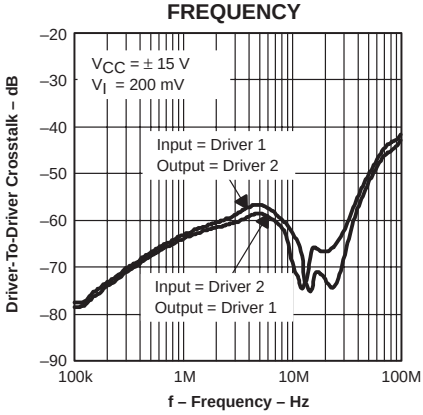


Figure 10

POWER SUPPLY REJECTION RATIO vs FREE-AIR TEMPERATURE

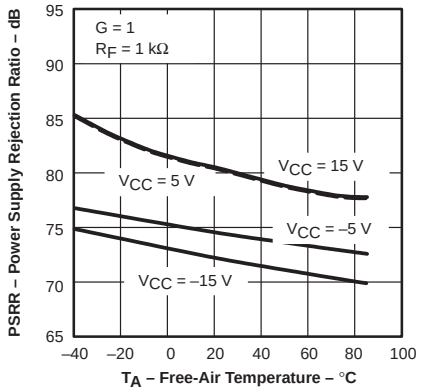


Figure 11

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

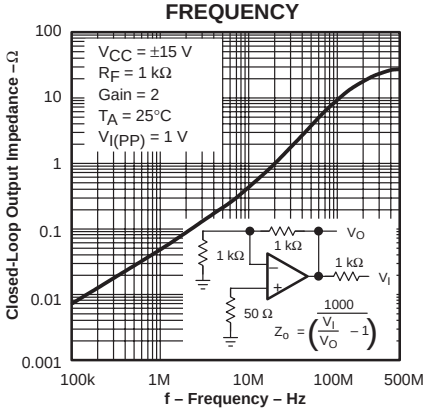


Figure 12

SUPPLY CURRENT vs SUPPLY VOLTAGE

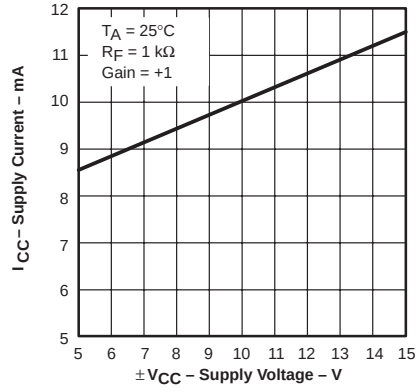


Figure 13

TYPICAL CHARACTERISTICS (DRIVER)

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

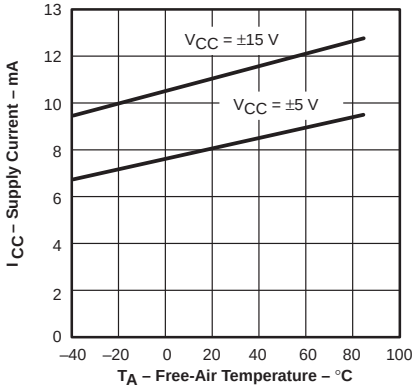


Figure 14

SLEW RATE vs OUTPUT STEP

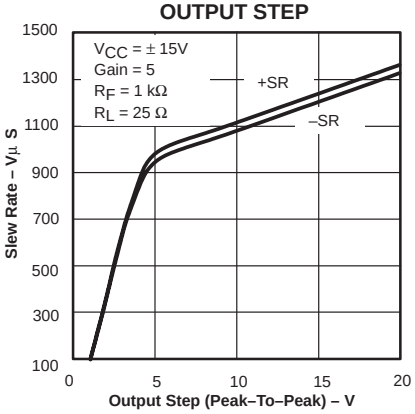


Figure 15

SLEW RATE vs OUTPUT STEP

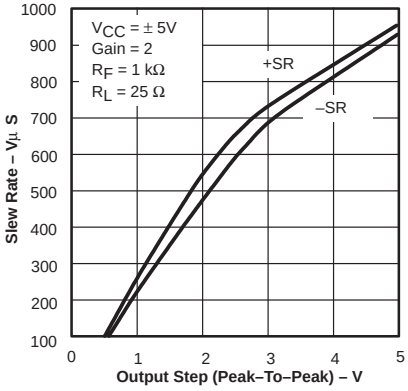


Figure 16

INPUT VOLTAGE AND CURRENT NOISE vs FREQUENCY

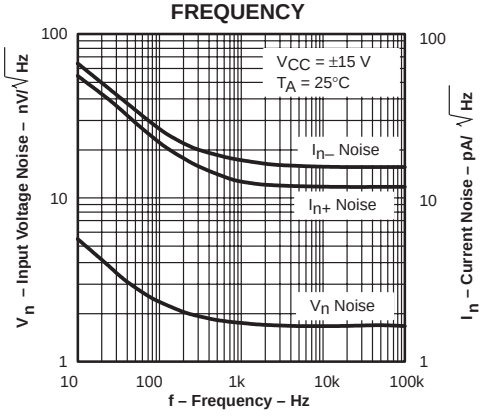


Figure 17

NORMALIZED FREQUENCY RESPONSE vs FREQUENCY

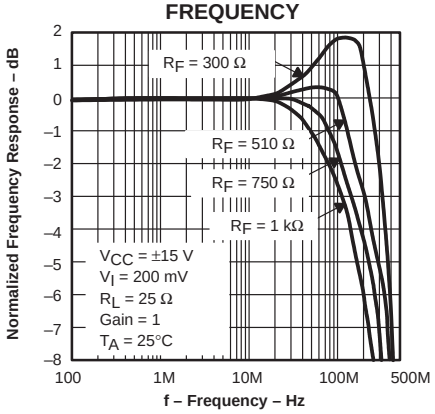


Figure 18

NORMALIZED FREQUENCY RESPONSE vs FREQUENCY

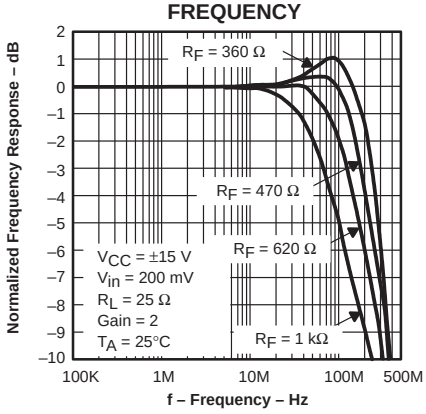


Figure 19

OUTPUT AMPLITUDE vs FREQUENCY

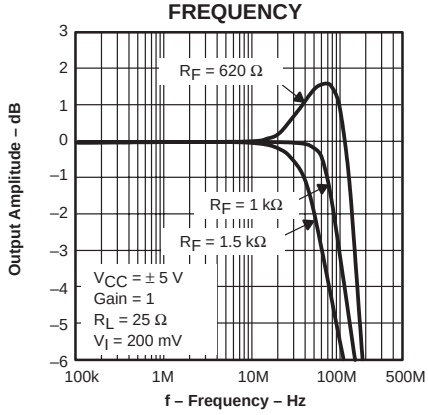


Figure 20

OUTPUT AMPLITUDE vs FREQUENCY

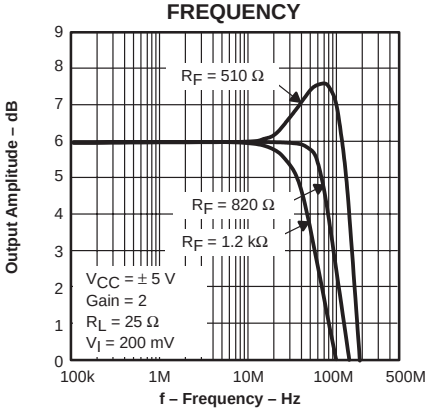


Figure 21

TYPICAL CHARACTERISTICS (DRIVER)

OUTPUT AMPLITUDE vs FREQUENCY

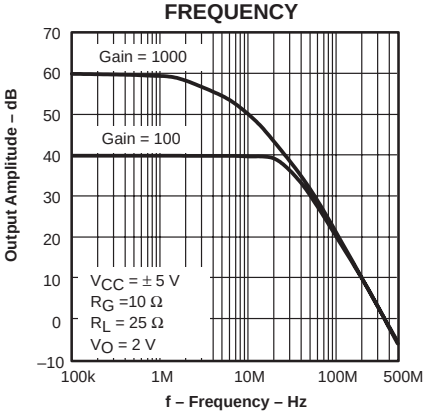


Figure 22

OUTPUT AMPLITUDE vs FREQUENCY

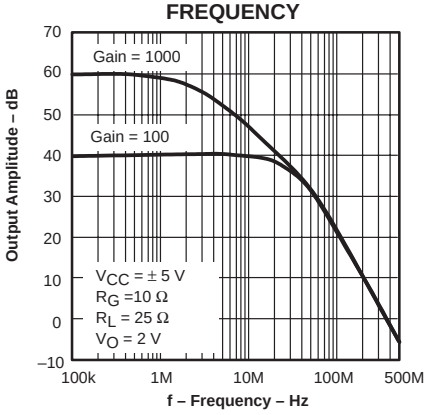


Figure 23

NORMALIZED OUTPUT RESPONSE vs FREQUENCY

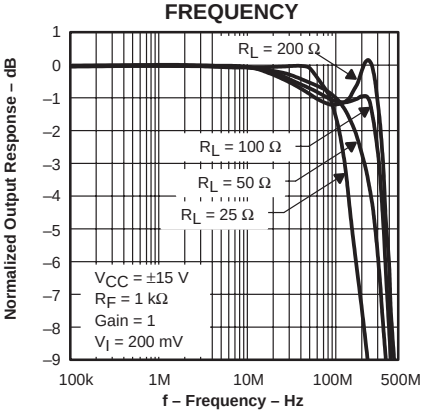


Figure 24

NORMALIZED OUTPUT RESPONSE vs FREQUENCY

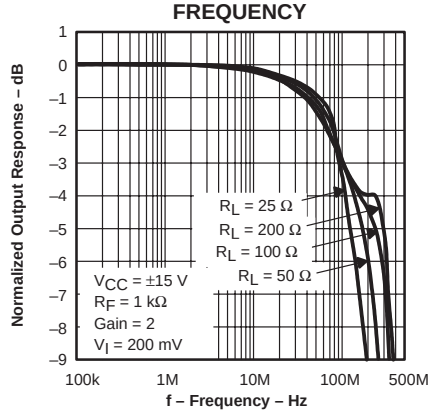


Figure 25

NORMALIZED OUTPUT RESPONSE vs FREQUENCY

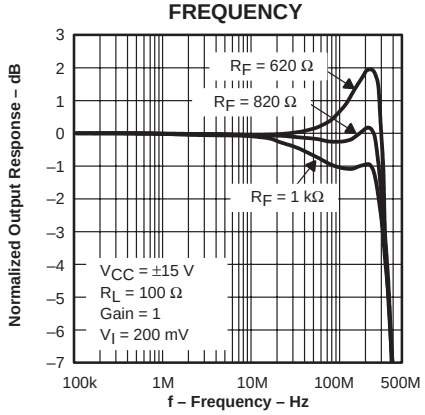


Figure 26

NORMALIZED OUTPUT RESPONSE vs FREQUENCY

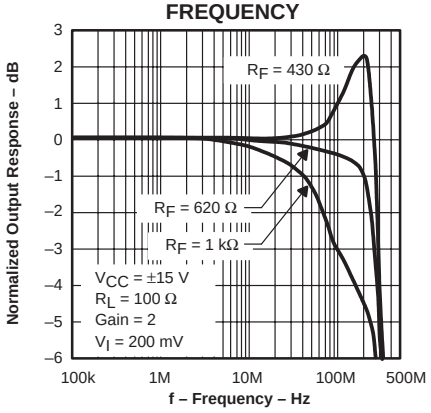


Figure 27

SMALL AND LARGE SIGNAL FREQUENCY RESPONSE

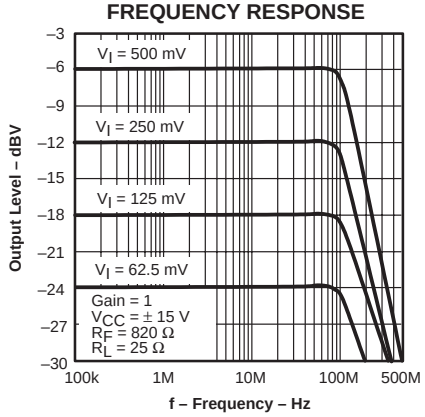


Figure 28

SMALL AND LARGE SIGNAL FREQUENCY RESPONSE

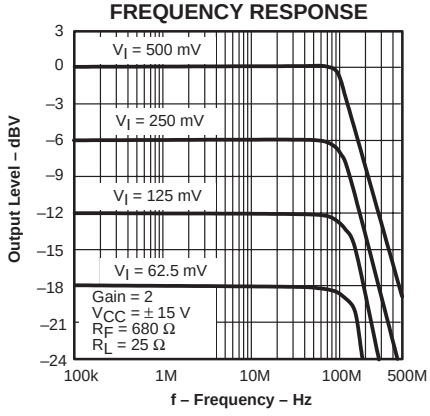


Figure 29

SINGLE–ENDED HARMONIC DISTORTION vs FREQUENCY

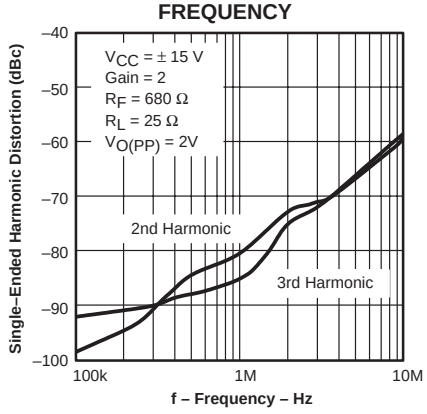


Figure 30

TYPICAL CHARACTERISTICS (DRIVER)

SINGLE–ENDED HARMONIC DISTORTION vs FREQUENCY

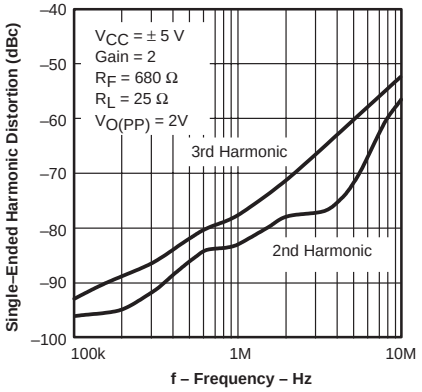


Figure 31

SINGLE–ENDED HARMONIC DISTORTION vs OUTPUT VOLTAGE

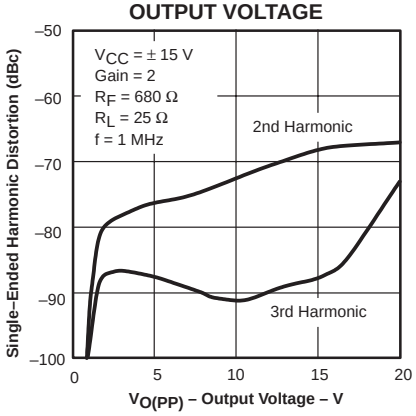


Figure 32

SINGLE–ENDED HARMONIC DISTORTION vs OUTPUT VOLTAGE

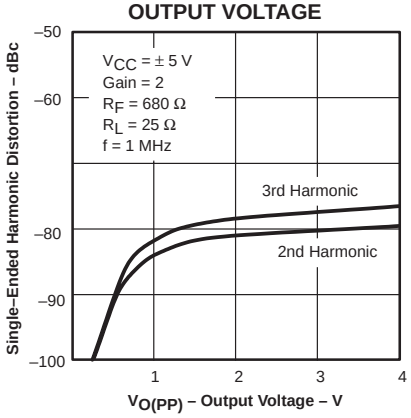


Figure 33

DIFFERENTIAL GAIN AND PHASE vs DC INPUT OFFSET VOLTAGE

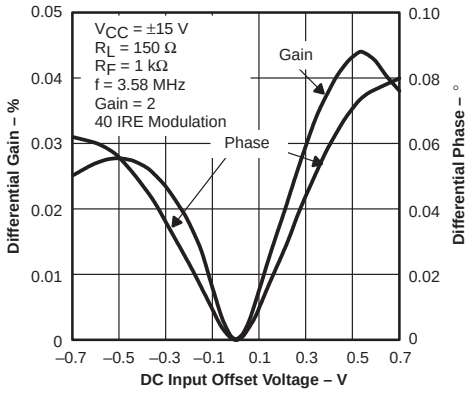


Figure 34

DIFFERENTIAL GAIN AND PHASE vs DC INPUT OFFSET VOLTAGE

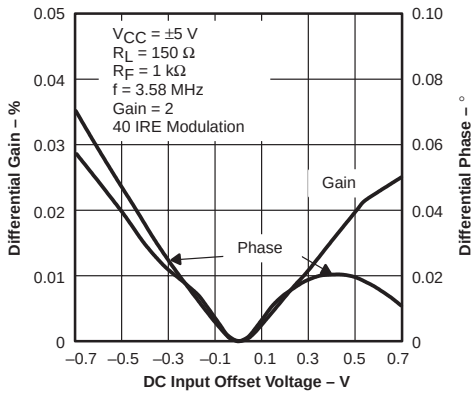


Figure 35

DIFFERENTIAL GAIN AND PHASE vs NUMBER OF 150-Ω LOADS

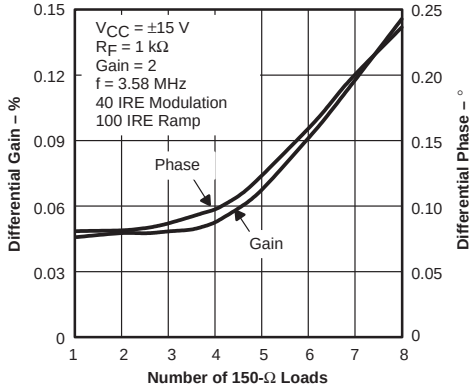


Figure 36

DIFFERENTIAL GAIN AND PHASE vs NUMBER OF 150-Ω LOADS

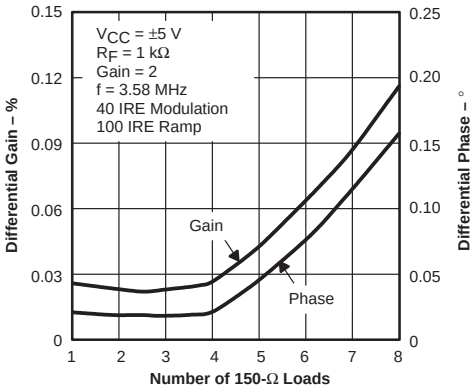
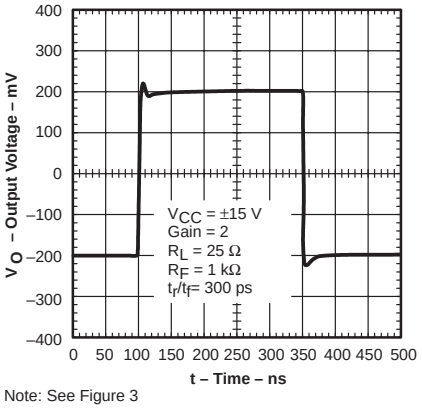


Figure 37

TYPICAL CHARACTERISTICS (DRIVER)

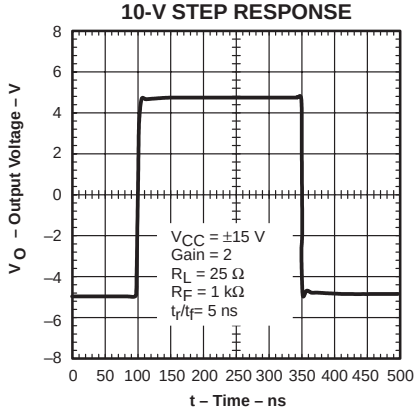
400-mV STEP RESPONSE



Note: See Figure 3

Figure 38

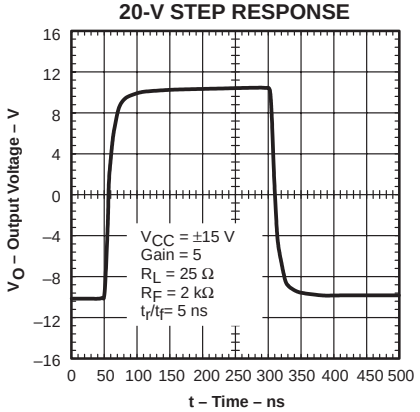
10-V STEP RESPONSE



Note: See Figure 3

Figure 39

20-V STEP RESPONSE



Note: See Figure 3

Figure 40

DRIVER-TO-RECEIVER CROSSTALK vs FREQUENCY

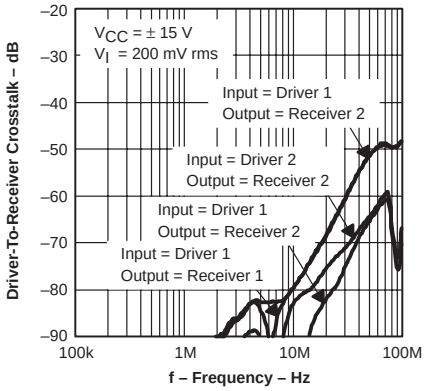


Figure 41

RECEIVER-TO-DRIVER CROSSTALK vs FREQUENCY

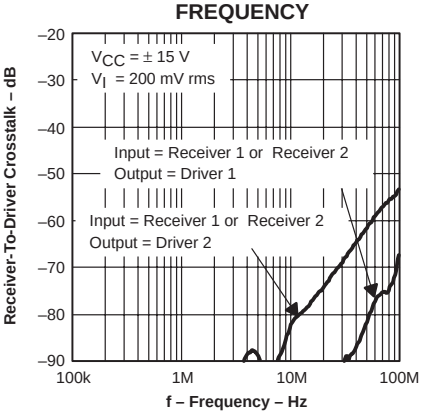


Figure 42

POWER SUPPLY REJECTION RATIO vs FREQUENCY

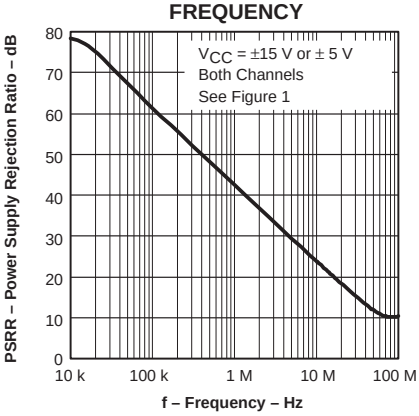


Figure 43

TYPICAL CHARACTERISTICS (RECEIVER)

OPEN LOOP GAIN & PHASE RESPONSE vs FREQUENCY

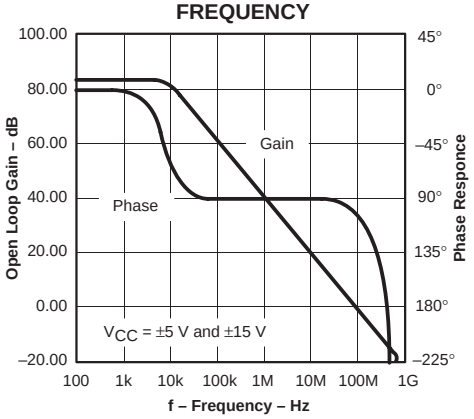


Figure 44

RECEIVER-TO-RECEIVER CROSSTALK vs FREQUENCY

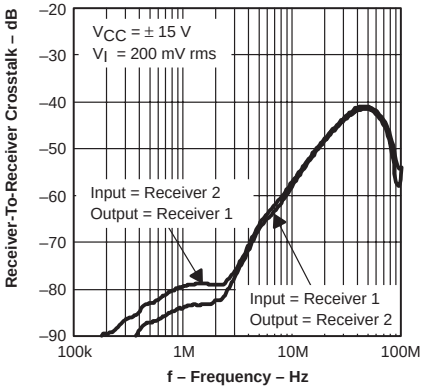


Figure 45

TOTAL HARMONIC DISTORTION vs FREQUENCY

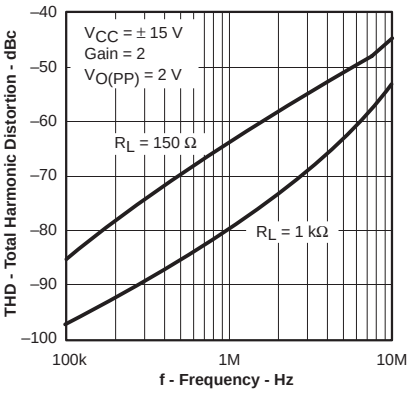


Figure 46

TOTAL HARMONIC DISTORTION vs FREQUENCY

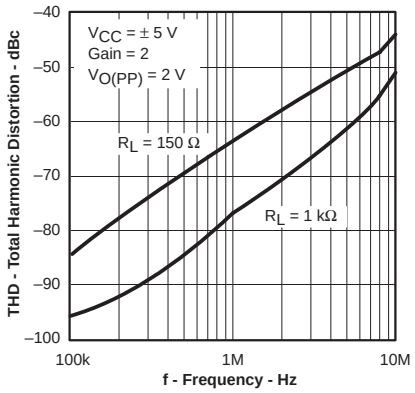


Figure 47

SETTLING vs OUTPUT STEP

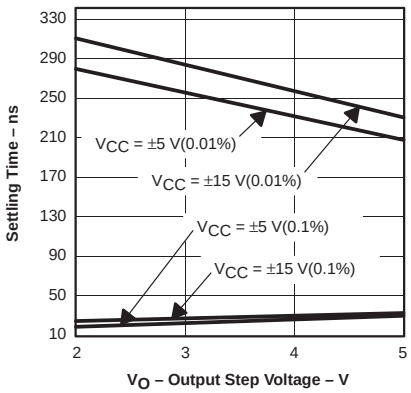


Figure 48

POWER SUPPLY REJECTION RATIO vs FREQUENCY

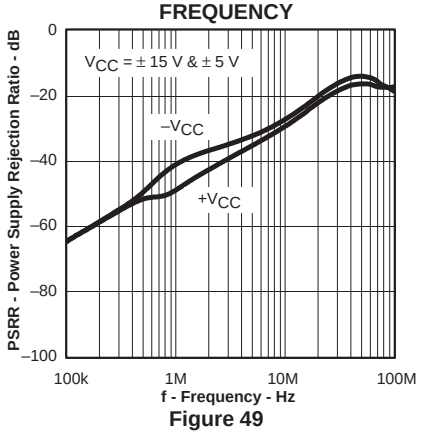


Figure 49

DISTORTION vs OUTPUT VOLTAGE

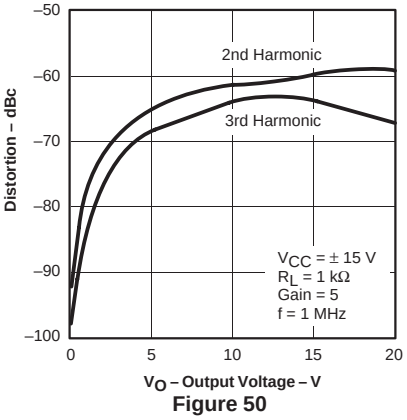


Figure 50

DISTORTION vs OUTPUT VOLTAGE

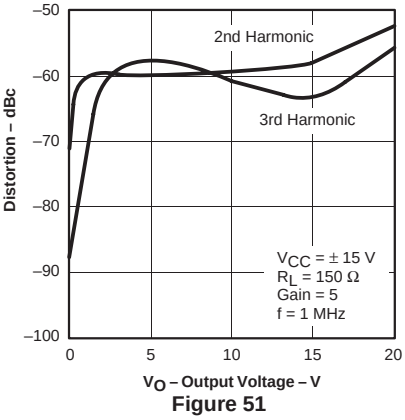


Figure 51

TYPICAL CHARACTERISTICS (RECEIVER)

DISTORTION vs FREQUENCY

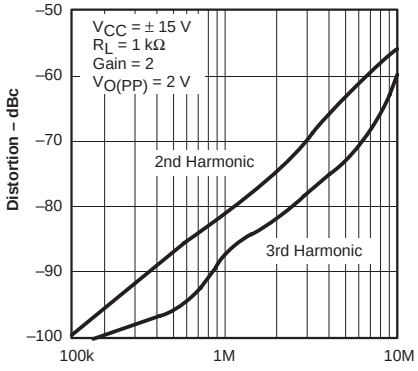


Figure 52

DISTORTION vs FREQUENCY

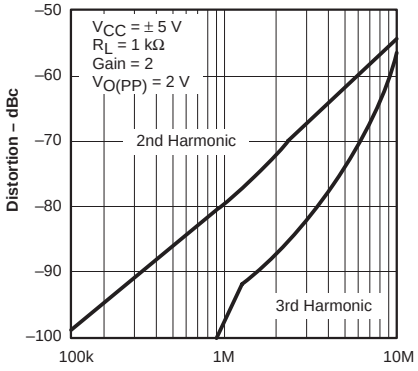


Figure 53

DISTORTION vs FREQUENCY

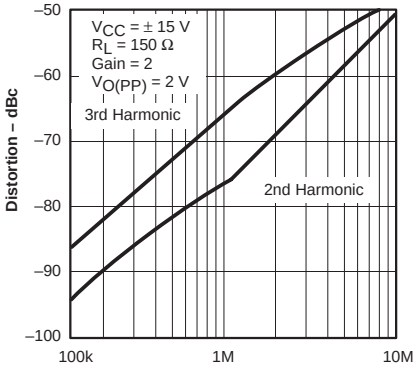


Figure 54

DISTORTION vs FREQUENCY

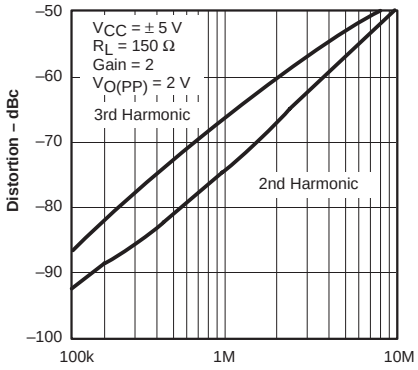


Figure 55

OUTPUT AMPLITUDE vs FREQUENCY

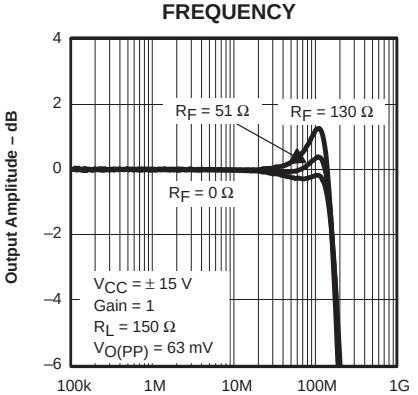


Figure 56

OUTPUT AMPLITUDE vs FREQUENCY

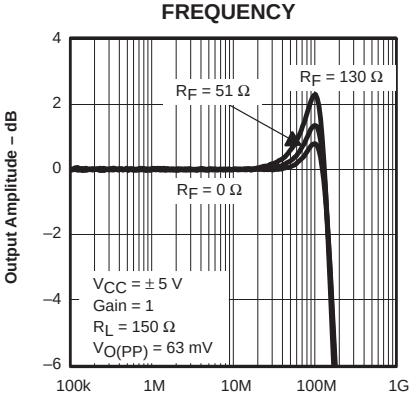


Figure 57

OUTPUT AMPLITUDE vs FREQUENCY

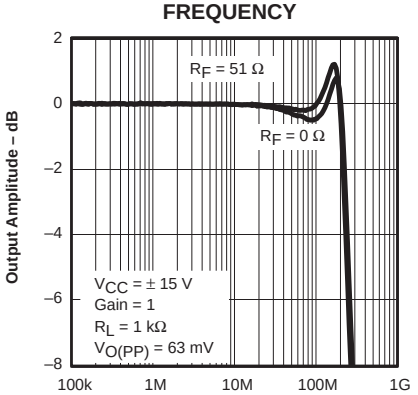


Figure 58

OUTPUT AMPLITUDE vs FREQUENCY

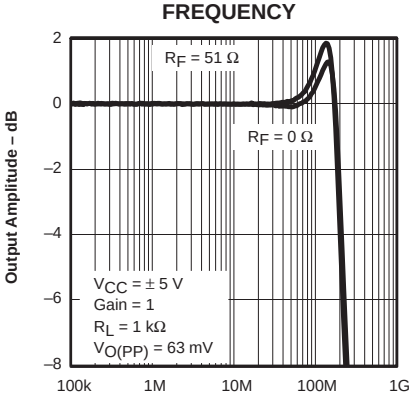


Figure 59

OUTPUT AMPLITUDE vs FREQUENCY

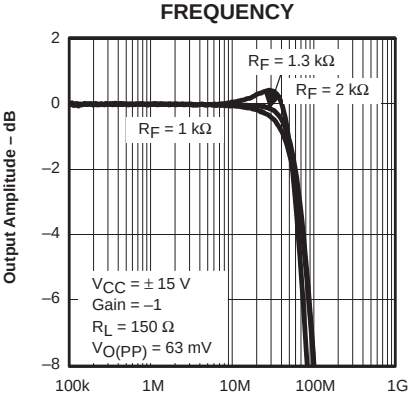


Figure 60

TYPICAL CHARACTERISTICS (RECEIVER)

OUTPUT AMPLITUDE vs FREQUENCY

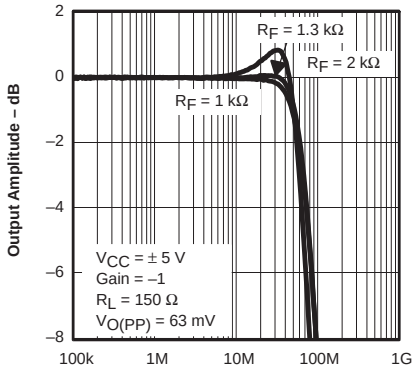


Figure 61

OUTPUT AMPLITUDE vs FREQUENCY

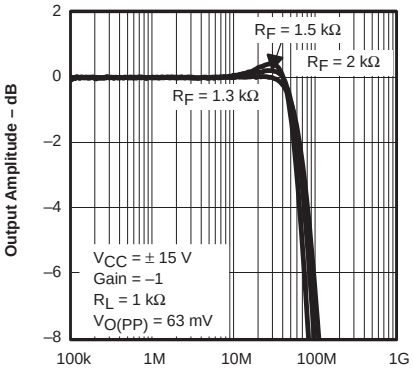


Figure 62

OUTPUT AMPLITUDE vs FREQUENCY

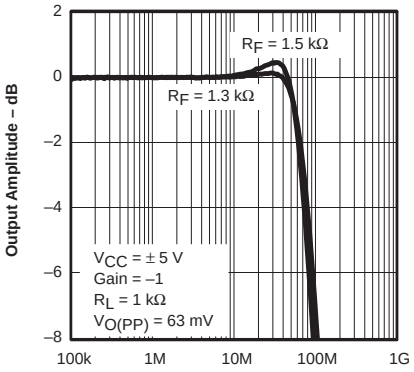


Figure 63

OUTPUT AMPLITUDE vs FREQUENCY

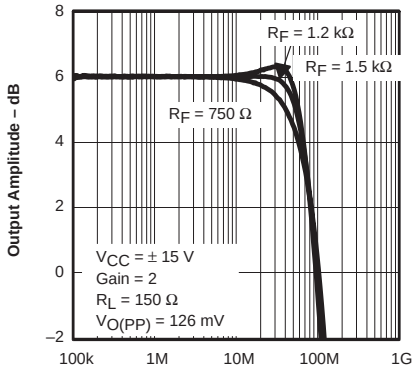


Figure 64

OUTPUT AMPLITUDE vs FREQUENCY

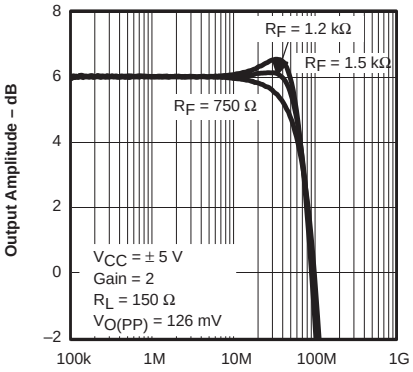


Figure 65

OUTPUT AMPLITUDE vs FREQUENCY

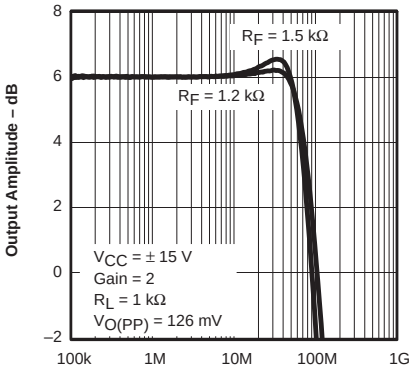


Figure 66

OUTPUT AMPLITUDE vs FREQUENCY

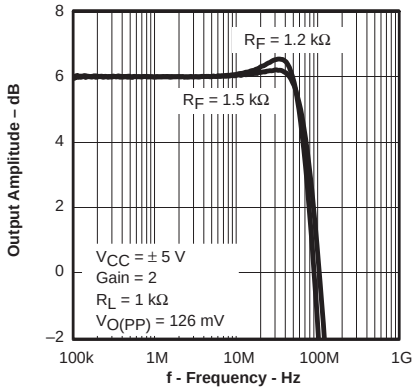


Figure 67

2-V STEP RESPONSE

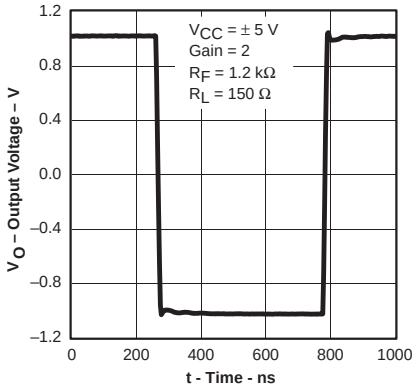


Figure 68

5-V STEP RESPONSE

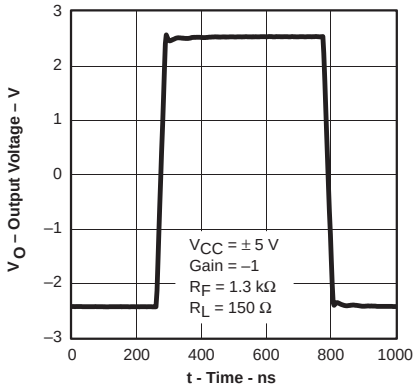


Figure 69

TYPICAL CHARACTERISTICS (RECEIVER)

2-V STEP RESPONSE

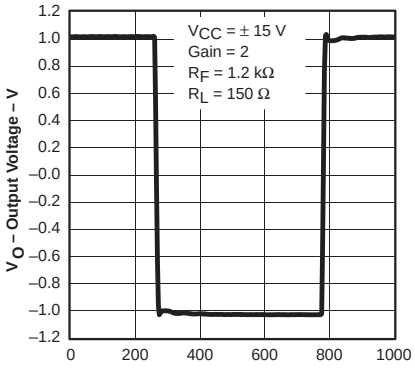


Figure 70

20-V STEP RESPONSE

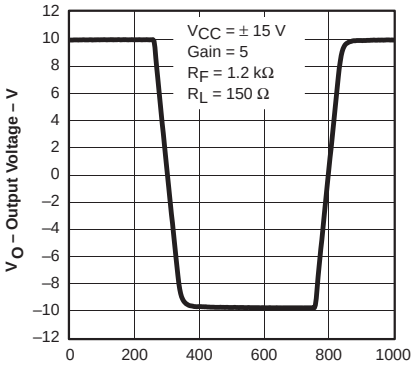


Figure 71

INPUT OFFSET VOLTAGE vs FREE-AIR TEMPERATURE

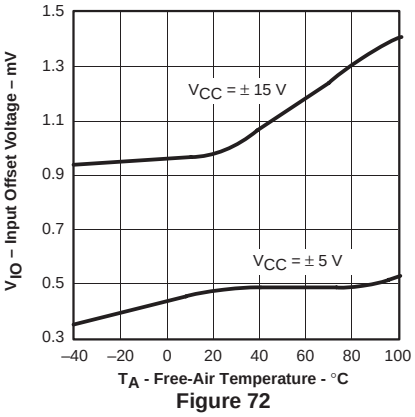


Figure 72

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

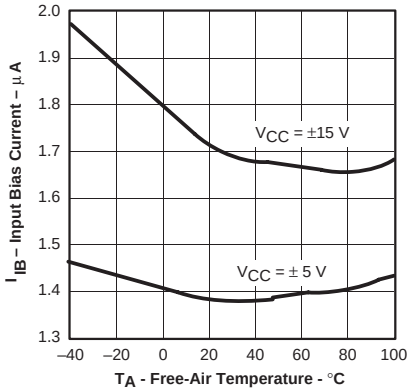


Figure 73

OUTPUT VOLTAGE vs SUPPLY VOLTAGE

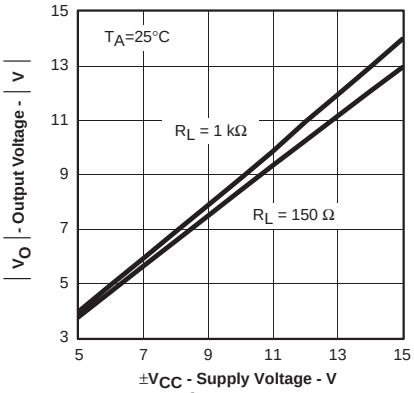


Figure 74

OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

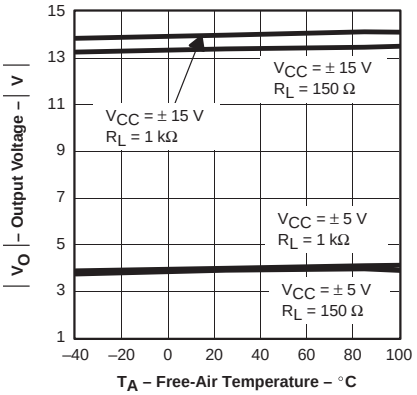


Figure 75

COMMON-MODE INPUT VOLTAGE vs SUPPLY VOLTAGE

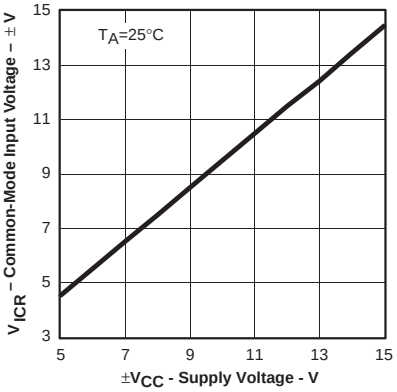


Figure 76

SUPPLY CURRENT vs SUPPLY VOLTAGE

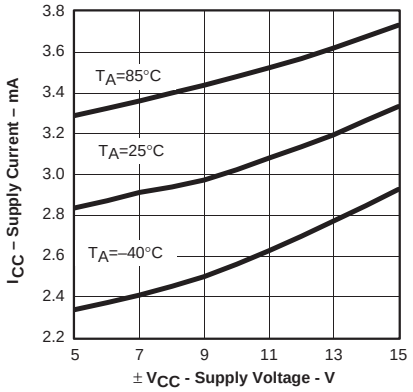


Figure 77

VOLTAGE AND CURRENT NOISE vs FREQUENCY

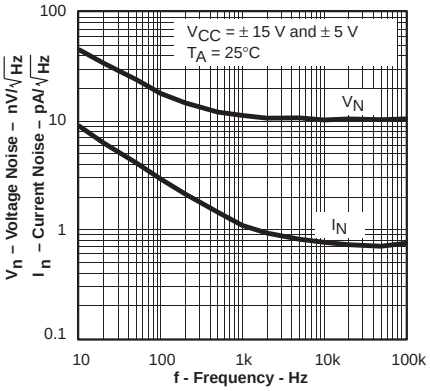


Figure 78

APPLICATION INFORMATION

ADSL

The THS6007 was primarily designed as a line driver and line receiver for ADSL (asymmetrical digital subscriber line). The driver output stage has been sized to provide full ADSL power levels of 20 dBm onto the telephone lines. Although actual driver output peak voltages and currents vary with each particular ADSL application, the THS6007 is specified for a minimum full output current of 400 mA at its full output voltage of approximately 12 V. This performance meets the demanding needs of ADSL at the central office end of the telephone line. A typical ADSL schematic is shown in Figure 79.

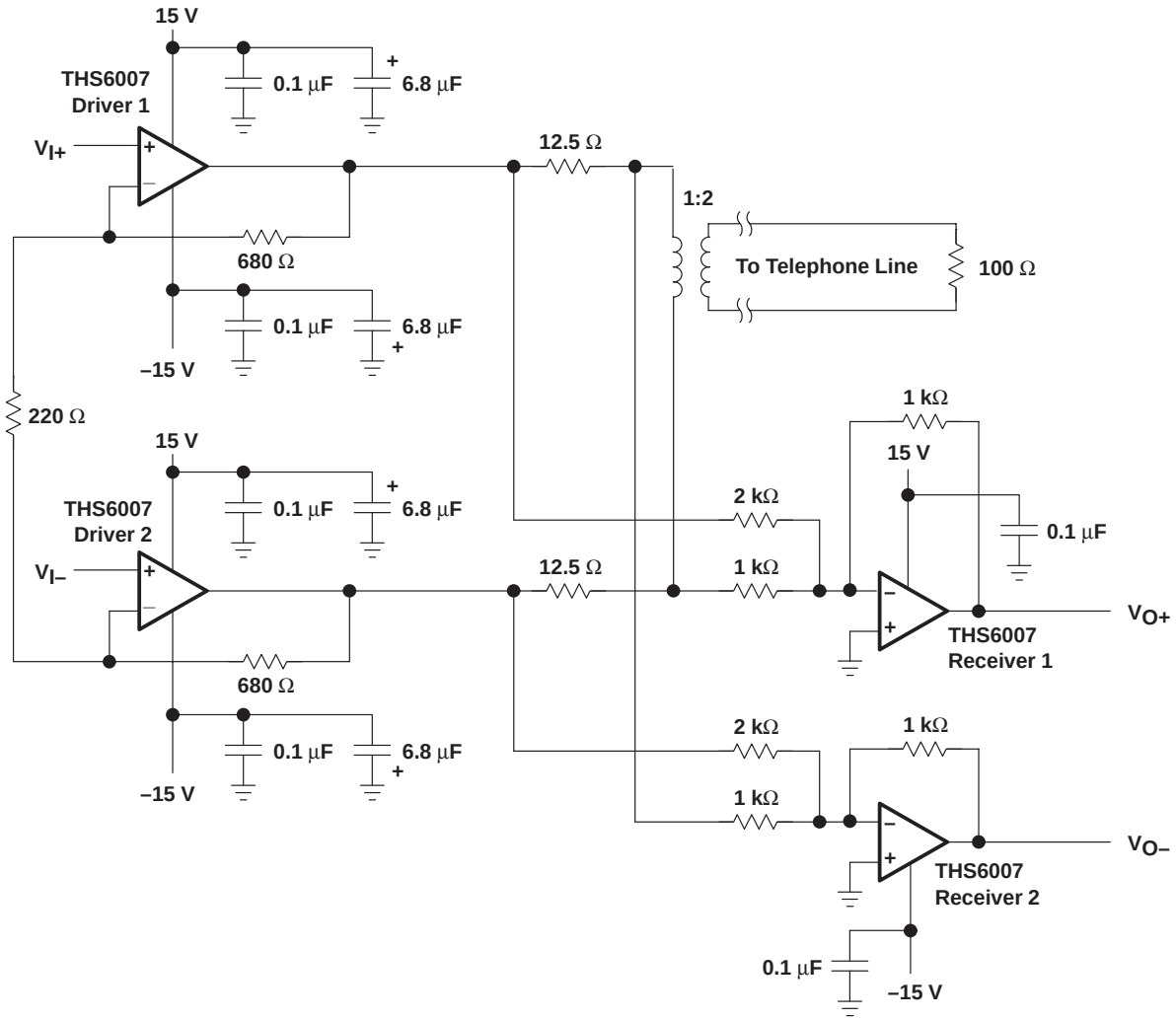


Figure 79. Typical THS6007 ADSL Application

APPLICATION INFORMATION

ADSL (continued)

The ADSL transmit band consists of 255 separate carrier frequencies each with its own modulation and amplitude level. With such an implementation, it is imperative that signals put onto the telephone line have as low a distortion as possible. This is because any distortion either interferes directly with other ADSL carrier frequencies or it creates intermodulation products that interfere with ADSL carrier frequencies.

The THS6007 has been specifically designed for ultralow distortion by careful circuit implementation and by taking advantage of the superb characteristics of the complementary bipolar process. Driver single-ended harmonic distortion measurements are shown in Figures 30 and 31. It is commonly known that in the differential driver configuration, the second order harmonics tend to be reduced by 6 dB or more. Thus, the dominant total harmonic distortion (THD) will be primarily due to the third order harmonics. For this test, the load was 25 Ω and the output signal produced a 2 $V_{O(PP)}$ signal. Thus, the test was run at full signal and full load conditions.

Another significant point is the fact that distortion decreases as the impedance load increases. This is because the output resistance of the amplifier becomes less significant as compared to the output load resistance.

ADSL receive line noise

Per ANSI T1.413, the receive noise power spectral density for an ADSL line is –140 dBm/$\sqrt{\text{Hz}}$. This results in a voltage noise requirement of less than 31.6 nV/$\sqrt{\text{Hz}}$ for the receiver in an ADSL system with a 1:1 transformer ratio.

Noise Power Spectral Density = –140 dBm/$\sqrt{\text{Hz}}$

Power = 1e–17 $\times$ 1 Hz = 0.01 fW

Assume: R_L = 100 Ω

$V_{noise} = \sqrt{(P \times R)} = \sqrt{(0.01\ \text{fW} \times 100\ \Omega)} = 31.6\ \text{nV}/\sqrt{\text{Hz}}$

For ADSL systems that use a 1:2 transformer ratio, such as central office line cards, the voltage noise requirement for the receiver is lowered to 15.8 nV/$\sqrt{\text{Hz}}$.

TRANSFORMER RATIO	V_{noise} ON LINE
1:1	31.6 nV/$\sqrt{\text{Hz}}$
1:2	15.8 nV/$\sqrt{\text{Hz}}$

The THS6007 receiver was designed to operate with 10 nV/$\sqrt{\text{Hz}}$ voltage noise, exceeding the noise requirements for an ADSL system operating with 1:1 or 1:2 transformer ratios.

APPLICATION INFORMATION

The THS6007 contains four independent operational amplifiers. Two are designated as drivers because of their high output current capability, and two are designated as receivers. The receiver amplifiers are voltage feedback topology amplifiers made for high-speed, low-power operation and are capable of driving output loads of at least 50 mA. The drivers are current feedback topology amplifiers and have been specifically designed to deliver the full power requirements of ADSL. They can deliver output currents of at least 400 mA at full output voltage.

The THS6007 is fabricated using Texas Instruments 30-V complementary bipolar process, BiCOM. This process provides excellent isolation and high slew rates that result in the device's excellent crosstalk and extremely low distortion.

independent power supplies

Each driver amplifier and both receivers of the THS6007 have their own power supply pins. This was specifically done to solve a problem that often occurs when multiple devices in the same package share common power pins. This problem is crosstalk between the individual devices caused by currents flowing in common connections. Whenever the current required by one device flows through a common connection shared with another device, this current, in conjunction with the impedance in the shared line, produces an unwanted voltage on the power supply. Proper power supply decoupling and good device power supply rejection helps to reduce this unwanted signal. What is left is crosstalk.

However, with independent power supply pins for each device, the effects of crosstalk through common impedance in the power supplies is more easily managed. This is because it is much easier to achieve low common impedance on the PCB with copper etch than it is to achieve low impedance within the package with either bond wires or metal traces on silicon.

APPLICATION INFORMATION

power supply restrictions

Although the THS6007 is specified for operation from power supplies of ±5 V to ±15 V (or singled-ended power supply operation from 10 V to 30 V), and each amplifier has its own power supply pins, several precautions must be taken to assure proper operation.

1. The power supplies for each driver amplifier must be the same value. For example, if driver 1 uses ±15 volts, then driver 2 must also use ±15 volts. Using ±15 volts for driver 1 and ±5 volts for driver 2 is not allowed.
2. The power supplies for the receiver amplifiers may be different than the driver supply voltages. Although it is recommended to use the same type of supply, either split supplies($\pm V_{CC}$) or single supply ($+V_{CC}$ and GND), for both drivers and receivers.

All the amplifiers within the THS6007 incorporate a standard Class A-B output stage. This means that some of the quiescent current is directed to the load as the load current increases. So under heavy load conditions, accurate power dissipation calculations are best achieved through actual measurements. For small loads, however, internal power dissipation for each amplifier in the THS6007 can be approximated by the following formula:

$$P_D \cong \left(2\ V_{CC}\ I_{CC}\right) + \left(V_{CC} - V_O\right) \times \left(\frac{V_O}{R_L}\right)$$

Where:

P_D = Power dissipation for one amplifier
V_{CC} = Split supply voltage
I_{CC} = Supply current for that particular amplifier
V_O = Output voltage of amplifier
R_L = Load resistance

To find the total THS6007 power dissipation, we simply sum up all four amplifier power dissipation results. Generally, the worst case power dissipation occurs when the output voltage is one-half the V_{CC} voltage. One last note, which is often overlooked: the feedback resistor (R_f) is also a load to the output of the amplifier and should be taken into account for low value feedback resistors.

APPLICATION INFORMATION

device protection features

The drivers of the THS6007 have two built-in protection features that protect the device against improper operation. The first protection mechanism is output current limiting. Should the drivers output become shorted to ground, the output current is automatically limited to the value given in the data sheet. While this protects the output against excessive current, the device internal power dissipation increases due to the high current and large voltage drop across the output transistors. Continuous output shorts are not recommended and could damage the device. Additionally, connection of the amplifier output to one of the supply rails ($\pm V_{CC}$) can cause failure of the device and is not recommended. The use of Schottky diodes from each amplifier's output to each power supply voltage rail is recommended. This will limit surges from the transmission line so as to not damage the THS6007.

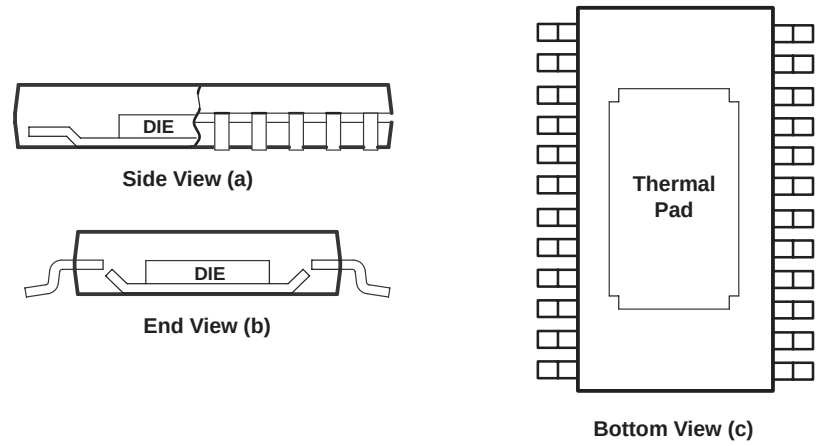
The drivers second built-in protection feature is thermal shutdown. Should the internal junction temperature rise above approximately 180°C, the device automatically shuts down. Such a condition could exist with improper heat sinking or if the output is shorted to ground. When the abnormal condition is fixed and the junction temperature drops below 150°C, the internal thermal shutdown circuit automatically turns the device back on.

thermal information

The THS6007 is packaged in a thermally-enhanced PWP package, which is a member of the PowerPAD™ family of packages. This package is constructed using a downset leadframe upon which the die is mounted [see Figure 80(a) and Figure 80(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 80(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD™ package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device. This is discussed in more detail in the *PCB design considerations* section of this document.

The PowerPAD™ package represents a breakthrough in combining the small area and ease of assembly of surface mount with the, heretofore, awkward mechanical methods of heatsinking.



NOTE A: The thermal pad is electrically isolated from all terminals in the package.

Figure 80. Views of Thermally Enhanced PWP Package

APPLICATION INFORMATION

recommended feedback and gain resistor values

As with all current-feedback amplifiers, the bandwidth of the THS6007 drivers is an inversely proportional function of the value of the feedback resistor. This can be seen from Figures 18 and 19. For the driver, the recommended resistors for the optimum frequency response for a 25-Ω load system are 680 Ω for a gain = 1 and 620 Ω for a gain = 2 or –1. These should be used as a starting point and once optimum values are found, 1% tolerance resistors should be used to maintain frequency response characteristics. Because there is a finite amount of output resistance of the operational amplifier, load resistance can play a major part in frequency response. This is especially true with the drivers, which tend to drive low-impedance loads. This can be seen in Figure 12, Figure 24, and Figure 25. As the load resistance increases, the output resistance of the amplifier becomes less dominant at high frequencies. To compensate for this, the feedback resistor should change. For 100-Ω loads, it is recommended that the feedback resistor be changed to 820 Ω for a gain of 1 and 560 Ω for a gain of 2 or –1. Although, for most applications, a feedback resistor value of 1 kΩ is recommended, which is a good compromise between bandwidth and phase margin that yields a very stable amplifier.

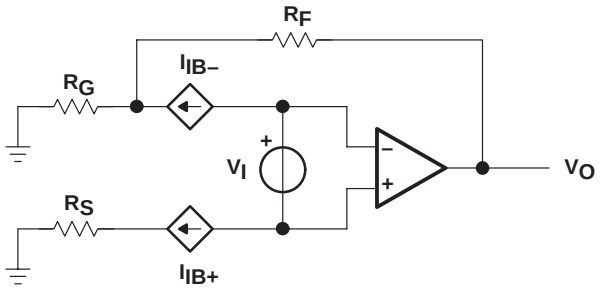
Consistent with current-feedback amplifiers, increasing the gain is best accomplished by changing the gain resistor, not the feedback resistor. This is because the bandwidth of the amplifier is dominated by the feedback resistor value and internal dominant-pole capacitor. The ability to control the amplifier gain independent of the bandwidth constitutes a major advantage of current feedback amplifiers over conventional voltage feedback amplifiers. Therefore, once a frequency response is found suitable to a particular application, adjust the value of the gain resistor to increase or decrease the overall amplifier gain.

Finally, it is important to realize the effects of the feedback resistance on distortion. Increasing the resistance decreases the loop gain and increases the distortion. It is also important to know that decreasing load impedance increases total harmonic distortion (THD). Typically, the third order harmonic distortion increases more than the second order harmonic distortion.

The receivers of the THS6007 are voltage feedback amplifiers (VFB). Therefore the amplifiers follow the classical amplifier use of a gain-bandwidth-product. As gain increases, the bandwidth (–3 dB) decreases accordingly. There are no limitations on using capacitors within the feedback loop of VFB amplifier circuits. Figures 56 through 67 show the effects of feedback resistance and gain versus frequency. Using these graphs as a reference point is highly recommended.

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:



$$V_{OO} = V_{IO}\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB+}\, R_S \left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-}\, R_F$$

Figure 81. Output Offset Voltage Model

APPLICATION INFORMATION

noise calculations and noise figure

Noise can cause errors on very small signals. This is especially true for the receiver amplifiers which are generally used for amplifying small signals coming over a transmission line. The noise model for current-feedback amplifiers (CFB) is the same as voltage-feedback amplifiers (VFB). The only difference between the two is that the CFB amplifiers generally specify different current noise parameters for each input while VFB amplifiers usually only specify one noise-current parameter. The noise model is shown in Figure 82. This model includes all of the noise sources as follows:

- e_n = Amplifier internal voltage noise (nV/$\sqrt{Hz}$)
- IN+ = Noninverting current noise (pA/$\sqrt{Hz}$)
- IN– = Inverting current noise (pA/$\sqrt{Hz}$)
- e_{Rx} = Thermal voltage noise associated with each resistor (e_{Rx} = 4 kTR_x)

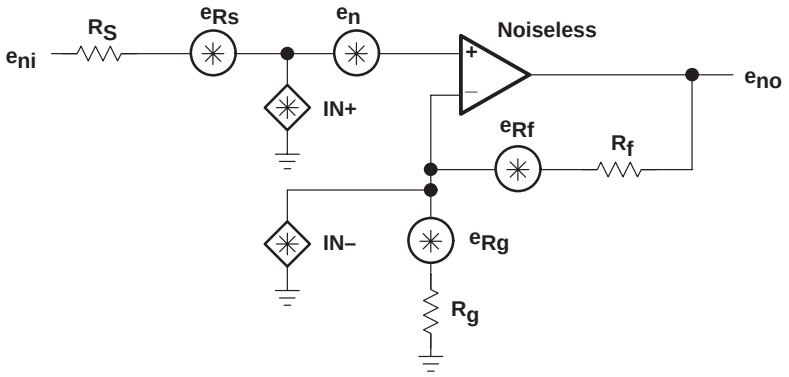


Figure 82. Noise Model

The total equivalent input noise density (e_{ni}) is calculated by using the following equation:

$$e_{ni} = \sqrt{(e_n)^2 + \left(IN + \times R_S\right)^2 + \left(IN- \times \left(R_F \parallel R_G\right)\right)^2 + 4\ kTR_S + 4\ kT\left(R_F \parallel R_G\right)}$$

Where:

k = Boltzmann's constant = 1.380658×10^{-23}
T = Temperature in degrees Kelvin (273 +°C)
$R_F \parallel R_G$ = Parallel resistance of R_F and R_G

To get the equivalent output noise of the amplifier, just multiply the equivalent input noise density (e_{ni}) by the overall amplifier gain (A_V).

$$e_{no} = e_{ni}\ A_V = e_{ni}\left(1 + \frac{R_F}{R_G}\right) \text{ (Noninverting Case)}$$

APPLICATION INFORMATION

noise calculations and noise figure (continued)

As the previous equations show, to keep noise at a minimum, small-value resistors should be used. As the closed-loop gain is increased (by reducing R_g), the input noise is reduced considerably because of the parallel resistance term. This leads to the general conclusion that the most dominant noise sources are the source resistor (R_S) and the internal amplifier noise voltage (e_n). Because noise is summed in a root-mean-squares method, noise sources smaller than 25% of the largest noise source can be effectively ignored. This can greatly simplify the formula and make noise calculations much easier to calculate.

This brings up another noise measurement usually preferred in RF applications, noise figure (NF). Noise figure is a measure of noise degradation caused by the amplifier. The value of the source resistance must be defined and is typically 50 Ω in RF applications.

$$NF = 10\log\left[\frac{e_{ni}^{2}}{e_{Rs}}\right]$$

Because the dominant noise components are generally the source resistance and the internal amplifier noise voltage, we can approximate the noise figure as:

$$NF = 10\log\left[1 + \frac{\left[\left(e_n\right)^2 + \left(IN + \times R_S\right)^2\right]}{4\ kTR_S}\right]$$

The Figure 83 shows the noise figure graph for the drivers of the THS6007. Figure 84 shows the noise figure graph for the receivers of the THS6007.

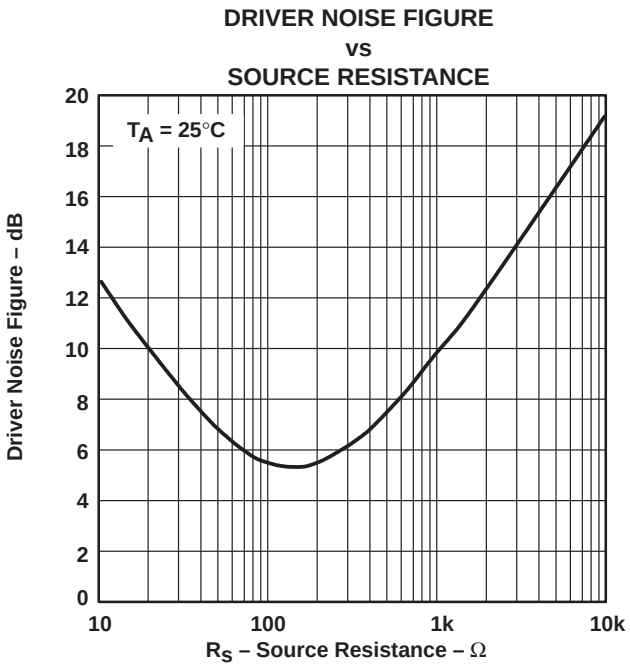


Figure 83

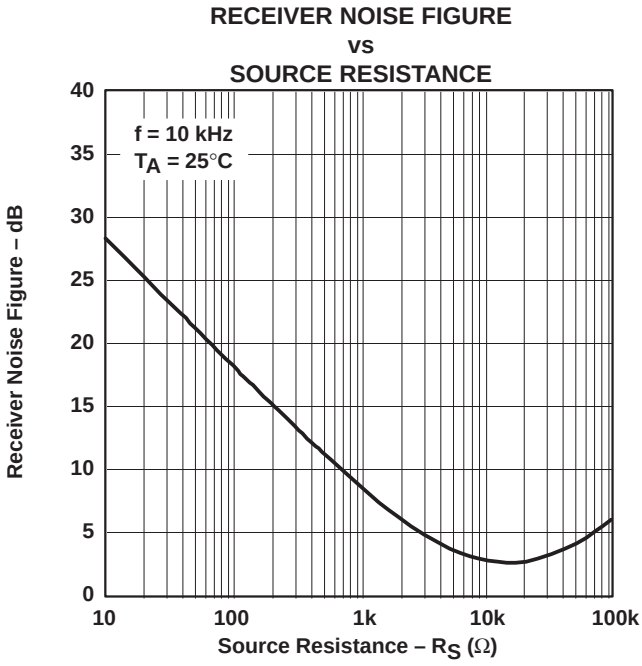


Figure 84

APPLICATION INFORMATION

PCB design considerations

Proper PCB design techniques in two areas are important to assure proper operation of the THS6007. These areas are high-speed layout techniques and thermal-management techniques. Because the THS6007 is a high-speed part, the following guidelines are recommended.

- Ground plane – It is essential that a ground plane be used on the board to provide all components with a low inductive ground connection. Although a ground connection directly to a terminal of the THS6007 is not necessarily required, it is recommended that the thermal pad of the package be tied to ground. This serves two functions. It provides a low inductive ground to the device substrate to minimize internal crosstalk and it provides the path for heat removal.
- Input stray capacitance – To minimize potential problems with amplifier oscillation, the capacitance at the inverting input of the amplifiers must be kept to a minimum. To do this, PCB trace runs to the inverting input must be as short as possible, the ground plane should be removed under any etch runs connected to the inverting input, and external components should be placed as close as possible to the inverting input. This is especially true in the noninverting configuration. An example of this can be seen in Figure 85, which shows what happens when 1.8 pF is added to the inverting input terminal in the noninverting configuration. The bandwidth increases dramatically at the expense of peaking. This is because some of the error current is flowing through the stray capacitor instead of the inverting node of the amplifier. Although, in the inverting mode, stray capacitance at the inverting input has little effect. This is because the inverting node is at a *virtual ground* and the voltage does not fluctuate nearly as much as in the noninverting configuration.

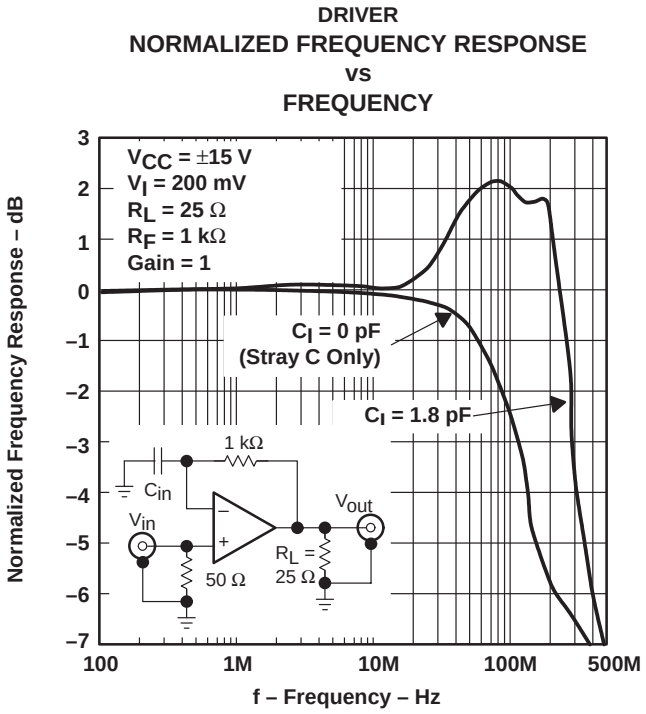


Figure 85. Driver Normalized Frequency Response vs Frequency

APPLICATION INFORMATION

PCB design considerations (continued)

- Proper power supply decoupling – Use a minimum of a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting etch makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminal and the ceramic capacitors.

Because of its power dissipation, proper thermal management of the THS6007 is required. Although there are many ways to properly heatsink this device, the following steps illustrate one recommended approach for a multilayer PCB with an internal ground plane.

1. Prepare the PCB with a top side etch pattern as shown in Figure 86. There should be etch for the leads as well as etch for the thermal pad.
2. Place the thermal transfer holes in the area of the thermal pad. These holes should be 13 mils in diameter. They are kept small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered so that wicking is not a problem.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, *do not* use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the IC package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its thermal transfer holes exposed. The bottom-side solder mask should cover the thermal transfer holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the THS6007 IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

APPLICATION INFORMATION

PCB design considerations (continued)

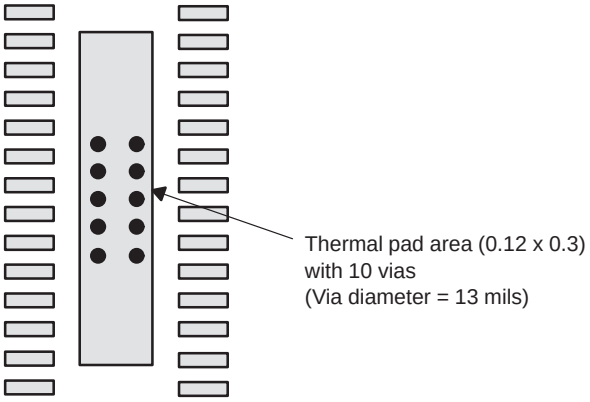


Figure 86. PowerPAD™ PCB Etch and Via Pattern

The actual thermal performance achieved with the THS6007 in its PowerPAD™ package depends on the application. In the previous example, if the size of the internal ground plane is approximately 3 inches × 3 inches, then the expected thermal coefficient, θ_{JA}, is about 27.9°C/W. For a given θ_{JA}, the maximum power dissipation is shown in Figure 87 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

P_D = Maximum power dissipation of THS6007 (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case (0.72°C/W)
θ_{CA} = Thermal coefficient from case to ambient

It is recommended to design the system to keep the junction temperature (T_J) at a minimum of 125°C. Junction temperatures higher 125°C than can lead to increased output distortion. Additionally, because the heat of the device is dissipated through the PCB, care must be taken to ensure the PCB does not become thermally saturated. Once this happens, the power dissipation of the system (PCB and active devices) becomes very in-efficient and the performance will suffer.

More complete details of the PowerPAD™ installation process and thermal management techniques can be found in the Texas Instruments Technical Brief, *PowerPAD™ Thermally Enhanced Package.* This document can be found at the TI web site (www.ti.com) by searching on the key word PowerPAD™. The document can also be ordered through your local TI sales office. Refer to literature number SLMA002 when ordering.

APPLICATION INFORMATION

PCB design considerations (continued)

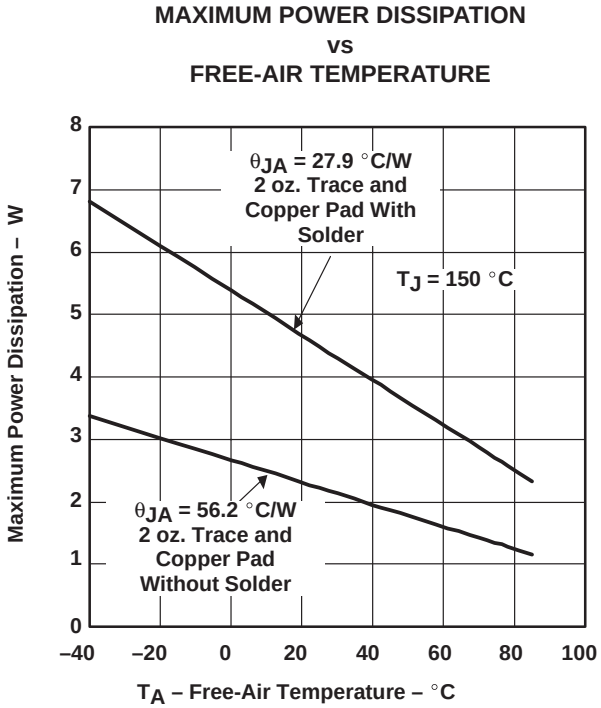
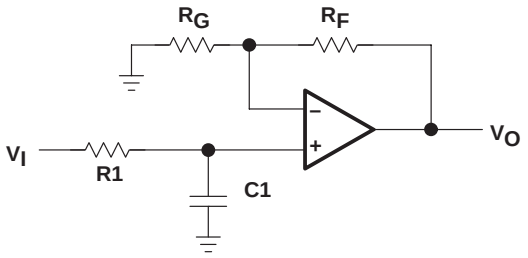


Figure 87. Maximum Power Dissipation vs Free-Air Temperature

APPLICATION INFORMATION

general configurations

A common error for the first-time CFB user is to create a unity gain buffer amplifier by shorting the output directly to the inverting input. A CFB amplifier in this configuration is now commonly referred to as an oscillator. The THS6007 drivers, like all CFB amplifiers, *must* have a feedback resistor for stable operation. Additionally, placing capacitors directly from the output to the inverting input is not recommended. This is because, at high frequencies, a capacitor has a very low impedance. This results in an unstable amplifier and should not be considered when using a current-feedback amplifier. Because of this, integrators and simple low-pass filters, which are easily implemented on a VFB amplifier, have to be designed slightly differently. If filtering is required, simply place an RC-filter at the noninverting terminal of the operational-amplifier (see Figure 88).

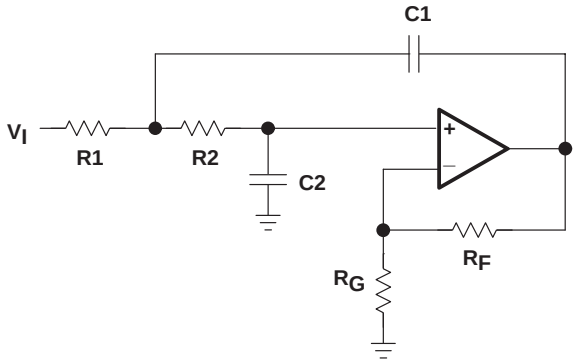


$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR1C1}\right)$$

$$f_{-3dB} = \frac{1}{2\pi R1C1}$$

Figure 88. Single-Pole Low-Pass Filter

If a multiple pole filter is required, a Sallen-Key filter can work very well with CFB amplifiers. This is because the filtering elements are not in the negative feedback loop and stability is not compromised. Because of their high slew-rates and high bandwidths, CFB amplifiers can create very accurate signals and help minimize distortion. An example is shown in Figure 89.



R1 = R2 = R
C1 = C2 = C
Q = Peaking Factor
(Butterworth Q = 0.707)

$$f_{-3dB} = \frac{1}{2\pi RC}$$

$$R_G = \frac{R_F}{\left(2 - \frac{1}{Q}\right)}$$

Figure 89. 2-Pole Low-Pass Sallen-Key Filter

APPLICATION INFORMATION

general configurations (continued)

THS6007 driver amplifiers can also be used as very good video distribution amplifiers. One characteristic of distribution amplifiers is the fact that the differential phase (DP) and the differential gain (DG) are compromised as the number of lines increases and the closed-loop gain increases. Be sure to use termination resistors throughout the distribution system to minimize reflections and capacitive loading.

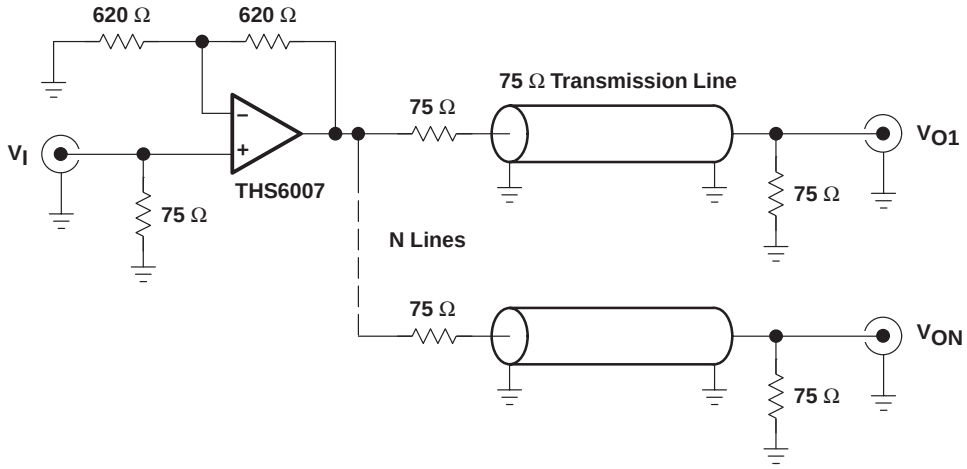


Figure 90. Video Distribution Amplifier Application

driving a capacitive load

Driving capacitive loads with high performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS6007 has been internally compensated to maximize its bandwidth and slew rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 91. A minimum value of 20 Ω should work well for most applications. For example, in 75-Ω transmission systems, setting the series resistor value to 75 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

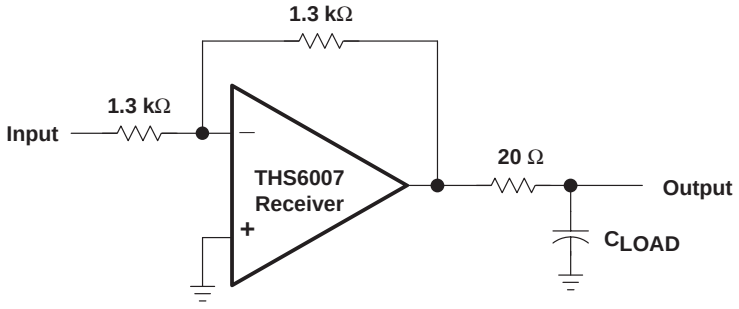
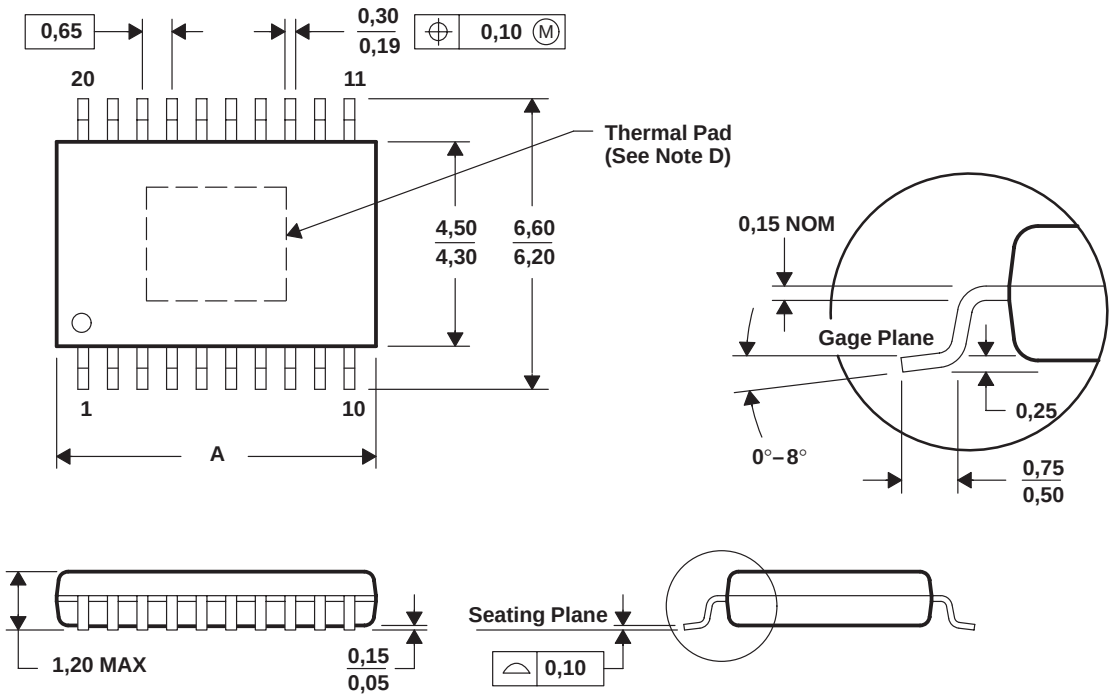


Figure 91. Driving a Capacitive Load

MECHANICAL INFORMATION

PWP (R-PDSO-G)** **PowerPAD™ PLASTIC SMALL-OUTLINE**

20 PINS SHOWN



DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/F 10/98

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.