TEXAS INSTRUMENTS

THS1215/30 EVM

User's Guide

December 2000

AAP Data Conversion

SLAU058

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Read This First

About This Manual

This document presents a description of the THS1215/30 evaluation module.

How to Use This Manual

This document contains the following chapters:

- ❏ Chapter 1 – Introduction
- ❏ Chapter 2 – Physical Description
- ❏ Chapter 3 – Circuit Functionality
- ❏ Chapter 4 – Control Modes
- ❏ Appendix A – Schematics

Information About Cautions and Warnings

This book may contain cautions and warnings.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

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Chapter 1

Introduction

This chapter gives an overview of the THS1215/30 evaluation module (EVM), and provides a general description of the features and functions to be considered when using the module.

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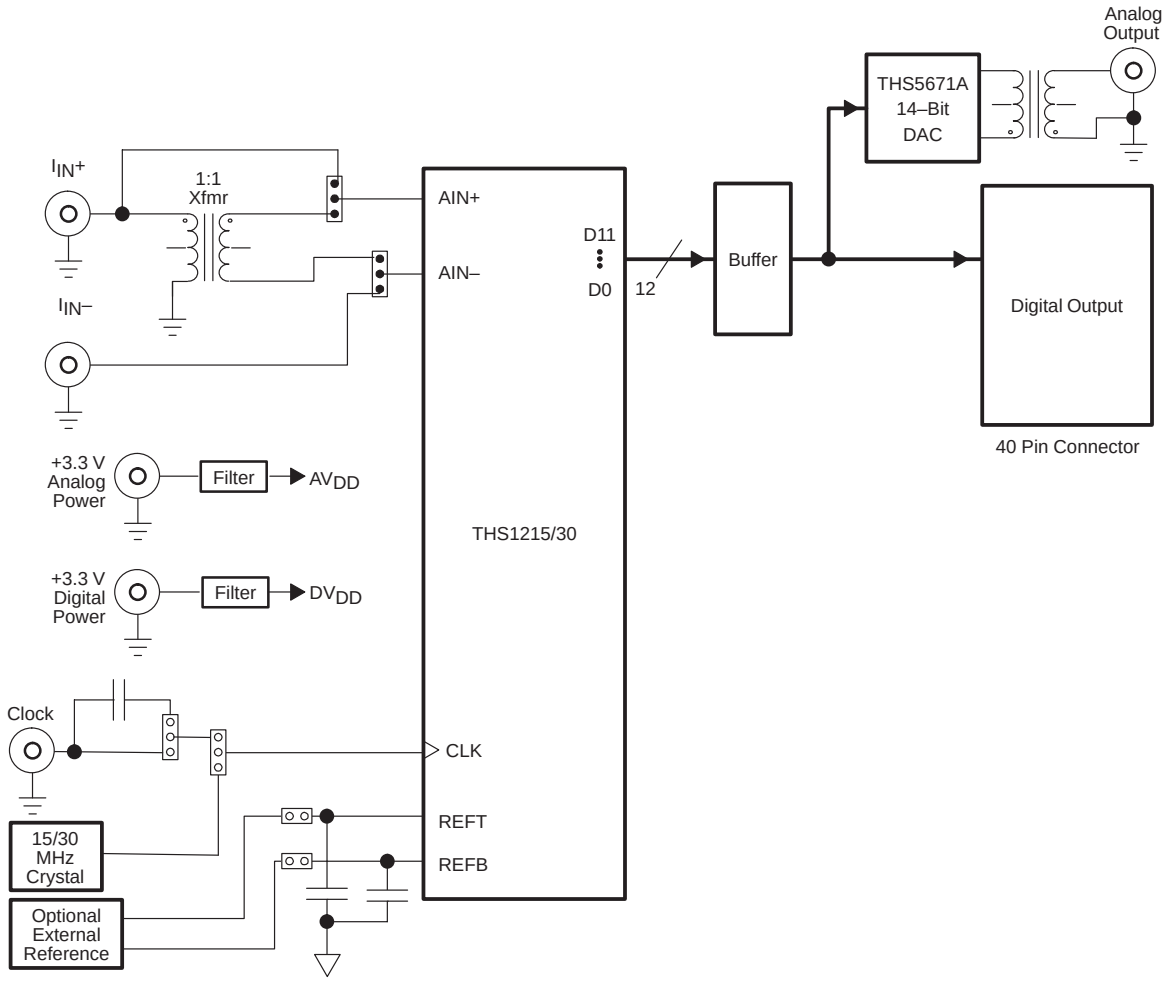
1.1 Purpose

The THS1215/30 EVM provides a platform for evaluating the THS1215/30 analog-to-digital converter (ADC) under various signal, reference, and supply conditions. The system block diagram is shown below. This illustration provides a general indication of the features and functions available. It should be used in combination with the circuit schematic supplied.

Figure 1–1. Block Diagram



1.2 EVM Basic Functions

Analog input to the ADC is provided via two external SMA connectors. The input can be configured onboard to be true differential, single-ended, or single-ended transformer coupled to the device.

The EVM provides an external SMA connection for input of the ADC clock. This can be configured to be either ac or dc-coupled. A crystal oscillator is provided on the board to perform this function, and can be used when required. Refer to the Internal Clock section for proper configuration and operation.

Digital output from the EVM is via a 40-pin connector. The digital lines from the ADC are buffered before going to this connector. More information on this connector can be found in the ADC output section.

Analog output from the EVM is via SMA connector J9. A THS5671A 14-bit DAC is used to recreate the analog signal from the ADC digital data. More information on this can be found in the ADC analog output section.

Power connections to the EVM are via 4mm banana sockets. Separate input connectors are provided for the analog and digital supply.

In addition to the internal reference provided by the THS1215/30 device, options are provided on the EVM to allow adjustment of the ADC reference via an onboard reference circuit. The reference voltages VRT and VRB for the THS1215/30 device are supplied by an LT1004-1.2 precision shunt voltage regulator, resistor network, TLV2464CD op amp, and two transistors. The LT1004-1.2 has initial accuracy of 0.33 % and a temperature coefficient (TC) of 20 ppm/°C, making the device a suitable voltage reference for a 12-bit ADC operating in a temperature controlled environment. Wide-range temperature operation requires a more precise voltage reference, such as the VRE3025.

1.3 Power Requirements

The EVM can be powered directly from a single 3.3 V supply. Provision is also made to allow the EVM to be powered with independent 3.3 V analog and digital supplies to provide higher performance.

Caution

Exceeding the 3.3 V maximum can damage EVM components. Under-voltage may cause improper operation of some or all of the EVM components.

1.4 THS1215/30 EVM Operational Procedure

The THS1215/30 EVM provides a flexible means of evaluating the THS1215/30 in a number of modes of operation. A basic set-up procedure, used as a board confidence check is as follows:

1) Verify all EVM jumper settings match the jumper configuration as listed in Tables 1-1 and 1-2.

2) Connect 3.3-V input power to the EVM J1 and J2, and GND to J8 and J3.

3) Switch power supplies on.

4) Use a function generator with 50-Ω output impedance to provide a 10 MHz, 1.5-V offset, 3-Vp-p amplitude square wave input signal to J4.

5) Use a function generator with 50-Ω output impedance to provide a 100-KHz, 0-V offset, 3-Vp-p amplitude sine wave input signal to J6.

6) The digital pattern on the output connector J5 represents a sine wave, and can be monitored using a logic analyzer. The output on connector J9 is a sine wave, and can be viewed using an oscilloscope.

Table 1–1. Two Pin Jumper List

Jumper	Function	Installed	Removed	Default
LNK4	Reference select	External	Internal	Removed
LNK1	External REFB feed	External	Internal	Removed
LNK38	External REFT feed	External	Internal	Removed
LNK3	Digital bus output enable	3-state bus	Active	Removed
LNK5†	Configuration Input 0	Mode LSB = 0	Mode LSB = 1	Removed
LNK2†	Configuration Input 1	Mode MSB = 1	Mode MSB = 0	Removed

† Table 4–1 describes the mode settings in detail

Table 1–2. Three Pin Jumper List

Jumper	Function	Jumper Location	Default
LNK 44	Internal oscillator External oscillator, AC coupled External oscillator, DC coupled	1-2 2-3 1-2	1-2
LNK 45	Internal oscillator External oscillator, AC coupled External oscillator, DC coupled	1-2 Removed 2-3	2-3
LNK 6	True differential or single-ended input Transformer coupled input	1-2 2-3	2-3
LNK 7	True differential or single-ended input Transformer coupled input	1-2 2-3	2-3
LNK 8	Transformer coupled input True differential or single-ended input	1-2 2-3	1-2

Chapter 2

Physical Description

This chapter describes the physical characteristics and PCB layout of the EVM and lists the components used on the module.

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2.1 PCB Layout

The EVM is constructed on a 4-layer, 125mm (4.9-inch) × 91mm (3.6-inch), 1,57 mm (0.062-inch) thick PCB using FR-4 material. Figures 2–1 through 2–5 show the component silkscreen and the individual layers of the printed-circuit board.

Figure 2–1. Component Silkscreen

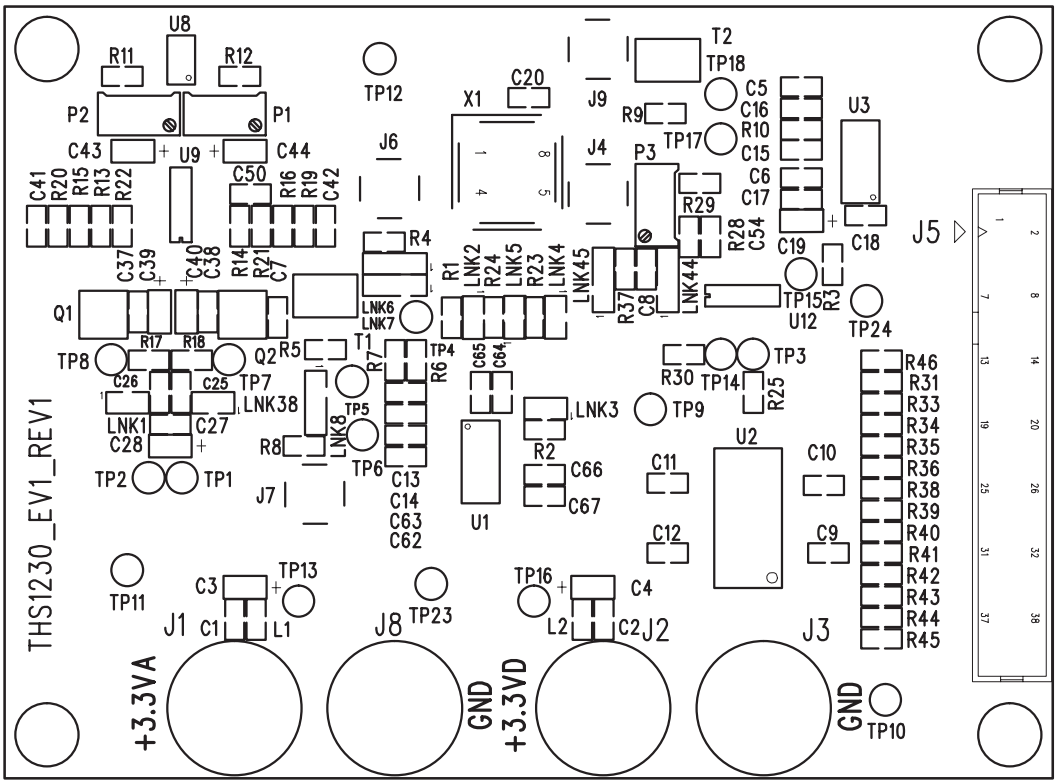


Figure 2–2. Top Layer

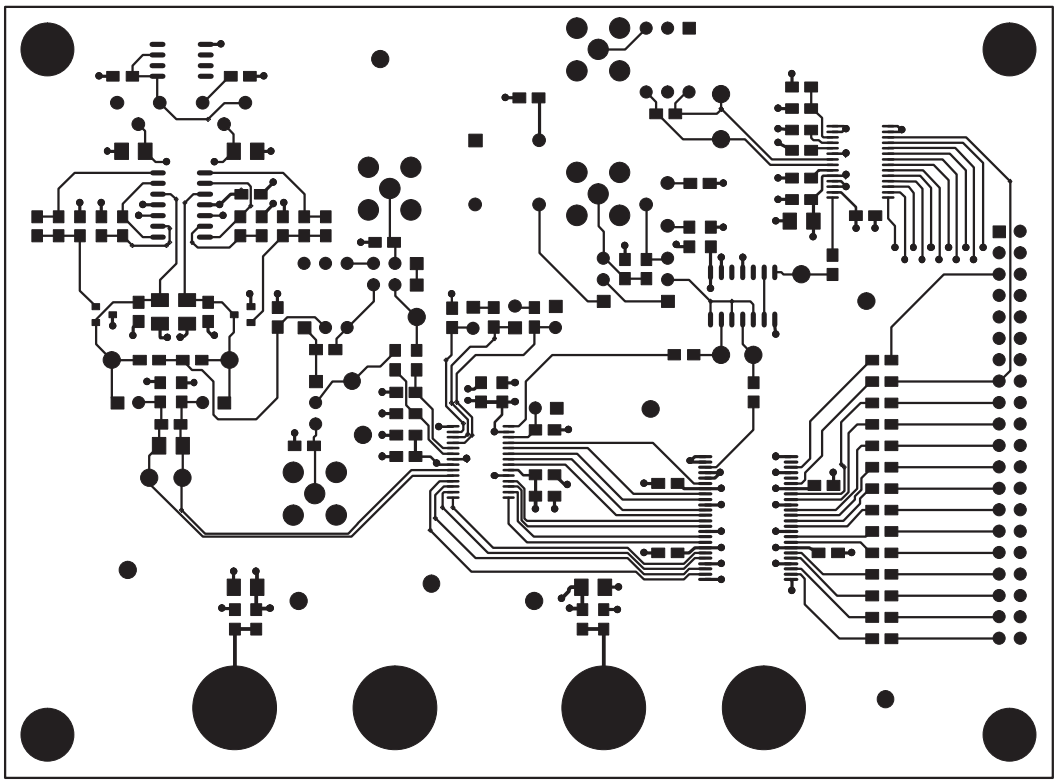


Figure 2–3. Inner Layer 1, Ground Plane

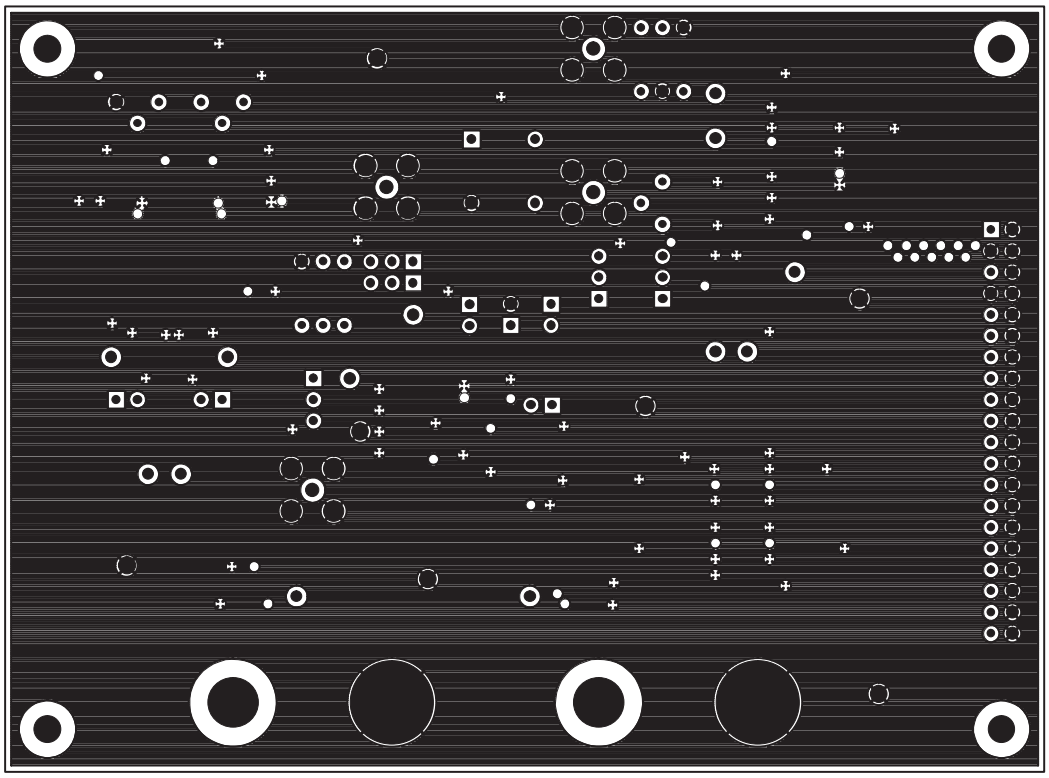


Figure 2–4. Inner Layer 2, Power Plane

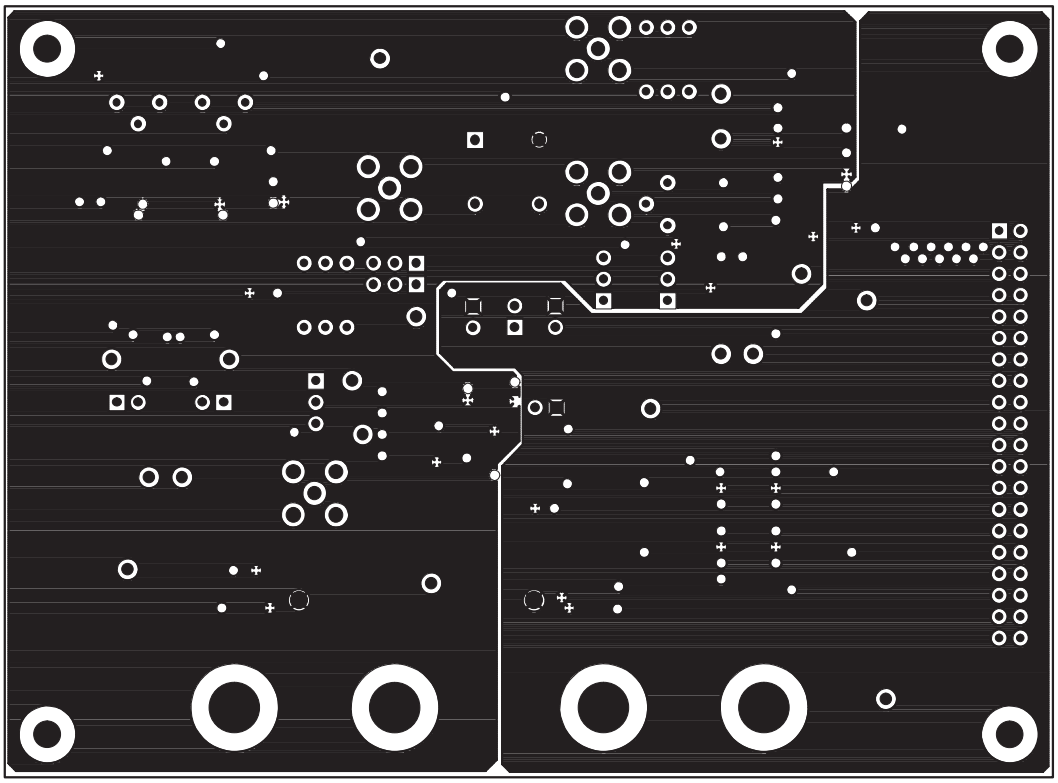
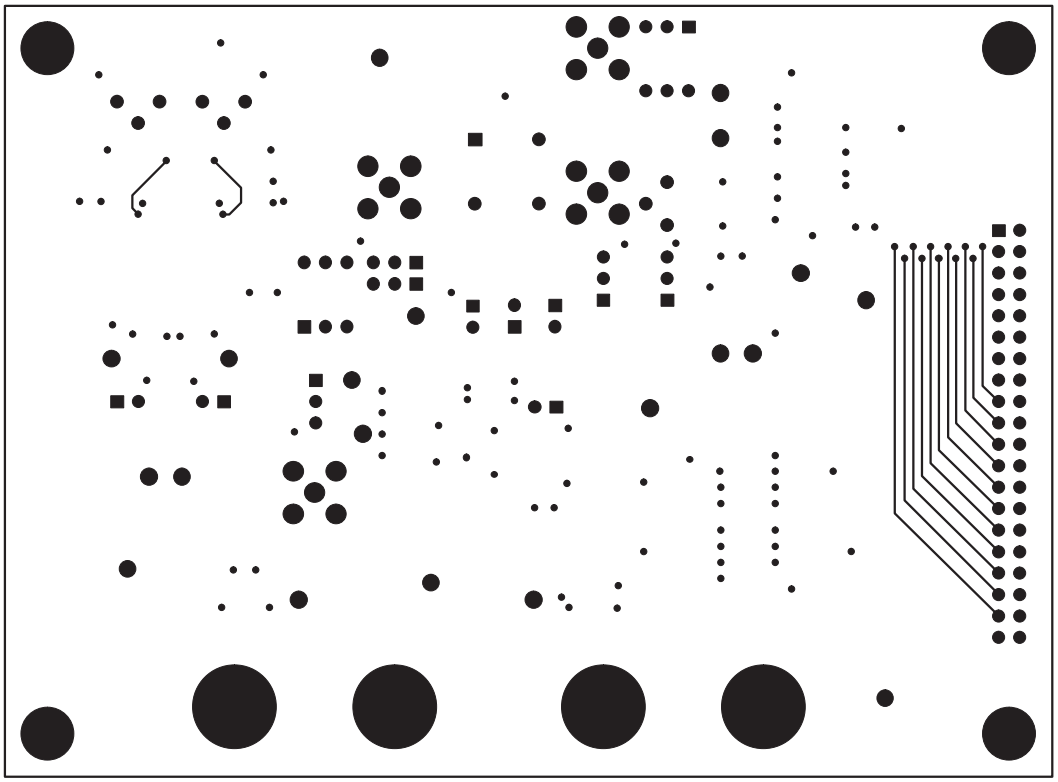


Figure 2–5. Bottom Layer



2.2 Parts List

Table 2–1 lists the parts used in constructing the EVM.

Table 2–1. Parts List

Qty	REF–DES	Description	Manufacturer	Part Number
26	C1–2, C5–12, C15, C17–18, C20, C25–27, C37–38, C41–42, C50, C54, C63, C65, C67	0.1 μF 0805 SMD ceramic capacitor 50 V X7R	Philips	08052R104K9B2
2	C13–14	Unpopulated site for 0805 SMD ceramic capacitor		
1	C16	0.01 μF 0805 SMD ceramic capacitor 50 V X7R	Philips	08052R103K9B2
8	C3–4, C19, C28, C39–40, C43–44	10 μF 10 V SMD tantalum capacitor case A	Kemet	T491A106K010AS
3	C62, C64, C66,	470 pF 0805 SMD ceramic capacitor 50 V NPO	Philips	0805CG471J9B2
4	J1–3, J8	4 mm noninsulated panel socket 16 A	Hirschmann	BO16
4	J4, J6–7, J9	SMA connector PCB mount 50 Ω vertical	Johnson Components	142–0701–206
1	J5	2×20 2.54 mm male PCB header LoPro vertical	Harting	09185407324
2	L1–2	0 Ω R 0805 resistor on 0805 ferrite bead site	Multicomp	772–227
6	LNK1–5, LNK38	1×2 PCB pin header 0.1“ vertical	Harwin	M20–9990205
5	LNK6–8 LNK44–45	1×3 PCB pin header 0.1“ vertical	Harwin	M20–9990305
2	P1–2	10 kΩ 3296Y potentiometer 0.5 W	Bourns	3296Y1103
1	P3	2 kΩ 3296Y potentiometer 0.5 W	Bourns	3296Y1202
1	Q1	MMBT3904 NPN bipolar transistor SOT23	Fairchild	MMBT3904
1	Q2	MMBT3906 PNP bipolar transistor SOT23	Fairchild	MMBT3906
1	R10	2 kΩ 0805 SMD chip resistor 1% 0.1 W	Multicomp	321–8090
1	R11	1 kΩ 0805 SMD chip resistor 1% 0.1 W	Multicomp	911–859
1	R12	1.5 kΩ 0805 SMD chip resistor 1% 0.1 W	Multicomp	911–872
4	R1–2, R23–24	47 kΩ 0805 SMD chip resistor 1% 0.1 W	Multicomp	912–050
1	R13	10 kΩ 0805 SMD chip resistor 1% 0.1 W	Multicomp	911–975
1	R14	15 kΩ 0805 SMD chip resistor 1% 0.1 W	Multicomp	911–999
2	R15–16	330 Ω R 0805 SMD chip resistor 1% 0.1 W	Multicomp	911–793
2	R17–18	180 Ω R 0805 SMD chip resistor 1% 0.1 W	Multicomp	911–768
2	R19–20	820 Ω R 0805 SMD chip resistor 1% 0.1 W	Multicomp	911–847
3	R21, R28–29	5.1 kΩ 0805 SMD chip resistor 1% 0.125 W	Rohm	MCR10EZHF5101
1	R22	11 kΩ 0805 SMD chip resistor 1% 0.125 W	Rohm	MCR10EZHF1102
17	R3, R25, R30–31, R33–36, R38–46	39 Ω R 0805 SMD chip resistor 1% 0.1 W	Multicomp	911–689
5	R4–5, R8–9, R37	49.9 Ω R 0805 SMD chip resistor 1% 0.125 W	Rohm	MCR10EZHF49R9
2	R6–7	0 Ω R 0805 SMD chip resistor 1% 0.1 W	Multicomp	772–239

Table 2–1. Parts List (Continued)

Qty	REF–DES	Description	Manufacturer	Part Number
2	T1–2	1:1 ratio 0.1–50 MHz transformer DIP	Mini-Circuits	TT1–6–X65
13	TP1–5, TP7–8, TP13–18	1.32 mm PCB test terminal red	W Hughes	100–107
7	TP6, TP9–12, TP23–24	1.32 mm PCB test terminal black	W Hughes	100–103
1	U1	THS1215 12-bit 15 MHz ADC THS1230 12-bit 30 MHz ADC	Texas Instruments	THS1215IPW THS1230IPW
1	U12	SN74HC14 Hex Schmitt inverter SO	Fairchild	MM74HC14M
1	U2	SN74ALVCH16244 16-bit low voltage driver SSO	Texas Instruments	SN74ALVCH16244DL
1	U3	THS5671 14-bit 125 MSPS current output DAC SSO	Texas Instruments	THS5671AIPW
1	U8	LT1004–1.2 1.2-V micropower voltage reference SO	Texas Instruments	LT1004–1.2
1	U9	TLV2464 quad low power rail-to-rail opamp SO	Texas Instruments	TLV2464CD
1	X1	3.3-V oscillator site DIL8	Golledge	GXO–U120H 15 MHz GXO–U120H 30 MHz

Chapter 3

Circuit Functionality

This chapter describes the function of the individual analog, digital, and power interface circuits of the ADC. Refer to the relevant data sheet for device operating characteristics.

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3.1 Analog Inputs

The ADC has either transformer-coupled input from a single-ended source, true differential analog inputs, or a single-ended input. These inputs are provided via SMA connectors J6 and J7 on the EVM, and can be configured in three ways as discussed in the following sections.

3.1.1 Differential Interface

For true differential input, the positive differential signal is connected to J6 and the negative differential signal is connected to J7. The jumper links on the board are then configured as follows: LNK6(1–2), LNK7(1–2), LNK8(2–3). The inputs have 50-Ω terminators.

3.1.2 Single-Ended Transformer-Coupled Interface

For transformer-coupled ADC input using a single-ended source, a positive signal is applied to connector J6. The jumper links on the board are then configured as follows: LNK6(2–3), LNK7(2–3), LNK8(1–2). Transformer T1 performs the single-ended to differential signal conversion. In this mode, the 50-Ω terminators R4 and R5 perform impedance matching to give the best distortion performance; but with the penalty that the source producing the input signal must be able to drive the 25-Ω load. A 50-Ω source can be used if R5 is removed from the board, with a resulting marginal increase in distortion.

3.1.3 Single-Ended Interface

For single-ended input, a positive signal is applied to connector J6. The jumper links on the board are then configured as follows: LNK6(1–2), LNK7(1–2), LNK8(2–3).

3.2 Digital Inputs

The THS1215/30 EVM utilizes jumpers for all digital inputs, with the exception of the clock. There are no connectors for setting the digital inputs. Refer to jumper Tables 1–1 and 1–2 in Chapter 1 for a description of the jumpers and their functions.

3.2.1 Internal Clock

The EVM provides flexibility as to the source of the ADC conversion clock.This clock can come from an external signal generator, as described in Section 3.2.2, or by enabling the onboard oscillator X1. Installing jumper LNK45 in pins 1-2 and LNK44 in pins 1-2, will direct clock oscillations from oscillator X1 to buffer U12. The EVM is shipped with external clock selected, LNK45 in pins 2-3, and LNK44 in pins 1-2.

3.2.2 External Clock

SMA Connector J4 can be used to input a clock signal to the board from an external source. If the source is not at the correct dc level for input to the MM74HC14M hex inverter IC (U12), then it can be ac coupled through C8, with the dc level trimmed using potentiometer P3 if necessary. The input source should be 50-Ω square wave signal with an amplitude of 3.3 V referenced to digital ground. This is the default setup for the EVM. A summary of the jumper link settings for the various clock options is shown in Table 3–1.

Table 3–1. Jumper Settings for Clock Options

Clock Options	Internal Oscillator	External Oscillator AC Coupled	External Oscillator DC Coupled
LNK44	1-2	2-3	1-2
LNK45	1-2	Removed	2-3

3.3 Analog Output

The ADC digital data is buffered and sent to a THS5671A 14-bit DAC. The outputs from the DAC are converted from current to voltage and from differential to single-ended , and made available on SMA connector J9. The THS5671A DAC latches the THS1215/30 data on the rising edge of DACCLK. For further information on the THS5671A, refer to the product folder on TI's website:

http://focus.ti.com/docs/prod/productfolder.jhtml?genericPartNumber=THS5671A

3.4 Digital Output

The data outputs from the ADC are buffered using a SN74ALVCH16244 before going to header J5 and feeding back into the DAC. Header J5 is a standard 40-pin device on a 100-mil grid, and allows easy connection to a logic analyzer. The outputs are 3.3 V LVTTL compatible. The connector pinout is listed in Table 3–2.

Table 3–2. Output Connector J5

J5 Pin	Name	Function	J5 Pin	Name	Function
1		NC	21	ADCDB03	DATA
2	GND	GND	22	GND	GND
3	GND	GND	23	ADCDB04	DATA
4	GND	GND	24	GND	GND
5	OUTCLKB	CLK	25	ADCDB05	DATA
6	GND	GND	26	GND	GND
7	GND	GND	27	ADCDB06	DATA
8	GND	GND	28	GND	GND
9		NC	29	ADCDB07	DATA
10	GND	GND	30	GND	GND
11		NC	31	ADCDB08	DATA
12	GND	GND	32	GND	GND
13		NC	33	ADCDB09	DATA
14	GND	GND	34	GND	GND
15	ADCDB00	DATA	35	ADCDB010	DATA
16	GND	GND	36	GND	GND
17	ADCDB01	DATA	37	ADCDB011	DATA
18	GND	GND	38	GND	GND
19	ADCDB02	DATA	39	ADCOVRNGB	OVFLOW IND
20	GND	GND	40	GND	GND

3.5 References

In addition to being able to use the internal reference of the ADC, a reference circuit has been included on the EVM. This uses a 1.2 V shunt reference diode (U8) as its primary source, and allows adjustment of the V_{REFT} and V_{REFB} signals to the ADC using potentiometers P1 and P2, respectively. Using a 2.7-V supply, the range of the external reference signals V_{REFT} is 0.60 V to 2.68 V, and V_{REFB}, is 0 V to 1.79 V. In order to use the ADC with external references, jumper links LNK1, LNK4, and LNK38 must be inserted. The maximum setting of the V_{REFT} and V_{REFB} signals to the ADC must never exceed the limits specified in the THS1215/30 data sheet.

3.6 Power

Power is supplied to the EVM via 4 mm banana sockets. For best performance, use a separate low-noise analog power supply connected to J1 (3.3 V) and J8 (GND). Use a separate low-noise digital power supply connected to J2 (3.3 V) and J3 (GND).

Chapter 4

Control Modes

This chapter describes the various features and functions of the THS1215/30.

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4.1 $\overline{OE}$

The $\overline{OE}$ pin is used for enabling the outputs of the ADC. The outputs are enabled with jumper LNK3 removed and are in 3-state configuration with the jumper link installed.

4.2 EXTREF

The EXTREF pin is used for selecting the internal or external reference to be used by the ADC. With jumper LINK4 removed, the device will operate using the internal reference source. With jumper LNK4 installed, the ADC will use the external reference voltages applied to pins REFT and REFB.

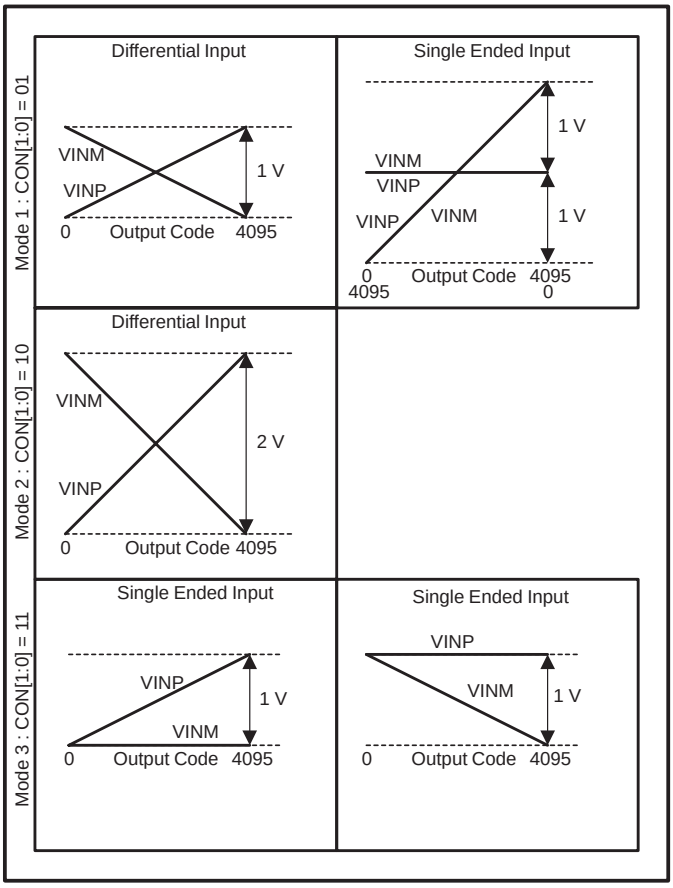
4.3 CON0 and CON1

The ADC has two mode pins, configuration Input 0 (CON0) and configuration input 1 (CON1). These control the input range and input configuration, i.e., differential or single ended input mode, of input pins VINP and VINM. Changing the gain of the on-chip PGA (programmable gain amplifier) controls the input range. The ADC mode of operation can be changed using jumper links LNK2 and LNK5 according to Table 4–1 and Figure 4–1.

Table 4–1. Mode Jumper Settings

CON1 (LNK2)	CON0 (LNK5)	Mode	Input Range (VINP–VINM)	Input Configuration	PGA Gain
0 (OUT)	1 (OUT)	1	±1 V	Differential/ Single Ended	X 1
1 (IN)	0 (IN)	2	±2 V	Differential	X 0.5
1 (IN)	1 (OUT)	3	1 V	Single Ended	X 2
0 (OUT)	0 (IN)	0	—	Device Power down	—

Figure 4–1. ADC Input Ranges

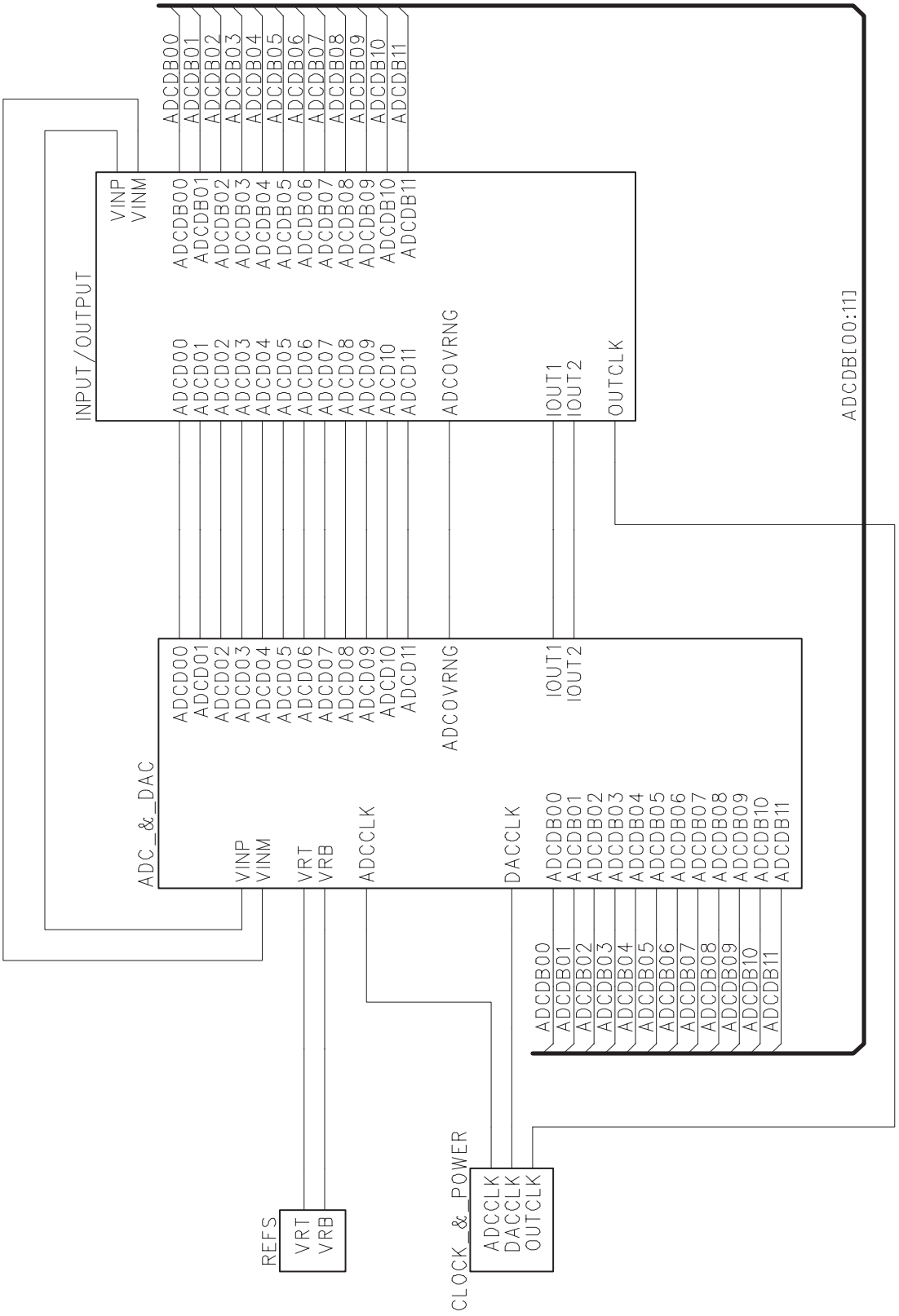


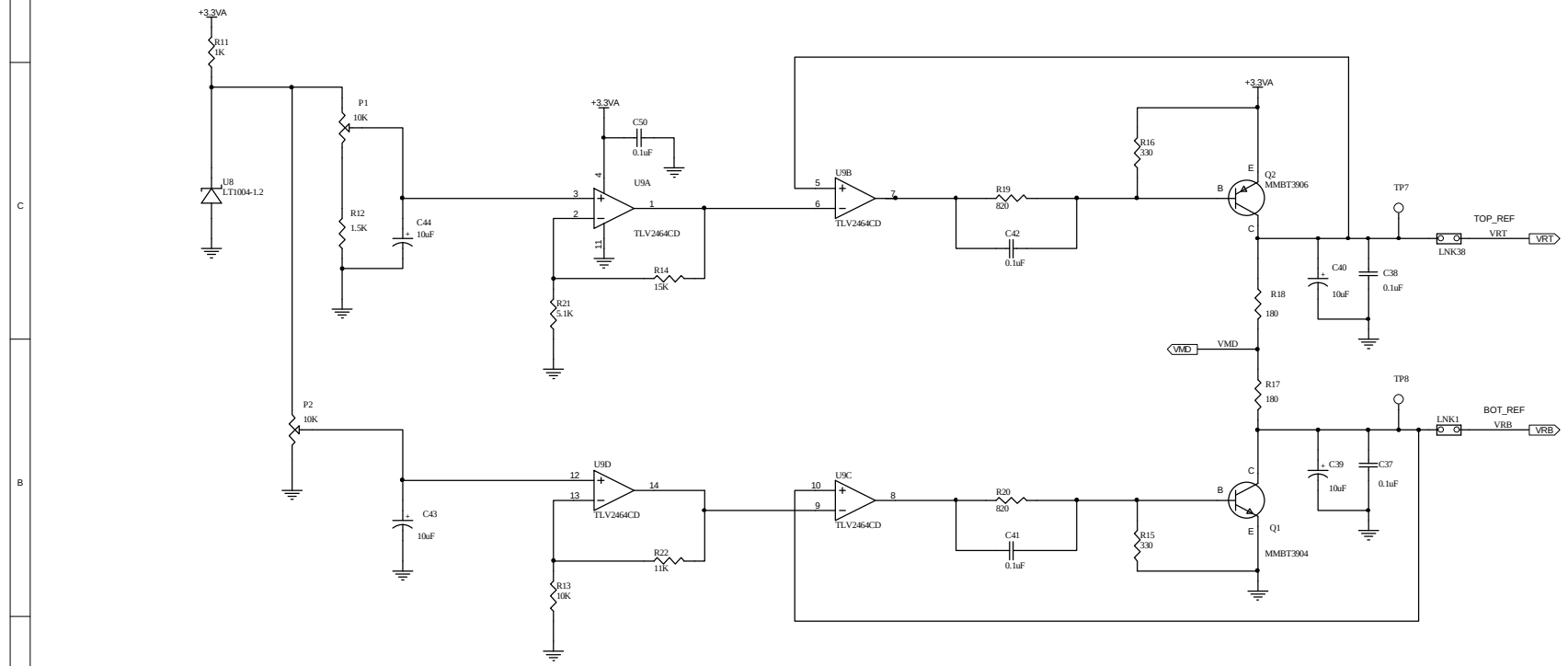
Appendix A

Schematics

This appendix contains the THS1215/30 EVM schematic diagrams.

Figure A–1. EVM Schematic Diagram—Functional Connectivity





Revision History		
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Drawn By:	SIZE: B	DATE: 29-Nov-2000
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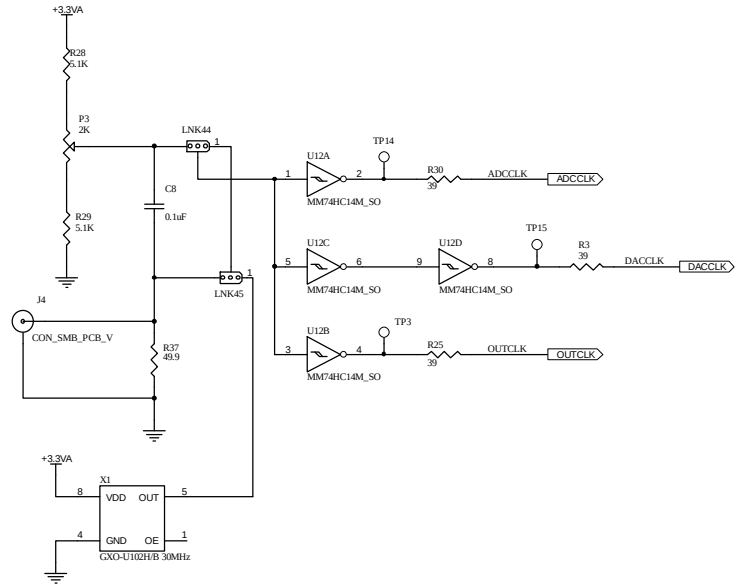

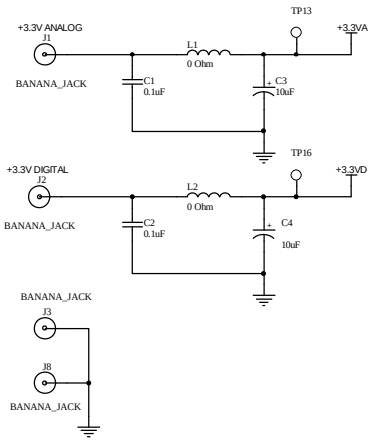

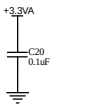

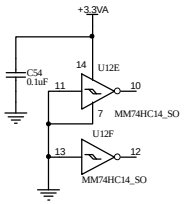

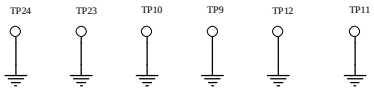

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Engineer:

Drawn By:

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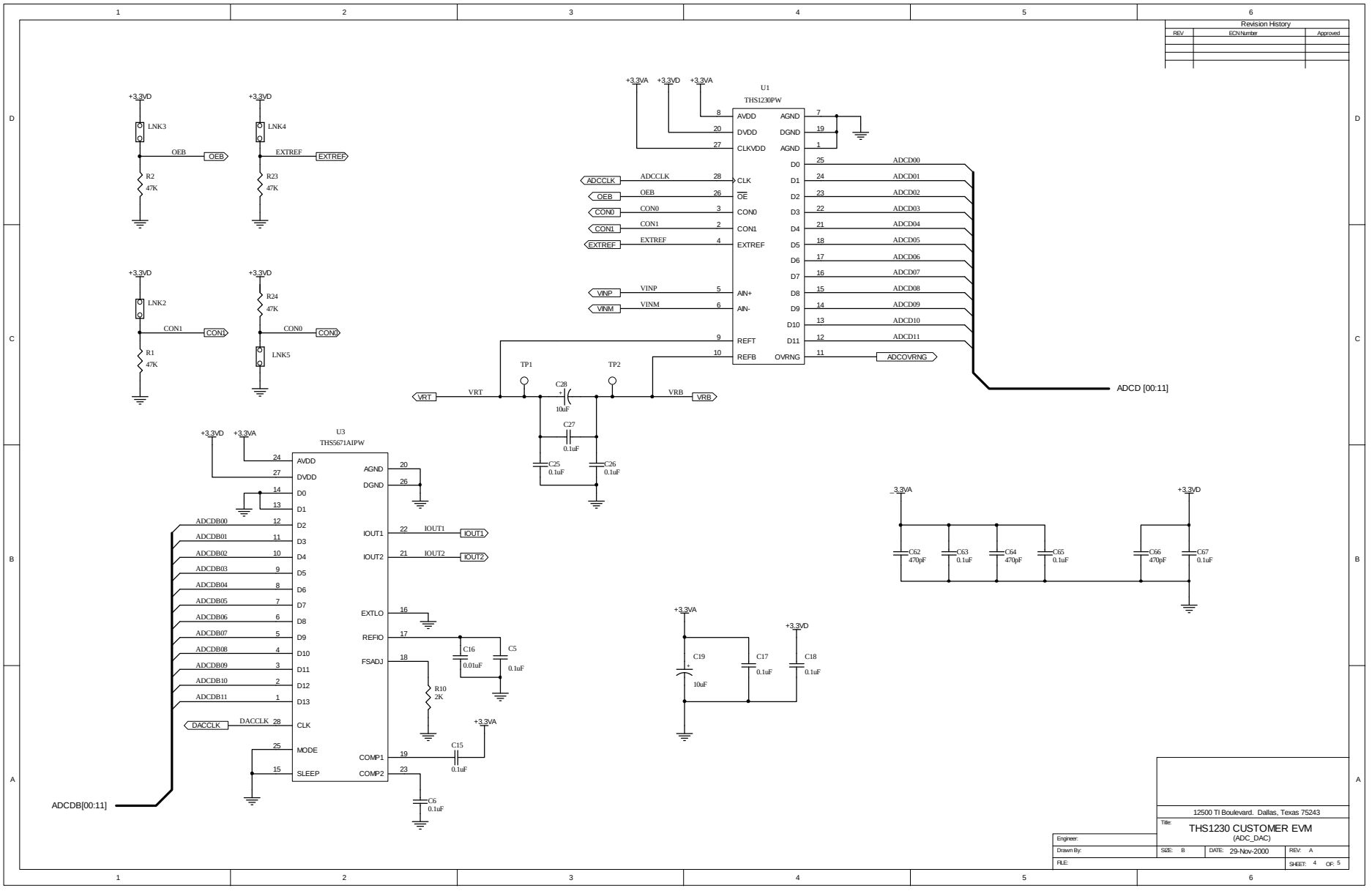
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R24 47K
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CON0
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VINM
VRT
VRB
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TP2
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C27 0.1uF
C25 0.1uF
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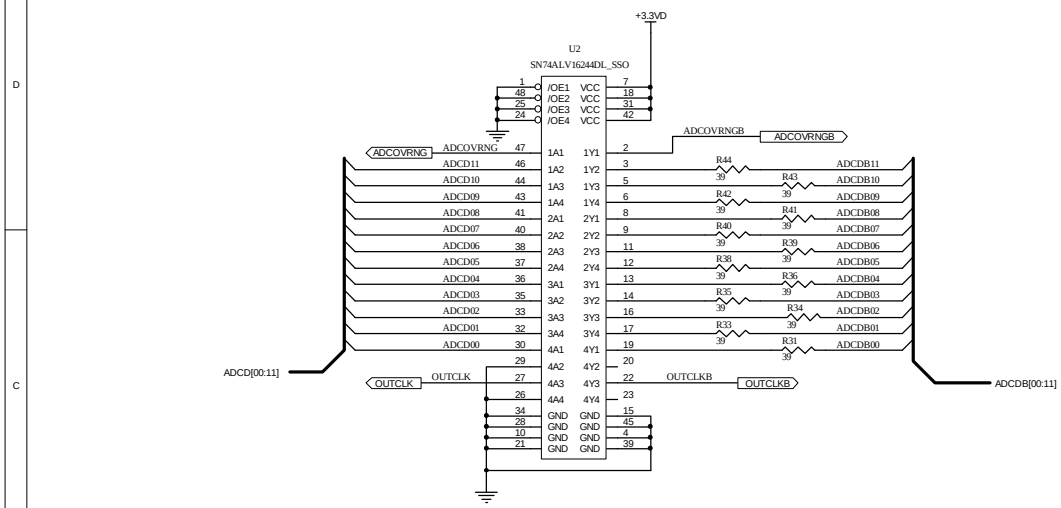
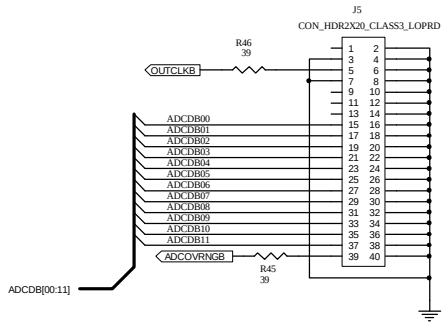
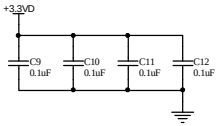
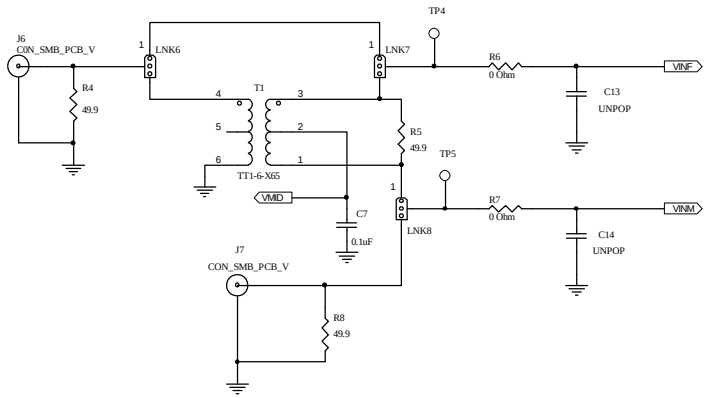
C15 0.1uF
C6 0.1uF
C19 10uF
C17 0.1uF
C18 0.1uF
C62 470pF
C63 0.1uF
C64 470pF
C65 0.1uF
C66 470pF
C67 0.1uF
ADCOVRNG
12500 TI Boulevard. Dallas, Texas 75243
THS1230 CUSTOMER EVM
(ADC_DAC)
Engineer:
Drawn By:
FILE:
SIZE: B
DATE: 29-Nov-2000
REV: A
SHEET: 4 OF: 5

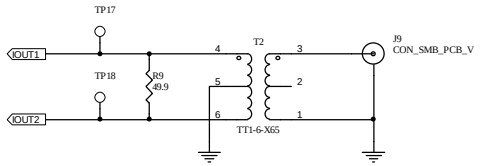
Revision History		
REV	ECN Number	Approved











Engineer:	12500 TI Boulevard. Dallas, Texas 75243		
Drawn By:	Title: THS1230 CUSTOMER EVM (INPUT_OUTPUT)		
FILE:	SIZE: B	DATE: 29-Nov-2000	REV: A
			SHEET: 5 OF: 5