TC35670FTG-006 Bluetooth® Smart + NFC Tag IC

Rev 2.1

Contents

1. General Description

1.1. Product Concept

TC35670FTG-006(Later omitted TC35670FTG.) is compliant with 2.4 GHz wireless communication Bluetooth® V4.1 Low Energy standard and has functions of NFC Forum Type 3 Tag (NFC Tag) equipped with FeliCa Contactless IC card Technology. With RF analog part and Baseband digital part, TC35670FTG provides Bluetooth® HCI (Host Control Interface) functions and Bluetooth Low Energy GATT profile functions defined in Bluetooth® specifications. Connected with external host processors, TC35670FTG realizes easy development of Bluetooth® Low Energy applications. Owing to the built-in ADC and GPIO's, stand-alone low power Bluetooth® application can also be realized. NFC Tag has a non-volatile memory (EEPROM) and provides a wireless interface which is compliant with NFC Forum Type 3 Tag standard and a wired interface by I^2C. EEPROM is accessed by the wired and wireless interfaces and includes 1520 bytes general user area. Data can be transferred from the wired interface to the wireless interface or from the wireless interface to the wired interface through a built-in RAM (Through mode function).

1.2. Features

- Compliant with Bluetooth® Ver4.1 Low Energy
  - Built-in Bluetooth® RF analog core and Baseband digital core
  - Built-in ARM7TDMI-S® core (Internal CPU clock 13 MHz)
  - On-chip Program Mask-ROM (320 KB)
  - On-chip Work RAM for Bluetooth® communication process (96 KB),
    On-chip RAM for application program storing (32 KB)
  - Supports patch program loader function
  - Supports sleep, deep sleep mode function.
- NFC Forum Type 3 Tag with wired interface
  - Built-in FeliCa Contactless IC Card Technology
  - Wireless interface: Automatic detection of transmission speed 212 kbps and 424 kbps
  - I^2C interface: Maximum operational clock 400 kHz
  - Built-in EEPROM: General user area 1520 bytes, Highly reliable program function prevents from programming an incomplete data, Writing time:5 ms(typ.), 1 bit error automatic correction , CRC automatic addition, and error detection of read data.
  - Security: Mutual authentication with Message authentication code (MAC).
    Read only, read and write, read after authentication, write after authentication and data write with MAC are supported.
- General Purpose IO (9 pins)
  - SPI interface (1 ch/General Purpose IO),I^2C interface (1 ch/General Purpose IO), UART interface (1 ch/General Purpose IO)
  - Host CPU Interface: UART interface (9600 bps to 921.6 kbps /General Purpose IO)
  - Built-in general purpose ADC(2 ch for external inputs , 1 ch for internal VDD detection)
  - Wake-up Interface (Wake-up input function from sleep and deep sleep /1 ch/General Purpose IO)
  - PWM Interface (1 ch/General Purpose IO)
- Base Clock Input
  - Built-in oscillator for external resonator connection (26 MHz)
  - Sleep Clock Input (External input supported 32.768 kHz)
- Built-in DCDC converter and LDO
  - Wide range of input power supply voltage supported
    (Supply voltage 1.8 to 3.6 V, Low-voltage detection for batteries,DCDC start more than 2.0 V)
- Package:
  - P-VQFN40-0606-0.50-001 [40 pin, 6 x 6 mm^2, 0.5 mm pitch, 0.9 mm thickness]

*FeliCa Technology refers to the following standards:

- JIS X 6319-4: Specification of implementation for integrated circuit (s) cards-Part 4: High speed proximity cards
- ISO/IEC 18092: Information technology -Telecommunications and information exchange between systems-Near Field Communication-Interface and Protocol-1(NFCIP-1)
- NFC Forum: http://www.nfc-forum.org/

2. Pin Function

2.1. Pin Assignment (Top View) ver. P-VQFN40-0606-0.50-001

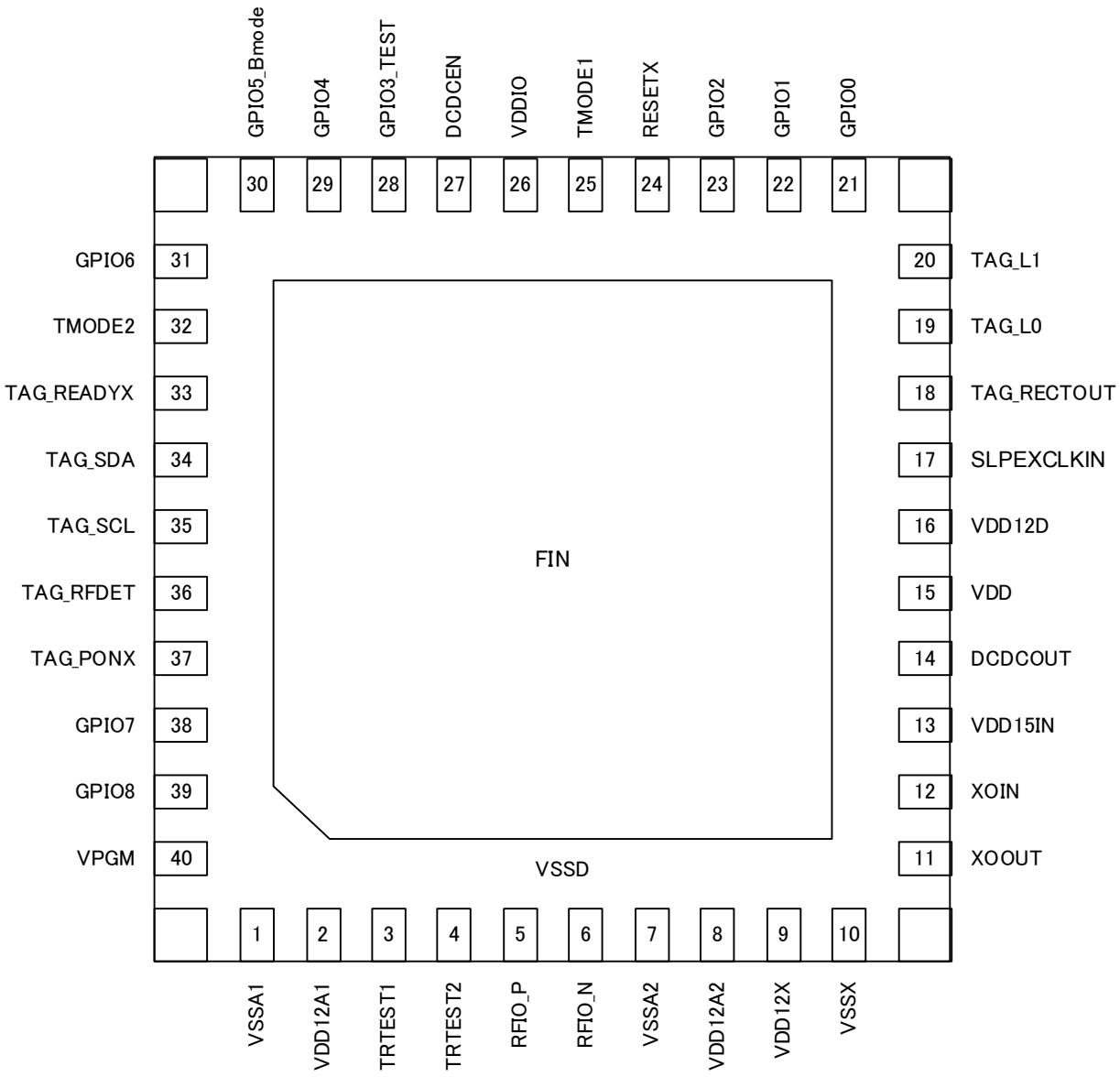


Figure 2-1 Pin Assignment (Top View)

2.2. Pin Function Descriptions

Table 2-1 shows attributes, input/output states for operating modes and descriptions for pin functions. Table 2-4 shows descriptions about power supply pins.

Table 2-1 Pin Functions

Pin name	Pin No	Attribute	Condition	Functional description
		VDD category Direction Type	Default (during reset)	
Reset interface				
RESETX	24	VDDIO IN Schmitt trigger	—	Hardware reset input pin. Low:Reset
DCDC enable pin				
DCDCEN	27	VDDIO IN Schmitt trigger	IN	DCDC enable pin. High level: internal DCDC is ON Low level: internal DCDC is OFF
Clock interface				
XOIN	12	VDD12X IN OSC	IN	Oscillator input pin for Baseband and RF reference clock (26 MHz) pin. OSC's frequency accuracy should be ±50 ppm. A feedback resistor is built in between XOIN pin and XOUT pin. This pin needs to be connected with the appropriate resistor and capacitor for the connected X'tal .
XOOUT	11	VDD12X OUT OSC	OUT	Oscillator output for Baseband and RF reference clock (26 MHz) pin A feedback resistor is built in between XOIN pin and XOUT pin. This pin needs to be connected with the appropriate resistor and capacitor for the connected X'tal .
SLPEXCLKIN	17	VDDIO IN OSC	IN	Sleep clock (32.768 kHz) input pin for low power consumption operation. Frequency accuracy of sleep clock should be ±500 ppm. When the clock is not supplied, this pin should be tied to GND.
RF interface				
RFIO_P RFIO_N	5 6	VDD12A IN/OUT Analog	Hi-Z	RF differential I/O pin. For external connection method of RF signal, please refer to the attached connection configuration example.
TAG Interface				
TAG_L0 TAG_L1	19 20	— IN/OUT Analog	Hi-Z	TAG Antenna coil connection pin

Pin name	Pin No	Attribute	Condition	Functional description
		VDD category Direction Type	Default (during reset)	
TAG_READYX	33	VDDIO OUT	OUT	Through mode ready output pin When data of Through mode is received through the wireless interface, this pin outputs low level. If response data is received through the wired interface, the level turns to the high level. When not used, this pin should be opened.
TAG_SDA	34	VDDIO IN/OUT Schmitt trigger	IN	I^2C interface for TAG This pin can act as SDA in I^2C. When not used, this pin should be fixed to Low level or High level.
TAG_SCL	35	VDDIO IN Schmitt trigger	IN	I^2C interface for TAG This pin can act as SCL in I^2C. When not used, this pin should be fixed to Low level or High level.
TAG_RFDET	36	VDDIO OUT	Pull down OUT	TAG Carrier detection pin If no TAG carrier, this pin becomes low level by Pull-down. If TAG wireless carrier is detected, this pin is cut off from Pull-down and becomes high level.
TAG_PONX	37	VDDIO IN Schmitt trigger	Pull up IN	TAG Power supply switch controlling and wired interface enable pin. In case of turning on power supply switch or using the wired interface, input low level. High level leads to turning off the power supply switch and disabling the wired interface When not used, this pin should be opened.

Pin name	Pin No	Attribute	Condition	Functional description
		VDD category Direction Type	Default (during reset)	
General purpose I/O port				
GPIO0	21	VDDIO IN/OUT Pull up/ Pull down Schmitt trigger	Hi-Z	General purpose I/O pin 0. During a reset and just after the reset release, this pin is set input-disabled. After the reset release, the firmware configures the pin function as wake up pin or general purpose IO pin. For sleep and deep sleep modes, after settings by firmware and external input, wake up function can be selected, which activates the chip. When not used, this pin should be pulled down to the ground with 100 kΩ resistor.
GPIO1	22	VDDIO IN/OUT Pull up/ Pull down Schmitt trigger	Analog	ADC input and I/O Pin1. During a reset, this pin is set input-disabled. After the reset is released, this pin is input-disabled with pull-up resistor off. Then, this pin is controlled by firmware. After configuration by processing of firmware, that configures pull-up or pull-down resistors. Then the pin can function as general ADC-input 1 or general purpose IO pin. When not used, this pin should be pulled down to the ground.
GPIO2	23	VDDIO IN/OUT Pull up/ Pull down Schmitt trigger	Analog	ADC input and I/O Pin 2. During a reset, this pin is set input-disabled. After the reset is released, this pin is input-disabled with pull-up resistor off. Then, this pin is controlled by firmware. After configuration by processing of firmware, that configures pull-up or pull-down resistors. Then the pin can function as general ADC-input 2, PWM output pin PWM0 or general purpose IO pin. When not used, this pin should be pulled down to the ground.

Pin name	Pin No	Attribute	Condition	Functional description
		VDD category Direction Type	Default (during reset)	
GPIO3_TEST	28	VDDIO IN/OUT Pull-up Pull-down Schmitt trigger	Pull-up	General purpose I/O pin 3. During a reset, this pin is set input-disabled with pull-up resistor on. It becomes IC manufacture test mode in a Low level input during the starting processing after reset release.Since Pull-up resistance checks the input level of a pin in the state of On, please use it to be set to open or a High level. By the start processing of after releasing the reset, UART1-TX, it will be set to the state of no Pull resistance.Then, in the case of host program download mode, assignment of UART1-TX is canceled, and Pull-up resistance is set up. This pin configures pull-up/pull-down resistance, GPIO input or output, UART1-TX (UART2-TX), or SPI-DOUT by a software process after normal starting. When not used, this pin should be opened.
GPIO4	29	VDDIO IN/OUT Pull-up Pull-down Schmitt trigger	Pull-up	General purpose I/O pin 4. During a reset, this pin is set input-disabled with pull-up resistor on. In the case of reset release in using of stand-alone, it is set to a state in UART1-RX without pull-up/pull-down resistance by the start-up processing. In use by a stand-alone, an external pull-up is always required. And, in the case of host connection, please do not open or fixed to the Low level at the time of start-up. Then, in the case of host program download mode, assignment of UART1-RX will be canceled, and Pull-up resistance will be set up. This pin configures pull-up/pull-down resistors, and general purpose IO, UART1-RX (UART2-RX), or SPI-DIN by a software process after normal starting.When setting up as UART1-RX (UART2-RX), cautions are required so that the pin may not be fixed to the Low level. (Please confirm firmware specifications for details.)

Pin name	Pin No	Attribute	Condition	Functional description
		VDD category Direction Type	Default (during reset)	
GPIO5_Bmode	30	VDDIO IN/OUT Pull up/ Pull down Schmitt trigger	Pull up	General purpose I/O pin 5. During a reset, this pin is input-disabled with pull-up resistor on. High input during power up sequence after reset enables host program download mode. (In case of the pin in open will be the High-level input by the internal pull-up.) After normal power up sequence with low input after reset, the firmware configures pull-up/pull-down resistors and general purpose IO, UART1-RTSX, UART2-TX (UART1-TX), or SPI chip select output pin SCS. If this pin is always set to the Low level, the current will flow through the internal pull-up resistor. Please remove the pull-up resistor by the setting command after starting by the normal mode as processing which reduces this current. (Please confirm firmware specifications for details.)
GPIO6	31	VDDIO IN/OUT Pull-up Pull-down Schmitt trigger	Pull-up	General purpose I/O pin 6. During reset, this pin is input disabled with pull-up resister on. After reset, firmware configures pull-up/pull-down resistors and the pin can function as GPIO, UART clear to send pin UART1-CTSX, UART data receiver pin UART2-RX (UART1-RX), or SPI data clock output pin SCLK. When not used, this pin should be opened. When using as UART2-RX (UART1-RX), cautions are required so that the pin may not be fixed to the Low level.
GPIO7	38	VDDIO IN/OUT Pull-up Pull-down Schmitt trigger	Pull-up	General purpose I/O pin 7. During reset, this pin is input disabled with pull-up resister on. After reset, the firmware configures pull-up/pull-down resistors and the pin can function as GPIO, I2C-SCL pin, or SPI data output pin DOUT When not used, this pin should be opened.
GPIO8	39	VDDIO IN/OUT Pull-up Pull-down Schmitt trigger	Pull-up	General purpose I/O pin 8. During reset, this pin is input disabled with pull-up resister on. After reset, the firmware configures pull-up/pull-down resistors and the pin can function as GPIO, I2C-SDA pin, orSPI data input pin DIN. When not used, this pin should be opened.

Pin name	Pin No	Attribute	Condition	Functional description
		VDD category Direction Type	Default (during reset)	
IC test interface				
TMODE1 TMODE2	25 32	VDDIO IN Schmitt trigger	—	Test mode setting pins These pins are used for IC manufacturing test and need to be connected to GND when assembled on a board.
TRTEST1 TRTEST2	3 4	VDD12A IN/OUT Analog	—	Analog test pins. These pins are used for IC manufacturing test and need to be connected to GND when assembled on a board.
TAG_RECTOUT	18	— OUT Analog	Hi-Z	Rectification circuit output pin A signal receiving from TAG wireless interface, output from the rectification circuit can be monitored. When not used, this pin should be opened.

2.3. GPIO function list

GPIO pins can be assigned to UART I/Fs, serial memory I/Fs or some other functions by TC35670FTG firmware or command from external Hosts. Table 2-2 shows available functions for each GPIO pin, and Table 2-3 examples of GPIO function settings.

Table 2-2 Available functions for GPIO

Pin	Analog input	Function 1	Function 2	Function 3	Function 4	Function 5
GPIO0	—	GPIO Digital I/O	Wake Up Input	—	—	—
GPIO1	ADC1 Input	GPIO Digital I/O	—	—	—	—
GPIO2	ADC2 Input	GPIO Digital I/O	PWM0 Output	—	—	—
GPIO3_TEST	—	GPIO Digital I/O	UART1-TX Output	—	SPI-DOUT Output	UART2-TX Output
GPIO4	—	GPIO Digital I/O	UART1-RX Input	—	SPI-DIN Input	UART2-RX Input
GPIO5_Bmode	—	GPIO Digital I/O	UART1-RTSX Output	UART2-TX Output	SPI-SCS Output	UART1-TX Output
GPIO6	—	GPIO Digital I/O	UART1-CTSX Input	UART2-RX Input	SPI-SCLK Output	UART1-RX Input
GPIO7	—	GPIO Digital I/O	—	I2C-SCL Output	SPI-DOUT Output	—
GPIO8	—	GPIO Digital I/O	—	I2C-SDA I/O	SPI-DIN Input	—

Note: Can be selected either GPIO8 or GPIO4 and GPIO7 or GPIO3_TEST, SPI-DOUT, SPI-DIN is, can not be set for dual.

Table 2-3 GPIO function list (example)

Pin name	Basic example	Example of UART1 + UART2 + I^2C	Example of SPI + I^2C	Example of UART + SPI
GPIO0	Wake Up	Wake Up	Wake Up	Wake Up
GPIO1	ADC- AIN1	ADC- AIN1	ADC- AIN1	ADC- AIN1
GPIO2	ADC-AIN2	ADC-AIN2	ADC-AIN2	PWM0
GPIO3_TEST	UART1-TX	UART1-TX	SPI-DOUT	UART1-TX
GPIO4	UART1-RX	UART1-RX	SPI-DIN	UART1-RX
GPIO5_Bmode	UART1-RTSX	UART2-TX	SPI-SCS	SPI-SCS
GPIO6	UART1-CTSX	UART2-RX	SPI-SCLK	SPI-SCLK
GPIO7	I2C-SCL	I2C-SCL	I2C-SCL	SPI-DOUT
GPIO8	I2C-SDA	I2C-SDA	I2C-SDA	SPI-DIN

Note: There are other functions than the above examples. About the detail of the other functions, refer to TC35670FTG firmware specification.

2.4. Power Supply Pins

Table 2-4 shows the attributes and descriptions of power supply pins for normal operations.

Table 2-4 Power supply pins

Pin name	Pin number	Attribute	Description
		Type VDD/GND	
VDD/GND			
VPGM	40	TEST —	Test pin VPGM should be connected to GND directly.
VDD	15	DCDCIN VDD	Power supply pin for DCDC and sleep circuit. When internal DCDC is not used, this pin needs to be connected to the power supply.
VDDIO	26	Digital VDD	Power supply pin for GPIO and TAG. This pin inputs the voltage for supply to the GPIO pin.
DCDCOUT	14	DCDCOUT —	DCDC output pin. Connect to VDD15IN pin.
VDD15IN	13	LDOIN VDD	Power supply pin for internal regulator. When DCDCEN pin is connected to VDD, this pin needs to be connected to DCDCOUT. When DCDCEN pin is connected to GND, this pin needs to be connected to external power supply.
VDD12A1	2	Analog VDD	LDO output 1.2 V is supplied to internal analog circuit. A capacitor of 0.1 μF or more at the operating temperature range needs to be connected as the load of the LDO.
VDD12D	16	Digital VDD	LDO output 1.1 V is supplied to internal digital circuit. A capacitor of 0.1 μF or more at the operating temperature range needs to be connected as the load of the LDO.
VDD12X	9	Analog VDD	LDO output 1.2 V is supplied to internal OSC circuit. A capacitor of 0.1 μF or more at the operating temperature range needs to be connected as the load of the LDO.
VDD12A2	8	Analog VDD	LDO output 1.2 V is supplied to internal analog circuit. A capacitor of 0.1 μF or more at the operating temperature range needs to be connected as the load of the LDO.
VSSA1	1	Analog GND	GND pin for analog, this pin needs to be connected to GND.
VSSA2	7	Analog GND	GND pin for analog, this pin needs to be connected to GND.
VSSX	10	Analog GND	GND pin for OSC, this pin needs to be connected to GND.
VSSD	FIN	Digital GND	Die pad and Fin. Connect the exposed Die Pad and Fin portion to digital GND.

3. System Configuration

3.1. Block Diagram

Figure 3-1 shows block diagram of TC35670FTG.
TC35670FTG is powered by single voltage between 1.8 V and 3.6 V.
The chip has built-in DCDC and LDO requiring external capacitors.
It uses 26 MHz base clock and 32.768 kHz sleep clock.
External Memory Interface is SPI or I^2C, and host CPU interface is UART.
TAG uses the I^2C interface that is separate from the serial memory connection.

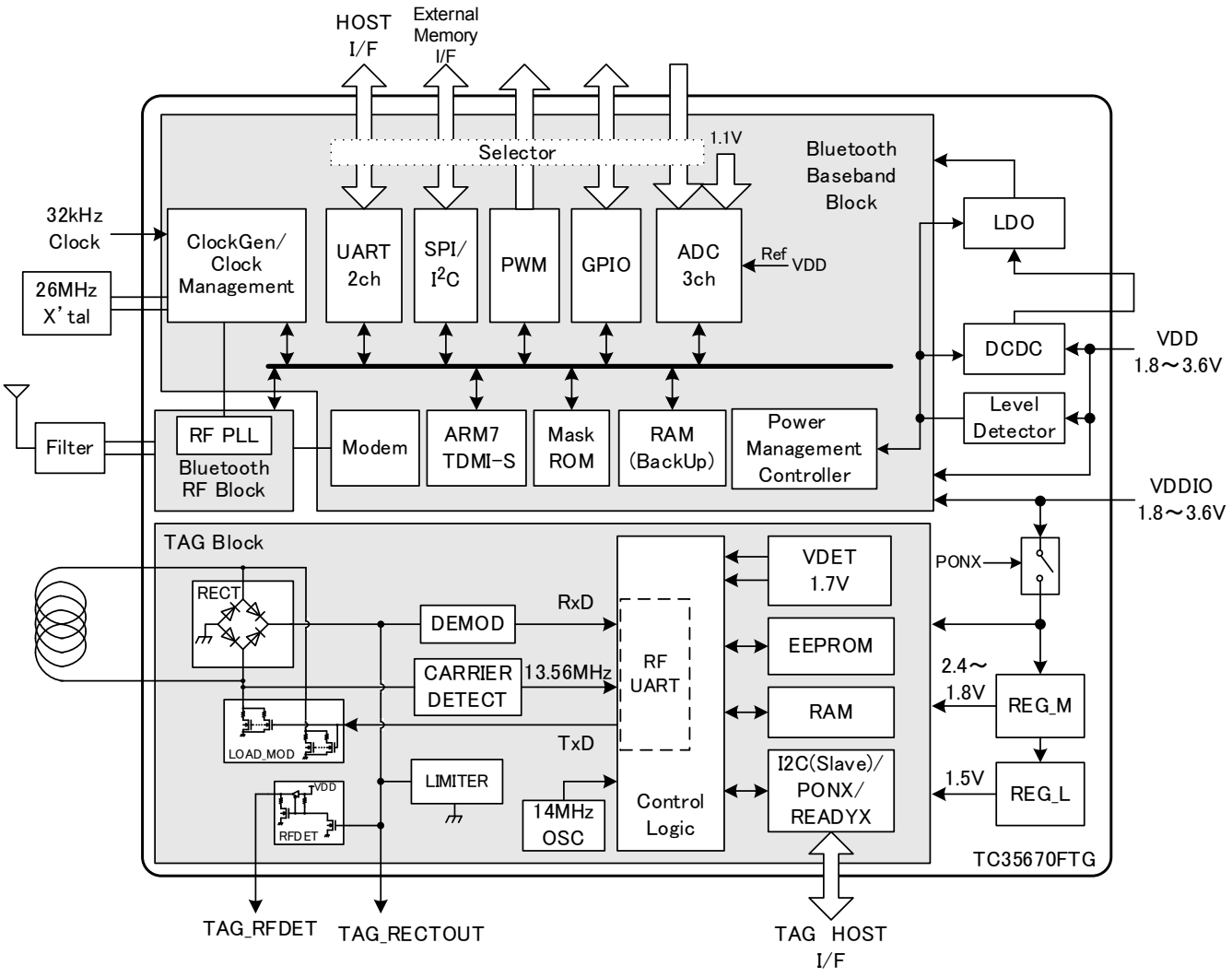


Figure 3-1 Example of TC35670FTG system configuration

4. Hardware Interfaces

4.1. Reset Interface (Power up sequence)

4.1.1. Features

Reset interface has the following features.

- 1.8 to 3.6 V operation
- Level sensitive asynchronous reset (Low level: reset)

The reset signal should be at reset status (RESETX = Low) when the power is turned on. Once the power supply has become stable, disabling the reset signal (RESETX = High) starts the X'tal oscillation after DCDC output has become stable If DCDC is used, or after each LDO output has reached its target voltage. Then, an internal timer releases internal reset 1 ms after the X'tal oscillation has become stable.

4.1.2. Connection Example

Figure 4-1 shows connection example where TC35670FTG is RC time constant circuit.
Reset signal can be given by RC time constant circuit on the power-supplied, or can be connected with an IC which has asynchronous and level sensitive reset function. Figure 4-2 shows the timings to reset and reset-release for the power supply.

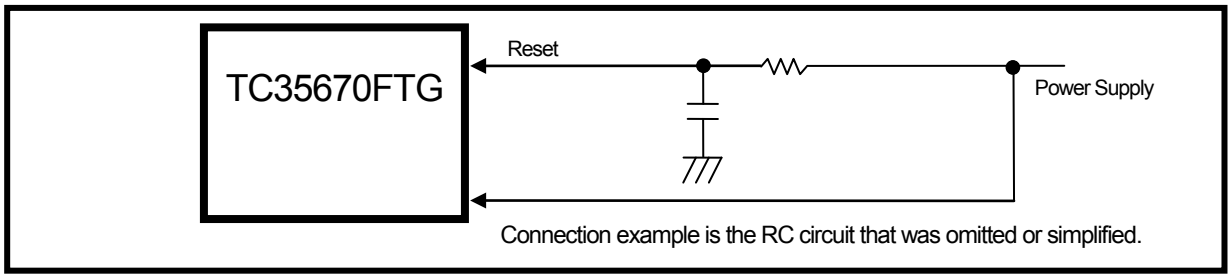


Figure 4-1 Reset signal connection example

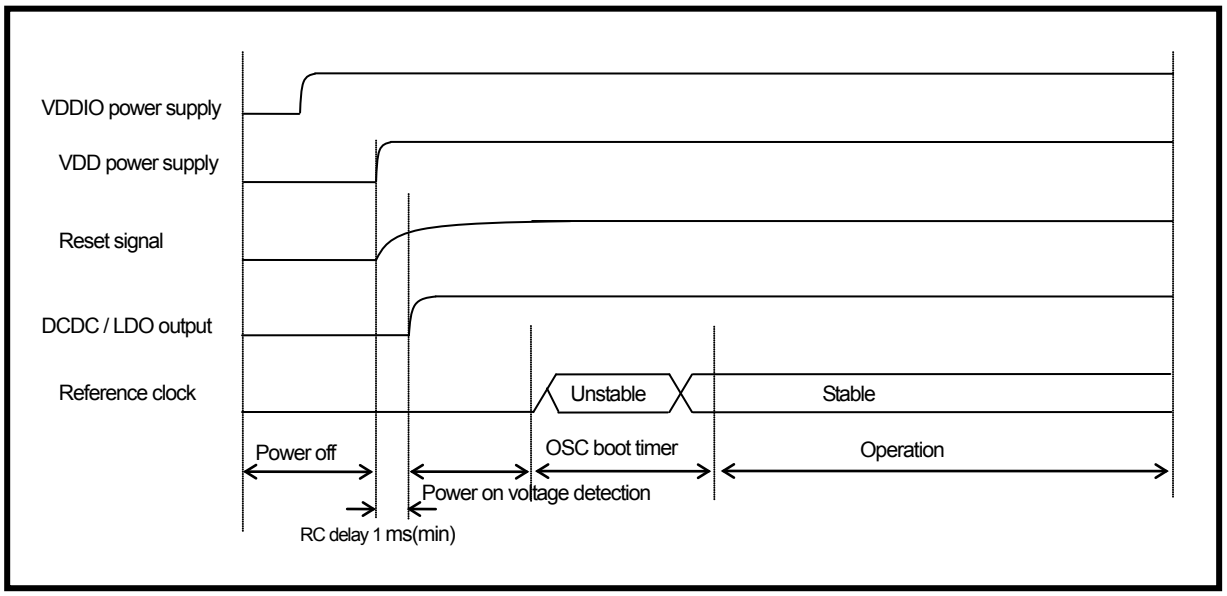


Figure 4-2 Power-on reset release sequence

4.2. UART Interface

4.2.1. Features

TC35670FTG UART interface has the following features.

- 1.8 to 3.6 V operation
- Full-duplex start-stop synchronization data transfer (RX, TX)
- Selectable between 2-line start-stop synchronous transfer (Reception data and Transmission data) and 4-line start-stop synchronous transfer (Reception data, Transmission data, Reception flow control, and Transmission flow control).
- Start bit field(1 bit),Data bit field(8 bits LSB first),Stop bit field(1bit),No parity bit
- UART transmit and receive data pins can be switched by the command of HCI mode. (UART2 function)
- Programmable baud rate setting (9600 bps to 921.6 kbps) (Only 9600 bps is available for UART2.)
- 12 (or more) character interval should be inserted between one transmission message and another transmission message. The length of the interval can be changed by a command.
- Error detection (character timeout, overrun error, framing error)
- Host wake-up function

TC35670FTG communicates commands, status, and data with a host CPU through UART interfaces.
The UART interfaces are shared with GPIO pins. GPIO pins may functioned as a 2-wire system UART interface pins that are assigned by the Boot process after reset release. The UART interfaces can operate at 1.8 to 3.6 V depending on the VDDIO power supply voltage. Sharing the power supply pins with other hardware interfaces, they cannot operate at a different voltage from the one other hardware interfaces operate at.

Table 4-1 UART function summary

	PIN setting	Baud rate	Flow Control	Host wake-up
UART1	GPIO3: Transmitted data (TX) GPIO4: Received data (RX)	Default 115.2 kbps 9600 to 921.6 kbps	**Disabled by default.** GPIO5: Receive flow control (RTSX) GPIO6: Transmission flow control (CTSX)	**Disabled by default.** This function can be set to GPIO pins on the command. Default 10 ms
UART2	**Disabled by default.** GPIO5: Transmitted data (TX) GPIO6: Received data (RX) *The UART2, it can be used in HCI mode, but can not be used simultaneously with UART1.	9600 bps	Unsupported	Unsupported

4.2.2. Connection Example

TC35670FTG UART can be connected with an UART interface on a host MCU. Figure 4-3 shows two-wire start-stop synchronization data transfer (RX, TX) connection example with an external host CPU. The timing chart to assign the GPIO pins to the UART function is shown in Figure 4-4.

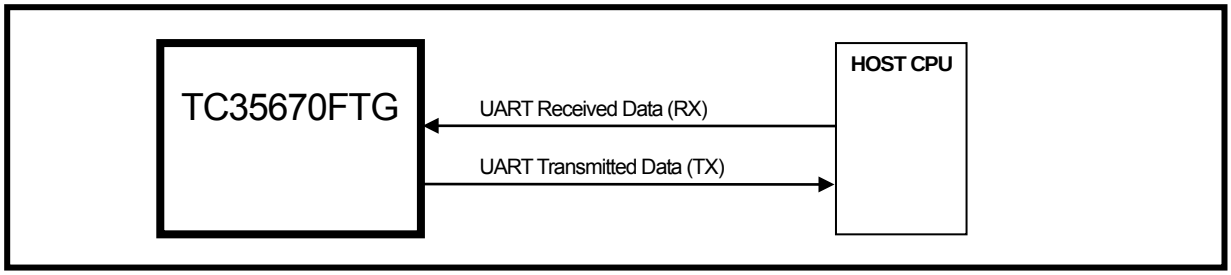


Figure 4-3 UART connection example

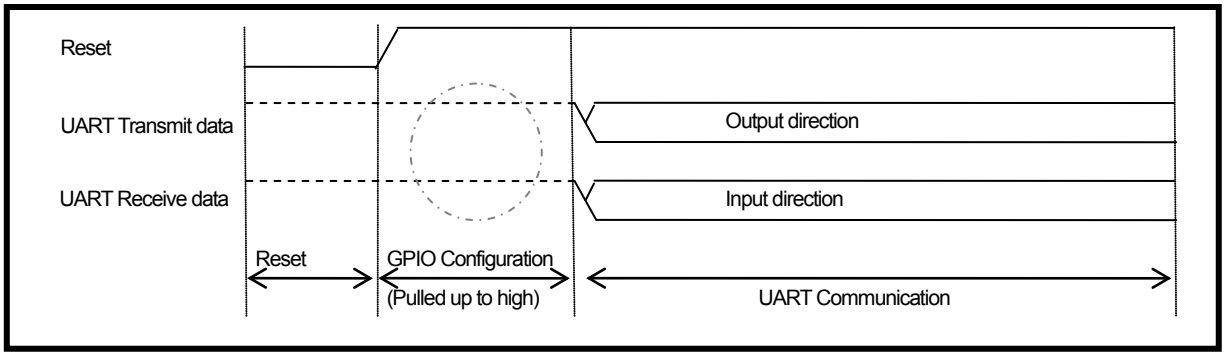


Figure 4-4 UART function assignment

4.2.3. Frame Format

TC35670FTG supports the following format.

- Number of data bits: 8 bits (LSB first)
- Parity bit: no parity
- Stop bit: 1 stop bit
- Flow control: RTSX/CTSX NOTE: Flow control is enabled only possible for UART1 in command.

Figure 4-5 shows UART data frame.

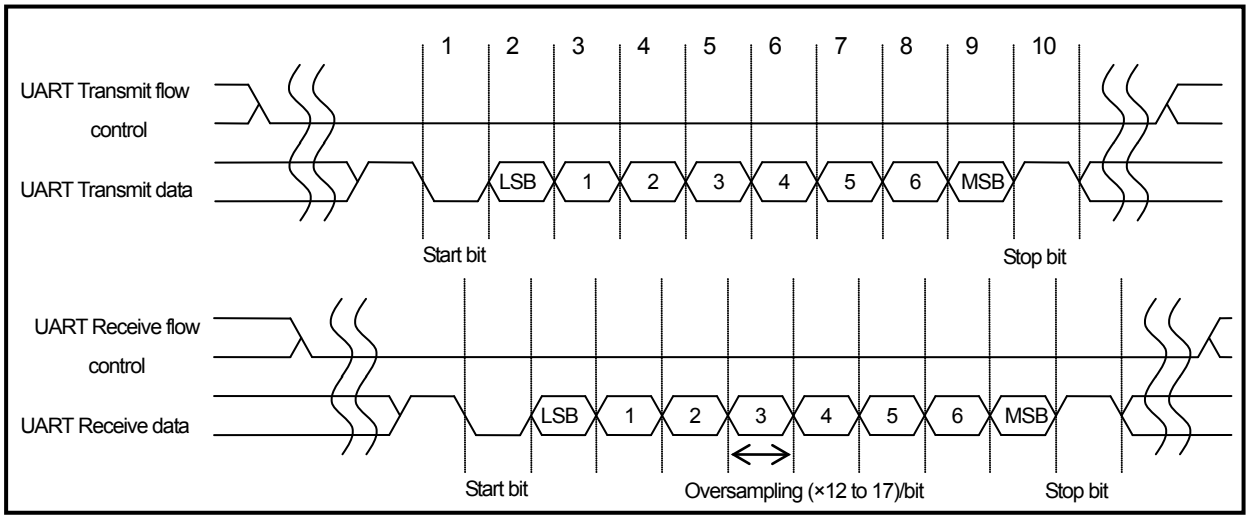


Figure 4-5 UART data frame

4.2.4. Host Wake up Function

TC35670FTG can wakes up its host before sending UART data to the host. This function is disabled by default, but can be assigned to GPIO by command. Host wake up time can be changed by command (10 ms by default).

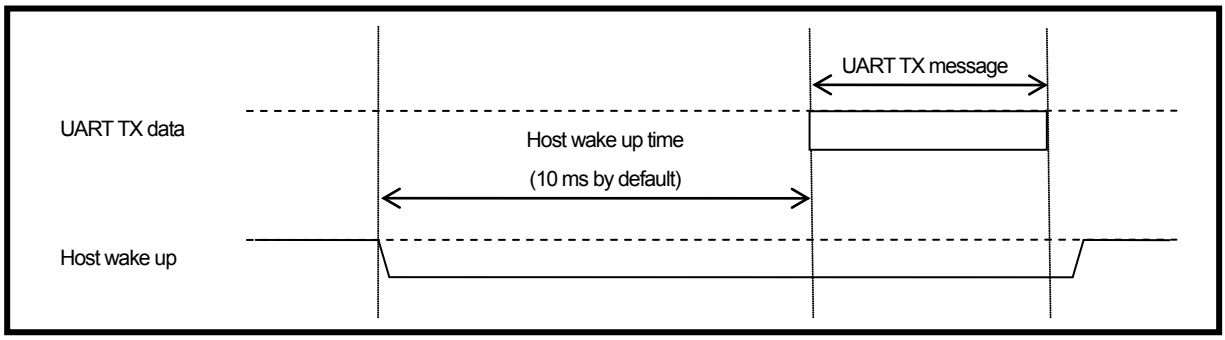


Figure 4-6 Host wake up

4.2.5. HCI mode

When TC35670FTG is used in the HCI mode, UART is the host interface to receive HCI commands.
The Bluetooth® wireless performance can be tested in HCI mode by the measurement equipment which connects the UART directly.

4.2.5.1. HCI Reset

Sends a HCI reset command from the host, at least 150μs from the command complete event can be processed the following command successfully.

4.3. SPI Interface

4.3.1. Features

TC35670FTG has the following main features for a serial memory interface

- Operation voltage: 1.8 to 3.6 V
- SPI interface
  - Chip select: 1 channel
  - Chip select polarity: High-active, Low-active
  - Serial clock master operation: Polarity and phase are adjustable (one out of four options can be selectable)
  - Serial clock frequency: 25 kHz to 6.5 MHz
  - Serial data transfer mode: MSB-first, LSB-first

SPI interface can operate at 1.8 to 3.6 V depending on VDDIO, however, cannot operate at different voltage from ones other interfaces are operate at.

4.3.2. Connection Example

Serial EEPROMs and serial Flash-ROMs can be connected to TC35670FTG SPI interface.
TC35670FTG has one chip select port. Figure 4-7 shows a connection example, where a serial Flash-ROM is connected to TC35670FTG.

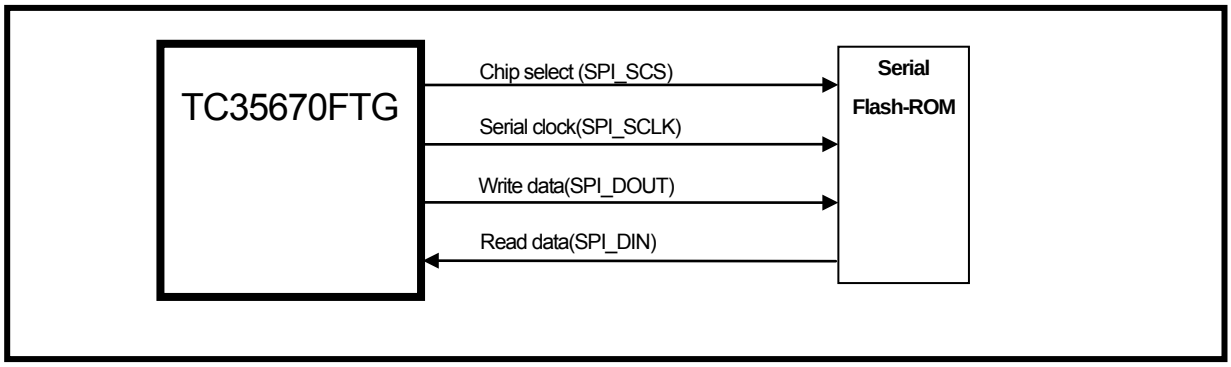


Figure 4-7 Connection example for serial Flash-ROM using SPI interface

4.4. I²C Interface

4.4.1. Features

TC35670FTG has the following main features for a serial memory interface.

- Operation voltage: 1.8 to 3.6 V
- I²C bus interface
  - ✓ Operation mode: I²C bus master
  - ✓ Serial clock frequency: Standard mode (Max 100 kHz), Fast mode (Min100 kHz to Max 400 kHz)
  - ✓ Output mode: Open-drain output, CMOS output
  - ✓ Device address format: 7 bits address (10 bits address is not supported)

I²C interface can operate at 1.8 to 3.6 V depending on VDDIO, however, cannot operate at different voltage from ones other interfaces are operate at.

4.4.2. Connection Example

Figure 4-8 shows a connection example of a serial EEPROM using I²C bus interface of the open-drain mode. External pull-up resistors (Rext) are necessary for both serial clock line and serial data line.
Figure 4-9 shows another connection example where I²C bus is in the CMOS output mode. Only the serial data line needs Rext because this line can be driven by neither TC35670FTG nor a serial EEPROM.

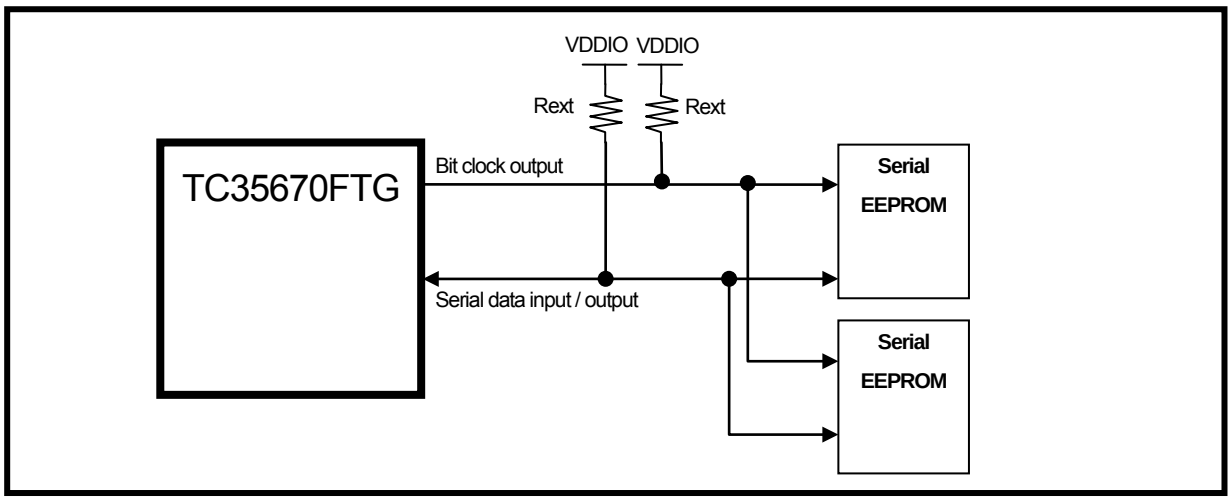


Figure 4-8 Connection example for serial EEPROM with I²C-bus interface (Open-drain output)

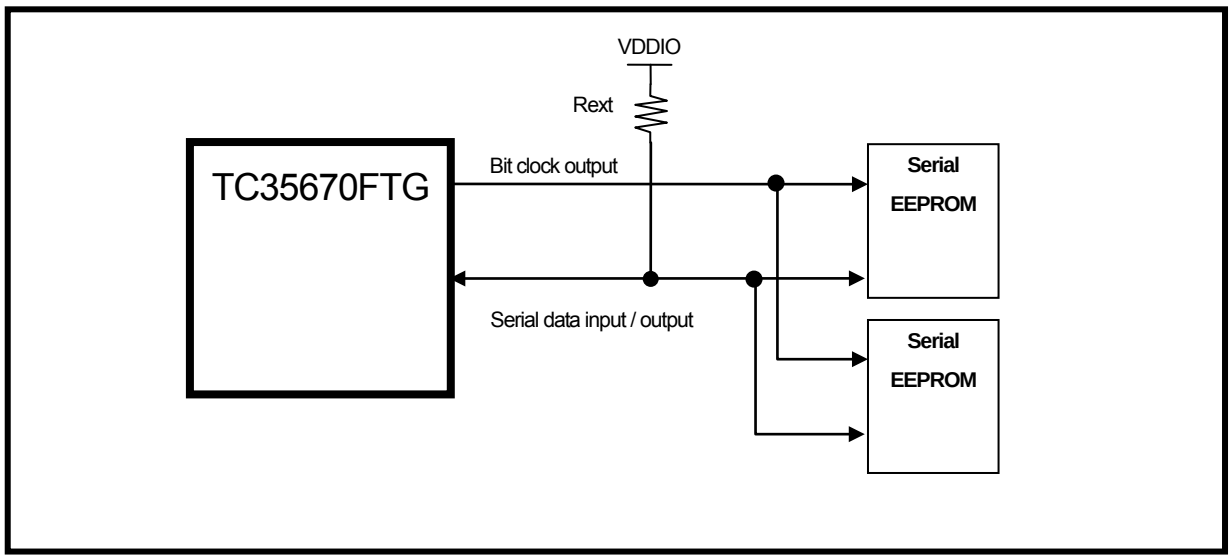


Figure 4-9 Connection example for serial EEPROM with I^2C-bus interface (CMOS output)

4.5. PWM Interface

TC35670FTG has a PWM interface that can be used for LED, buzzer control, etc.
The PWM interface has the following features.

- Arbitrary pulse generation function
- It can select the source clock from 13 MHz and 32.768 kHz
- It has 12 bits clock division setting up to 1/4096: 8 Hz to 16.384 kHz (32.768 kHz), 3.17 kHz to 6.5 MHz (13 MHz)
- It can mask the pulse output on the basis of 50 ms (rhythm function)
- The interrupt can be generated in synchronization with the cycle of 1s rhythm pattern.
- It can switch the pulse output to Low / High active
- Duty of the pulse output is adjustable.

4.5.1. Pulse Generation Function

Figure 4-10 shows a brief explanation of the pulse generation. TC35670FTG can adjust output pulse frequency by changing its cycle. Also it can adjust on/off ratio by changing its duty.
The cycle (frequency) can be set from 8 Hz to 16.384 kHz for 32.768 kHz clock, and from 3.17 kHz to 6.5 MHz for 13 MHz clock.
The duty can be set from 0% to 100%

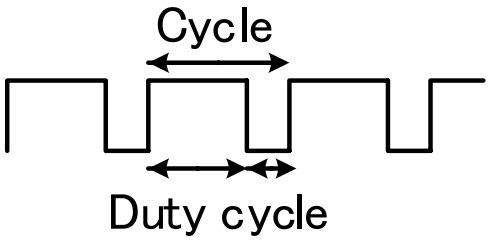


Figure 4-10 PWM pulse generation function

4.5.2. Rhythm Function (Output Masking)

Figure 4-11 shows the brief explanation of PWM rhythm function. In addition to the one for pulse generation, TC35670FTG has another timer that has 50 ms x 20 = 1s (rhythm counter). That timer has 20 bits register (pattern register), each bit corresponds to the rhythm counter that counts down in every 50 ms. When the pattern register is zero, the PWM output is masked to zero or one. Using this function, LED or buzzer can be on with 1s periodical pattern

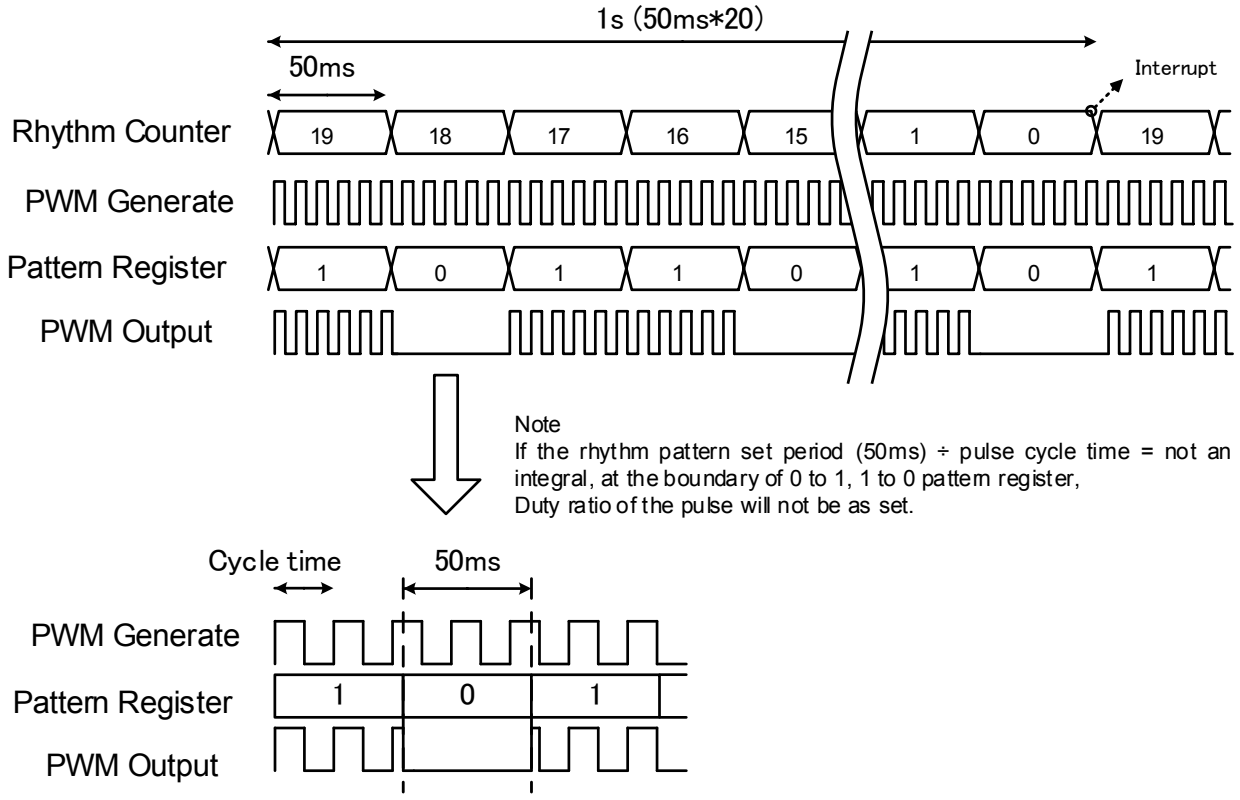


Figure 4-11 PWM Rhythm Function

4.6. ADC

4.6.1. Features

TC35670FTG has 3 channels of 10 bits ADCs for battery monitoring, analog inputs from external sensors, for example. The ADC has the following features.

- 2 channels for analog inputs (shared with GPIO pins)
- 1 channel for VDD voltage monitor
  The reference input is connected to VDD, and the analog input is to built-in LDO output 1.1V.
  Please refer to 4.6.2 for how to calculate VDD absolute value.
- Maximum conversion rate: 1 MS/s

4.6.2. Descriptions

The ADC has 10 bits conversion accuracy and can work for input voltages from 0 V to 3.6 V (VDD). It has 3 channels of analog inputs. And the channel 0 is connected to LDO output 1.1V. And the channels 1 to 2 are shared with GPIO pins.
When a battery is used as power source, the reference voltage can slide over time because the battery is connected as reference voltage. In that case, the LDO output voltage connected to Channel 0 can be used as a reference voltage. So the input voltage to Channel 1 or Chanel 2 is converted by the reference voltage of Channel0 and the converted value is used to calculate a correct digital value by the CPU. The following shows the conversion method of the input voltage.

Voltage A at time T can be calculated as follows

(1) LDO 1.1V is AD converted. This is X.
(2) Voltage A is AD converted. This is Y
(3) Assuming absolute value of voltage A is Z, 1.1:X = Z:Y
Z [V] = 1.1 × Y/X
Calculation example:
Suppose 1.1V LDO output at ch0 is converted to 0x0188, and measurement target at ch1 0x0134, the absolute voltage at ch1 Z [v] is given by 1.1 × 0x0188 / 0x0134 = 1.1 × 392 / 308 = 1.4 [V].

Figure 4-12 shows conceptual of voltage conversion.

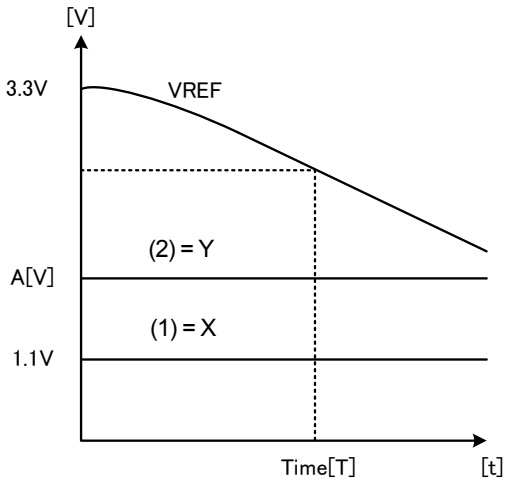


Figure 4-12 Voltage conversion concep

The ADC converts inputs from channels selected by register settings. When a conversion has finished, the CPU detects it by the interrupt or register polling, and then returns the results. The maximum sampling rate depends on software load on the CPU.

4.7. IC Reference Clock Interface

4.7.1. Features

TC35670FTG has the following features for IC reference clock interface which receives an external clock.

- Clock frequency: 26 MHz (The deviation should be adjusted within 50 ppm at the temperature in use)

TC35670FTG has an internal feed-back resistor between XOIN and XOOUT and doesn't require external feedback resistors. Please adjust external capacitors (C_{IN} and C_{OUT}) based on PCB layout and assembly if necessary within the range of the X'tal's specification.

4.7.2. Connection Example

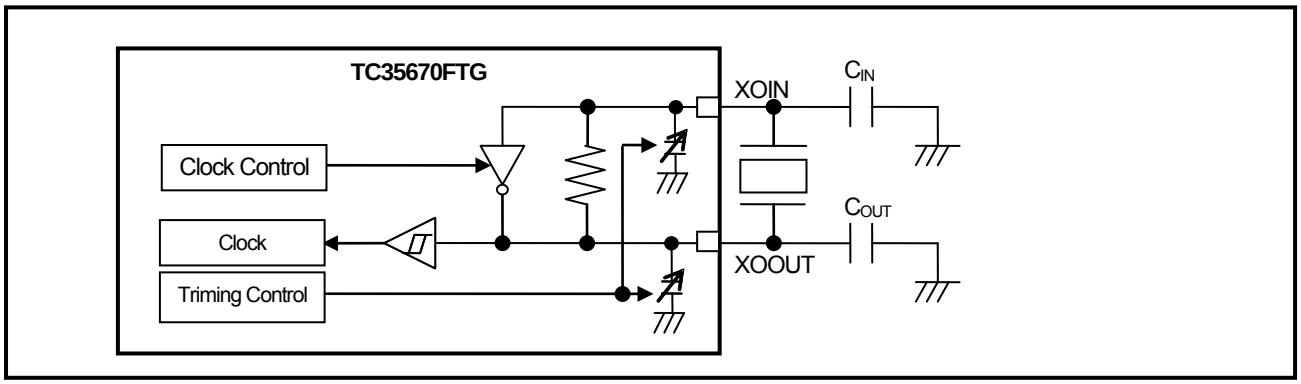


Figure 4-13 Crystal oscillator connection example

4.7.3. Oscillation Frequency Adjust Function

Crystal OSC circuit has a capacitor array inside, and the OSC frequency can be trimmed by a register bit value from 0 to 31. Figure 4-14 shows an example of the adjusted frequency measured with our test board using 26 MHz Crystal. This characteristic can vary depending on the crystal itself, external capacitors, resistors and PCB patterns.

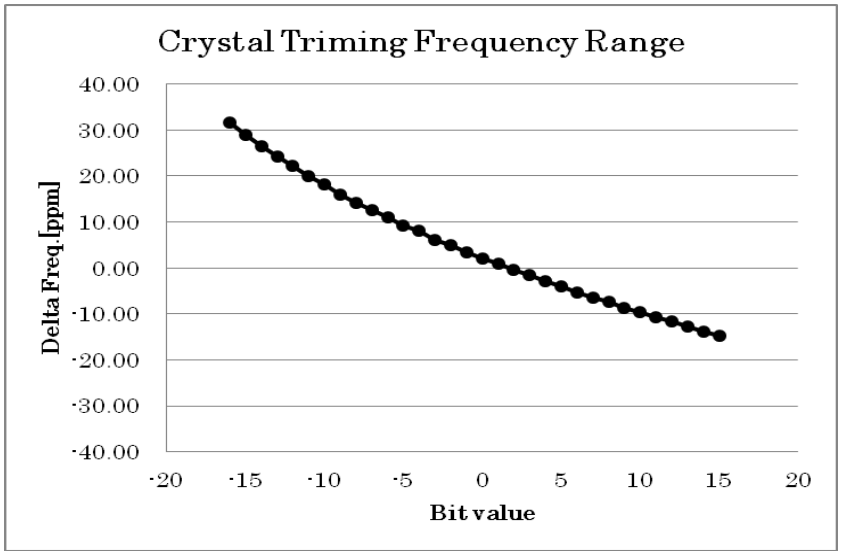


Figure 4-14 Trimming frequency range example

4.8. TAG- wireless interface

TC35670FTG has a NFC Forum Type 3 Tag (NFC Tag) function built-in, which is equipped with FeliCa contactless IC card technology. NFC Tag provides non-volatile memory (EEPROM), wireless interface which conforms to NFC Forum Type 3 Tag standards, and wired interface by I^2C.
This section will explain a wireless interface of NFC tag.

4.8.1. Features

Table 4-2 shows propagation performace of TAG wireless interface.

Table 4-2 Transmission characteristic of the wireless interface

Item	Remarks
Data transmission format	Half duplex, Synchronization
Carrier frequency (fc)	13.56 MHz
Modulation method	ASK
Bit coding	Manchester code, MSB First
Data transmission speed	212 kbps/424 kbps (Automatic detection)

4.8.2. Character format

Figure 4-15 shows character format. The character consists of 8 bits data. There is no start bit, no stop bit, and no parity. Character is transmitted MSB first. Multiple characters are successively transferred. There is no space between characters.

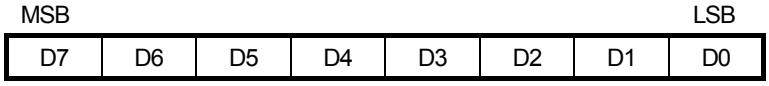


Figure 4-15 Character format

4.8.3. Frame format

Figure 4-16 shows frame format. The frame consists of multiple characters. Sync code, LEN, packet data, and CRC fields are defined within the frame.
Packet is the addition of preamble (6bytes 00h) and frame. Data is communicated to wireless reader/writer by packet unit.
Packet received by TC35670FTG is a command. Packet transmitted by TC35670FTG is a response. Table 4-3 shows field definition of packet.

(2bytes)	(1byte)	(n bytes)	(2 bytes)
Sync code	LEN	Packet data	CRC

Figure 4-16 Frame format

Table 4-3 Field definition of packet

Field name	Byte length	Definition
Preamble	6	00h 00h 00h 00h 00h 00h
Sync code	2	B2h 4Dh
LEN(data length)	1	Value of n+1
Packet data	n	Packet data of command or response
CRC	2	Check sum by CRC-CCITT of data length and packet data (Big endian) Initial value: 00h 00h Generating polynomial: $X^{16}+X^{12}+X^5+1$

Command packet data consists of command code (top 1 byte) and command data. Command code is a code which identifies command type.

(1 Byte)	(n-1Byte)
Command code	Command data

Figure 4-17 packet data of command

Packet data of response consists of response code (top 1 byte) and response data. Response code is a code which recognizes response type.

(1byte)	(n-1 byte)
Response code	Response data

Figure 4-18 Packet data of response

4.8.4. Command type

Table 4-4 shows commands which TC35670FTG supports.

Table 4-4 Command type

Command name	Command code value	Response code value	Functional outline
Polling	00h	01h	Command by which wireless read/writer catches / identifies TC35670FTG
Read Without Encryption	06h	07h	Reading block data
Write Without Encryption	08h	09h	Writing block data

4.8.5. Operation sequence

If wireless carrier is detected, TAG_RFDET pin outputs high level. If wireless carrier disappears, it turns back to low level due to pull-down resistance. VDDIO and VDD pin needs power supply for TAG_RFDET pin to output high.
At Write without Encryption or Read without Encryption, if IDm stored in TC35670FTG and iDm with command are consistent, TAG_READYX pin outputs high level. After that, during supply of internal power source, the high is kept. VDDIO and VDD pin needs power supply for TAG_READYX pin to output high.
By becoming high in TAG_READYX pin, HOST can get to know that wireless reader writer accesses TC35670FTG.

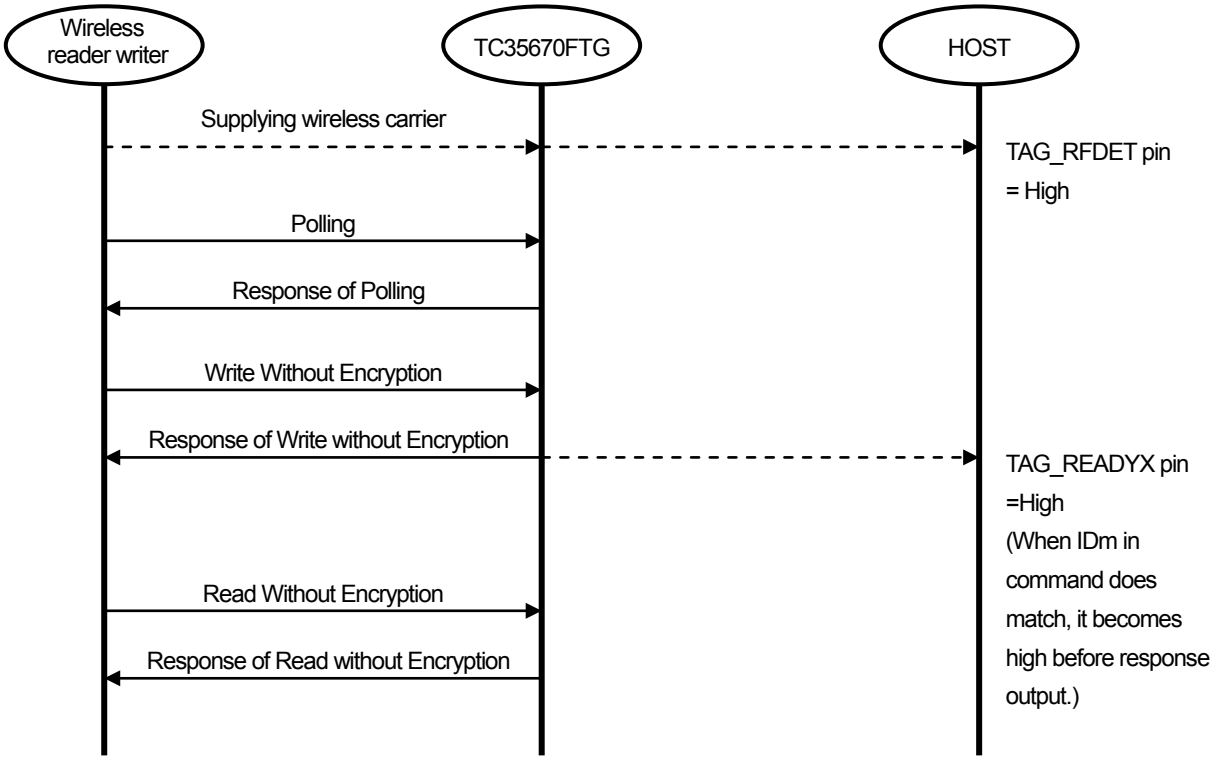


Figure 4-19 Sequence example of operation over the wireless interface

4.8.6. Warning

① At the period which is from reading WCNT value to writing with MAC, commands of wired interface execute and WCNT may change. In this case, at the execution of Write without Encryption, WCNT value is changed. Therefore, in case of writing with MAC, error of inconsistency of MAC value occurs. If this error occurs, read WCNT value again and then write with MAC. Or, before reading WCNT value, set to prohibit Set Write Command of the wired interface by using WLOCK block.

② During the execution of wired interface command, receiving commands of wireless interface are ignored and no response to the wireless reader writer is made (no response). In this case, resend commands from the wireless reader writer.

③ In case that TC35670FTG prohibits Write without Encryption by using WLOCK block, TC35670FTG does not make a response to Write Without Encryption. In this case, resend commands to the wireless reader writer until Write Without Encryption is permitted in wired interface side.

④ The TAG_RECTOUT pin can be used to optimize the value of the condenser between the TAG_L0 pin and the TAG_L1 pin. The output voltage of the TAG_RECTOUT pin should be monitored. The wireless reader and writer should not be close to the pin. The higher output voltage is monitored when the resonance condenser value is closer to the optimized value.

4.9. TAG Wire Interface

TC35670FTG has the I^2C interface which operates as the TAG-dedicated slave (TAG-I^2C interface).
The features of the TAG-I^2C mode are as follows:

4.9.1. Features

- 7 bits address capability , slave operating
- Serial clock frequency: 400 kHz(max)
- Slave address value is set in EEPROM (UC block).
- Error detection function(Redundancy Code (RC) error is detected)

4.9.2. Connection Example

The connection to the host in the TAG-I^2C mode is shown in Figure 4-20. Serial clock (SCL) and Data (SDA) line are connected to pull-up resistances. If SCL pin in HOST is CMOS output, only SDA line should be connected to the pull-up resistance.
To decide pull-up values, refer to the electric characteristics and the datasheet of the host.

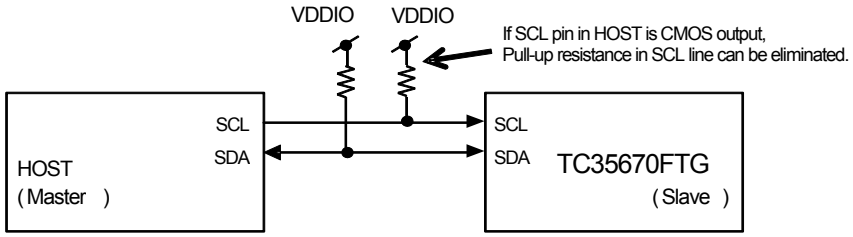


Figure 4-20 Connection example in usage of TAG-I^2C mode

4.9.3. Operation explanation

When TAG-I^{2}C detects start condition, it receives 7 bits slave address of top character and W/R selection. If slave address stored in UC block and received slave address are consistent, TAG-I^{2}C outputs ACK. If W is selected in the W/R selection, TAG-I^{2}C prepares for received commands since then. TAG-I^{2}C outputs ACK every received character. If R is selected in the W/R selection, TAG-I^{2}C prepares for sending responses since then. Every sent character, TAG-I^{2}C checks ACK or NACK which HOST outputs.
If TAG-I^{2}C detects stop condition, it completes receiving commands.

If slave address of top character is inconstant with slave address stored in UC block, TAG-I^{2}C G does not output ACK.
In this time, if W is selected in the W/R selection, TAG-I^{2}C ignores receiving commands since then and does not output ACK. If R is selected in the W/R selection, TAG-I^{2}C ignores transmission requests of response since then and does not output data. When stop condition is detected, TAG-I^{2}C moves to the status of waiting start condition again.

After receiving commands, TAG-I^{2}C becomes status of waiting of sending responses. If received top character is W selection in this condition, TAG-I^{2}C outputs ACK to top character. However it ignores receiving commands since then and does not output ACK. If top character is R selection, TAG-I^{2}C outputs ACK and prepares for sending responses since then. TAG-I^{2}C checks ACK or NACK which is output from HOST every sent character. However, if NACK is detected, it stops sending. If SCL is input after NACK, TAG-I^{2}C outputs FFh. If TAG-I^{2}C detects stop condition, it completes receiving commands.

If strat condition is detected (no stop condition) in the middle of commands, response or character, TAG-I^{2}C interrupts receiving or sending process and moves to status of waiting of receiving top character (7 bits slave address and W/R selection)
Stop bit is detected in the middle of commands or response, TAG-I^{2}C interrupts receiving or sending process and moves to status of waiting of receiving top character (7 bits slave address and W/R selection).

In I^{2}C mode, TAG-I^{2}C is not capable of general call address and 10 bits slave address assignment. And, TAG-I^{2}C never outputs low level to TAG_SCL pin (clock stretch).

4.9.4. Frame format

Figure 4-21 shows frame format. The frame consists of multiple characters. Fields such as SYN, CMD/STR, Payload, and RC are defined in the frame.

(1 byte)	(1 byte)	(0 to 230 bytes)	(1 byte)
SYN	CMD/STR	Payload	RC

Figure 4-21 Frame format

Frame is used as packet and data is communicated to wire reader writer by packet unit. Packet which TC35670FTG receives is a command. Packet which TC35670FTG sends is a response. Table 4-5 shows definition of packet field.

Table 4-5 Packet field definition

Field name	Byte length	Definition
SYN	1	Sync code (In case of I^2C, 7 bits slave address and W/R selection (W: command R: Response) is specified to SYN. Wire reader-writer outputs SYN of response.) (In case of SPI/UART, 80h is specified as sync code.)
CMD/STR	1	CMD: Command assignment STR: Response status
Payload	0 to 230	Command/ response dependable
RC	1	Check sum (Exclusive OR between CMD/STR , Payload and FFh)

4.9.5. Command type

Table 4-6 shows commands which TC35670FTG supports. Type of commands is specified with CMD.

Table 4-6 Command type

Command name	Value of CMD	Outline of function
Set Write Command	01h	Stating the execution of Write without Encryption (wireless interface receiving invalid)
Set Read Command	02h	Starting of the execution of Read without Encryption (wireless interface receiving invalid)
Get Status	03h	Obtaining status
Get Length	04h	Obtaining data length of execution result
Get Response	05h	Obtaining an execution result (Wireless interface receiving valid)
Get TM Data	07h	Obtaining data in Through mode
Put TM Data	08h	Setting data in Through mode (Wireless interface receiving valid)

STR which is included in response indicates status for command. Table 4-7 shows the content of STR.
Value of STR might be OR between higher 4 bits and lower 4 bits.

Table 4-7 Content of STR

Value of STR	content in status
8Xh	In process of wired interface command
4Xh	In process of wireless interface command
1Xh	Presence of Through mode data
X8h	Framing error (only UART mode)
X4h	Abnormality in condition of command execution
X2h	Value of CMD is not defined.
X1h	RC abnormality
00h	No information (Command processing completion)

4.9.6. Operation Sequence

- Operating sequence of wired interface(Get Status/Get Length are not used.)

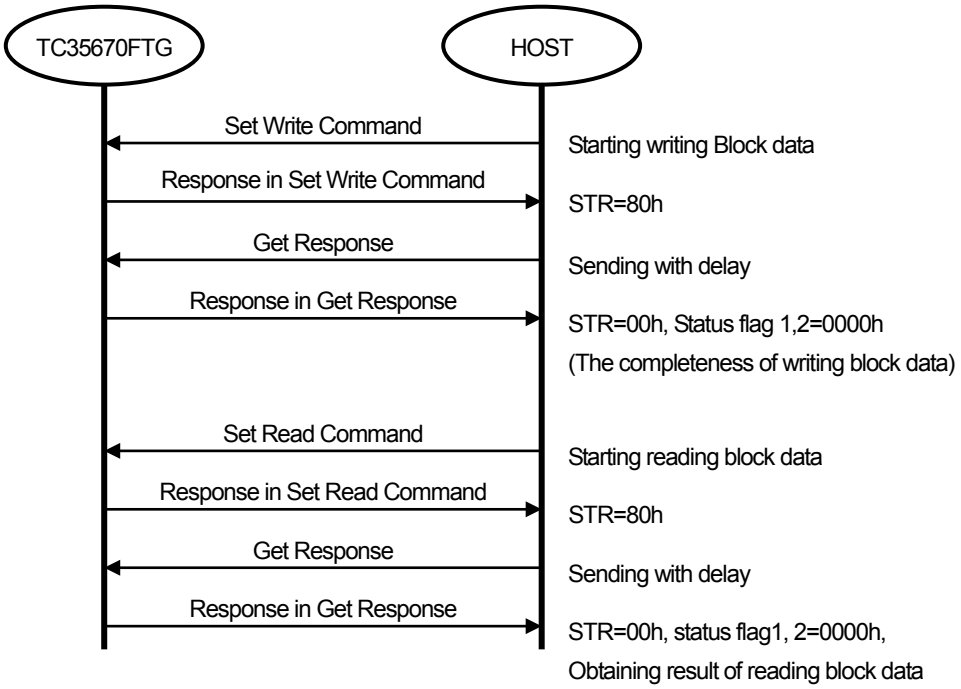


Figure 4-22 Operating sequence over the wired interface(Get Status/Get Length are not used)

- Operating sequence of wired interface (Get Status/Get Length are used)

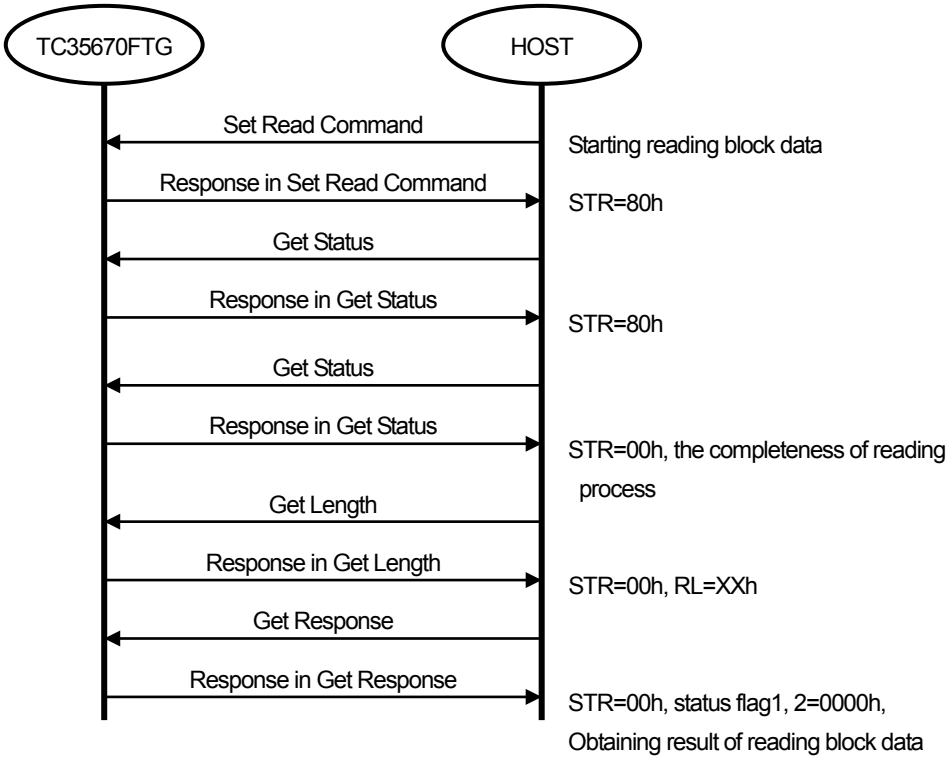


Figure 4-23 Operating sequence over the wired interface (Get Status/Get Length are used)

- Command processing of wireless interface

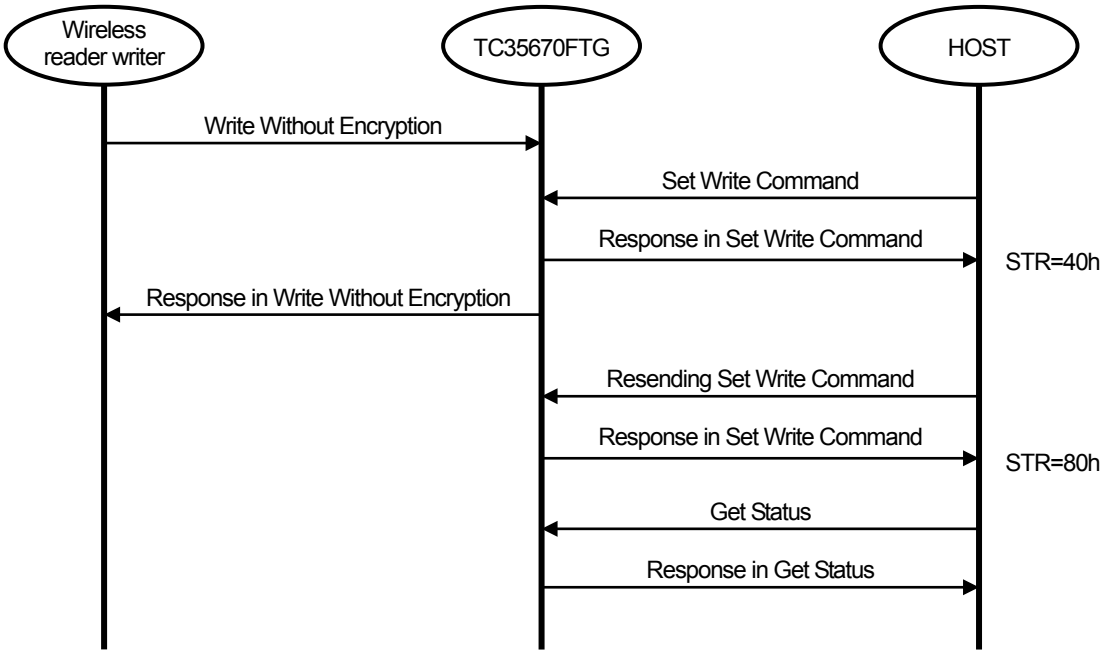


Figure 4-24 Command processing sequence of wireless interface

- Command processing of wired interface

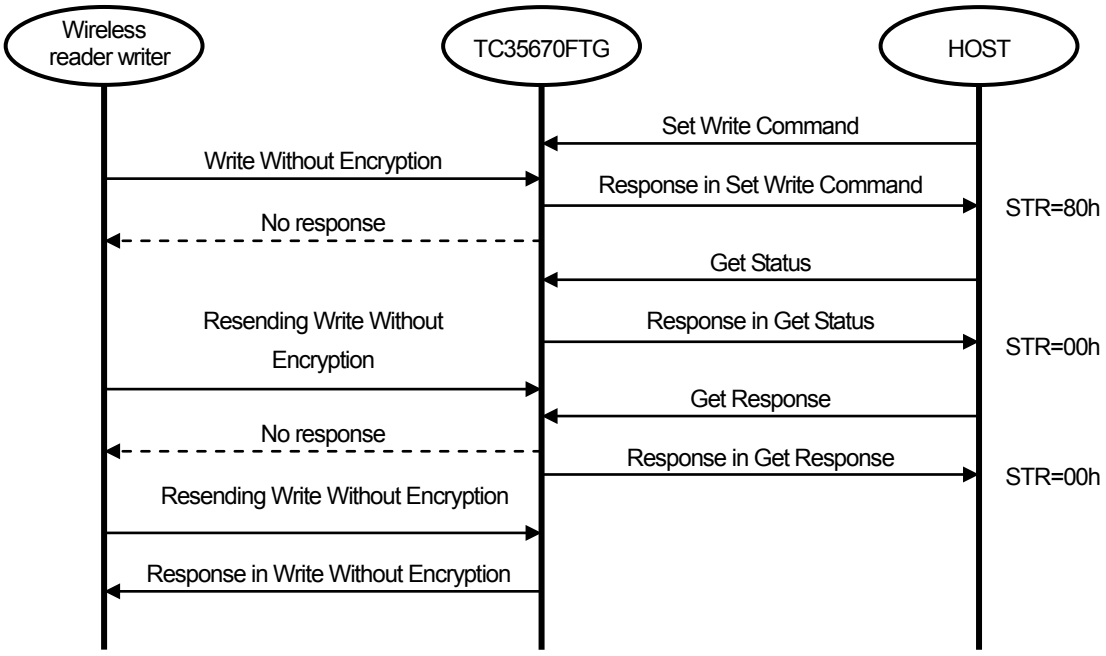


Figure 4-25 command processing sequence of wired interface

4.9.7. Warning

① In case that, in I^2C mode, many SCL K is input and response which is longer than command assignment is requested, TC35670FTG outputs FFh.

② Even if excessive data is received after RC, if RC is correct, TC35670FTG processes commands.

③ If STR in the Response for Get Response is 00h (Command procedure completes), at the response of Get Response, do not resend Get Response. STR of response at resending is 04h. To obtain the result of command process again, try again from Set Write Command /Set Read Command

④ During the period from reading WCNT value to writing with MAC, commands of wireless interface might be executed and WCNT value might change. In this case, at the execution of Set Write Command, WCNT value already changes. Consequently, in case of writing with MAC, inconsistency error occurs. If this error occurs, read WCNT value again and write with MAC. Or, before reading WCNT value, prohibit “Write Without Encryption” of wireless interface by using WLOCK block.

⑤ If STR is 04h (abnormal command execution condition) in a response for Get Response, its command processing has not been done. Therefore, start again from Set Write Command /Set Read Command.

4.10. TAG Through function

4.10.1. Features

Features of Through mode are shown in the below.

- Data can be transferred from wireless interface to wired interface or from wired interface to wireless interface by using internal built-in RAM.
- Maximum 192 byte packet data can be temporarily stored.

4.10.2. Operation explanation

When TC35670FTG receives the Write Without Encryption command which is indicated with the block number B0h to BBh (TM block) by the TAG wireless interface, the block data is stored to the RAM and the response is returned with the wireless interface. And it enters the through mode. Then the TAG_READYX pin outputs Low level and the reception of the TAG wireless interface is disabled.
After the transition to the through mode, the TAG- I^2C can acquire the block data which is stored in the RAM. Get TM Data is used to acquire the block data. If the Set Write Command/Set Read Command is executed during the through mode and Get TM Data execution, an error occurs. After Get TM Data is executed, the Set Write Command/Set Read Command is available.
If TAG wireless interface returns data, Put TM Data transmits the block data. When the TAG receives Put TM Data, it returns Put TM Data. Then, High level is output from the TAG_READYX pin, and the through mode is finished. After the end of the through mode, TAG wireless interface can receive data. If no data returned by the TAG wireless interface is present, LEN is set to 01h and Put TM Data is transmitted. When the TAG wireless interface receives the Read Without Encryption command which indicates the block number B0h to BBh, the block data stored in the RAM is returned as the response.
It is necessary that the block list in the Write Without Encryption command and the Read Without Encryption command should be indicated to one of the block numbers B0h to BBh. Owing to those features the TAG realizes the through mode function.
After transiting to the through mode, the reception by the TAG wireless interface is disabled. Even though the wireless reader and writer issues a command in the through mode, TC35670FTG ignores the command and returns no response.
Figure 4-26 shows operating sequence.

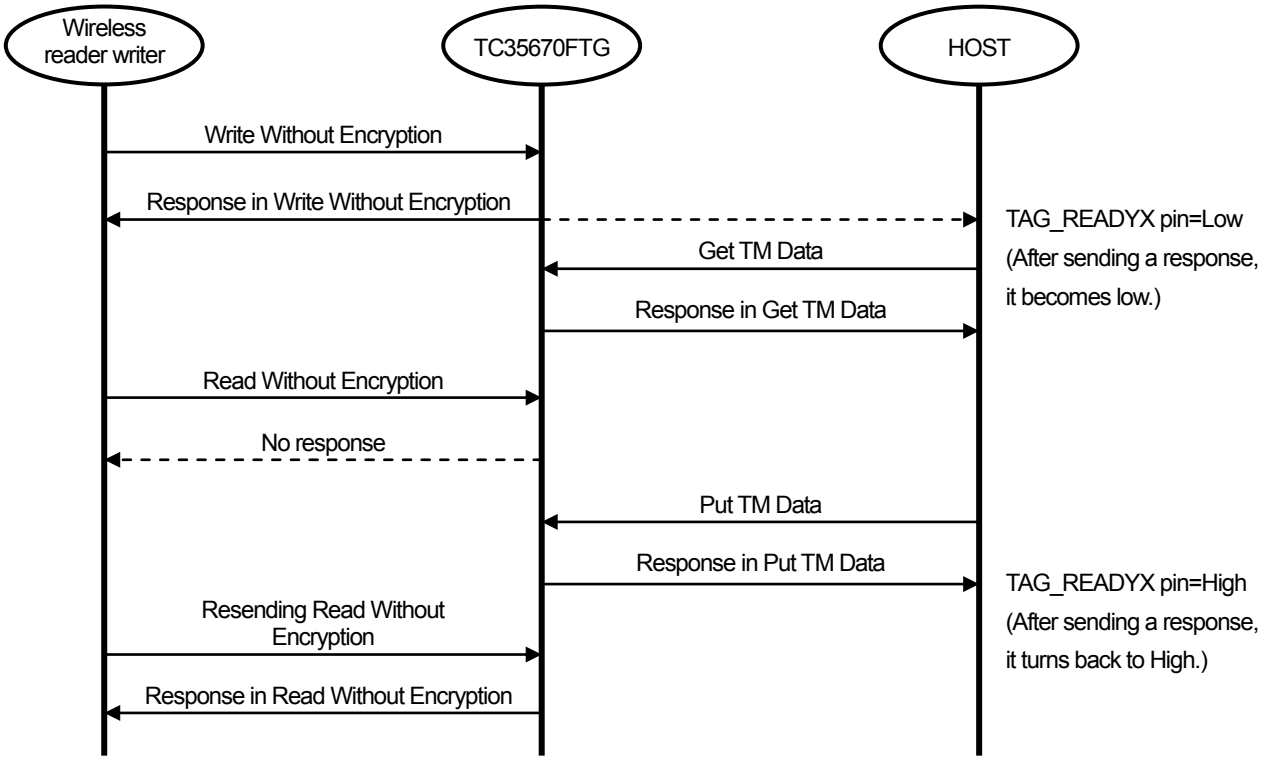


Figure 4-26 Operating sequence in Through mode

4.10.3. Packet Explanation

Figure 4-27 shows packet which wireless reader writer exchanges with HOST in Through mode function. Inside of () indicates byte length. Maximum 12 blocks can be transferred. (n=1-12)
The host acquires the block data of the Write Without Encryption command with Get TM Data. The block data of Put TM Data is acquired by the wireless reader and writer as the block data of the Read Without Encryption command.

If Read Without Encryption requests block data output which is larger than block data set by Put TM Data, TC35670FTG outputs data set by Put TM Data and 00 ••• 00h. If the number of specified block is larger than 12 blocks, an error arises. Block number which is specified in block list should be any of B0h-BBh. The order and specifying start position are not asked. For example, it correctly works even if all specified blocks are same (like B0h). TC35670FTG checks if block number is within B0h-BBh.In case of mixture of B0h-BBh and other block numbers, TC35670FTG outputs an error.

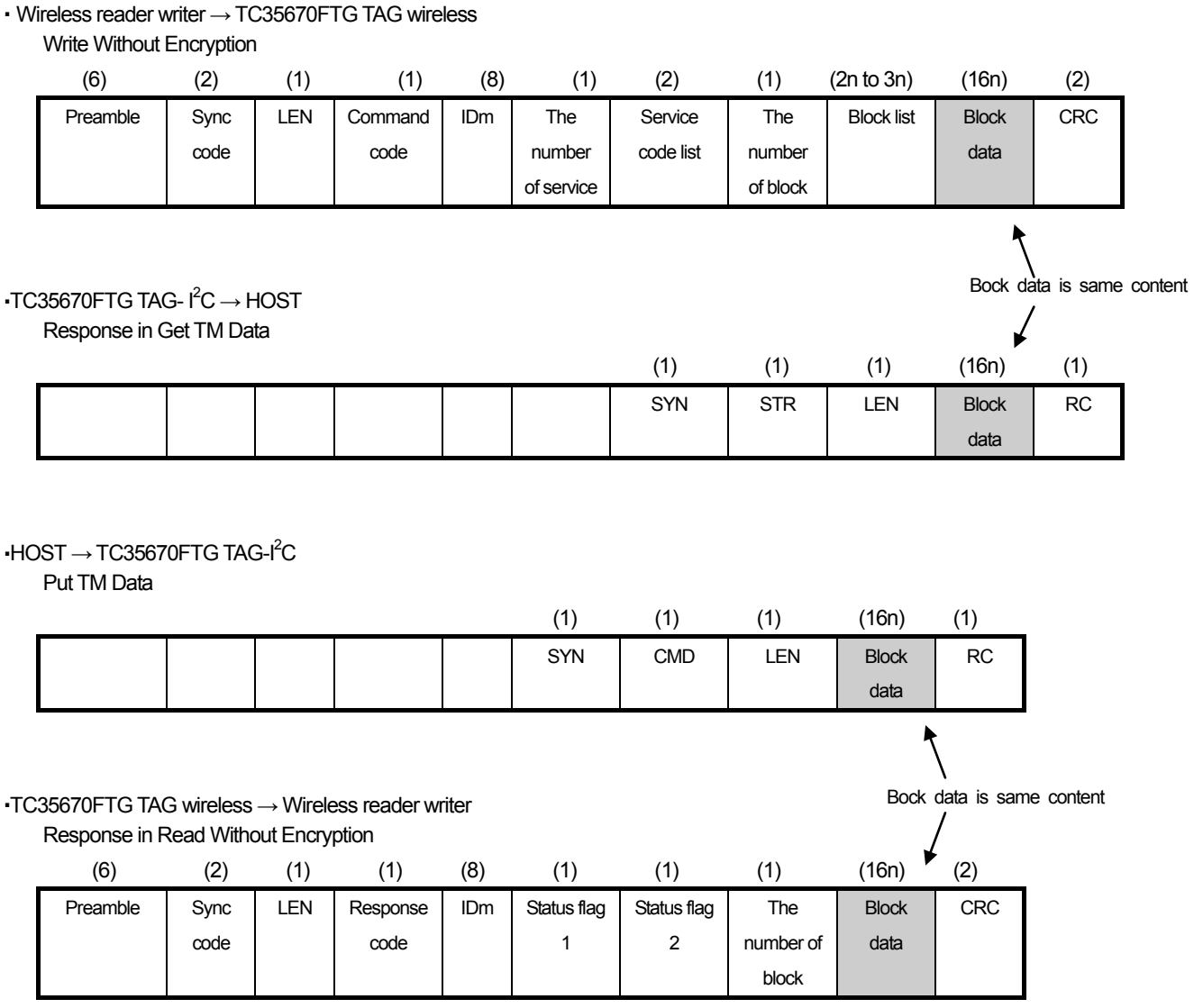


Figure 4-27 The explanation of packet in Through mode

Table 4-8 shows error factors of Write Without Encryption in the selection of Through mode. SF1 and SF2 indicate status flag 1 and 2.

Table 4-8 Error factors of Write Without Encryption in the designation of Through mode

Error factors	Response	SF1	SF2
LEN is not a specified value(It is not stratified with minimum command length)	No	—	—
IDm is inconsistent			
The number of service is not 01h.	Yes	FFh	A1h
The number of block is not greater than 01h and smaller than **0Ch.**			A2h
LEN is not a specified value (data length of block list is not correct.)	No	—	—
Access mode of block list element is not 000b.	Yes	Note	A7h
The order of service code list of block list element is not 0000b			A3h
Service code of service code list is inconsistent.		01h	A6h
Service attribute of service code of service code list is not 001001b , 001011b.			
D2 in block number is not 00b.		Note	A8h

Note: The order of block list elements in which error was detected is set.

Bit 0=1b: Abnormality is detected in the 1st or 9th block list.
Bit 1=1b: Abnormality is detected in the 2nd or 10th block list.
Bit 2=1b: Abnormality is detected in the 3rd or 11th block list.
Bit 3=1b: Abnormality is detected in the 4th or 12th block list.
Bit 4=1b: Abnormality is detected in the 5th block list.
Bit 5=1b: Abnormality is detected in the 6th block list.
Bit 6=1b: Abnormality is detected in the 7th block list.
Bit 7=1b: Abnormality is detected in the 8th block list.

Table 4-9 shows error factors of Read Without Encryption in the selection of Through mode. SF1 and SF2 mean status flag 1 and 2.

Table 4-9 Error factors of Read Without Encryption when Through mode is assigned

Error factors	Response	SF1	SF2
LEN is not a specified value. (It does not satisfy with minimum command length.)	No	—	—
IDm is inconsistent.			
The number of service is not 01h	Yes	FFh	A1h
The number of block is not greater than 01h and smaller than **0Ch.**			A2h
LEN is not a specified value (Data length of block list is not correct.)	No	—	—
Access mode of block list element is not 000b.	Yes	Note	A7h
The order of service code list of block list element is not 0000b			A3h
Service code of service code list is inconsistent.		01h	A6h
Service attribute of service code of service code list is not 001001b , 001011b.			
D2 in block number is not 00b.		Note	A8h

Note: The order of block list elements in which error was detected is set.

Bit 0=1b: Abnormality is detected in the 1st or 9th block list.
Bit 1=1b: Abnormality is detected in the 2nd or 10th block list.
Bit 2=1b: Abnormality is detected in the 3rd or 11th block list.
Bit 3=1b: Abnormality is detected in the 4th or 12th block list.
Bit 4=1b: Abnormality is detected in the 5th block list.
Bit 5=1b: Abnormality is detected in the 6th block list.
Bit 6=1b: Abnormality is detected in the 7th block list.
Bit7 =1b: Abnormality is detected in the 8th block list.

4.10.4. Operation sequence

·Sequence of the usage of Get Length before Get TM Data in Trough mode

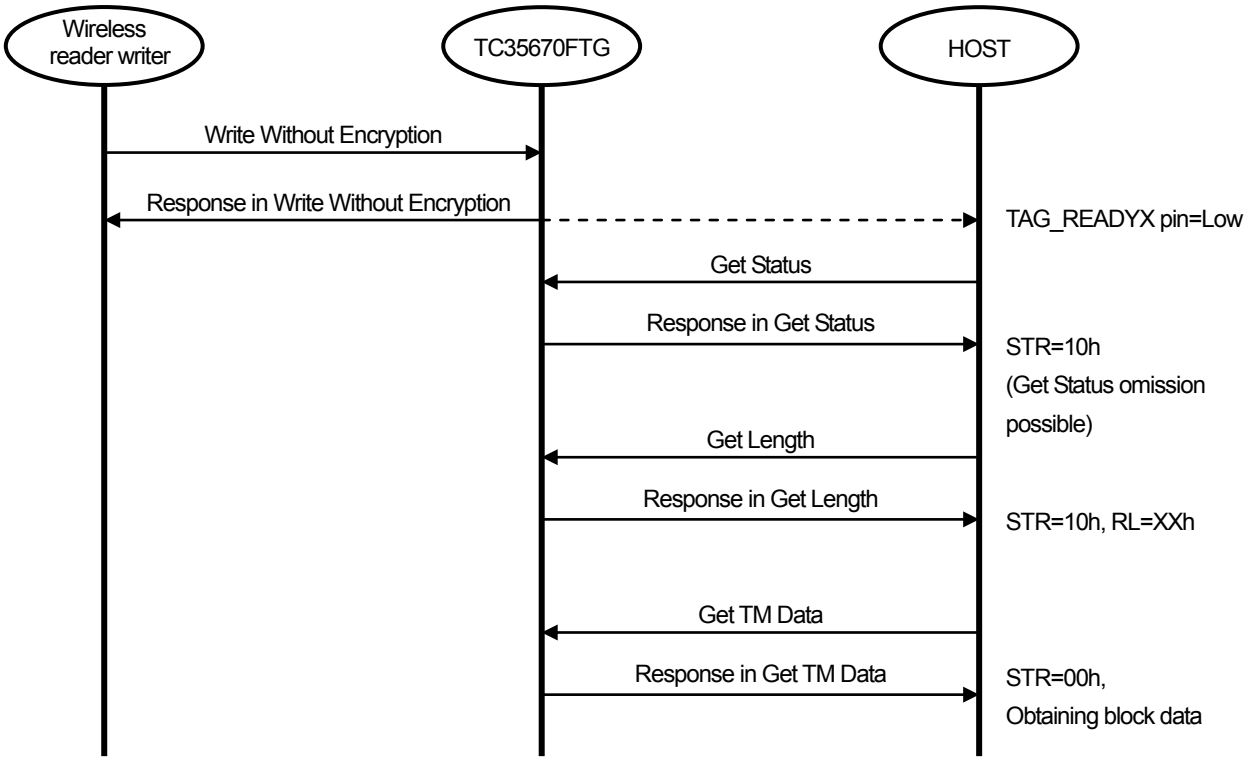


Figure 4-28 Sequence of the usage of Get Length before Get TM Data in Trough mode

·Sequence of continuous usage of Write Without Encryption command in through mode

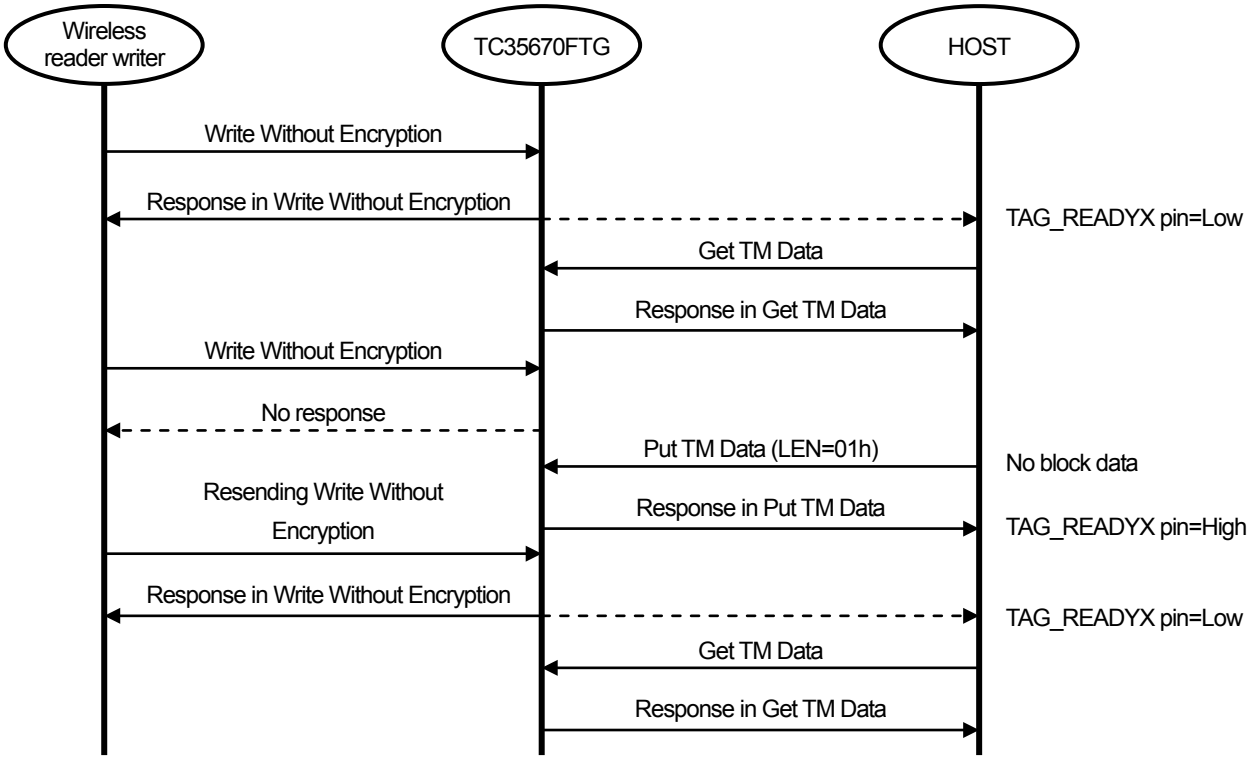


Figure 4-29 Sequence of continuous usage of Write Without Encryption command in through mode

・Sequence of usage of Set Write Command in Through mode

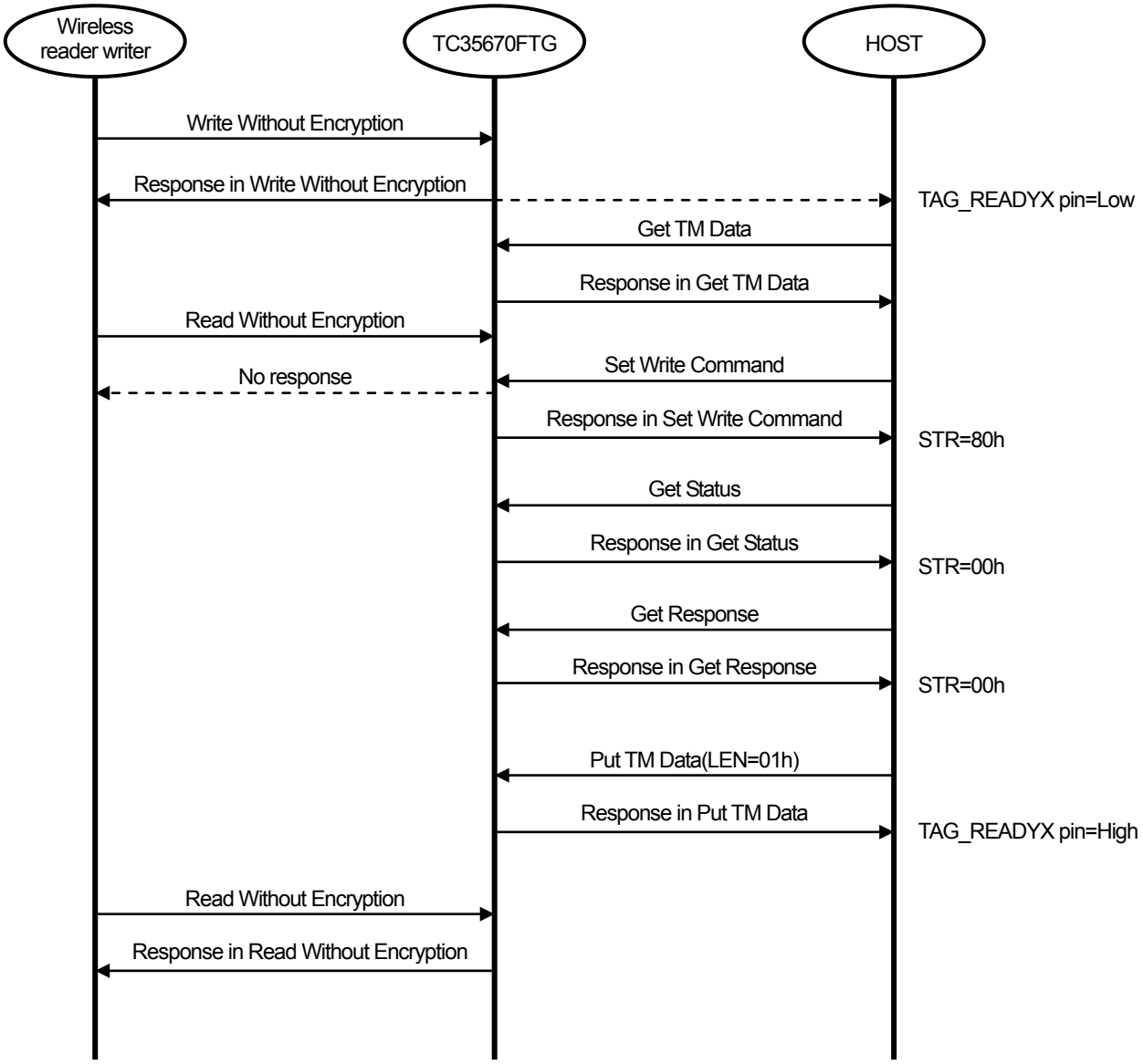


Figure 4-30 Sequence of usage of Set Write Command in Through mode

・Sequence of resending Read Without Encryption

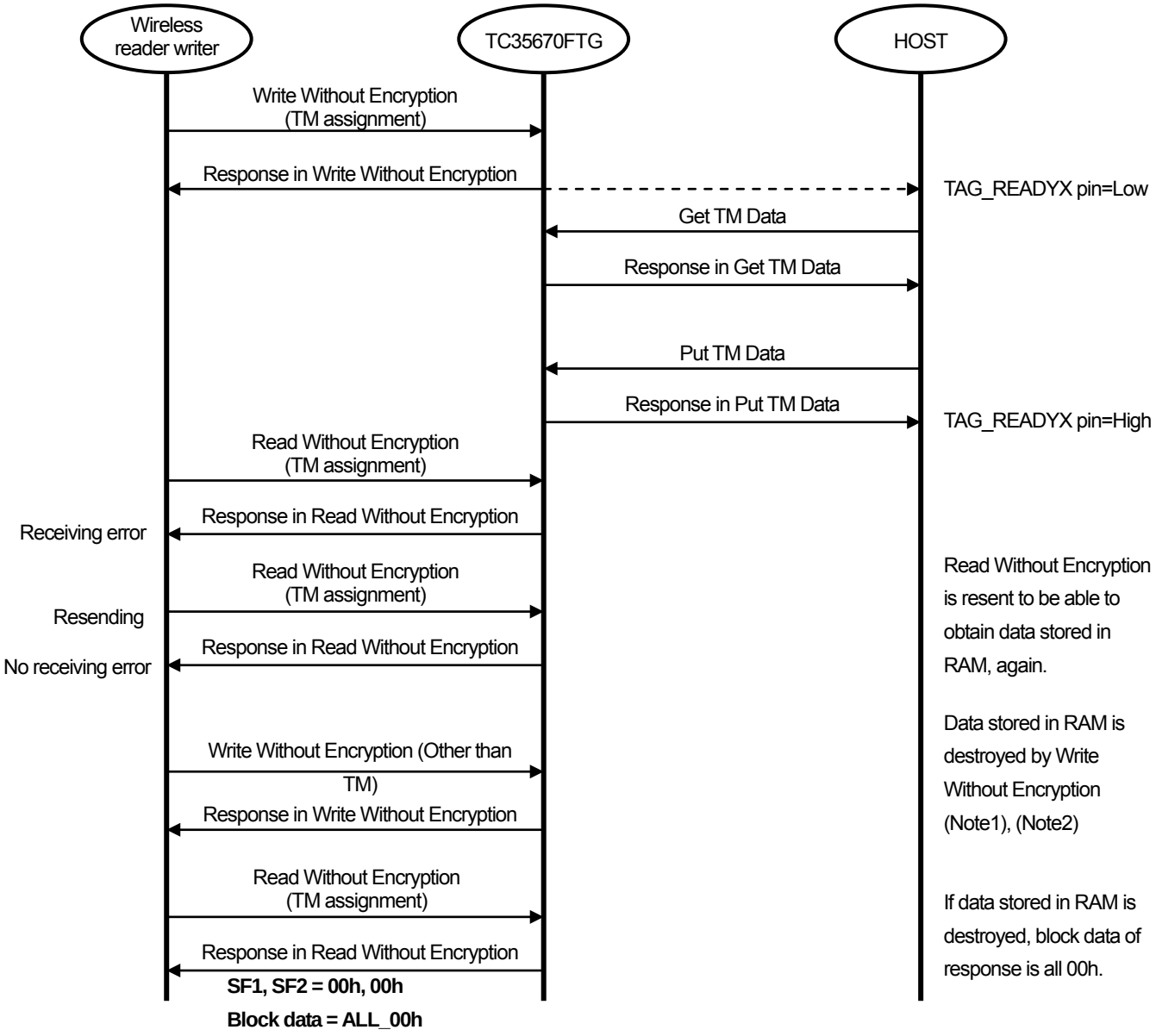


Figure 4-31 Sequence of resending Read Without Encryption

Note1: The conditions in which data stored in RAM is destroyed are shown in the below.

- The execution of Write Without Encryption
- The execution of Read Without Encryption which specifies other than Through mode
- The execution of Set Write Command
- The execution of Set Read Command

Note2: In case of destruction of data stored in RAM or no data stored in RAM, block data of response in Read Without Encryption is all 00h. And the status flag is 0000h.

5. TAG Built-in EEPROM and Block

5.1. Features

Features of built-in EEPROM of the TAG Block in TC35670FTG are shown in the below.

- General purpose user area: 1520 bytes
- High reliability writing function: Prevention of defective writing
- Write time: 5 ms(typ.)
- 1 bit error automatic correction
- CRC automatic addition and error detection in reading
- Page writing unit: 16bytes+2 bytes(CRC)

5.2. Functional explanation

EEPROM is composed of units called 18 byte pages. Data is written by page unit. One page is 16 byte data and 2 byte CRC data. In page writing, 16 byte CRC is automatically added. Then 16 byte data and CRC data are written. In reading, CRC data is also read to verify read 16 byte data.
Because of the High reliability in writing function, it takes 5 ms (typ.) to write. However, writing defective data can be prevented.
When defective data write occurs due to power-down, TC35670FTG restores its data at start-up. At start-up, TC35670FTG selects "returning back to the condition of previous page writing "or "updating the data, which was written in half way, to end". Then it executes selected one.
EEPROM has a parity every 2 byte data. If one bit error in the 2 byte occurs, its data is automatically corrected in reading.
If 2 bits or more occurs, its data is not corrected. This condition can be detected as abnormal CRC data.

Built-in EEPROM can be accessed by specifying block number with command.
From next section, block specification will be described.

5.3. Block

5.3.1. Block list

TC35670FTG manages its EEPROM area by dividing into 16 byte-unit areas which are called “blocks”.
Each block is assigned individual number called “block number”. These blocks can be accessed by specifying “block number” by command. A part of RAM and registers also have their own “block number”. They can be accessed by command. Table 5-1 shows those block list.

Table 5-1 Block list

Block No.	Name	Block Name	Remarks
00h	S_PAD0	Scratch pad0 block	General purpose area
01h	S_PAD1	Scratch pad1 block	General purpose area
02h	S_PAD2	Scratch pad2 block	General purpose area
03h	S_PAD3	Scratch pad3 block	General purpose area
⋮	⋮	⋮	⋮
0Dh	S_PAD13	Scratch pad13 block	General purpose area
0Eh	S_PAD14 or RAG	Scratch pad14 block Or subtraction register block	General purpose area or block with write value limitation (Setting by UC block)
0Fh	S_PAD15	Scratch pad15 Block	General purpose area
⋮	⋮	⋮	⋮
5Dh	S_PAD93	Scratch pad93 Block	General purpose area
5Eh	S_PAD94	Scratch pad94 Block	General purpose area
80h	RC	Random challenge block	For writing random number to generate MAC
81h	MAC	MAC Block	Block for reading the result of MAC calculation
82h	ID	ID block	Block for storing ID
83h	D_ID	Device ID block	Block for storing IDd and PMm
84h	SER_C	Service code block	Block for storing service code
85h	SYS_C	System code block	Block for storing system code
86h	CKV	Card key version block	Block for card key version
87h	CK	Card key block	Block for storing card key
88h	MC	Memory configuration block	Setting access permission to block, NDEF setting, RF parameter setting
90h	WCNT	WCNT block	Block for reading write count value
91h	MAC_A	MAC_A block	Block for reading/writing MAC value
92h	STATE	STATE block	Block for external authentication and polling response setting
A0h	CRC_CHECK	CRC_CHECKblock	Block for indication of CRC verification for all blocks
B0h to BBh	TM	Through Mode block	Block for specifying Through Mode
BCh	WLOCK	Write lock block	Temporary prohibition of writing to wire or wireless interface
BDh	UC	User configuration block	Setting operating mode of wired interface, Communication parameter setting, REG Block usage setting
BEh	MC2	Memory configuration 2block	Setting access permission 2 to block
BFh	MC3	Memory configuration 3block	Setting access permission 3 to block

5.3.2. Warning

(1) DFC(data format code) is two byte values to specify a data format stored in TAG. For an application of DFC, please contact our company. Sony Corporation deals with numbering and granting of DFC.

(2) For generation of MAC value, please contact our company.

(3) Before shipment to market, write MC [2] =00h and bit7=0 in MC [1]. It can prevent a wrong writing to system block (ID,D_ID,SER_C,CKV, CK,UC block), and MC/MC2/MC3 blocks.

(4) For the software development and the execution of the reader and writer, refer to the following documents.

http://www.sony.co.jp/Products/felica/business/tech-support/index.html

・FeliCa Lite-S starter manual

"3 DFC"

"6.1 Identification of FeliCa Lite-S card"

"6.2 Identification of Data Format"

・Software development technical note for FeliCa Lite-S

"1.1 Product Specification" and "3 Precaution for Certification" are not applied.

6. Boot control TAG part

6.1. Features

Features of start-up in TC35670FTG TAG are shown in the below.

- Built-in power supply switch : Terminal setting (TAG_PONX pin) turns off power switch , which realizes low power consumption at stand-by.

6.2. Functional Explanation

Power is supplied to VDDIO and VDD pins and Low level is input to TAG_PONX pin. Then, power switch in VDD side is turned on and power is supplied to the internal power supply (IVDD). If voltages in IVDD is 1.7V (typ.) or more, internal reset is released and TAG executes Boot process
After the Boot procedure completes, the TAG wired interface and the TAG wireless interface are available.
When the IVDD voltage is lower than 1.7 V (Typ.), the internal reset is asserted.
If voltages in IVDD is 1.7V (typ.) or more again, internal reset is released.
TAG_PONX pin inputs high level, power switch in VDD side is turned off and TAG becomes low power consumption status.
The PON start-up timing can be determined by monitoring the TAG_RFDET pin to use the TAG wireless interface. Wireless carrier is detected and TAG_RFDET pin outputs high level.

6.3. Boot time

TAG can accept commands within 3.5 ms after start-up. When defective data writing by shut-down or something is detected, it can accept them within 5.3 ms after start-up.

MC [2] is written 00h and then power is shut down. In this case, WCNT is reset after next start-up. Time at this start-up is 24ms at most.
If power shut-down occurs while the start-up procedure, the start-up should be done again. The WCNT reset is re-asserted.

6.4. Boot timing TAG part

Figure 6-1 shows a timing of reset releasing and reset in TAG.

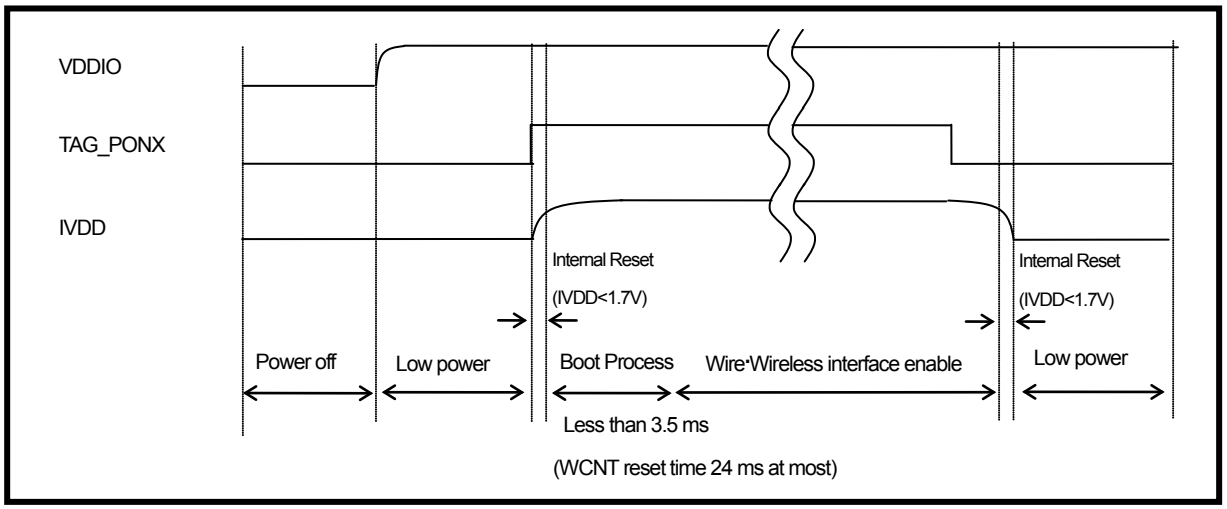


Figure 6-1 Timing of reset releasing and reset in TAG.

7. TAG Clock control

7.1. Features

Features of TAG clock control in TC35670FTG are shown in the below.

- Automatic discrimination function of clock source
- Operating by clock of wireless carrier or internal oscillator

7.2. Functional Explanation

There are two types of clock sources in TC35670FTG. One is carrier clock extracted from wireless carrier and its frequency is 13.56 MHz (typ.). The other is OSC clock which is output from the built-in oscillator and its frequencies are 12.8 MHz (typ.)

8. TAG Security functions

8.1. Features

TAG security features of TC35670FTG are shown in the below.

- Mutual authentication function with message authentication code (MAC)
- Various access attribute can be set.

  Reading only, reading/writing, reading after authentication, writing after authentication, writing with MAC

  Reading only can be set separately for the wired interface and the wireless interface.
- The wireless interface and wired interface separately keep external authentication statuses.
- The wireless interface and the wired interface use same card key (CK1 and CK2),

8.2. Functional Explanation

In TC35670FTG, the wireless interface and the wired interface separately keep external authentication status. Thus, even if external authentication is conducted over the wireless interface, but if external authentication is not conducted over the wired interface, access by wired interface is limited.

RC blocks separately exist for the wireless interface and wired interface. However, access can be done with the same block number. The wireless interface and the wired interface keep session key separately. In the wired interface, Byte 1 in STATE block is valid and in external authentication, Byte1 is written 01h.

When message authentication code (MAC) is used, writing over the wireless interface or the wired interface can be temporally prohibited by WLOCK block.

In case of start-up by wire power supply and the usage of the wireless interface and then detection of wireless carrier disappearing, the below things are cleared.

- External authentication status for the wireless interface. (Byte 0 in STATE block)
- RC block writing status over the wireless interface
- Polling command response setting (Byte 8 in STATE block)
- Writing prohibition setting for wired interface (Byte0 in WLOCK block)
- IDd(ID[0]-[7]) in ID Block

9. Electrical Characteristics

9.1. Absolute maximum rating

Absolute maximum ratings must not be exceeded even for a moment. Voltages, currents, and temperatures that exceed the absolute maximum ratings can cause break-downs, degradations, and damages not only for ICs but also for other components and boards. Please make sure application designs not to exceed the absolute maximum ratings in any situation.

Table 9-1 Absolute maximum rating (VSSA1=VSSA2=VSSD=VSSX=0 V)

Items	Symbols	Ratings		Units
		Min	Max	
Power supply	VDD, VDDIO (Note1)	-0.3	+3.9	V
Input voltage	V_{IN}	-0.3	VDDIO+0.3(Note2)	V
Output voltage	V_{OUT}	-0.3	VDDIO+0.3(Note2)	V
Input current	I_{IN}	-10	+10	mA
Input power	RFIO	—	+6	dBm
Input voltage	V_{L01}(L0,L1pin)	—	15	V
Input current	I_{L01}(L0,L1pin)	—	25	mA
Storage temperature	Tstg	-40	+125	°C

Note1: It is not supposed that VDD is grounded while VDDIO is supplied. It can trigger current path from VDDIO to VDD through internal circuitry, and may cause degradations and break-downs.

Note2: Keep VDDIO + 0.3 V < 3.9 V.

9.2. Operating Conditions

TC35670FTG can operate normally with proven quality under the operating conditions. Any deviation from the operating conditions may cause false operation. Thus, please make sure application design to comply these operating conditions.

Table 9-2 Operating conditions (VSSA1=VSSA2=VSSD=VSSX= 0 V)

Items	Symbols	Ratings			Units
		Min	Typ.	Max	
Power supplies	VDDopr1	1.80	3.00	3.60	V
	VDDopr2	1.96	3.00	3.60	V
	VDDIOopr	1.80	3.00	3.60	V
	VDD15IN	1.45	1.50	3.60	V
	VDD12A1 / VDD12A2 / VDD12X.	—	1.2	—	V
	VDD12D	—	1.1	—	V
RF frequency	Fc	2400	—	2483.5	MHz
Clock frequencies	Reference clock Fck	25.99870	26.00000	26.00130	MHz
	Sleep clock fslclk	32.751616	32.768000	32.784384	kHz
Ambient operating temperature.	Ta	-30	+25	+85	°C

Note1: VDD pin has a built-in low-voltage detection function, and it will stop functioning at less than the minimum voltage of VDDopr1. Because the low-voltage detection voltage has a hysteresis so that it will not start again due to the load variation after stopping, it starts at the minimum voltage of the VDDopr2 at the voltage rising. To make the power supply by an external power source, it must have more than the minimum voltage of the VDDopr2.

Note2: Please refer to other documents (application note) for our connection examples.

Note3: Please do not input power supply and do connect external capacitors to VDD12A1, VDD12A2, VDD12D, and VDD12X because they are supplied by the internal LDO.

9.3. DC electrical characteristics

9.3.1. Current Consumption

This section shows current consumption. When the operating temperature (Ta) is 25°C, and the operation of each power supply pin is in the recommendation connection state of our company, the current consumption is an average value.

Table 9-3 Current consumtion (VDD=VDDIO=3.0 V, VSSA1=VSSA2=VSSD=VSSX=0 V, DCDCEN=VDD)

Items	Symbols	Conditions	Pins	Ratings			Unit
			(Note)	Min	Typ.	Max	
Digital operation	IDD_{DIG} (Active1)	—	VDD	—	1.8	—	mA
RX	IDD_{RX} (Active2)	—		—	6.3	—	
TX	IDD_{TX} (Active3)	Output Power= -4dBm		—	6.3	—	
Low power mode With Connection	IDDS1 (Sleep)	26 MHz crystal oscillator disabled 32 kHz external oscillator enabled	VDD	—	10	—	μA
Low power mode Without Connection	IDDS2 (Backup)	26 MHz crystal oscillator disabled 32 kHz external oscillator enabled		—	5.0	—	
Low power mode Without Connection	IDDS (Deep Sleep)	26 MHz crystal oscillator disabled 32 kHz external oscillator disabled		—	0.05	—	

Note: Current consumption of IO part in Active operation can be changed by buffer setting.

Table 9-4 current consumption TAG (VDD=VDDIO=3.0 V,VSSA1=VSSA2=VSSD=VSSX=0 V)

Parameter	Symbol	Condition	Measurement Terminal	Specification			Unit
				Min	Typ.	Max	
Operation	IDD_{OPE}	TAG_PONX=0 V Without RF carrier	VDDIO	—	0.4	—	mA
Low Power Mode (PONB=High)	IDDS5	TAG_PONX=VDDIO Without RF carrier	VDDIO	—	0.1	—	μA

Table 9-5 shows DC electrical characteristics for each pin at 25°C ambient temperature.

Table 9-5 Electrical Characteristics (VDD=VDDIO=3.0 V,VSSD=VSSA1=VSSA2=VSSX= 0 V)

Item	Symbol	Condition		Measuring Pin (Note 1)	Rating			Unit
		I/F Voltage	Other Condition		Min	Typ.	Max	
High Level Input Voltage	VIH	3.0 V	LVCMOS	VDDIO	0.8×VDDIO	—	—	V
Low Level Input Voltage	VIL	3.0 V	LVCMOS	VDDIO	—	—	0.2×VDDIO	
High Level Input Current	IIH	VDDIO = Input Voltage of each pin	Pull-down Off	VDDIO	-10	—	10	μA
			Pull-down On		10	—	200	
Low Level Input Current	IIL		Pull-up Off		-10	—	10	
			Pull-up On		-200	—	-10	
High Level Output Voltage	VOH	3.0 V	IOH = 1 mA	VDDIO	VDDIO-0.6	—	—	V
Low Level Output Voltage	VOL	3.0 V	IOL = 1 mA	VDDIO	—	—	0.4	V
External 32 kHz Clock Input level	VIH SLPCLK	3.0 V	—	SLPEXCLKIN	0.8×VDDIO	—	—	V
	VIL SLPCLK	3.0 V	—	SLPEXCLKIN	—	—	0.2×VDDIO	V

Note1: Please refer to Table 2-4 for power supply line for each pin.It shows the power supply system of each functional pin.

Table 9-6 Electrical Characteristics TAG part (VDD=VDDIO=3.0V,VSSD=VSSA1=VSSA2=VSSX= 0V)

Parameter	Symbol	Condition	Measurement Terminals (Note1)	Specification			Unit
				Min	Typ.	Max	
High Level Input Voltage	VIH2	—	TAG_SCL, TAG_SDA, TAG_PONX	0.7×VDDIO	—	—	V
Low Level Input Voltage	VIL2	—		—	—	0.3×VDDIO	
High Level Input Current	IIH2	VIN=VDDIO to VDDIO×0.7	TAG_SCL, TAG_SDA	-1	—	1	μA
		VIN=VDDIO to VDDIO×0.7	TAG_PONX	-10	— (Pull-up: Resistance 400kΩ(typ.))	1	
Low Level Input Current	IIL2	VIN=VDDIO×0.3 to GND	TAG_SCL, TAG_SDA	-1	—	1	
		VIN=VDDIO×0.3 to GND	TAG_PONX	-20	— (Pull-up: Resistance 400kΩ(typ.))	-1	
		VIN=VDDIO×0.3 to GND Without RF Carrier	TAG_RFDET	-1	— (Pull-down: Resistance 200kΩ(typ.))	20	
High Level Output Voltage	VOH2	IOH = -1 mA	TAG_READYX	VDDIO-0.3	—	—	V
		IOH = -1 mA With RF Carrier	TAG_RFDET	VDDIO-0.3	—	—	V
Low Level Output Voltage	VOL2	IOL = 1 mA	TAG_READYX	—	—	0.3	V

Note1: Please refer to Table 2-4 for power supply line for each pin.

9.4. Built-in Regulator Characteristics

Table 9-7 Built-in regulator characteristics (VDD = 1.8 to 3.6 V, VSSA1 = VSSA2 = VSSD = VSSX = 0 V)

Item	Symbol	Pin names and conditions	Ratings			Units
			Min	Typ.	Max	
Output voltages	Vout1	DCDCOUT	—	1.5	—	V
	Vout2	VDD12A1 / VDD12A2 /VDD12X	—	1.2	—	V
	Vout3	VDD12D	—	1.1	—	V

9.5. ADC Characteristics

Table 9-8 ADC characteristics (VDD = 1.8 to 3.6 V, VSSA1 = VSSA2 = VSSD = VSSX = 0 V)

Item	Symbol	Condition	Ratings			Unit
			Min	Typ.	Max	
Analog reference voltage	VREFH		1.8	3.0	3.6	V
Analog input voltage	VAIN	–	VSSD	–	VREFH	V

9.6. RF Characteristics

The following conditions are applicable unless otherwise specified.

- Ta = 25°C
- VDD = 3.0 V, DCDCEN = VDD
- fx'tal = 26 MHz (Frequency accuracy is adjusted to ±2 ppm at normal temperature)
- PAOUT= 0 dBm

Table 9-9, Table 9-10 shows RF receiving characteristics and RF transmitting characteristics based on Bluetooth® Core Spec. V4.1 low energy.
About the characteristics data here, some are design value, not measured value.

Table 9-9 RF Characteristics

Test Item	Packet	bit	ch.	Condition	Spec.			Unit
					Min	Typ.	Max	
Output Power	37 octets	PRBS9	0,12, 19,39	peak	—	—	Pavg+ 3dB	dBm
				average	—	0	–	
In-band Spurious Emissions	37 octets	PRBS9	0,12, 19,39	-5 MHz	—	-60	-30	dBm
				-4 MHz	—	-60	-30	
				-3 MHz	—	-57	-30	
				-2 MHz	—	-50	-20	
				2 MHz	—	-50	-20	
				3 MHz	—	-57	-30	
				4 MHz	—	-60	-30	
				5 MHz	—	-60	-30	
Modulation Characteristics	37 octets	11110000	0,12, 19,39	Δf1avg (11110000)	225	254	275	kHz
		10101010		Δf2max (min-min) (10101010)	185	208	—	
		—		Δf2avg /Δf1avg	0.8	0.90	—	Ratio
Carrier frequency offset (CFO)	37 octets	10101010	0,12, 19,39	average	—	3	—	kHz
				worst	-150	—	150	
Drift	37 octets	10101010		Absolute maximum	—	10	50	kHz
Drift Rate	37 octets	10101010		Absolute maximum	—	4	20	kHz/50 μs

Table 9-10 RF Characteristics

Test Item	Sub Item	Packet	bit	ch.	Condition	Min	Typ.	Max	Unit
Rx Sensitivity		37 octets		0,12, 19,3	PER=30.8% at 1500 packets with dirty	—	-92	—	dBm
C/I Performance	PER=30.8% at 1500 packets with dirty	37 octets	D wave: PRBS9 U wave: GFSK PRBS15	0,2,12, 19,37, 39	<=-6 MHz	—	-36	-27	dB
					-5 MHz	—	-36	-27	
					-4 MHz	—	-36	-27	
					-3 MHz	—	-36	-27	
					-2 MHz	—	-27.5	-17	
					-1 MHz	—	12.5	15	
					0 MHz	—	11	21	
					1 MHz	—	12.5	15	
					2 MHz	—	-27.5	-17	
					3 MHz	—	-34	-27	
					4 MHz	—	-25	-15	
					5 MHz	—	-18	-9	
					6 MHz	—	-25	-15	
					=>7 MHz	—	-38	-15	
Blocking Performance	—	37 octets	D wave: PRBS9 U wave:CW	12	30-2000 MHz	-30	—	—	dBm
					2003-2399 MHz	-35	—	—	
					2484-2997 MHz	-35	—	—	
					3000M-12.75 GHz	-30	—	—	
Intermodulation	1500 packets	37 octets	f1=-50dBm with un-modulation f2=-50dBm with PRBS15	0,12, 19,39	-4 MHz	30.8	–	—	%
					+4 MHz				
Max Input	PER	37 octets	PRBS9	0,12, 19,39	-10dBm	30.8	0	—	%
Max Input	PER	37 octets	PRBS9	0,12, 19,39	-30dBm	50	50	65.4	%

Note: Blocking characteristic has a disturbance characteristic more than ±3 MHz, the relief specs of the logo attestation test of Bluetooth® maybe applied. The blocking characteristic measures D wave as 12ch.

9.7. Rectifier circuit clamp charactersitic in TAG part

Table 9-11 Rectifier circuit clamp characteristic in TAG part

Item	Symbol	Condition	Rating			Unit
			Min	Typ.	Max	
Clamp characteristic in operation	V_{CLA1}	TAG_RECTOUT:3.3mA TAG_PONX=0 V	4.8	5.5	6.2	V
Clamp characteristic in non-operation	V_{CLA2}	TAG_RECTOUT:3.3 mA TAG_PONX=VDDIO	2.8	4.2	5.2	V

9.8. Voltage detection characteristic in TAG part

Table 9-12 Voltage detection characteristic in TAG part

Item	Symbol	Condition	Rating			Unit
			Min	Typ.	Max	
Voltage detection characteristic	V_{DET0}	VDDIO voltage which releases internal reset TAG_PONX=0 V	—	1.7	1.79	V

9.9. OSC frequency characteristic in TAG part

Table 9-13 OSC frequency characteristic in TAG part

Item	Symbol	Condition	Rating			Unit
			Min	Typ.	Max	
OSC frequency characteristic	f_{TAGOSC}	TAG_PONX=0 V	11.5	12.8	14.1	MHz

9.10. Terminal capacitance in TAG part

Table 9-14 Terminal capacitance in value TAG part

Item	Symbol	Condition	Rating			Unit
			Min	Typ.	Max	
Terminal capacitance between TAG_L0-TAG_L1	C_{L01}	—	—	8.6	—	pF

9.11. EEPROM characteristic in TAG part

Table 9-15 EEPROM characteristic in TAG part

Item	Symbol	Condition	Rating			Unit
			Min	Typ.	Max	
The number of rewriting	—	Ta=25°C	10^5	—	—	Times
Data storage period	—	Ta=85°C	10	—	—	Year

9.12. AC Interface Characteristics

9.12.1. UART Interface

Table 9-16 UART Interface AC characteristics

Symbols	Items	Min	Typ.	Max	Unit
tCLDTDLY	CTSX falling edge to Data transmission start	192	—	—	ns
tCHDTDLY	CTSX rising edge to Data transmission completion	—	—	2	byte
tRLDTDLY	RTSX falling edge to Data reception start	0	—	—	ns
tRHDTDLY	RTSX rising edge to Data reception completion	—	—	8	byte

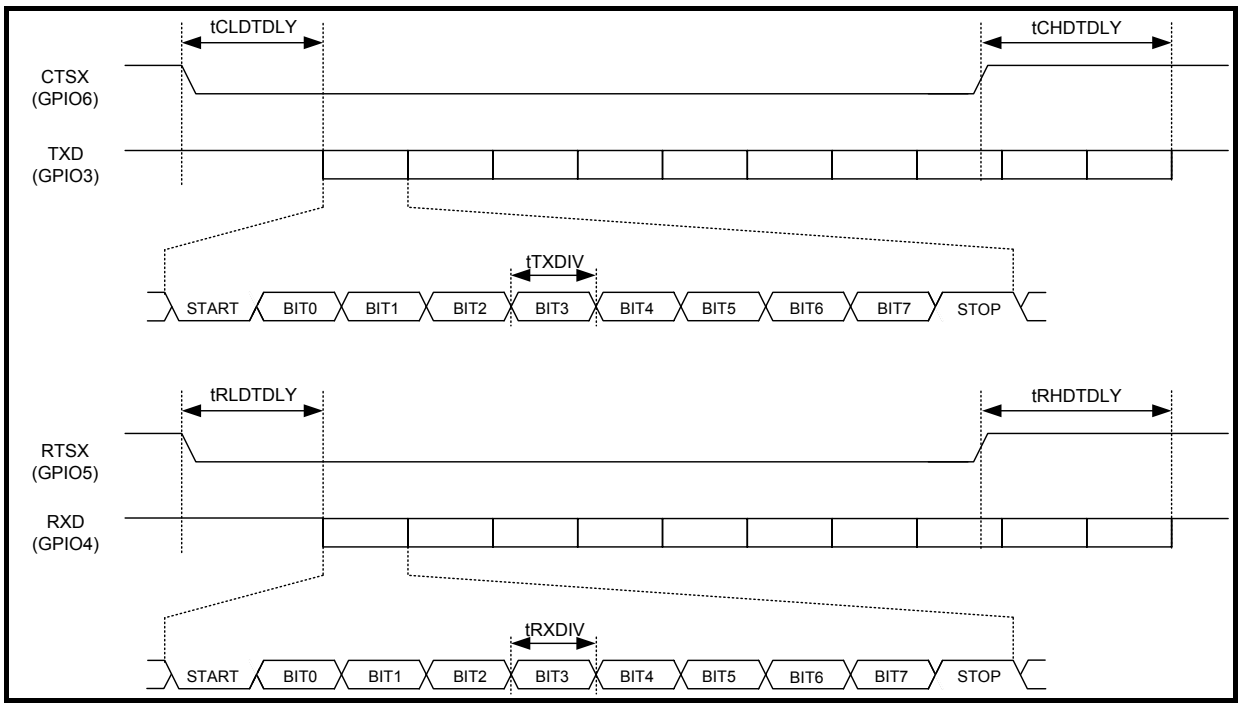


Figure 9-1 UART Interface Timing Diagram

9.12.2. I²C Interface

9.12.2.1. Normal Mode

Table 9-17 I²C Interface Normal mode AC Characteristics

Symbols	Items	Min	Typ.	Max	Unit
tDATS	Data set-up time	250	—	—	ns
tDATH	Data hold time	300	—	—	ns
tDATVD	Datavalidity period	—	—	3450	ns
tACKVD	ACKvalidity period	—	—	3450	ns
tSTAS	Restart condition set-up time	4700	—	—	ns
tSTAH	Restart condition hold time	4000	—	—	ns
tSTOS	Stop condition set-up time	4000	—	—	ns
tBUF	Bus open period from stop condition to start condition	4700	—	—	ns
tr	Rise up time	—	—	1000	ns
tf	Fall down time	—	—	300	ns
tHIGH	Serial clock period of High	4000	—	—	ns
tLOW	Serial clock period of Low	4700	—	—	ns
Cb	Bus load capacitance	—	—	400	pF

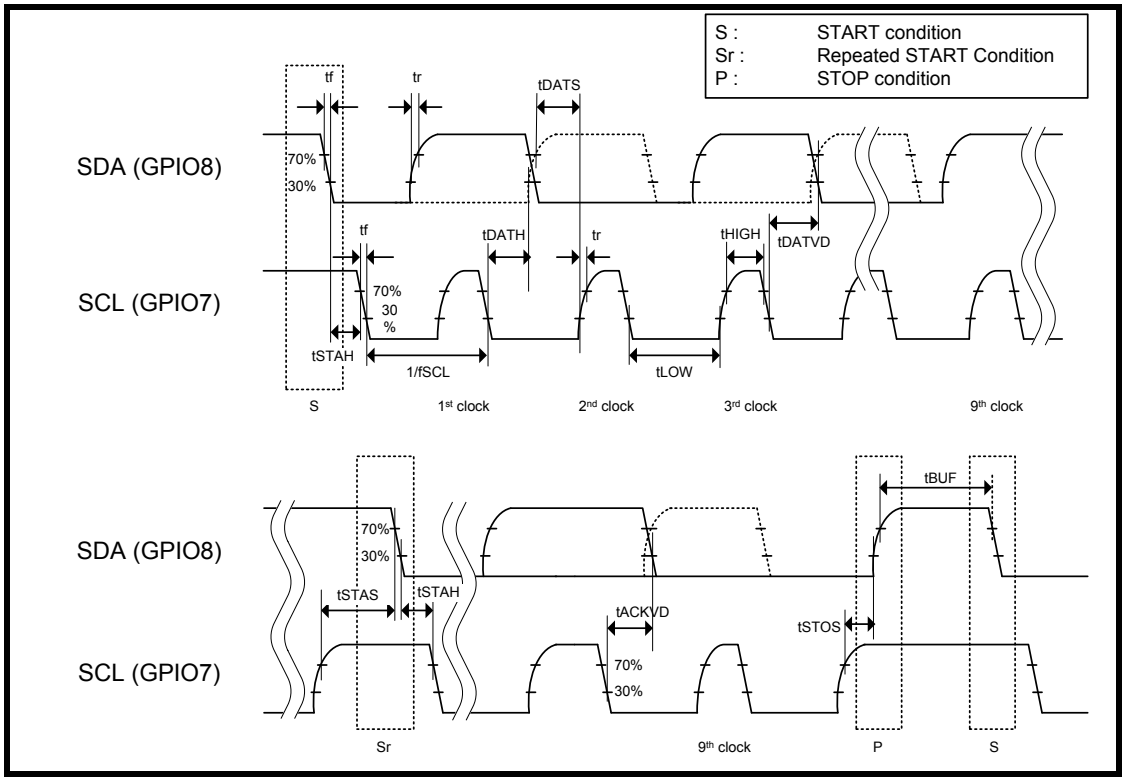


Figure 9-2 I²C Interface Normal mode Timing diagram

9.12.2.2. Fast mode

Table 9-18 I²C Interface Fast mode AC Characteristics

Symbols	Items	Min	Typ.	Max	Unit
tDATS	Data set-up time	100	—	—	ns
tDATH	Data hold time	300	—	—	ns
tDATVD	Datavalidity period	-	—	900	ns
tACKVD	ACKvalidity period	-	—	900	ns
tSTAS	Restart condition set-up time	600	—	—	ns
tSTAH	Restart condition hold time	600	—	—	ns
tSTOS	Stop condition set-up time	600	—	—	ns
tBUF	Bus open period from stop condition to start condition	1300	—	—	ns
tr	Rise up time	20 + 0.1Cb	—	300	ns
tf	Fall down time	20 + 0.1Cb	—	300	ns
tSP	Spike pulse width that can be removed	0	—	50	ns
tHIGH	Serial clock period of High	—	1423	—	ns
tLOW	Serial clock period of Low	—	1423	—	ns
Cb	Bus load capacitance	—	—	400	pF

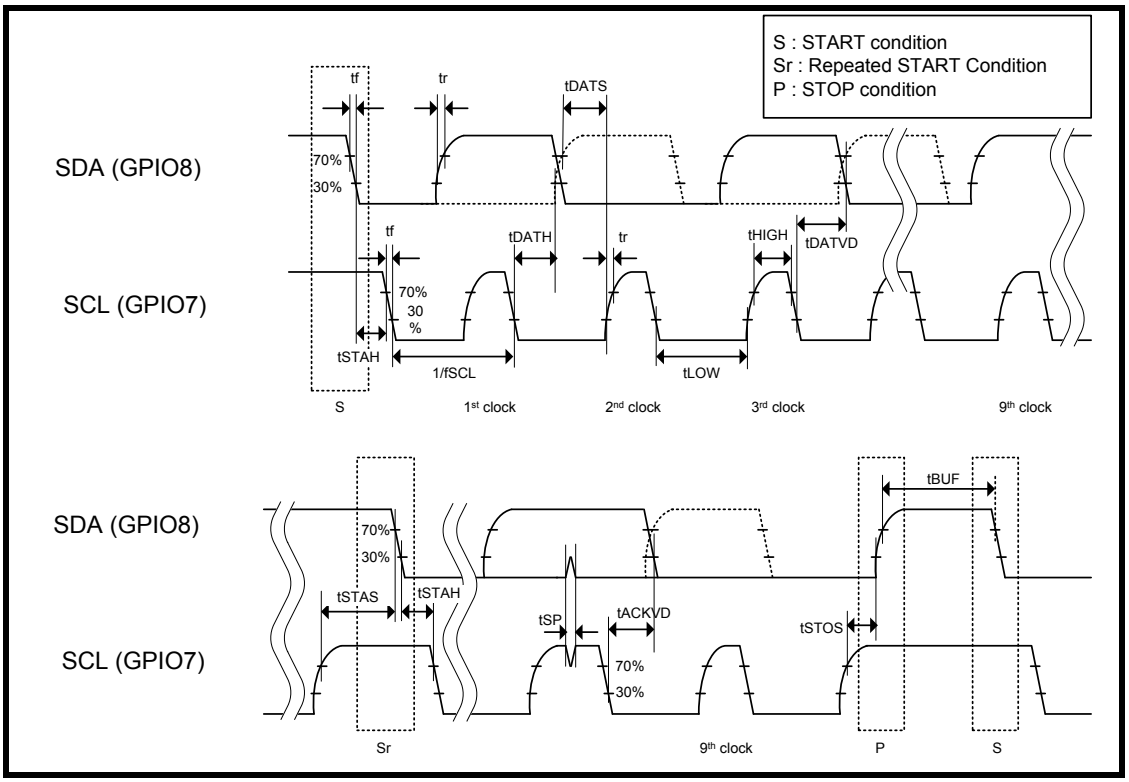


Figure 9-3 I²C Interface Fast mode Timing diagram

9.12.3. SPI Interface

Table 9-19 SPI Interface

Symbols	Items	Min	Typ.	Max	Unit
tSPICLKCYC	SPI clock frequency	154	—	—	ns
tSPICLKHPW	SPI clock high pulse width	77	—	—	ns
tSPICLKLPW	SPI clock low pulse width	77	—	—	ns
tSPICSS	SPI chip select setup time	38	—	—	ns
tSPICSH	SPI chip select hold time	77	—	—	ns
tSPIIW	SPI transfer idle pulse width	54	—	—	ns
tSPIAS	SPI address setup time	38	—	—	ns
tSPIAH	SPI address hold time	77	—	—	ns
tSPIDS	SPI data setup time	38	—	—	ns
tSPIDH	SPI data hold time	77	—	—	ns

Note: SPIIinterface operates on the basis of 1/n frequency of half the frequency of ARM7™ core clock (6.5 MHz for 13 MHz core clock)

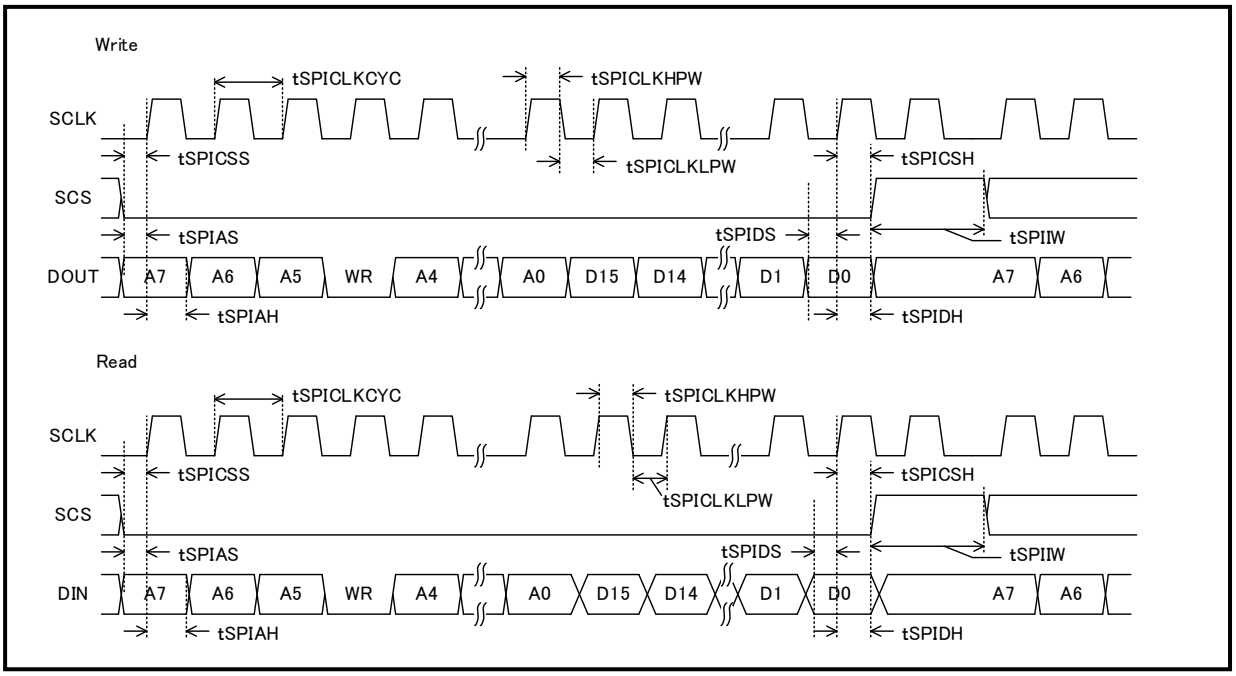


Figure 9-4 SPI Interface timing diagram

9.12.4. I²C Interface TAG part

Table 9-20 I²C Interface Tag part AC Characteristics

Symbols	Items	Min	Typ.	Max	Unit
tDATS	Data set-up time	100	—	—	ns
tDATH	Data hold time	300	—	—	ns
tDATVD	Datavalidity period	—	—	900	ns
tACKVD	ACKvalidity period	—	—	900	ns
tSTAS	Restart condition set-up time	600	—	—	ns
tSTAH	Restart condition hold time	600	—	—	ns
tSTOS	Stop condition set-up time	600	—	—	ns
tBUF	Bus open period from stop condition to start condition	1300	—	—	ns
tr	Rise up time	20 + 0.1Cb	—	300	ns
tf	Fall down time	20 + 0.1Cb	—	300	ns
tSP	Spike pulse width that can be removed	0	—	50	ns
tHIGH	Serial clock period of High	600	—	—	ns
tLOW	Serial clock period of Low	1300	—	—	ns
Cb	Bus load capacitance	—	—	400	pF

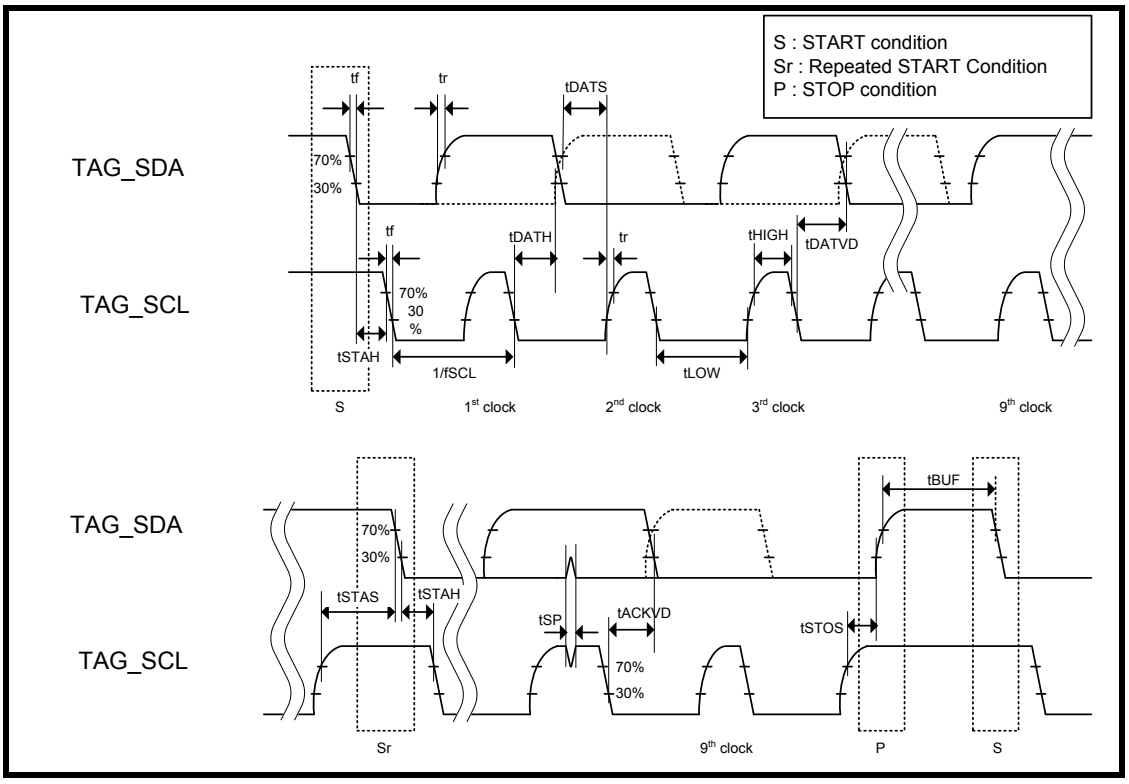


Figure 9-5 I²C Interface Tag part Timing diagram

10. System Configuration Example

An example of system configuration is shown in the following figures.

10.1. In case of Host CPU connection

- Host interface = UART and 26 MHz Reference Clock= XOSC Connection.
- GPIO of connection is the connection example of when not in use.

Note: When the host CPU connection, GPIO3, 4 is when it is changed to UART2 and SPI, will become uncontrollable not accept the command.

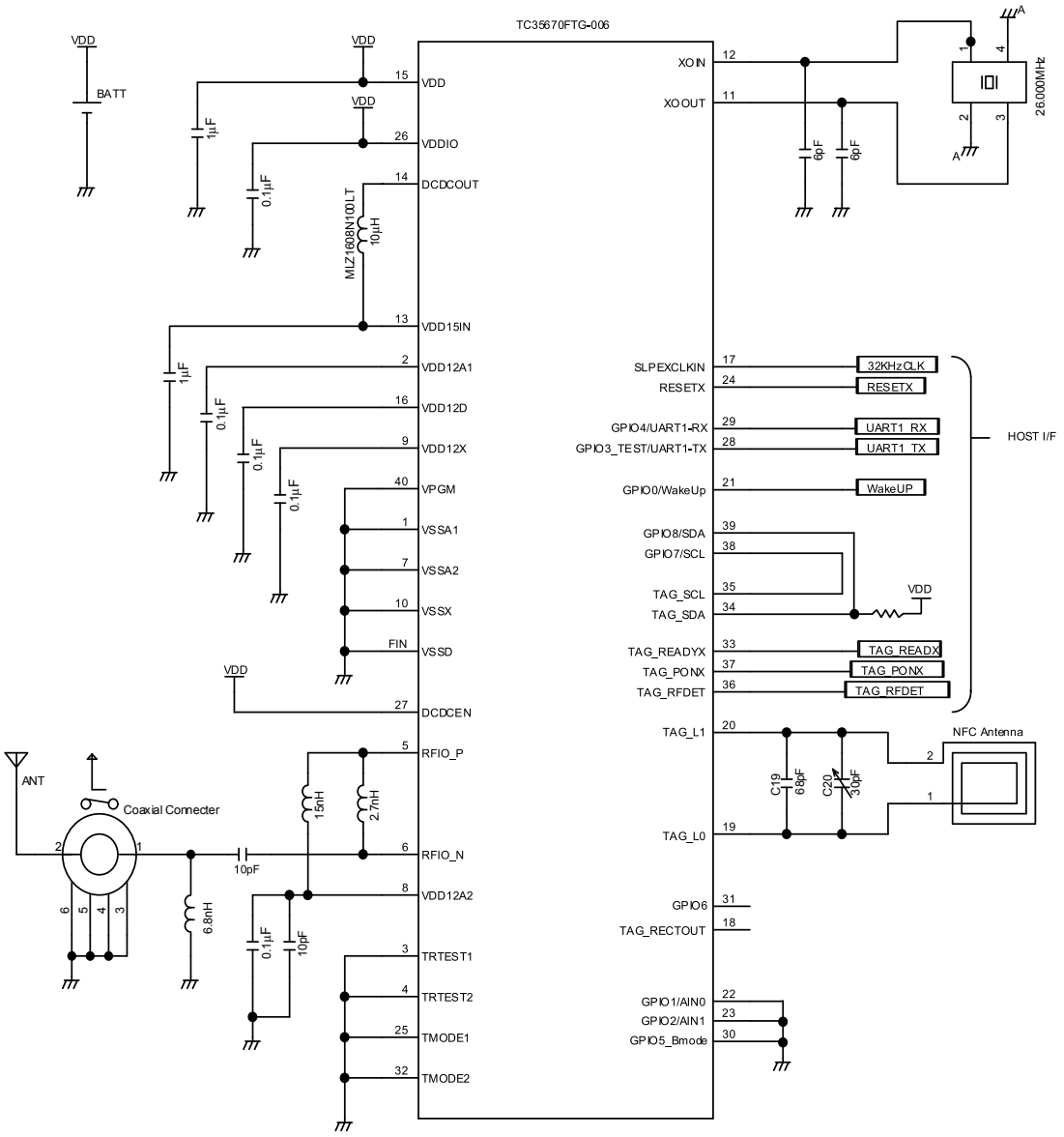


Figure 10-1 Example of TC35670FTG system configuration (HOST CPU connection)

10.2. In case of Standalone

- GPIO of connection is the connection example of when not in use.
- To prepare the test for the interface, set the GPIO5 to the switching control pin for H (stand-alone) / L (HCI mode).Then set the GPIO3,4 to UART1 (command input).Then connect the GPIO3,4,and 5 with external control equipment. Even in this case, please becomes therefore attention an external pull-up is required at all times to GPIO4.

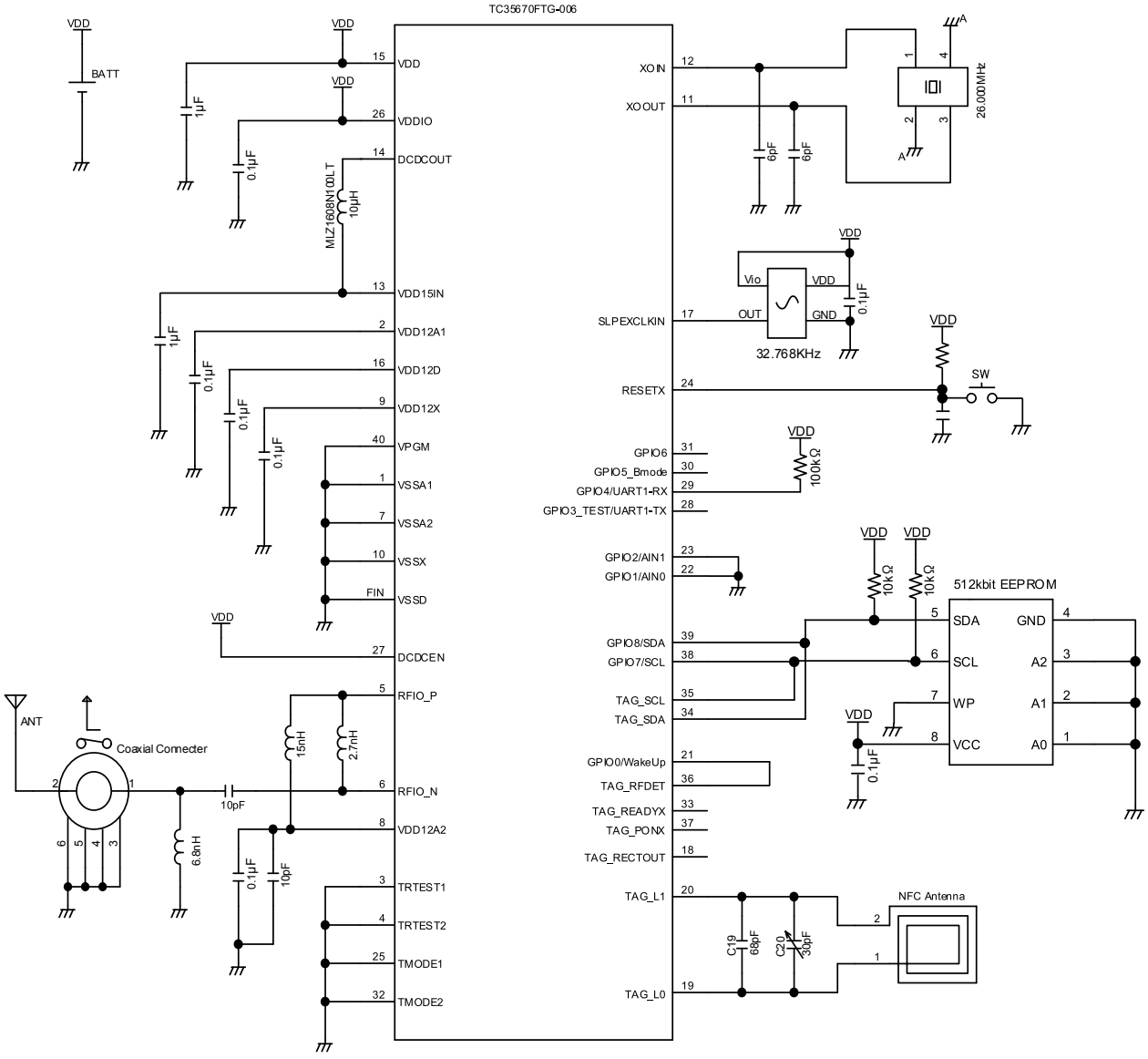
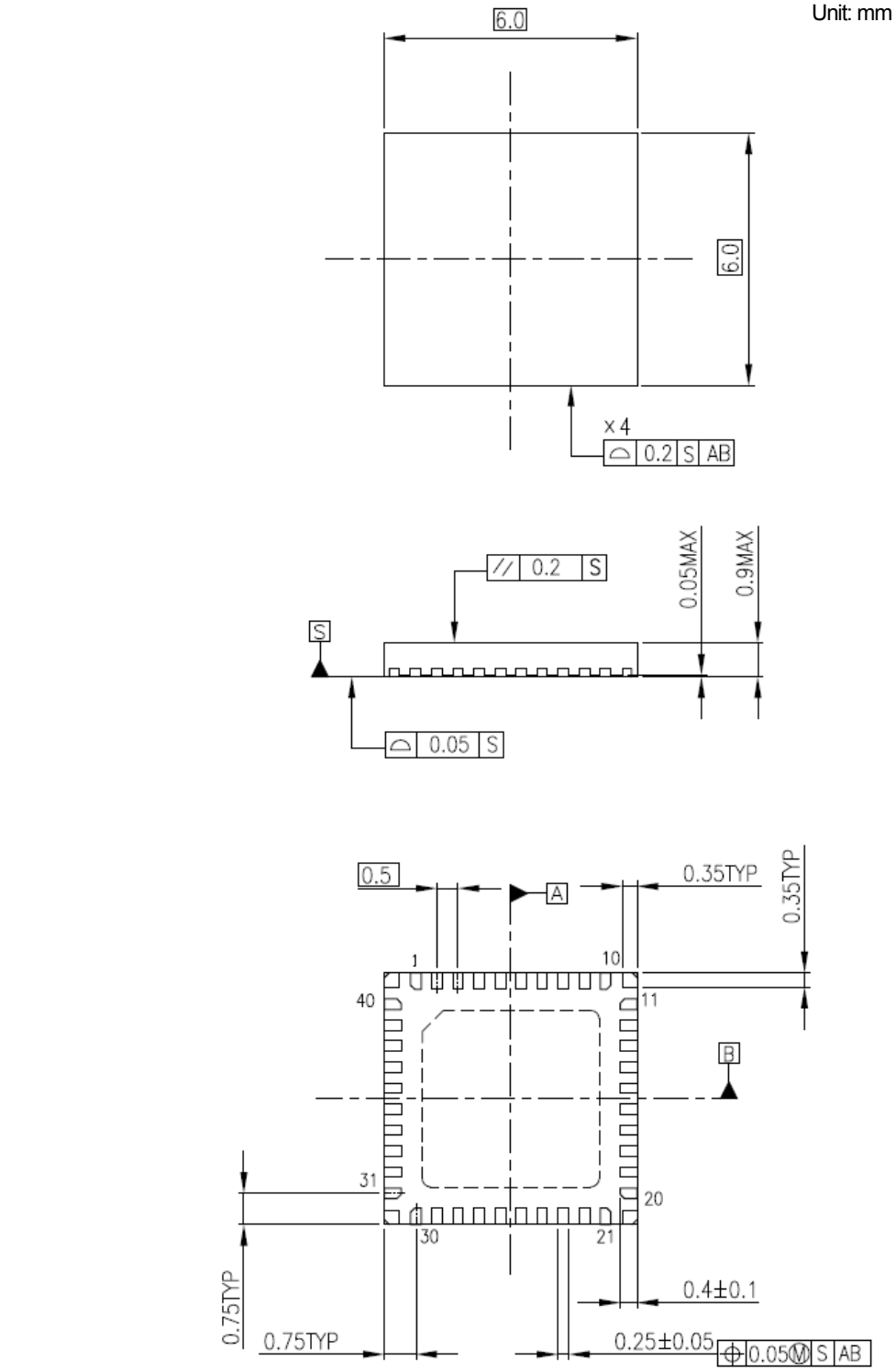


Figure 10-2 Example of TC35670FTG system configuration (Stand-alone)

11. Package outline

11.1. Outline dimensional drawing

Unit: mm



Weight: 0.112 g (Typ.)

Figure 11-1 Package outline (P-VQFN40-0606-0.50-001)

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