Texas Instruments

TAS5076–5182C6EVM

Evaluation Module for the TAS5076 Six-Channel Digital Audio PWM Processor and the TAS5182 Digital Power MOSFET Driver

User's Guide

November 2003

Digital Audio and Video Products

SLEU048

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 0 V to 40 V for the output stage and 15 V ±10% for the control gate drive.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 75°C. The EVM is designed to operate properly with certain components above 75°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

Preface

Read This First

About This Manual

This manual describes the operation of the TAS5076−5182C6EVM evaluation module from Texas Instruments.

How to Use This Manual

This document contains the following chapters:

Chapter 1 − Overview

Chapter 2 − System Interface

Chapter 3 − Protection

Information About Cautions and Warnings

This book may contain cautions and warnings.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

Related Documentation From Texas Instruments

The following is a list of technical documentation that may be usefule to a user of the TAS5026−5182C6EVM. It includes data sheets having detailed descriptions of the integrated circuits used in the design of the TAS5026−5182C6EVM, as well as other potentially useful documents. These items can be obtained at http://www.ti.com.

Data Sheets	**Literature Number**
True Digital Audio Amplifier TAS5076 Digital Audio PWM Processor	SLES090
TAS5182 100W Stereo Digital Amplifier Power Stage Controller	SLES045
TPS79133, Ultra Low Noise, HIgh PSRR, Fast RF, Low-Enable, 100 mA Low Dropout Regulator	SLVS325
TPS3801K33, Ultra-Small Supply Voltage Supervisors	SLVS219
LM317M, 3-Terminal, 500 mA, Adjustable Positive Voltage Regulator	SCVS297I
SN74AHC1G08 Single 2-Input Positive AND Gate	SCLS314
SN74LV123A Dual Retriggerable Monostable Multivibrators With Schmitt-Trigger Inputs	SCLS393
Application Report	
TAS5076-5182C6EVM Application Report	SLEA026
Digital Audio Measurements	SLAA114
System Design Considerations for True Digital Audio Power Amplifiers (Rev. A)	SLAA117

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Contents

Figures

Tables

Chapter 1

Overview

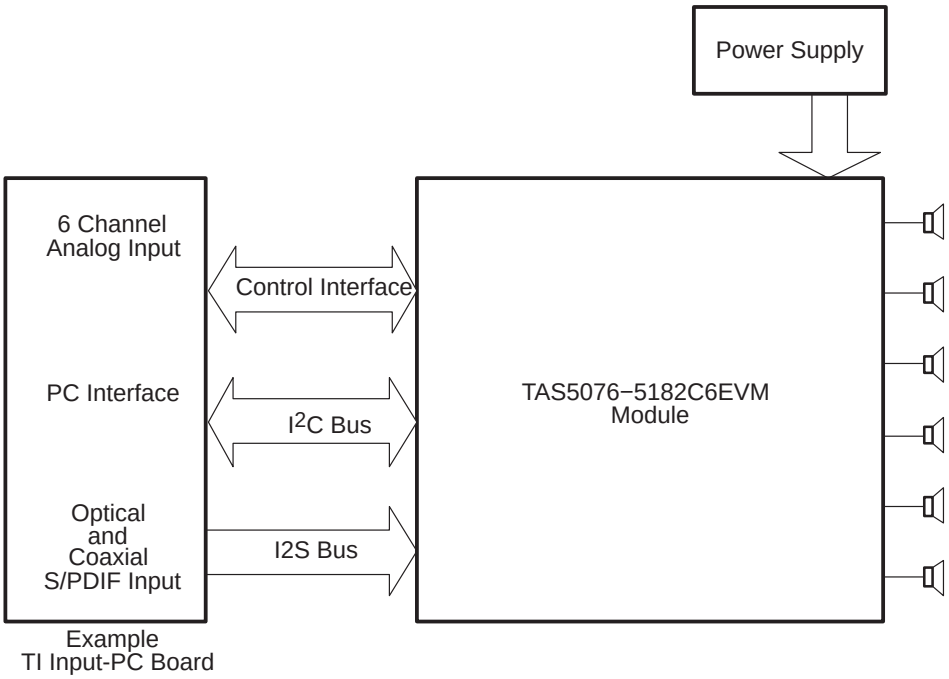
The TAS5076−5182C6EVM board is a six channel Pure Path Digital™ evaluation module for the integrated circuits TAS5076PFC and TAS5182DCA from Texas Instruments (TI). The TAS5076PFC is a 24-bit multi channel Pure Path Digital pulse-width modulator based on Equibit™ technology. The TAS5182DCA is a high-performance MOSFET gate driver with built-in overcurrent and over temperature protection for the MOSFETs.

The TAS5076 and TAS5182 together with 24 IRFIZ24N MOSFETs provide the complete conversion of a 3.3-V digital audio input stream to six times 100 W into 6-Ω impedance. The chipset is ideal for applications requiring absolute highest audio quality, minimum size and weight, and high power efficiency. The chipset can be used in a range of products such as high-end slim-line AV receivers, high-end DVD receivers, and multi-way active speakers.

The TAS5076−5182C6EVM module is an integrated true digital audio amplifier system, which includes digital volume control interface and failure protection reporting.

Topic **Page**

Figure 1−1. Integrated True Digital Audio Amplifier System



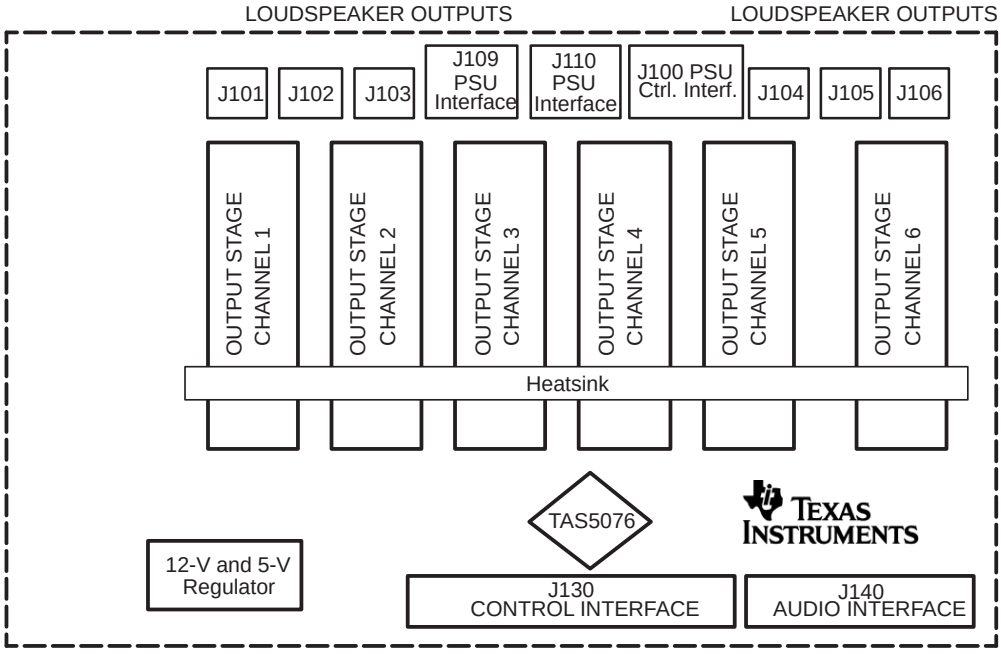
1.1 TAS5076−5182C6EVM Features

- Six channel TDAA reference design (double-sided plated-through PCB layout)
- Self-contained protection system (short circuit and thermal)
- Standard I^2S and I^2C / Control connector for TI input board

1.2 PCB Outline

The physical structure for the TAS5076−5182C6EVM is illustrated in Figure 1−2.

Figure 1−2. Physical Structure for the TAS5076−5182C6EVM (Rough Outline)



Chapter 2

System Interface

This chapter describes the TAS5076−5182C6EVM board in regards to power supplies and system interfaces.

Topic **Page**

2.1 PSU Interface (J109 and J110)

The TAS5076−5182C6EVM module must be powered from external power supplies. High-end audio performance requires a stabilized power supply with low ripple voltage and low output impedance throughout the audio band, see the application note *Power Supply Considerations TDAA AV-Receivers (SLEA028)*.

Note:

The length of power supply cable must be minimized. Increasing length of PSU cable is equal to increasing the distortion for the amplifier at high output levels and low frequencies.

The maximum output stage supply voltage depends on the speaker load resistance. Check the maximum supply voltage in the TAS5182 data sheet.

Table 2−1. Recommended Supply Voltages

Description	Voltage limitations	Current Recommendations
System power supply voltage	15 V (min. 14.5 V, max 29.5 V)	0.15 A
Output stage supply voltage	0 V−40.55 V	5.5 A†

† the rated current corresponds to two channel full scale (100 W each) at 1 kHz.

The recommended TAS5182 power-up sequence is shown in the Figure 2−1. For proper TAS5182 operation the $\overline{\text{RESET}}$ signal should be kept low during power up. $\overline{\text{RESET}}$ is pulled low during power up for 200 ms by the onboard reset generator (U681).

Figure 2−1. Recommended Power-Up Sequence

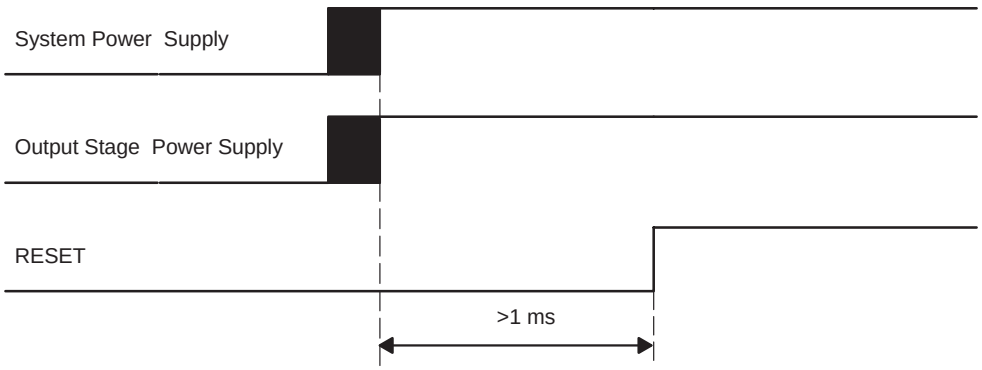


Figure 2−2. J109 and J110 Pin Numbers (PCB Connector Top View)

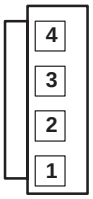


Table 2−2. J109 Pin Description

Pin #	Net-Name at Schematics	Description
1	V−HBRIDGE	Output stage supply voltage
2	−	System power supply
3	GND	Ground
4	GND	Ground

Table 2−3. J110 Pin Description (For decrease of impedance to reach performance)

Pin #	Net-Name at Schematics	Description
1	V−HBRIDGE	Extra output stage supply voltage
2	V−HBRIDGE	Extra output stage supply voltage
3	GND	Extra ground
4	GND	Extra ground

2.2 PSU Control Interface (J100)

This interface is used for onboard sensing of output supply voltage and for future use.

Figure 2−3. Pin Numbers at PSU Control Interface

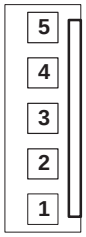


Table 2−4. J100 Pin Description

Pin #	Net-Name at Schematics	Description
1	NOT USED	−
2	V−HBRIDGE	Sense of output supply voltage
3	GND	Ground
4	$\overline{\text{RESET}}$	System reset (bidirectional)
5	V−HBRIDGE−CTRL	Power supply output voltage control signal

2.3 Loudspeaker Connectors (J101, J102, J103, J104, J105, and J106)

Caution

Both positive and negative speaker outputs are floating and may not be connected to ground (e.g., through and oscilloscope).

Figure 2−4. Pin Numbers at Loudspeaker Connectors

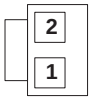


Table 2−5. Pin Description of Loudspeaker Connectors

Pin #	Net-Name at Schematics	Description
1	OUT−1	Speaker negative output
2	OUT−2	Speaker positive output

2.4 Control Interface (J130)

This interface connects the TAS5076−5182C6EVM board to the micro-controller section.

Table 2−6. J130 Pin Description

Pin #	Net-Name at Schematics	Description
1	GND	Ground
2	V−HBRIDGE−CTRL	Power supply output voltage control
3	GND	Ground
4	$\overline{\text{RESET}}$	System reset (bidirectional). TAS5076 enters a 4-ms initiation sequence before PWM signals are present at output. Activate $\overline{\text{MUTE}}$ before $\overline{\text{RESET}}$ for quiet reset.
5	$\overline{\text{ERR−RCVY}}$	Error recovery (or soft reset) provides reduced click and pop reset, without resetting I^2C volume register settings.
6	$\overline{\text{MUTE}}$	Ramp volume from any setting to noiseless soft mute. Mute can also be activated by I^2C.
7	RESERVED	−
8	RESERVED	−
9	RESERVED	−
10	SDA	I^2C data clock
11	GND	Ground
12	SCL	I^2C bit clock
13	RESERVED	−
14	RESERVED	−
15	RESERVED	−
16	RESERVED	−
17	GND	Ground
18	RESERVED	−
19	RESERVED	−
20	$\overline{\text{SHUTDOWN}}$	Shutdown error reporting. Activated if one or more TAS5182 has overcurrent or over temperature.

Table 2−6. J130 Pin Description (Continued)

Pin #	Net-Name at Schematics	Description
21	RESERVED	−
22	$\overline{\text{TEMP−WARNING}}$	Temperature warning. Activated if one or more TAS5182 has reached warning temperature level.
23	RESERVED	−
24	RESERVED	−
25	GND	Ground
26	GND	Ground
27	RESERVED	−
28	RESERVED	−
29	RESERVED	−
30	RESERVED	−
31	GND	Ground
32	GND	Ground
33	+5V	+5-V supply (out)
34	+5V	+5-V supply (out)

2.5 PWM Tming, ABD and Inter Channel Delay Register Setting

For maximum performance, the PWM timing shall be optimized for the configuration and layout. These so called ABD and inter-channel delays shall be programmed by I^2C to the TAS5076 at startup and at every reset. See the TAS5076 data manual for these register programming details.

Table 2−7. ABD and Inter Channel Delay Register Setting

Register Description	Register	Setting
Inter channel delay channel 1	0Ch	01h
Inter channel delay channel 2	0Dh	49h
Inter channel delay channel 3	0Eh	91h
Inter channel delay channel 4	0Fh	39h
Inter channel delay channel 5	10h	21h
Inter channel delay channel 6	11h	69h
ABD delay	12h	1Dh

2.6 Digital Audio Interface (J140)

The digital audio interface contains digital audio signal data (I2S), clocks, etc. See the TAS5076 data manual for signal timing and details not explained in this document.

Table 2−8. J140 Pin Description

Pin #	Net-Name at Schematics	Description
1	GND	Ground
2	MCLK	Master clock input. Low jitter system clock for PWM generation and reclocking. Ground connection from source to the TAS5076 must be a low impedance connection.
3	GND	Ground
4	SDIN1	I2S Data 1, Channel 1 and 2
5	SDIN2	I2S Data 2, Channel 3 and 4
6	SDIN3	I2S Data 3, Channel 5 and 6
7	RESERVED	–
8	GND	Ground
9	GND	Ground
10	GND	Ground
11	SCLK	I2S bit clock
12	GND	Ground
13	LRCLK	I2S left/right clock
14	GND	Ground
15	RESERVED	–
16	GND	Ground

Table 2−9. Clock Rates

Speed	TAS5076 System Control Register 0 (x02h)	Sample Frequency Fs	LRCLK	SCLK (64xFs)	MCLK
Normal Speed MCLK = 256xFs	D7 = 0 D6 = 0	32 kHz	32 kHz	2.048 MHz	8.192 MHz
		44.1 kHz	44.1 kHz	2.8224 MHz	11.2896 MHz
		48 kHz	48 kHz	3.072 MHz	12.288 MHz
Double Speed MCLK = 256xFS	D7 = 0 D6 = 1	64 kHz	64 kHz	4.096 MHz	16.384 MHz
		88 kHz	88.2 kHz	5.6448 MHz	22.5792 MHz
		96 kHz	96 kHz	6.144 MHz	24.576 MHz
Quad Speed MCLK = 128xFS	D7 = 1 D6 = 0	176 kHz	176.4 kHz	11.2896 MHz	22.579 MHz
		192 kHz	192 kHz	12.288 MHz	24.576 MHz

Chapter 3

Protection

The TAS5182 protects the output MOSFET devices and provides fault reporting (including over-temperature protect and short circuit protection). The TAS5182 is on the evaluation module configured in latching mode after all errors. In this mode error recovery is handled by TAS5076.

Topic **Page**

3.1 Device Fault Reporting

The $\overline{\text{ERR0}}$ and $\overline{\text{SHUTDOWN}}$ outputs from the TAS5182 indicate fault conditions. See the TAS5182 data sheet for a description of these pins.

The $\overline{\text{ERR0}}$ signals at the TAS5076−5182C6EVM board are all joined (wire-or) to one single warning signal.

Shutdown signals are all jointed (wired-or) to one single shutdown signal.

The shutdown signal together with the $\overline{\text{ERR0}}$ (temperature warning) at the PWM interface (J130) gives chip state information as described in Table 3−1. Device fault reporting outputs are open-drain outputs.

Table 3−1. TAS5182 Warning/Error Signal Decoding

$\overline{\text{ERR0}}$	$\overline{\text{SHUTDOWN}}$	DEVICE CONDITION
0	0	Over-temperature error and/or overcurrent error
0	1	Over-temperature warning
1	0	Undervoltage lockout due to GVDD or overcurrent error
1	1	Normal operation, no errors/warnings

3.2 Autorecovery System

The TAS5076−5182C6EVM is configured in autorecovery mode, as closed loop between the TAS5076 and shutdown signal from the TAS5182. In autorecovery mode, the $\overline{\text{SHUTDOWN}}$ signal from the TAS5182 is connected to the $\overline{\text{ERR−RCVY}}$ input on the PWM processor.

The short circuit protection error condition results in the following autorecovery sequence:

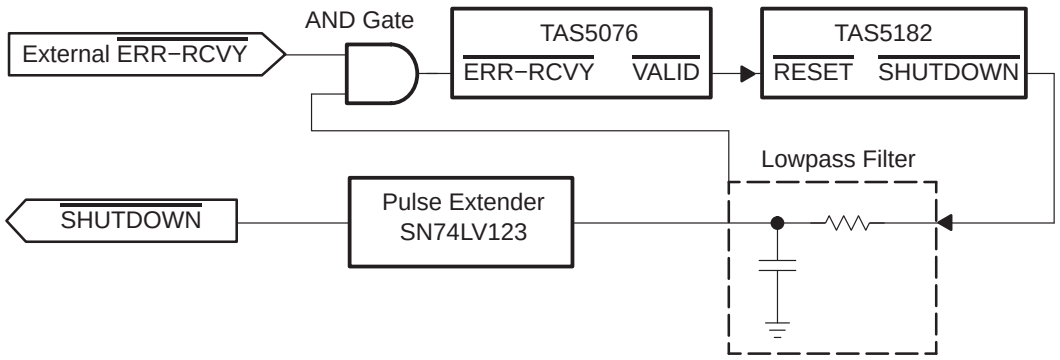
1) H-bridge output is in high impedance state (Hi-Z state) just after short circuit.

2) $\overline{\text{ERR−RCVY}}$ at the PWM processor is forced low by TAS5182 $\overline{\text{SHUTDOWN}}$ signal.

3) $\overline{\text{RESET}}$ at the TAS5182 is forced low by the PWM processor /VALID signal.

4) The $\overline{\text{RESET}}$ signal goes high after approx. 4 ms, which restarts switching of TAS5182.

Figure 3−1. Autorecovery Loop



The EXTERNAL−ERR−RCVY (J130) pin 5 is used to provide click and pop reduced error recovery without resetting the TAS5076 registers. This can also be used as a soft reset.

The SHUTDOWN (J130) pin 20 can be used for external microprocessor for registration of overcurrent events, which leads to deactivation of the amplifier (because of possible short circuit of output) when repeated constantly.