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T40N Smart Video Application Processor

DATA SHEET

Release Date: August. 25, 2021

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1 Overview

T40N is a smart video application processor targeting for video devices like mobile camera, security survey, video talking, video analysis and so on. This SoC introduces a kind of innovative architecture to fulfill both high performance computing and high quality image and video encoding requirements addressed by video devices. T40N provides high-speed CPU computing power, excellent image signal process, fluent 3840x2160 resolution video recording.

The CPU (Central Processing Unit) core, equipped with 32kB instruction and 32kB data L1 cache, and 128kB~1024kB configurable L2 cache, operating at 1.0GHz, and full feature MMU function performs OS related tasks. At the heart of the CPU core is XBurst®-2 processor engine. XBurst®-2 is an industry leading microprocessor core which delivers superior high performance and best-in-class low power consumption. A hardware floating-point unit which compatible with IEEE754 2008 and MIPS32 ISA R5 plus MIPS SIMD instruction set architecture:512bit MSA also included.

The VPU (Video Processing Unit) core is a video encoder engine designed to process video streams using the HEVC(ISO/IEC 23008-2 High Efficiency Video Coding) and AVC(ISO/IEC 14496-10 Advanced Video Coding) standards. It also supports still picture encoding using the JPEG standard(ITU T.81). Together with the on chip video accelerating engine and post image processing unit, T40N delivers high video performance. The maximum resolution of 4096x4096 in the format of AVC are supported in encoding. Up to 40Mbit/s for H.264, 20Mbit/s for H.265, 1080P@60fps.

The ISP (Image signal processor) core supports excellent image process with the image from up to 3 sensors. Supports DVP, MIPI and TOF sensors. With the functions, such as 3A, 2D and 3D denoise, WDR/HDR, lens shading and so on. It can supply maximum resolution 3840x2160 resolution image for view or encoding to store or transfer.

For more quickly and easily to use T40N, DDR2 KGD is integrated on chip.

On-chip modules such as audio CODEC, multi-channel SAR_ADC controller and camera interface offer designers a economical suite of peripherals for video application. WLAN, Bluetooth and expansion options are supported through high-speed SPI and eMMC/SD/SDIO host controllers. Other peripherals such as USB OTG, MAC, UART and SPI as well as general system resources provide enough computing and connectivity capability for many applications.

1.1 Block Diagram

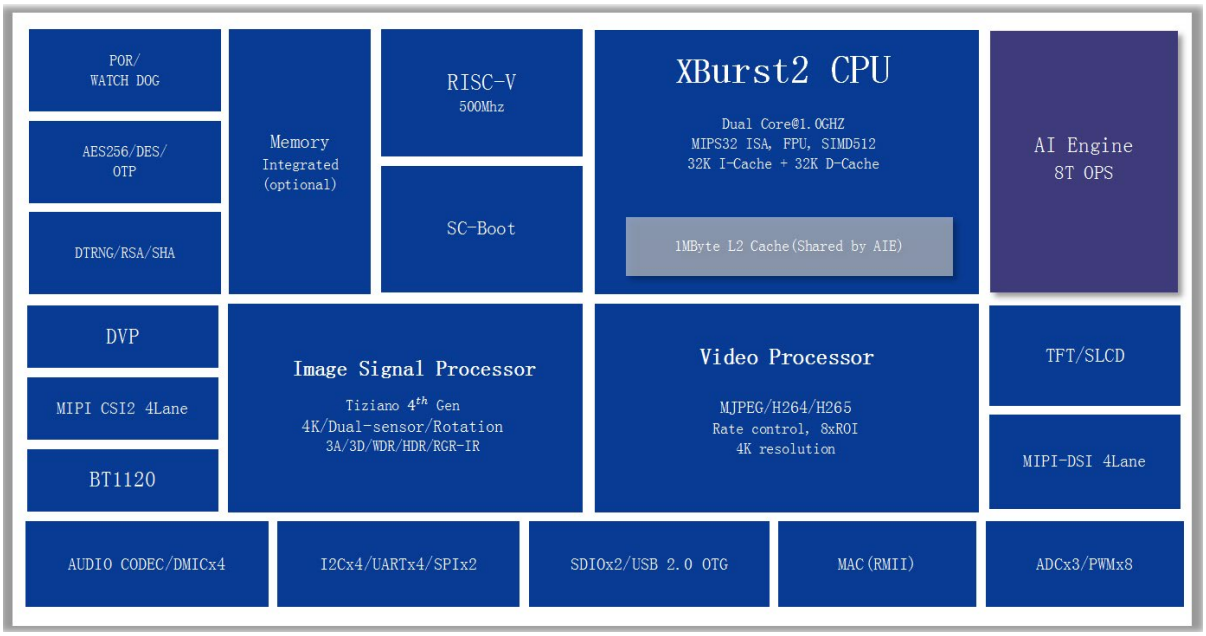


Figure 1-1 T40N Diagram

1.2 Features

1.2.1 CPU

- XBurst®2 up to 1.0GHz, Dual Core, Dual-issue, high performance and low power implementation of MIPS32 ISA R5
- MIPS32 ISA R5 plus Ingenic SIMD512 ISA
- Dual-issue, super-scalar, super pipeline with Simultaneous Multi-Threading(SMT)
  - Two hardware threads per physical core
  - Quad instruction fetches per cycle
  - Dual issue instructions per cycle per thread
- 32K L1 D cache + 32K L1 I cache, 128~1024K L2 cache
- High-performance Floating-point Unit and SIMD Engine: FSE
  - 32x512-bit register set, 512-bit loads/stores to/from SIMD unit
  - IEEE-754 2008 compliant

- Programmable Memory Management Unit(MMU)
  - 1st level mini-TLBs(MTLBs)-8x2 entry instruction TLB, 16x2 entry data TLB
  - 2nd level TLBs:32x2 entry VTLB, 256x2 entry 4-way set associative FTLB
- The XBurst®2 processor system supports little endian only

1.2.2 MCU

- 500MHz RISC-V co-processor
- 32bit, in-order, 5-stage pipeline core
- 32K L1-cache and 32K L1 D-cache
- RV32IM instruction set architecture

1.2.3 AI Engine

- Built-in neural network accelerator
- Typical Performance: 8TOPS
- Support int16/int8/int4/int2 bit width
- Shared 1MB memory pool
- Magik AI algorithm develop platform available

1.2.4 AI Co-Processing Unit(AIU)

- Color conversion
- Re-size
- Hardware matrix operations

1.2.5 Video Processor Unit(VPU)

- Support H.264/H.265/JPEG combo Encoder
- Real-time H.256/H.264 encoding capabilities:3840x2160@20fps
- Support maximum resolution up to 4096x4096
- JPEG snapshot at 8 megapixels

1.2.6 Image Signal Processor(ISP)

- Support up to 3 sensors
- Support MIPI and DVP interface sensor
- Support maximum resolution 3840x2160
- 3A (Auto Exposure/Auto White Balance/Auto Focus) and able to output the statistical information
- Green equalization
- Black level correction
- Lens Shading Correction
- Lens Distortion Correction
- Dynamic/Static Defect pixel correction
- Demosaic
- 2D/3D Color Correction
- Gamma Correction
- Brightness/Contrast/Saturation/Hue Adjustment
- Adaptive Dynamic Range Compression
- Defog, WDR
- Adaptive Local Contrast Enhancement
- Sharpen
- 2D/3D Denoise
- Chroma Noise Reduction
- 3 Independent Image Scale Up/Down Engine
- Crop, Mirror and Flip

1.2.7 Display Process Controller(DPU)

- MIPI-DSI four lane interface
  - Display size up to 1920x1080@60Hz

- SLCD controller
  - Display size up to 640x480@60Hz,24BPP
  - Support different size of display panel
- RGB controller
  - Display size up to 1280x720@60Hz,24BPP
  - Supports input format, ARGB8888, ARGB1555, RGB888, RGB565, RGB555, YUV422, YUV420
  - Support 4 modes parallel interface, 24-bit, 18-bit, 16-bit and 8-bit(third times)
  - Support frame buffer crop and dither

1.2.8 Video Input and Output

- Video Input
  - Support 8/10/12 bit RGB Bayer input
  - Support DVP, BT1120(serial model)/BT656/BT601
  - Support MIPI CSI (lane up to 1.5Gbps, and support one 4-Lane or two 2-Lane sensor)
  - Support maximum:3840x2160@20fps
  - Support up to 3 sensor inputs (DVP/BT, two CSI 2lane)
- Video output
  - Support BT656 serial/parallel mode
  - Support BT1120 serial/parallel mode
  - Support MIPI DSI 4lane

1.2.9 Audio System

- Integrated Audio Codec
  - 24 bits DAC with 93dB SNR
  - 24 bits ADC with 92dB SNR
  - Support signal-ended and differential microphone input and line input

- Automatic Level Control (ALC) for smooth audio recording
- Pure logic process: no need for mixed signal layers and less mask cost
- Programmable input and output analog gains
- Digital interpolation and decimation filter integrated
- Sampling rate 8K/12K/16K/24K/32/44.1K/48K/96K

- Digital MIC controller
  - 16 bits data interface and 20bit precision internal controller
  - SNR:90dB, THD:-90dB @ FS -20dB
  - Linear high pass filter include. Attenuation: -2.9dB@100Hz, -22dB@27Hz, -36dB@10Hz
  - Low power voice trigger when waiting to start talking
  - 1/2/3/4 channel digital MIC support
  - Support voice data pre-fetch when trigger enable and the data interface disable, but do not increase the power dissipation
  - Sample frequency supported: 8K, 16K
  - Support low power mode, user for decrease DMIC sensor and DMIC controller power dissipation
- Standard Audio I2S Interface
  - 16,20 and 24 bit audio sample data sizes supported, 16 bits packed sample data is supported
  - DMA transfer mode supported
  - Stop serial clock supported
  - Support mono PCM data to stereo PCM data expansion on audio play back
  - Support endian switch on 16-bits normal audio samples play back
  - Internal programmable or internal serial clock and optional system clock supported for I2S or MSB-Justified format
  - Two FIFOs for transmit and receive respectively
  - Support different sample rate for transmit and receive
  - Support echo cancellation function in the condition of the same sample rate in transmit

and receive

1.2.10 Memory Interface

- Integrated 1G bit DDR2 on chip

1.2.11 System Functions

- Clock generation and power management
  - On-chip 12/24/48MHZ oscillator circuit
  - One four-chip phase-locked loops (PLL) with programmable multiplier
  - CCLK, HHCLK, H2CLK, PCLK, H0CLK, DDR_CLK, VPU_CLK frequency can be changed separately for software by setting registers
  - SSI clock supports 50M clock
  - MSC clock supports 100M clock
  - Functional-unit clock gating
  - Shut down power supply for CPU, ISP, VPU, IPU
- Timer and counter unit with PWM output and/or input edge counter
  - Provide eight separate channels, six of them have input signal transition edge counter
  - 16-bit A counter and 16-bit B counter with auto-reload function every channel
  - Support interrupt generation when the A counter underflow
  - Three clock sources: RTCLK (real time clock), EXCLK (external clock input), PCLK (APB Bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected
  - Every channel has PWM output
- OS timer controller
  - 64-bit counter and 32-bit compare register
  - Support interrupt generation when the counter matches the compare register
  - Two clock sources: RTCLK (real time clock), HCLK (system bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected
- Interrupt controller

  - Total 64 interrupt sources
  - Each interrupt source can be independently enabled
  - Priority mechanism to indicate highest priority interrupt
  - All the registers are accessed by CPU
  - Unmasked interrupts can wake up the chip in sleep mode
  - Another set of source, mask and pending registers to serve for PDMA
- Watchdog timer
  - Generates WDT reset
  - A 16-bit Data register and a 16-bit counter
  - Counter clock uses the input clock selected by software
- PCLK, EXTAL and RTCLK can be used as the clock for counter
- The division ratio of the clock can be set to 1, 4, 16, 64, 256 and 1024 by software
- Direct memory access controllers
  - Support up to 32 independent DMA channels
  - Descriptor or No-Descriptor Transfer mode compatible with previous ingenic SoC
  - Transfer data units: 1-byte, 2-byte, 4-byte, 16-byte, 32-byte, 64-byte, 128-byte
  - Transfer number of data unit: 1 ~ 2^{24} - 1
  - Independent source and destination port width: 8-bit, 16-bit, 32-bit
  - Fixed three priorities of channel groups: 0~3, highest; 4~11: mid; 12~31: lowest
  - An extra INTC IRQ can be bound to one programmable DMA channel
- SAR A/D Interface
  - 4 single-ended input channels and 4 Standard I/O cell multiplexed
  - 12-bit resolution, up to 2MS/s sampling rate
  - DNL<1LSB,INL<2LSB
  - Max Frequency: 24MHz
  - Current consumption:2.5mA@2MS/s
- OTP Slave Interface

- Total 2048 bits. and used as 1024 bits for safe

- Power On Reset(POR)
  - Provides reliable reset function for general applications
  - Monitor 1.8V supply for IO and 0.9V for core
  - Typical 1.35V threshold for 1.8V supply
  - Typical 0.6V threshold for 0.9V supply

1.2.12 Peripherals

- General-Purpose I/O ports
  - Input/output/function port configurable
  - Low/high, rising/falling edge triggering. Every interrupt source can be masked independent
  - four interrupts, each interrupt corresponds to the group, to INTC

- Four I2C Controller(SMB0, SMB1, SMB2, SMB3)
  - Two-wire I2C serial interface – consists of a serial data line (SDA) and a serial clock (SCL)
  - Three speeds mode
    - Standard mode (100 Kb/s)
    - Fast mode (400 Kb/s)
    - High speed mode(3.4Mb/s)
  - Programmable SCL generator
  - Master or slave I2C operation
  - 7-bit addressing/10-bit addressing
  - The number of devices that you can connect to the same I2C-bus is limited only by the maximum bus capacitance of 400pF

- One High Speed Synchronous serial interfaces (SFC)

- 3 protocols support: National's Micro-wire, TI's SSP, and Motorola's SPI
- transmit-only or receive-only operation
- MSB first for command and data transfer, and LSB first for address transfer
- 64 entries x 32 bits wide data FIFO
- one device select
- Configurable sampling point for reception
- Configurable timing parameters: t_{SLCH}, t_{CHSH} and t_{SHSL}
- Configurable flash address wide are supported
- transfer formats: Standard SPI only
- two data transfer mode: slave mode and DMA mode
- Configurable 6 phases for software flow

- Normal Speed Synchronous serial interfaces (SSI0, SSI1)
  - 3 protocols support: National's Micro-wire, TI's SSP, and Motorola's SPI
  - Full-duplex or transmit-only or receive-only operation
  - Programmable transfer order: MSB first or LSB first
  - 128 entries deep x 32 bits wide transmit and receive data FIFOs
  - Configurable normal transfer mode or Interval transfer mode
  - Programmable clock phase and polarity for Motorola's SSI format
  - Back-to-back character transmission/reception mode
  - Loop back mode for testing

- Four UARTs (UART0, UART1, UART2,UART3)
  - Full-duplex operation
  - 5-, 6-, 7- or 8-bit characters with optional no parity or even or odd parity and with 1, 1½, or 2 stop bits
  - 64x8 bit transmit FIFO and 64x11bit receive FIFO

- Independently controlled transmit, receive (data ready or timeout), line status interrupts
- Internal diagnostic capability Loopback control and break, parity, overrun and framing-error is provided
- Separate DMA requests for transmit and receive data services in FIFO mode
- Supports modem flow control by software or hardware
- Slow infrared asynchronous interface that conforms to IrDA specification

- Two MMC/SD/SDIO controllers (MSC0, MSC1)
  - All support eMMC 5.1(command queuing Engine)
  - Support SD Specification 3.0
  - Support SD I/O Specification 1.0 with 1 command channel and 4 data channels
  - Consumer Electronics Advanced Transport Architecture (CE-ATA – version 1.1)
  - Maximum data rate is 104MBps
  - Both support MMC data width 1bit, 4bit
  - Single or multi block access to the card including erase operation
  - The maximum block length is 4096bytes

- USB 2.0 OTG interface
  - Complies with the USB 2.0 standard for high-speed (480 Mbps) functions and with the On-The-Go supplement to the USB 2.0 specification
  - Operates either as the function controller of a high- /full-speed USB peripheral or as the host/peripheral in point-to-point or multi-point communications with other USB functions
  - Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP)
  - UTMI+ Level 3 Transceiver Interface
  - Soft connect/disconnect
  - 16 Endpoints
  - Dedicate FIFO

- Supports control, interrupt, ISO and bulk transfer

- Ethernet Media Access controller
  - 10/100 Mbps operation
  - Supports MII and RMII PHY interfaces
  - Support IEEE 1588-2002

- Digital True Random Number Generator(DTRNG)
  - Pure digital logic circuits
  - True random number
  - Interrupt mode and no interrupt mode

1.2.13 Bootrom

22kB Boot ROM memory

1.3 Characteristic

Item	Characteristic
Process Technology	22nm CMOS low power
Power supply voltage	General purpose I/O: 1.8~3.3V DDR I/O: 1.8V(DDR2) ± 0.1V EFUSE programming: 1.8V ± 10% Analog power supply 1: 1.8V ± 10% Analog power supply 2: 3.3V ± 10% Core: 0.9V ± 0.1V
Package	BGA356, 14mm x 14mm x 1.22mm, 0.65mm pitch
Operating frequency	1.0GHz

2 Packaging and Pinout Information

2.1 Overview

T40N processor is offered in BGA356, show in Figure 2-1. The T40N pin to ball assignment is show in Figure 2-2. The detailed pin description is listed in Table 2-1~Table 2-12.

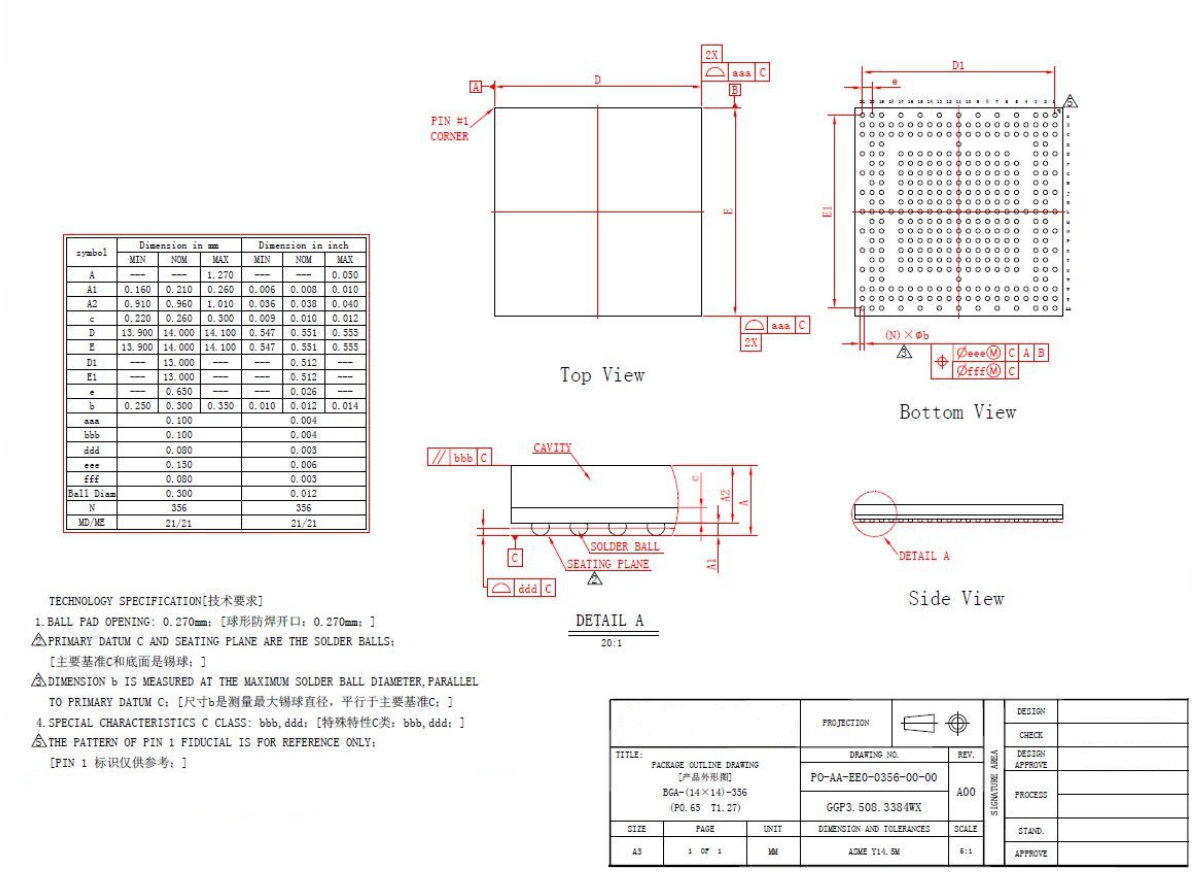
2.2 Solder Process

T40N package is lead-free. It's reflow profile follows the IPC/JEDEC lead-free reflow profile as contained in J-STD-020C.

2.3 Moisture Sensitivity Level

T40N package moisture sensitivity is level 3.

2.4 T40N Package



symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	----	----	1.270	----	----	0.050
A1	0.160	0.210	0.260	0.006	0.008	0.010
A2	0.910	0.960	1.010	0.036	0.038	0.040
c	0.220	0.260	0.300	0.009	0.010	0.012
D	13.900	14.000	14.100	0.547	0.551	0.555
E	13.900	14.000	14.100	0.547	0.551	0.555
D1	----	13.000	----	----	0.512	----
E1	----	13.000	----	----	0.512	----
e	----	0.650	----	----	0.026	----
b	0.250	0.300	0.350	0.010	0.012	0.014
aaa	0.100			0.004		
bbb	0.100			0.004		
ddd	0.080			0.003		
eee	0.150			0.006		
fff	0.080			0.003		
Ball Diam	0.300			0.012		
N	356			356		
MD/ME	21/21			21/21		

Figure 2-1 T40N package outline drawing

T40N Ball Assignment Ver1.5

BGA356, 14mm X 14mm X 1.22mm, 0.65pitch, top view

	0	1	2	3	4	5	6	7	8	9	10	
A		EFUSE_AVDD	CIM1_MCLK_PC30	MSC1_D2_SSI1_GPC_PC12		MSC1_D1_SSI1_DR_PC11		UART2_TXD_I2S_DAC_LRCK_PC18		UART0_TXD_SMB2_SDA_PC14		A
B		PPRST_	PWM1_PC28	CIM2_MCLK_PC29	MSC1_CMD_SSI1_CE0_PC09	MSC1_D0_SSI1_DT_PC10	SSI_SLV_CE0_I2S_SDTO_PC21	SSI_SLV_DR_I2S_ADC_LRCK_PC23	UART2_RTS_PWM0_PC27	UART0_CTS_I2S_DAC_MCLK_SMB0_SDA_PC16	UART2_CTS_DMIC_DAT1_PC26	B
C		POR_CTL	RST_OUT	CIM0_MCLK_PC31	MSC1_D3_SSI1_CE1_PC13	MSC1_CLK_SSI1_CLK_PC08	SSI_SLV_CLK_I2S_SDTI_PC20	SSI_SLV_DT_I2S_ADC_BCLK_PC22	UART2_RXD_I2S_DAC_BCLK_PC19	UART0_RTS_I2S_ADC_MCLK_SMB0_SCK_PC17	UART0_RXD_SMB2_SCK_PC15	C
D			VDDIO	TEST_TE								D
E		PLL_VDD	PLL_AVDD	PLL_AVSS			VSS	VSS	VSS	VSS	VSS	E
F			EXCLK_XI	EXCLK_XO		DDRVDD	DDRVDD	DDRVDD	DDRVDD	DDRVDD	DDRVDD	F
G		DVP_BT_PCLK_DMIC_DAT1_PA14	DVP_VSYNC_BT_D13_PA16	DVP_HSYNC_BT_D12_PA15		VDDMEM	VDDMEM	VDDMEM	VDDMEM	VDDMEM	VDDMEM	G
H			SA2_DVP_BT_D10_UART0_TXD_PA10	CS1_DVP_BT_D11_UART0_RXD_PA11		VSS	VSS	VSS	VSS	VSS	VSS	H
J		SD7_DVP_BT_D7_UART2_RXD_PA07	SA0_DVP_BT_D8_UART0_CTS_PA08	SA1_DVP_BT_D9_UART0_RTS_PA09		VDD	VDD	VDD	VDD	VDD	VDD	J
		1	2	3	4	5	6	7	8	9	10	

Figure 2-2 T40N pin to ball assignment(Part 1)

T40N Ball Assignment Ver1.5
BGA356, 14mm X 14mm X 1.22mm, 0.65pitch, top view

	11	12	13	14	15	16	17	18	19	20	21	
A	DMIC_CLK_PC24		TRST		UART3_RTS_TDO_PWM7_PD23		UART0_RXD_SSI0_DT_PWM0_PC02		PWM3_PB31	SMB3_SDA_UART2_TXD_SSI1_GPC_PB28	DRV_VBUS_UART2_CTS_SSI1_DR_PB27	A
B	DMIC_DAT0_PC25	SMB1_SDA_PWM0_PD26	BOOT_SEL0_PC00	UART3_TXD_TCK_PD24	UART3_CTS_TDI_PWM6_PD22	UART3_TXD_SSI0_CE1_PWM4_PC06	UART0_CTS_SSI0_DR_PWM1_PC03	UART1_RXD_PB24	PWM2_UART2_RTS_SSI1_CE0_PB30	SMB2_SCK_PWM5_SSI1_CLK_PB26	SMB2_SDA_PWM4_SSI1_DT_PB25	B
C	DDRPLL_VCCA	SMB1_SCK_PWM1_PD27	BOOT_SEL1_PC01	UART3_RXD_TMS_PD25	UART3_RXD_SSI0_GPC_PWM5_PC07	UART0_TXD_SSI0_CE0_PWM3_PC05	UART0_RTS_SSI0_CLK_PWM2_PC04	UART1_TXD_PB23	SMB3_SCK_UART2_RXD_SSI1_CE1_PB29	RGB_PCLK_BT656_1120_PCLK_SLCD_WR_PD08	RGB_HSYNC_PD17	C
D	DDRPLL_AVSS								RGB_VSYNC_SSI_SLV_DT_PD20	RGB_DE_SSI_SLV_DR_PD21		D
E	VSS	VSS	VSS	VSS	VSS	VSS	VREF		RGB_D17_SSI_SLV_CE0_PD19	RGB_D16_SSI_SLV_CLK_PD18	RGB_D15_BT1120_D15_PD16	E
F	DDRVDD	DDRVDD	DDRVDD	DDRVDD	DDRVDD	DDRVDD	NC		RGB_D14_BT1120_D14_PD15	RGB_D13_BT1120_D13_PD14		F
G	VDDMEM	VDDMEM	VDDMEM	VDDMEM	VDDMEM	VDDMEM	VDDMEM		RGB_D12_BT1120_D12_PD13	RGB_D11_BT1120_D11_SLCD_RDY_PD12	RGB_D10_BT1120_D10_SLCD_DC_PD11	G
H	VSS	VSS	VSS	VSS	VSS	VSS	VSS		RGB_D9_BT1120_D9_SLCD_CS_PD10	RGB_D8_BT1120_D8_SLCD_TE_PD09		H
J	VDD	VDD	VDD	VDD	VDD	VDD	VDD		RGB_D7_BT656_1120_D7_SLCD_D7_PD07	RGB_D6_BT656_1120_D6_SLCD_D6_PD06	RGB_D5_BT656_1120_D5_SLCD_D5_PD05	J
	11	12	13	14	15	16	17	18	19	20	21	

Figure 2-3 T40N pin to ball assignment(Part 2)

T40N Ball Assignment Ver1.5
BGA356, 14mm X 14mm X 1.22mm, 0.65pitch, top view

	0	1	2	3	4	5	6	7	8	9	10	
K			SD5_DVP_BT_D5_UART2_RTS_PA05	SD6_DVP_BT_D6_UART2_TXD_PA06		VDD	VDD	VDD	VDD	VDD	VDD	K
L		SD4_DVP_BT_D4_UART2_CTS_PA04	SD3_DVP_BT_D3_UART3_RXD_PA03	SD2_DVP_BT_D2_UART3_TXD_PA02	VDDIO33_DVP	VDD	VDD	VSS	VSS	VSS	VSS	L
M			SD1_DVP_BT_D1_UART3_RTS_PA01	SD0_DVP_BT_D0_UART3_CTS_PA00		VDD	VDD	VSS	VSS	VSS	VSS	M
N		RD_SMB0_SCK_DMIC_DAT0_PA13	CS2_SMB0_SDA_DMIC_CLK_PA12	VDDIO18_DVP		VDD	VDD	VSS	VSS	VSS	VSS	N
P			RX_DATAN0	RX_DATAP0		VDD	VDD	VSS	VSS	VSS	VSS	P
R		CSI_VCC18	RX_DATAN1	RX_DATAP1		VDD	VDD	VSS	VSS	VSS	VSS	R
T			RX_CLKN	RX_CLKP		VSS	VSS	VSS	VSS	VDD	VDD	T
U		CSI_VSSA	RX_CLKN1	RX_CLKP1		VSS	VSS	VSS	VSS	VDD	VDD	U
V			RX_DATAN2	RX_DATAP2								V
W		RX_DATAN3	RX_DATAP3	SADC_AUX0	SADC_AGND	USB0PP	USB_VSSA	USB_AVD18	SMB1_SCK_UART1_RXD_PA18	D_EFSYNC1_PA20	SFC_CE0_PA28	W
Y		CSI_VCC09	SADC_AUX2	SADC_AVDD	USB0PN	USB_AVD33	USB0ID	USB_AVD09	D_EFSYNC0_PA19	BT_D14_SMB3_SDA_PA21	SFC_D1_DR_PA24	Y
AA		SADC_AUX1	SADC_AUX3	SADC_VREFP		VBUS		SMB1_SDA_UART1_TXD_PA17		WAIT_BT_D15_SMB3_SCK_PA22		AA
		1	2	3	4	5	6	7	8	9	10	

Figure 2-4 T40N pin to ball assignment(Part 3)

T40N Ball Assignment Ver1.5
BGA356, 14mm X 14mm X 1.22mm, 0.65pitch, top view

	11	12	13	14	15	16	17	18	19	20	21	
K	VDD	VDD	VDD	VDD	VDD	VDD	VDD		RGB_D4_BT656_1120_D4_SLCD_D4_PD04	RGB_D3_BT656_1120_D3_SLCD_D3_PD03		K
L	VSS	VSS	VSS	VSS	VSS	VDD	VDD	RGB_D0_BT656_1120_D0_SLCD_D0_PD00	CODEC_AVSS	RGB_D1_BT656_1120_D1_SLCD_D1_PD01	RGB_D2_BT656_1120_D2_SLCD_D2_PD02	L
M	VSS	VSS	VSS	VSS	VSS	VDD	VDD		CODEC_AVDD	HPOUTL		M
N	VSS	VSS	VSS	VSS	VSS	VDD	VDD		MICNR	MICPR	VCM	N
P	VSS	VSS	VSS	VSS	VSS	VDD	VDD		MICNL	MICPL		P
R	VSS	VSS	VSS	VSS	VSS	VDD	VDDIO18		DSI_VCCA09	DSI_VSSA	MICBIAS	R
T	VDD	VDD	VDD	VDD	VDD	VDD	VDDIO18		TX_DATAN3	TX_DATAP3		T
U	VDD	VDD	VDD	VDD	VDD	VDDIO33	VDDIO33		TX_CLKP	TX_DATAN2	TX_DATAP2	U
V	SFC_D3_HOLD_PA26								DSI_VCCA18	TX_CLKN		V
W	SFC_D2_WP_PA25	MSC0_D0_PB00	MSC0_D3_PB03	MSC1_D1_SMB3_SDA_PB20	MSC1_CMD_SMB1_SCK_PB18	MSC1_D2_SMB3_SCK_PB21	GMAC_RXDV_I2S_ADC_MCLK_PB09	GMAC_RXD1_I2S_SDTO_PB16	GMAC_TXD1_I2S_ADC_LRCK_PB14	TX_DATAN1	TX_DATAP1	W
Y	SFC_D0_DT_PA23	MSC0_D1_PB01	MSC0_CMD_PB05	MSC0_D2_PB02	MSC1_CLK_SMB1_SDA_PB17	MSC1_D3_PB22	GMAC_MDCK_I2S_DAC_BCLK_PB10	GMAC_RXD0_I2S_SDTI_PB15	GMAC_PHY_CLK_PWM7_PB07	TX_DATAN0	TX_DATAP0	Y
AA	SFC_CLK_PA27		MSC0_CLK_PB04		MSC1_D0_PB19		GMAC_MDIO_I2S_DAC_LRCK_PB11		GMAC_TXCLK_PWM6_PB06	GMAC_TXD0_I2S_ADC_BCLK_PB13	GMAC_TXEN_I2S_DAC_MCLK_PB08	AA
	11	12	13	14	15	16	17	18	19	20	21	

Figure 2-5 T40N pin to ball assignment(Part 4)

2.5 Pin Description

2.5.1 Static Memory/DVP/I2Cx/UARTx/DMIC

Table 2-1 Static Memory/DVP/I2Cx/UARTx/DMIC Pins(23)

Pin Names	IO	Loc	IO Char.	Pin Description	Power
SD0	IO	M3	6mA	SD0: Static memory data bus bit 0	VDDIO3318_DVP
DVP_BT_D0	I			DVP_BT_D0: DVP or BT data bit 0	
UART3_CTS	I		Hi-Z-rst	UART3_CTS: UART 3 clear-to-send	
PA00	IO			PA00: GPIO group A bit 00	
SD1	IO	M2	6mA	SD1: Static memory data bus bit 1	VDDIO3318_DVP
DVP_BT_D1	I			DVP_BT_D1: DVP or BT data bit 1	
UART3_RTS	O		Hi-Z-rst	UART3_RTS: UART 3 request-to-send	
PA01	IO			PA01: GPIO group A bit 01	
SD2	IO	L3	6mA	SD2: Static memory data bus bit 2	VDDIO3318_DVP
DVP_BT_D2	I			DVP_BT_D2: DVP or BT data bit 2	
UART3_TXD	O		Hi-Z-rst	UART3_TXD: UART 3 transmit data	
PA02	IO			PA02: GPIO group A bit 02	
SD3	IO	L2	6mA	SD3: Static memory data bus bit 3	VDDIO3318_DVP
DVP_BT_D3	I			DVP_BT_D3: DVP or BT data bit 3	
UART3_RXD	I		Hi-Z-rst	UART3_RXD: UART 3 receive data	
PA03	IO			PA03: GPIO group A bit 03	
SD4	IO	L1	6mA	SD4: Static memory data bus bit 4	VDDIO3318_DVP
DVP_BT_D4	I			DVP_BT_D4: DVP or BT data bit 4	
UART2_CTS	I		Hi-Z-rst	UART2_CTS: UART 2 clear-to-send	
PA04	IO			PA04: GPIO group A bit 04	

Pin Names	IO	Loc	IO Char.	Pin Description	Power
SD5	IO	K2	6mA	SD5: Static memory data bus bit 5	VDDIO3318_DVP
DVP_BT_D5	I			DVP_BT_D5: DVP or BT data bit 5	
UART2_RTS	O		Hi-Z-rst	UART2_RTS: UART 2 request-to-send	
PA05	IO			PA05: GPIO group A bit 05	
SD6	IO	K3	6mA	SD6: Static memory data bus bit 6	VDDIO3318_DVP
DVP_BT_D6	I			DVP_BT_D6: DVP or BT data bit 6	
UART2_TXD	O		Hi-Z-rst	UART2_TXD: UART 2 transmit data	
PA06	IO			PA06: GPIO group A bit 06	
SD7	IO	J1	6mA	SD7: Static memory data bus bit 7	VDDIO3318_DVP
DVP_BT_D7	I			DVP_BT_D7: DVP or BT data bit 7	
UART2_RXD	I		Hi-Z-rst	UART2_RXD: UART 2 receive data	
PA07	IO			PA07: GPIO group A bit 07	
SA0	O	J2	6mA	SA0: Static memory address bus bit 0	VDDIO3318_DVP
DVP_BT_D8	I			DVP_BT_D8: DVP or BT data bit 8	
UART0_CTS	I		Hi-Z-rst	UART0_CTS: UART 0 clear-to-send	
PA08	IO			PA08: GPIO group A bit 08	
SA1	O	J3	6mA	SA1: Static memory address bus bit 1	VDDIO3318_DVP
DVP_BT_D9	I			DVP_BT_D9: DVP or BT data bit 9	
UART0_RTS	O		Hi-Z-rst	UART0_RTS: UART 0 request-to-send	
PA09	IO			PA09: GPIO group A bit 09	

Pin Names	IO	Loc	IO Char.	Pin Description	Power
SA2 DVP_BT_D10 UART0_TXD PA10	O I O IO	H2	6mA Hi-Z-rst	SA2: Static memory address bus bit 2 DVP_BT_D10: DVP or BT data bit 10 UART0_TXD: UART 0 transmit data PA10: GPIO group A bit 10	VDDIO3318_DVP
CS1_ DVP_BT_D11 UART0_RXD PA11	O I I IO	H3	6mA Hi-Z-rst	CS1_: Static memory chip 1 select DVP_BT_D11: DVP or BT data bit 11 UART0_RXD: UART 0 receive data PA11: GPIO group A bit 11	VDDIO3318_DVP
CS2_ SMB0_SDA DMIC_CLK PA12	O IO O IO	N2	6mA Hi-Z-rst	CS2_: Static memory chip 2 select SMB0_SDA: I2C 0 serial data DMIC_CLK: Digital microphone Clock output PA12: GPIO group A bit 12	VDDIO3318_DVP
RD_ SMB0_SCK DMIC_DAT0 PA13	O O I IO	N1	6mA Hi-Z-rst	RD_: Static memory read signal SMB0_SCK: I2C 0 serial clock DMIC_DAT0: Digital microphone data bit 0 PA13: GPIO group A bit 13	VDDIO3318_DVP
DVP_BT_PCLK DMIC_DAT1 PA14	O I IO	G1	6mA Hi-Z-rst	DVP_BT_PCLK: camera sensor pixel clock input for DVP or BT model DMIC_DAT1: Digital microphone data bit 1 PA14: GPIO group A bit 14	VDDIO3318_DVP
DVP_HSYNC_BT_D12 PA15	I IO	G3	6mA Hi-Z-rst	DVP_HSYNC_BT_D12: DVP horizontal sync or BT data bit 12 PA15: GPIO group A bit 15	VDDIO3318_DVP

Pin Names	IO	Loc	IO Char.	Pin Description	Power
DVP_VSYNC_ BT_D13 PA16	I IO	G2	6mA Hi-Z-rst	DVP_VSYNC_BT_D13: DVP vertical sync or BT data bit 13 PA16: GPIO group A bit 16	VDDIO3318_DVP
SMB1_SDA UART1_TXD PA17	IO O IO	AA7	6mA Hi-Z-rst	SMB1_SDA: I2C 1 serial data UART1_TXD: UART 1 transmit data PA17: GPIO group A bit 17	VDDIO3318_DVP
SMB1_SCK UART1_RXD PA18	O I IO	W8	6mA Hi-Z-rst	SMB1_SCK: I2C 1 serial clock UART1_RXD: UART 1 receive data PA18: GPIO group A bit 18	VDDIO3318_DVP
D_EFSYNC0 PA19	O IO	Y8	6mA Hi-Z-rst	D_EFSYNC0: ISP for sensor control bit 0 PA19: GPIO group A bit 19	VDDIO3318_DVP
D_EFSYNC1 PA20	O IO	W9	6mA Hi-Z-rst	D_EFSYNC1: ISP for sensor control bit 1 PA20: GPIO group A bit 20	VDDIO3318_DVP
BT_D14 SMB3_SDA PA21	I IO IO	Y9	6mA Hi-Z-rst	BT_D14: BT data bit 14 SMB3_SDA: I2C 3 serial data PA21: GPIO group A bit 21	VDDIO3318_DVP
WAIT_ BT_D15 SMB3_SCK PA22	I I O IO	AA9	6mA Hi-Z-rst	WAIT_: Static memory/device wait signal BT_D15: BT data bit 15 SMB3_SCK: I2C 3 serial clock PA22: GPIO group A bit 22	VDDIO318_DVP

2.5.2 SFC

Table 2-2 SFC Pins(6)

Pin Names	IO	Loc	IO Char.	Pin Description	Power
SFC_D0_DT	IO	Y11	9mA	SFC_D0_DT: Serial Flash data	VDDIO33
PA23	IO		Hi-Z-rst	PA23: GPIO group A bit 23	
SFC_D1_DR	IO	Y10	9mA	SFC_D1_DR: Serial Flash data	VDDIO33
PA24	IO		Hi-Z-rst	PA24: GPIO group A bit 24	
SFC_D2_WP	IO	W11	9mA	SFC_D2_WP: Serial Flash write protect signal	VDDIO33
PA25	IO		Hi-Z-rst	PA25: GPIO group A bit 25	
SFC_D3_HOLD	IO	V11	9mA	SFC_D3_HOLD: Serial Flash hold signal	VDDIO33
PA26	IO		Pullup-rst	PA26: GPIO group A bit 26	
SFC_CLK	O	AA11	9mA	SFC_CLK: Serial Flash clock output	VDDIO33
PA27	IO		Hi-Z-rst	PA27: GPIO group A bit 27	
SFC_CE0	O	W10	9mA	SFC_CE0: Serial Flash chip enable	VDDIO33
PA28	IO		Pullup-rst	PA28: GPIO group A bit 28	

2.5.3 MSCx/GMAC/PWMx/UARTx/I2Cx/SSI1/I2S

Table 2-3 MSCx/GMAC/PWMx/UARTx/I2Cx/SSI1/I2S Pins (31)

Pin Names	IO	Loc	IO Char.	Pin Description	Power
MSC0_D0	IO	W12	6mA	MSC0_D0: MSC (MMC/SD) 0 data bit 0	VDDIO33
PB00	IO		Hi-Z-rst	PB00: GPIO group B bit 00	
MSC0_D1	IO	Y12	6mA	MSC0_D1: MSC (MMC/SD) 0 data bit 1	VDDIO33
PB01	IO		Hi-Z-rst	PB01: GPIO group B bit 01	
MSC0_D2	IO	Y14	6mA	MSC0_D2: MSC (MMC/SD) 0 data bit 2	VDDIO33
PB02	IO		Hi-Z-rst	PB02: GPIO group B bit 02	

Pin Names	IO	Loc	IO Char.	Pin Description	Power
MSC0_D3 PB03	IO IO	W13	6mA Hi-Z-rst	MSC0_D3: MSC (MMC/SD) 0 data bit 3 PB03: GPIO group B bit 03	VDDIO33
MSC0_CLK PB04	O IO	AA13	6mA Hi-Z-rst	MSC0_CLK: MSC (MMC/SD) 0 clock output PB04: GPIO group B bit 04	VDDIO33
MSC0_CMD PB05	IO IO	Y13	6mA Hi-Z-rst	MSC0_CMD: MSC (MMC/SD) 0 command PB05: GPIO group B bit 05	VDDIO33
GMAC_TXCLK PWM6 PB06	I O IO	AA19	6mA Pulldown-rst	GMAC_TXCLK: gmac transmitting clock PWM6: PWM channel 6 output PB06: GPIO group B bit 06	VDDIO33
GMAC_PHY_CLK PWM7 PB07	O O IO	Y19	6mA Pulldown-rst	GMAC_PHY_CLK: gmac phy clock PWM7: PWM channel 7 output PB07: GPIO group B bit 07	VDDIO33
GMAC_TXEN I2S_DAC_MCLK PB08	O O IO	AA21	6mA Hi-Z-rst	GMAC_TXEN: gmac transmitting enable I2S_DAC_MCLK: I2S DAC clock PB08: GPIO group B bit 08	VDDIO33
GMAC_RXDV I2S_ADC_MCLK PB09	I O IO	W17	6mA Hi-Z-rst	GMAC_RXDV: gmac receive data valid I2S_ADC_MCLK: I2S ADC clock PB09: GPIO group B bit 09	VDDIO33
GAMC_MDCK I2S_DAC_BCLK PB10	O IO IO	Y17	6mA Hi-Z-rst	GAMC_MDCK: gmac manage data clock I2S_DAC_BCLK: I2S DAC bit clock PB10: GPIO group B bit 10	VDDIO33

Pin Names	IO	Loc	IO Char.	Pin Description	Power
GMAC_MDIO I2S_DAC_LRCK PB11	IO O IO	AA17	6mA Hi-Z-rst	GMAC_MDIO: gmac MDIO which is clocked by MDC I2S_DAC_LRCK: I2S DAC left/right clock PB11: GPIO group B bit 11	VDDIO33
GMAC_TXD0 I2S_ADC_BCLK PB13	O IO IO	AA20	6mA Hi-Z-rst	GMAC_TXD0: gmac transmit data bit 0 I2S_ADC_BCLK: I2S ADC bit clock PB13: GPIO group B bit 13	VDDIO33
GMAC_TXD1 I2S_ADC_LRCK PB14	O O IO	W19	6mA Hi-Z-rst	GMAC_TXD1: gmac transmit data bit 1 I2S_ADC_LRCK: I2S ADC left/right clock PB14: GPIO group B bit 14	VDDIO33
GMAC_RXD0 I2S_SDTI PB15	I I IO	Y18	6mA Hi-Z-rst	GMAC_RXD0: gmac receive data bit 0 I2S_SDTI: I2S serial data input signal PB15: GPIO group B bit 15	VDDIO33
GMAC_RXD1 I2S_SDTO PB16	I O IO	W18	6mA Hi-Z-rst	GMAC_RXD1: gmac receive data bit 1 I2S_SDTO: I2S serial data output signal PB16: GPIO group B bit 16	VDDIO33
MSC1_CLK SMB1_SDA PB17	O IO IO	Y15	6mA Hi-Z-rst	MSC1_CLK: MSC (MMC/SD) 1 clock output SMB1_SDA: I2C 1 serial data PB17: GPIO group B bit 17	VDDIO33
MSC1_CMD SMB1_SCK PB18	IO O IO	W15	6mA Hi-Z-rst	MSC1_CMD: MSC (MMC/SD) 1 command SMB1_SCK: I2C 1 serial clock PB18: GPIO group B bit 18	VDDIO33

Pin Names	IO	Loc	IO Char.	Pin Description	Power
MSC1_D0 PB19	IO IO	AA15	6mA Hi-Z-rst	MSC1_D0: MSC (MMC/SD) 1 data bit 0 PB19: GPIO group B bit 19	VDDIO33
MSC1_D1 SMB3_SDA PB20	IO IO IO	W14	6mA Hi-Z-rst	MSC1_D1: MSC (MMC/SD) 1 data bit 1 SMB3_SDA: I2C 3 serial data PB20: GPIO group B bit 20	VDDIO33
MSC1_D2 SMB3_SCK PB21	IO O IO	W16	6mA Hi-Z-rst	MSC1_D2: MSC (MMC/SD) 1 data bit 2 SMB3_SCK: I2C 3 serial clock PB21: GPIO group B bit 21	VDDIO33
MSC1_D3 PB22	IO IO	Y16	6mA Hi-Z-rst	MSC1_D3: MSC (MMC/SD) 1 data bit 3 PB22: GPIO group B bit 22	VDDIO33
UART1_TXD PB23	O IO	C18	6mA Pullup-rst	UART1_TXD: UART 1 transmit data PB23: GPIO group B bit 23	VDDIO33
UART1_RXD PB24	I IO	B18	6mA Pullup-rst	UART1_RXD: UART 1 receive data PB24: GPIO group B bit 24	VDDIO33
SMB2_SDA PWM4 SSI1_DT PB25	IO O O IO	B21	6mA Hi-Z-rst SMT-rst	SMB2_SDA: I2C 2 serial data PWM4: PWM channel 4 output SSI1_DT: SSI 1 transmit data PB25: GPIO group B bit 25	VDDIO33
SMB2_SCK PWM5 SSI1_CLK PB26	O O O IO	B20	6mA Hi-Z-rst SMT-rst	SMB2_SCK: I2C 2 serial clock PWM5: PWM channel 5 output SSI1_CLK: SSI 1 clock PB26: GPIO group B bit 26	VDDIO33

Pin Names	IO	Loc	IO Char.	Pin Description	Power
DRV_VBUS	O	A21	6mA	DRV_VBUS: USB-5V control	VDDIO33
UART2_CTS	I			UART2_CTS: UART 2 clear-to-send	
SSI1_DR	I		Hi-Z-rst	SSI1_DR: SSI 1 receive data	
PB27	IO			PB27: GPIO group B bit 27	
SMB3_SDA	IO	A20	6mA	SMB3_SDA: I2C 3 serial data	VDDIO33
UART2_TXD	O			UART2_TXD: UART 2 transmit data	
SSI1_GPC	O		Hi-Z-rst	SSI1_GPC: SSI 1 general-purpose control	
PB28	IO			PB28: GPIO group B bit 28	
SMB3_SCK	O	C19	6mA	SMB3_SCK: I2C 3 serial clock	VDDIO33
UART2_RXD	I			UART2_RXD: UART 2 receive data	
SSI1_CE1	O		Hi-Z-rst	SSI1_CE1: SSI 1 chip 1 select	
PB29	IO			PB29: GPIO group B bit 29	
PWM2	O	B19	6mA	PWM2: PWM channel 2 output	VDDIO33
UART2_RTS	O			UART2_RTS: UART 2 request-to-send	
SSI1_CE0	O		Pullup-rst	SSI1_CE0: SSI 1 chip 0 select	
PB30	IO			PB30: GPIO group B bit 30	
PWM3	O	A19	6mA	PWM3: PWM channel 3 output	VDDIO33
PB31	IO		Pulldown-rst	PB31: GPIO group B bit 31	

2.5.4 UARTx/PWMx/SSI0

Table 2-4 UARTx/ PWMx/SSI0(6)

Pin Names	IO	Loc	IO Char.	Pin Description	Power
UART0_RXD	I	A17	6mA Hi-Z-rst	UART0_RXD: UART 0 receive data	VDDIO33
SSI0_DT	O			SSI0_DT: SSI 0 transmit data	
PWM0	O			PWM0: PWM channel 0 output	
PC02	IO			PC02: GPIO group C bit 02	
UART0_CTS	I	B17	6mA Hi-Z-rst	UART0_CTS: UART 0 clear-to-send	VDDIO33
SSI0_DR	I			SSI0_DR: SSI 0 receive data	
PWM1	O			PWM1: PWM channel 1 output	
PC03	IO			PC03: GPIO group C bit 03	
UART0_RTS	O	C17	6mA Hi-Z-rst	UART0_RTS: UART 0 Request-to-Send	VDDIO33
SSI0_CLK	O			SSI0_CLK: SSI 0 clock	
PWM2	O			PWM2: PWM channel 2 output	
PC04	IO			PC04: GPIO group C bit 04	
UART0_TXD	O	C16	6mA Hi-Z-rst	UART0_TXD: UART 0 transmit data	VDDIO33
SSI0_CE0	O			SSI0_CE0: SSI 0 chip 0 select	
PWM3	O			PWM3: PWM channel 3 output	
PC05	IO			PC05: GPIO group C bit 05	
UART3_TXD	O	B16	6mA Hi-Z-rst	UART3_TXD: UART 3 transmit data	VDDIO33
SSI0_CE1	O			SSI0_CE1: SSI 0 chip 1 select	
PWM4	O			PWM4: PWM channel 4 output	
PC06	IO			PC06: GPIO group C bit 06	

Pin Names	IO	Loc	IO Char.	Pin Description	Power
UART3_RXD	I	C15	6mA	UART3_RXD: UART 3 receive data	VDDIO33
SSI0_GPC	O			SSI0_GPC: SSI 0 general-purpose control	
PWM5	O		Hi-Z-rst	PWM5: PWM channel 5 output	
PC07	IO			PC07: GPIO group C bit 07	

2.5.5 UARTx/CIMx/PWMx/I2Cx/MSC1/DMIC/SSI1/SSI_SLV/I2S

Table 2-5 UARTx/CIMx/PWMx/I2Cx/MSC1/DMIC/SSI1/SSI_SLV/I2S(24)

Pin Names	IO	Loc	IO Char.	Pin Description	Power
MSC1_CLK	O	C5	10mA	MSC1_CLK: MSC (MMC/SD) 1 clock output	VDDIO
SSI1_CLK	O			SSI1_CLK: SSI 1 clock	
PC08	IO		Hi-Z-rst	PC08: GPIO group C bit 08	
MSC1_CMD	IO	B4	10mA	MSC1_CMD: MSC (MMC/SD) 1 command	VDDIO
SSI1_CE0	O			SSI1_CE0: SSI 1 chip 0 select	
PC09	IO		Hi-Z-rst	PC09: GPIO group C bit 09	
MSC1_D0	IO	B5	10mA	MSC1_D0: MSC (MMC/SD) 1 data bit 0	VDDIO
SSI1_DT	O			SSI1_DT: SSI 1 transmit data	
PC10	IO		Hi-Z-rst	PC10: GPIO group C bit 10	
MSC1_D1	IO	A5	10mA	MSC1_D1: MSC (MMC/SD) 1 data bit 1	VDDIO
SSI1_DR	I			SSI1_DR: SSI 1 receive data	
PC11	IO		Hi-Z-rst	PC11: GPIO group C bit 11	
MSC1_D2	IO	A3	10mA	MSC1_D2: MSC (MMC/SD) 1 data bit 2	VDDIO
SSI1_GPC	O			SSI1_GPC: SSI 1 general-purpose control	
PC12	IO		Hi-Z-rst	PC12: GPIO group C bit 12	

Pin Names	IO	Loc	IO Char.	Pin Description	Power
MSC1_D3 SSI1_CE1 PC13	IO O IO	C4	10mA Hi-Z-rst	MSC1_D3: MSC (MMC/SD) 1 data bit 3 SSI1_CE1: SSI 1 chip 1 select PC13: GPIO group C bit 13	VDDIO
UART0_TXD SMB2_SDA PC14	O IO IO	A9	10mA Hi-Z-rst	UART0_TXD: UART 0 transmit data SMB2_SDA: I2C 2 serial data PC14: GPIO group C bit 14	VDDIO
UART0_RXD SMB2_SCK PC15	I O IO	C10	10mA Hi-Z-rst	UART0_RXD: UART 0 receive data SMB2_SCK: I2C 2 serial clock PC15: GPIO group C bit 15	VDDIO
UART0_CTS I2S_DAC_MCLK SMB0_SDA PC16	I O IO IO	B9	10mA Hi-Z-rst	UART0_CTS: UART 0 Clear-to-Send I2S_DAC_MCLK: I2S DAC clock output SMB0_SDA: I2C 0 serial data PC16: GPIO group C bit 16	VDDIO
UART0_RTS I2S_ADC_MCLK SMB0_SCK PC17	O O O IO	C9	10mA Hi-Z-rst	UART0_RTS: UART 0 Request-to-Send I2S_ADC_MCLK:I2S ADC clock output SMB0_SCK: I2C 0 serial clock PC17: GPIO group C bit 17	VDDIO
UART2_TXD I2S_DAC_LRCK PC18	O IO IO	A7	10mA Hi-Z-rst	UART2_TXD: UART 2 transmit data I2S_DAC_LRCK: I2S DAC left/right clock PC18: GPIO group C bit 18	VDDIO
UART2_RXD I2S_DAC_BCLK PC19	I IO IO	C8	10mA Hi-Z-rst	UART2_RXD: UART 2 receive data I2S_DAC_BCLK: I2S DAC bit clock PC19: GPIO group C bit 19	VDDIO

Pin Names	IO	Loc	IO Char.	Pin Description	Power
SSI_SLV_CLK I2S_SDTI PC20	I I IO	C6	10mA Pulldown-rst SMT-rst	SSI_SLV_CLK: SSI slave clock I2S_SDTI: I2S serial data input signal PC20: GPIO group C bit 20	VDDIO
SSI_SLV_CE0 I2S_SDTO PC21	I O IO	B6	10mA Pullup-rst SMT-rst	SSI_SLV_CE0: SSI slave chip 0 select I2S_SDTO: I2S serial data output signal PC21: GPIO group C bit 21	VDDIO
SSI_SLV_DT I2S_ADC_BCLK PC22	O IO IO	C7	10mA Hi-Z-rst	SSI_SLV_DT: SSI slave transmit data I2S_ADC_BCLK: I2S ADC bit clock PC22: GPIO group C bit 22	VDDIO
SSI_SLV_DR I2S_ADC_LRCK PC23	I IO IO	B7	10mA Hi-Z-rst	SSI_SLV_DR: SSI slave receive data I2S_ADC_LRCK: I2S ADC left/right clock PC23: GPIO group C bit 23	VDDIO
DMIC_CLK PC24	O IO	A11	10mA Hi-Z-rst	DMIC_CLK: Digital microphone clock output PC24: GPIO group C bit 24	VDDIO
DMIC_DAT0 PC25	I IO	B11	10mA Hi-Z-rst	DMIC_DAT0: Digital microphone data bit 0 PC25: GPIO group C bit 25	VDDIO
UART2_CTS DMIC_DAT1 PC26	I I IO	B10	10mA Hi-Z-rst	UART2_CTS: UART 2 Clear-to-Send DMIC_DAT1: Digital microphone data bit 1 PC26: GPIO group C bit 26	VDDIO
UART2_RTS PWM0 PC27	O O IO	B8	10mA Hi-Z-rst	UART2_RTS: UART 2 Request-to-Send PWM0: PWM channel 0 output PC27: GPIO group C bit 27	VDDIO

Pin Names	IO	Loc	IO Char.	Pin Description	Power
PWM1 PC28	O IO	B2	10mA Hi-Z-rst	PWM1: PWM channel 1 output PC28: GPIO group C bit 28	VDDIO
CIM2_MCLK PC29	O IO	B3	10mA Hi-Z-rst	CIM2_MCLK: sensor clock 2 output PC29: GPIO group C bit 29	VDDIO
CIM1_MCLK PC30	O IO	A2	10mA Hi-Z-rst	CIM1_MCLK: sensor clock 1 output PC30: GPIO group C bit 30	VDDIO
CIM0_MCLK PC31	O IO	C3	10mA Hi-Z-rst	CIM0_MCLK: sensor clock 0 output PC31: GPIO group C bit 31	VDDIO

2.5.6 DPU/SSI_SLV/PWMx/JTAG/I2C1/UART3

Table 2-6 DPU/SSI_SLV/PWMx/JTAG/I2C1/UART3 Pins(2)

Pin Names	IO	Loc	IO Char.	Pin Description	Power
RGB_D0 BT656_1120_D0 SLCD_D0 PD00	O O O IO	L18	6mA Hi-Z-rst	RGB_D0: LCD data output bit 0 BT656_1120_D0: BT656/1120 data bit 0 SLCD_D0: smart lcd data output bit 0 PD00: GPIO group D bit 00	VDDIO33
RGB_D1 BT656_1120_D1 SLCD_D1 PD01	O O O IO	L20	6mA Hi-Z-rst	RGB_D1: LCD data output bit 1 BT656_1120_D1: BT656/1120 data bit 1 SLCD_D1: smart lcd data output bit 1 PD01: GPIO group D bit 01	VDDIO33

Pin Names	IO	Loc	IO Char.	Pin Description	Power
RGB_D2	O	L21	6mA	RGB_D2: LCD data output bit 2	VDDIO33
BT656_1120_D2	O			BT656_1120_D2: BT656/1120 data bit 2	
SLCD_D2	O		Hi-Z-rst	SLCD_D2: smart lcd data output bit 2	
PD02	IO			PD02: GPIO group D bit 02	
RGB_D3	O	K20	6mA	RGB_D3: LCD data output bit 3	VDDIO33
BT656_1120_D3	O			BT656_1120_D3: BT656/1120 data bit 3	
SLCD_D3	O		Hi-Z-rst	SLCD_D3: smart lcd data output bit 3	
PD03	IO			PD03: GPIO group D bit 03	
RGB_D4	O	K19	6mA	RGB_D4: LCD data output bit 4	VDDIO33
BT656_1120_D4	O			BT656_1120_D4: BT656/1120 data bit 4	
SLCD_D4	O		Hi-Z-rst	SLCD_D4: smart lcd data output bit 4	
PD04	IO			PD04: GPIO group D bit 04	
RGB_D5	O	J21	6mA	RGB_D5: LCD data output bit 5	VDDIO33
BT656_1120_D5	O			BT656_1120_D5: BT656/1120 data bit 5	
SLCD_D5	O		Hi-Z-rst	SLCD_D5: smart lcd data output bit 5	
PD05	IO			PD05: GPIO group D bit 05	
RGB_D6	O	J20	6mA	RGB_D6: LCD data output bit 6	VDDIO33
BT656_1120_D6	O			BT656_1120_D6: BT656/1120 data bit 6	
SLCD_D6	O		Hi-Z-rst	SLCD_D6: smart lcd data output bit 6	
PD06	IO			PD06: GPIO group D bit 06	
RGB_D7	O	J19	6mA	RGB_D7: LCD data output bit 7	VDDIO33
BT656_1120_D7	O			BT656_1120_D7: BT656/1120 data bit 7	
SLCD_D7	O		Hi-Z-rst	SLCD_D7: smart lcd data output bit 7	
PD07	IO			PD07: GPIO group D bit 07	

Pin Names	IO	Loc	IO Char.	Pin Description	Power
RGB_PCLK BT656_1120_PCLK SLCD_WR PD08	O O O IO	C20	6mA Hi-Z-rst	RGB_PCLK: LCD pixel clock BT656_1120_PCLK: BT656/1120 pixel clock SLCD_WR: smart lcd write data control PD08: GPIO group D bit 08	VDDIO33
RGB_D8 BT1120_D8 SLCD_TE PD09	O O I IO	H20	6mA Hi-Z-rst	RGB_D8: LCD data output bit 8 BT1120_D8: BT1120 data bit 8 only SLCD_TE: smart lcd tearing effect PD09: GPIO group D bit 09	VDDIO33
RGB_D9 BT1120_D9 SLCD_CS PD10	O O O IO	H19	6mA Hi-Z-rst	RGB_D9: LCD data output bit 9 BT1120_D9: BT1120 data bit 9 only SLCD_CS: smart lcd chip select PD10: GPIO group D bit 10	VDDIO33
RGB_D10 BT1120_D10 SLCD_DC PD11	O O O IO	G21	6mA Hi-Z-rst	RGB_D10: LCD data output bit 10 BT1120_D10: BT1120 data bit 10 only SLCD_DC: smart lcd cmd/data identify PD11: GPIO group D bit 11	VDDIO33
RGB_D11 BT1120_D11 SLCD_RDY PD12	O O I IO	G20	6mA Hi-Z-rst	RGB_D11: LCD data output bit 11 BT1120_D11: BT1120 data bit 11 only SLCD_RDY: smart lcd work status PD12: GPIO group D bit 12	VDDIO33

Pin Names	IO	Loc	IO Char.	Pin Description	Power
RGB_D12 BT1120_D12 PD13	O O IO	G19	6mA Hi-Z-rst	RGB_D12: LCD data output bit 12 BT1120_D12: BT1120 data bit 12 only PD13: GPIO group D bit 13	VDDIO33
RGB_D13 BT1120_D13 PD14	O O IO	F20	6mA Hi-Z-rst	RGB_D13: LCD data output bit 13 BT1120_D13: BT1120 data bit 13 only PD14: GPIO group D bit 14	VDDIO33
RGB_D14 BT1120_D14 PD15	O O IO	F19	6mA Hi-Z-rst	RGB_D14: LCD data output bit 14 BT1120_D14: BT1120 data bit 14 only PD15: GPIO group D bit 15	VDDIO33
RGB_D15 BT1120_D15 PD16	O O IO	E21	6mA Hi-Z-rst	RGB_D15: LCD data output bit 15 BT1120_D15: BT1120 data bit 15 only PD16: GPIO group D bit 16	VDDIO33
RGB_HSYNC PD17	O IO	C21	6mA Hi-Z-rst	RGB_HSYNC: LCD line sync PD17: GPIO group D bit 17	VDDIO33
RGB_D16 SSI_SLV_CLK PD18	O I IO	E20	6mA Hi-Z-rst	RGB_D16: LCD data output bit 16 SSI_SLV_CLK: SSI slave clock PD18: GPIO group D bit 18	VDDIO33
RGB_D17 SSI_SLV_CE0 PD19	O I IO	E19	6mA Hi-Z-rst	RGB_D17: LCD data output bit 17 SSI_SLV_CE0: SSI slave chip 0 select PD19: GPIO group D bit 19	VDDIO33
RGB_VSYNC SSI_SLV_DT PD20	O O IO	D19	6mA Hi-Z-rst	RGB_VSYNC: LCD frame sync SSI_SLV_DT: SSI slave transmit data PD20: GPIO group D bit 20	VDDIO33

Pin Names	IO	Loc	IO Char.	Pin Description	Power
RGB_DE SSI_SLV_DR PD21	O I IO	D20	6mA Hi-Z-rst	RGB_DE: LCD data enable SSI_SLV_DR: SSI slave receive data PD21: GPIO group D bit 21	VDDIO33
UART3_CTS TDI PWM6 PD22	I I O IO	B15	6mA Hi-Z-rst	UART3_CTS: UART 3 clear-to-send TDI: JTAG data input PWM6: PWM channel 6 output PD22: GPIO group D bit 22	VDDIO33
UART3_RTS TDO PWM7 PD23	O O O IO	A15	6mA Hi-Z-rst	UART3_RTS: UART 3 request-to-send TDO: JTAG data output PWM7: PWM channel 7 output PD23: GPIO group D bit 23	VDDIO33
UART3_TXD TCK PD24	O I IO	B14	6mA Hi-Z-rst	UART3_TXD: UART 3 transmit data TCK: JTAG clock input PD24: GPIO group D bit 24	VDDIO33
UART3_RXD TMS PD25	I I IO	C14	6mA Hi-Z-rst	UART3_RXD: UART 3 receive data TMS: JTAG mode select PD25: GPIO group D bit 25	VDDIO33
SMB1_SDA PWM0 PD26	IO O IO	B12	6mA Hi-Z-rst	SMB1_SDA: I2C 1 serial data PWM0: PWM channel 0 output PD26: GPIO group D bit 26	VDDIO33
SMB1_SCK PWM1 PD27	O O IO	C12	6mA Hi-Z-rst	SMB1_SCK: I2C 1 serial clock PWM1: PWM channel 1 output PD27: GPIO group D bit 27	VDDIO33

2.5.7 System Boot Select

Table 2-7 Boot Select Pins(2)

Pin Names	IO	Loc	IO Char.	Pin Description	Power
(BOOT_SEL0) PC00	I IO	B13	6mA Pullup-rst	It is taken as BOOT select bit 0 by Boot ROM code PC00: GPIO group C bit 00	VDDIO33
(BOOT_SEL1) PC01	I IO	C13	6mA Pulldown-rst	It is taken as BOOT select bit 1 by Boot ROM code PC01: GPIO group C bit 01	VDDIO33

2.5.8 System Control

Table 2-8 System Control Pins(5)

Pin Names	IO	Loc	IO Char.	Pin Description	Power
TRST_	I	A13	6mA Pulldown	TRST_: JTAG reset	VDDIO33
PPRST_	I	B1	10mA Pullup	PPRST_: Power on reset and RESET-KEY reset input	VDDIO
TEST_TE	I	D3	10mA Pulldown	TEST_TE: Manufacture test enable, program enable	VDDIO
POR_CTL	I	C1	10mA Pullup	POR_CTL: Power-on-Reset model bypass control	VDDIO
RST_OUT_	I	C2	10mA Pulldown	RST_OUT_: System Reset output	VDDIO

2.5.9 Digital IO/CORE Power/Ground

Table 2-9 Digital IO/CORE Power Supplies Pins (7)

Pin Names	IO	Loc	Pin Description	Power
VDD	P	J5,J6,J7,J8,J9,J10,J11,J12,J13,J14,J15,J16,J17,K5,K6,K7,K8,K9,K10,K11,K12,K13,K14,K15,K16,K17,L5,L6,L16,L17,M5,M6,M16,M17,N5,N6,N16,N17,P5,P6,P16,P17,R5,R6,R16,T9,T10,T11,T12,T13,T14,T15,T16,U9,U10,U11,U12,U13,U14,U15	VDD: CORE digital power, 0.9V	-
VSS	P	E6,E7,E8,E9,E10,E11,E12,E13,E14,E15,E16,H5,H6,H7,H8,H9,H10,H11,H12,H13,H14,H15,H16,H17,L7,L8,L9,L10,L11,L12,L13,L14,L15,M7,M8,M9,M10,M11,M12,M13,M14,M15,N7,N8,N9,N10,N11,N12,N13,N14,N15,P7,P8,P9,P10,P11,P12,P13,P14,P15,R7,R8,R9,R10,R11,R12,R13,R14,R15,T5,T6,T7,T8,U5,U6,U7,U8	VSS: IO analog ground and CORE digital ground	-
VDDIO	P	D2	VDDIO*: 1.8V, for Fail-Safe type IO power supply	-
VDDIO18_DVP	P	N3	VDDIO18_DVP*: For DVP function type IO power supply, 1.8V	-
VDDIO3318_DVP	P	L4	VDDIO3318_DVP*: For DVP function type IO power supply, 3.3V or 1.8V	-
VDDIO18	P	R17,T17	VDDIO18*: For 1.8V type IO power supply	-
VDDIO33	P	U16,U17	VDDIO33: For 3.3V type IO power supply	-

NOTES:

1. VDDIO18_DVP/VDDIO3318_DVP: Power domain 0(VDDIO0)

a) If DVP function pad need support 1.8V voltage input, VDDIO18_DVP and VDDIO3318_DVP supply 1.8V.

b) If DVP function pad need support 3.3V voltage input, VDDIO18_DVP supply 1.8V and VDDIO3318_DVP supply 3.3V

2. VDDIO18/VDDIO33: Power domain 1(VDDIO1), VDDIO18 must supply 1.8V voltage, no matter what voltage for this power domain.

3. VDDIO: Power domain 2(VDDIO2), just support 1.8V voltage, support Fail-Safe feature

2.5.10 DDR PHY and KGD IO/Power Supply

Table 2-10 DDR PHY and KGD IO/Power Supply Pins (6)

Pin Names	IO	Loc	Pin Description	Power
NC	AIO	F17	floating	-
VREF	P	E17	VREF: For SDRAM, reference voltage	-
DDRPLL_VCCA	P	C11	DDRPLL_VCCA: 1.8V, DDR PHY PLL power supply for analog	-
DDRPLL_AVSS	P	D11	DDRPLL_AVSS: DDR PHY PLL ground for analog	-
DDRVDD	P	F5,F6,F7,F8,F9,F10,F11,F12,F13,F14,F15,F16	DDRVDD: DDR KGD power supply (1.8V for DDR2)	-
VDDMEM	P	G5,G6,G7,G8,G9,G10,G11,G12,G13,G14,G15,G16,G17	VDDMEM: DDR PHY IO power supply(1.8V for DDR2)	-

2.5.11 USB 2.0 PHY IO/Power Supply

Table 2-11 USB 2.0 PHY IO/Power Supply Pins(8)

Pin Names	IO	Loc	Pin Description	Power
USB0PP	AIO	W5	USB0PP/ USB0PN: The differential input/output signals of the	USB_AVD

Pin Names	IO	Loc	Pin Description	Power
USB0PN	AIO	Y4	PHY that support multiple modes. Depending on mode of operation, they are either signaling 3.3 or 800mV differential.	33
USB0ID	AI	Y6	USB0ID: Used to identify the device attached to the PHY. The state of the pin is one of: high impedance(>1MΩ) or low impedance(<10Ω to ground)	USB_AVD 18
VBUS	AIO	AA5	VBUS: The VBUS power supply can be used for a combination of function.	USB_AVD 33
USB_AVD09	P	Y7	USB_AVD09: This is the analog supply that is used to support 0.9V circuits within the PHY.	-
USB_AVD18	P	W7	USB_AVD18: This is the analog supply that is used to support 1.8V signaling.	-
USB_AVD33	P	Y5	USB_AVD33: This is the analog supply that is used to support 3.3V signaling.	-
USB_VSSA	P	W6	USB_VSSA: This is the analog ground.	-

2.5.12 MIPI Rx and Tx IO/Power Supply

Table 2-12 MIPI Rx and Tx IO/Power Supply Pins(28)

Pin Names	IO	Loc	Pin Description	Power
RX_DATAP0	AIO	P3	RX_DATAN0/ RX_DATAP0: MIPI RX D-PHY data lane 0 serial pad	CSI_VCC18
RX_DATAN0		P2		
RX_DATAP1	AIO	R3	RX_DATAN1/RX_DATAP1: MIPI RX D-PHY data lane 1 serial pad	CSI_VCC18
RX_DATAN1		R2		
RX_DATAP2	AIO	V3	RX_DATAN2/RX_DATAP2: MIPI RX D-PHY data lane 2 serial pad	CSI_VCC18
RX_DATAN2		V2		

Pin Names	IO	Loc	Pin Description	Power
RX_DATAP3	AIO	W2	RX_DATAN3/RX_DATAP3: MIPI RX D-PHY data lane 3 serial pad	CSI_VCC18
RX_DATAN3		W1		
RX_CLKP	AIO	T3	RX_CLKN/RX_CLKP: MIPI RX D-PHY clock lane serial pad	CSI_VCC18
RX_CLKN		T2		
RX_CLKP1	AIO	U3	RX_CLKN1/ RX_CLKP1: MIPI RX D-PHY clock lane 1 serial pad	CSI_VCC18
RX_CLKN1		U2		
CSI_VCC18	P	R1	CSI_VCC18: power analog supply for IO	-
CSI_VCC09	P	Y1	CSI_VCC09: power analog supply for core	-
CSI_VSSA	P	U1	CSI_VSSA: power analog ground	-
TX_DATAP0	AIO	Y21	TX_DATAN0/TX_DATAP0: MIPI TX D-PHY data lane 0 serial pad	DSI_VCCA18
TX_DATAN0		Y20		
TX_DATAP1	AIO	W21	TX_DATAN1/TX_DATAP1: MIPI TX D-PHY data lane 1 serial pad	DSI_VCCA18
TX_DATAN1		W20		
TX_DATAP2	AIO	U21	TX_DATAN2/TX_DATAP2: MIPI TX D-PHY data lane 2 serial pad	DSI_VCCA18
TX_DATAN2		U20		
TX_DATAP3	AIO	T20	TX_DATAN3/TX_DATAP3: MIPI TX D-PHY data lane 3 serial pad	DSI_VCCA18
TX_DATAN3		T19		
TX_CLKP	AIO	U19	TX_CLKN/TX_CLKP: MIPI TX D-PHY clock lane serial pad	DSI_VCCA18
TX_CLKN		U20		
DSI_VCCA18	P	V19	DSI_VCCA18: power analog supply for IO	-
DSI_VCCA09	P	R19	DSI_VCCA09: power analog supply for core	-

Pin Names	IO	Loc	Pin Description	Power
DSI_VSSA	P	R20	DSI_VSSA: power analog ground	-

2.5.13 Successive Approximation ADC(SAR_ADC) IO/Power Supply

Table 2-13 Successive Approximation ADC(SAR_ADC) IO/Power Supply Pins (7)

Pin Names	IO	Loc	Pin Description	Power
SADC_AUX0	AIO	W3	SADC_AUX0: channel 0 input	SADC_AVDD
SADC_AUX1	AIO	AA1	SADC_AUX1: channel 1 input	SADC_AVDD
SADC_AUX2	AIO	Y2	SADC_AUX2: channel 2 input	SADC_AVDD
SADC_AUX3	AIO	AA2	SADC_AUX3: channel 3 input	SADC_AVDD
SADC_VREFP	P	AA3	SADC_VREFP: Positive reference Voltage input	-
SADC_AVDD	P	Y3	SADC_AVDD: analog power, 1.8 V	-
SADC_AGND	P	W4	SADC_AGND: analog power, ground	-

2.5.14 Audio CODEC IO and Power Supply

Table 2-14 Audio CODEC IO and Power Supply Pins (9)

Pin Names	IO	Loc	Pin Description	Power
MICNR	AIO	N19	MICNR: differential microphone input	CODEC_AVDD
MICPR	AIO	N20	MICPR: differential microphone input	CODEC_AVDD
MICNL	AIO	P19	MICNL: differential microphone input	CODEC_AVDD
MICPL	AIO	P20	MICPL: differential microphone input	CODEC_AVDD
HPOUTL	AIO	M20	HPOUTL: headphone output	CODEC_AVDD
VCM	AIO	N21	VCM: Reference voltage output	CODEC_AVDD

Pin Names	IO	Loc	Pin Description	Power
MICBIAS	AIO	R21	MICBIAS: Microphone bias output	CODEC_AVDD
CODEC_AVDD	P	M19	CODEC_AVDD:1.8V analog supply	-
CODEC_AVSS	P	L19	CODEC_AVDD: ground analog supply	-

2.5.15 OTP Power Supply

Table 2-15 OTP Power Supply Pins (1)

Pin Names	IO	Loc	Pin Description	Power
EFUSE_AVDD	P	A1	EFUSE_AVDD: EFUSE programming power, 1.8V	-

2.5.16 OSC and PLL IO/Power Supply

Table 2-16 OSC and PLL IO/Power Supply Pins (5)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
EXCLK_XI	AI	F2	2~30 MHz Oscillator, OSC on/off	EXCLK_XI: external oscillator clock input or external 24MHz clock input	PLL_AVDD
EXCLK_XO	AO	F3		EXCLK_XO: external oscillator clock output	PLL_AVDD
PLL_VDD	P	E1	-	PLL_VDD: PLL analog power, 0.9V	-
PLL_AVDD	P	E2	-	PLL_AVDD: PLL analog power, 1.8V	-
PLL_AVSS	P	E3	-	PLL_AVSS: PLL analog power, ground	-

NOTES:

1 The meaning of phases in IO cell characteristics are:

- 6/10mA out: The IO cell's output driving strength is about 8/16mA.
- Pullup: The IO cell contains a pull-up resistor and fixed pull up.
- Pulldown: The IO cell contains a pull-down resistor and fixed pull down.

- Pullup-rst: The IO cell during reset and after the pull up function is enabled.
- Pulldown-rst: The IO cell during reset and after the pull down function is enabled.
- Hi-Z-rst: The IO cell during reset and after the pull up and down function is disabled.
- SMT: The IO cell is Schmitt trigger input and fixed.
- SMT-rst: The IO cell during reset and after the Schmitt trigger input function is enabled.
- SR-rst: The IO cell during reset and after the slew-rate function select fast mode.

3 Electrical Specifications

3.1 Absolute Maximum Ratings

The absolute maximum ratings for the processors are listed in Table 3-1. Do not exceed these parameters or the part may be damaged permanently. Operation at absolute maximum ratings is not guaranteed.

Table 3-1 Absolute Maximum Ratings

Parameter	Min	Max	Unit
Storage Temperature	-65	150	°C
Operation Temperature	-40	125	°C
VDDMEM power supplies voltage	-0.1	1.98	V
DDRVDD power supplies voltage	-0.1	1.98	V
DDRPLL_VCCA power supplies voltage	-0.1	1.98	V
VDDIO power supplies voltage	-0.5	1.98	V
VDDIO18 power supplies voltage	-0.5	1.98	V
VDDIO33 power supplies voltage	-0.5	3.63	V
VDDIO18_DVP power supplies voltage	-0.5	1.98	V
VDDIO33_DVP power supplies voltage	-0.5	3.63	V
VDD power supplies voltage	-0.1	0.99	V
PLL_VDD power supplies voltage	-0.1	0.99	V
PLL_AVDD power supplies voltage	-0.1	1.98	V
EFUSE_AVDD power supplies voltage	-0.1	1.98	V
SADC_AVDD power supplies voltage	-0.1	1.98	V
CSI_VCC09 power supplies voltage	-0.1	0.99	V
CSI_VCC18 power supplies voltage	-0.1	1.98	V
DSI_VCCA09 power supplies voltage	-0.1	0.99	V

DSI_VCCA18 power supplies voltage	-0.1	1.98	V
USB_AVD09 power supplies voltage	-0.1	0.99	V
USB_AVD18 power supplies voltage	-0.1	1.98	V
USB_AVD33 power supplies voltage	-0.1	3.6	V
CODEC_AVDD power supplies voltage	-0.1	1.98	V
Maximum ESD stress voltage, Human Body Model; Any pin to any supply pin, either polarity, or Any pin to all non-supply pins together, either polarity. Three stresses maximum.	-	2000	V

3.2 Recommended operating conditions

Table 3-2 Recommended operating conditions for power supplies

Symbol	Description	Min	Typ	Max	Unit
VDDMEM	VDDMEM voltage for SSTL18 (DDR2)	1.7	1.8	1.9	V
DDRVDD	DDR KGD power supplies voltage(DDR2)	1.7	1.8	1.9	V
DDRPLL_VCCA	DDR PLL power supplies voltage	1.62	1.8	1.98	V
VDDIO	GPIO power domain 2 supplies voltage	1.62	1.8	1.98	V
VDDIO18	GPIO power domain 1 supplies voltage	1.62	1.8	1.98	V
VDDIO33	GPIO power domain 1 supplies voltage	3.0	3.3	3.63	V
VDDIO18_DVP	GPIO power domain 0 supplies voltage	1.5	1.8	1.98	V
VDDIO3318_DVP	GPIO power domain 0 supplies voltage	1.62	3.3	3.63	V
VDD	VDD core supplies voltage	0.81	0.9	0.99	V
PLL_VDD	PLL digital voltage	0.81	0.9	0.99	V
PLL_AVDD	PLL analog voltage	1.62	1.8	1.98	V
EFUSE_AVDD	EFUSE program supplies voltage	1.62	1.8	1.98	V
SADC_AVDD	SAR_ADC analog voltage	1.62	1.8	1.98	V

CSI_VCC09	MIPI RX CORE analog voltage	0.81	0.9	0.99	V
CSI_VCC18	MIPI RX IO analog voltage	1.62	1.8	1.98	V
DSI_VCC09	MIPI TX CORE analog voltage	0.81	0.9	0.99	V
DSI_VCC18	MIPI TX IO analog voltage	1.62	1.8	1.98	V
USB_AVD09	USB PHY VCCCORE analog voltage	0.81	0.9	0.99	V
USB_AVD18	USB PHY VCC18 analog voltage	1.62	1.8	1.98	V
USB_AVD33	USB PHY VCCA3P3 analog voltage	3.0	3.3	3.6	V
CODEC_AVDD	CODEC analog voltage	1.62	1.8	1.98	V

Table 3-3 Recommended operating conditions for VDDIO0/VDDIO1/VDDIO2 supplied pins

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH18}	Input high voltage for 1.8V I/O application	*0.65	-	+0.3	V
V_{IL18}	Input low voltage for 1.8V I/O application	-0.3	-	*0.35	V
V_{IH33}	Input high voltage for 3.3V I/O application	2	-	+0.3	V
V_{IL33}	Input low voltage for 3.3V I/O application	-0.3	-	0.8	V

Table 3-4 Recommended operating conditions for others

Symbol	Description	Min	Typ	Max	Unit
T_A	Ambient temperature	-20	25	+85	°C
T_J	Junction temperature	-40	25	+125	°C

3.3 General Purpose Input/Output(GPIO)

Power Domain	Voltage Supply
VDDIO0	VDDIO18_DVP/VDDIO_3318_DVP
VDDIO1	VDDIO18/VDDIO33

VDDIO2	VDDIO

3.3.1 Power Domain VDDIO0 DC Characteristics

Parameter		Min	Nom	Max	Unit
V_{IL}	Input Low Voltage	-0.3	-	0.58	V
V_{IH}	Input High Voltage	1.27	-	2	V
V_T	Threshold Point	0.91	0.97	1.03	V
V_{T+}	Schmitt Trigger Low to High Threshold Point	1.03	1.07	1.12	V
V_{T-}	Schmitt Trigger High to Low Threshold Point	0.75	0.83	0.91	V
V_{TPU}	Threshold Point with Pull-up Resistor Enabled	0.9	0.96	1.02	V
V_{TPD}	Threshold Point with Pull-down Resistor Enabled	0.91	0.97	1.06	V
$V_T^+{}_{PU}$	Schmitt Trigger Low to High Threshold Point with Pull-up Resistor Enabled	1.02	1.06	1.11	V
$V_T^-{}_{PU}$	Schmitt Trigger High to Low Threshold Point with Pull-up Resistor Enabled	0.74	0.82	0.9	V
$V_T^+{}_{PD}$	Schmitt Trigger Low to High Threshold Point with Pull-down Resistor Enabled	1.03	1.08	1.13	V
$V_T^-{}_{PD}$	Schmitt Trigger High to Low Threshold Point with Pull-down Resistor Enabled	0.75	0.83	0.92	V
I_I	Input Leakage Current @ V_I = 1.8V or 0V	-	-	±10µ	A
I_{OZ}	Tri-state Output Leakage Current @ V_O = 1.8V or 0V	-	-	±10µ	A
R_{SPU}	Strong Pull-up Resistor	-	-	-	Ω
R_{PU}	Pull-up Resistor	33k	60k	92k	Ω
R_{PD}	Pull-down Resistor	34k	61k	158k	Ω
V_{OL}	Output Low Voltage	-	-	0.45	V
V_{OH}	Output High Voltage	1.4	-	-	V

I_{OL}	Low Level Output Current @ V_{OL}(max)				
	(DS1,DS0) = ‘00’	4.9	7.8	11.1	mA
	(DS1,DS0) = ‘01’	7.4	11.7	16.3	mA
	(DS1,DS0) = ‘10’	9.8	15.5	21.6	mA
	(DS1,DS0) = ‘11’	12.2	19.1	26.6	mA
	(DS2,DS1,DS0) = ‘000’	4.9	7.8	11.1	mA
	(DS2,DS1,DS0) = ‘001’	7.4	11.7	16.4	mA
	(DS2,DS1,DS0) = ‘010’	9.8	15.5	21.7	mA
	(DS2,DS1,DS0) = ‘011’	12.2	19.2	26.7	mA
	(DS2,DS1,DS0) = ‘100’	14.6	23.0	31.9	mA
	(DS2,DS1,DS0) = ‘101’	17.0	26.6	36.8	mA
	(DS2,DS1,DS0) = ‘110’	19.4	30.2	41.6	mA
	(DS2,DS1,DS0) = ‘111’	21.7	33.7	46.2	mA
I_{OH}	High Level Output Current @ V_{OH}(min)				
	(DS1,DS0) = ‘00’	3.6	6.2	9.6	mA
	(DS1,DS0) = ‘01’	5.4	9.3	14.3	mA
	(DS1,DS0) = ‘10’	7.3	12.4	19.1	mA
	(DS1,DS0) = ‘11’	9.1	15.5	23.8	mA
	(DS2,DS1,DS0) = ‘000’	3.6	6.2	9.5	mA
	(DS2,DS1,DS0) = ‘001’	5.4	9.3	14.3	mA
	(DS2,DS1,DS0) = ‘010’	7.2	12.4	19.1	mA
	(DS2,DS1,DS0) = ‘011’	9.0	15.4	23.8	mA
	(DS2,DS1,DS0) = ‘100’	10.8	18.5	28.5	mA
	(DS2,DS1,DS0) = ‘101’	12.6	21.6	33.1	mA
	(DS2,DS1,DS0) = ‘110’	14.4	24.6	37.8	mA
	(DS2,DS1,DS0) = ‘111’	16.2	27.7	42.5	mA

3.3.2 Power Domain VDDIO1 DC Characteristics

Parameter		Min	Nom	Max	Unit
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{IH}	Input High Voltage	2.0	-	VDDIO1 + 0.3	V
V_T	Threshold Point	1.03	1.18	1.36	V
V_{T+}	Schmitt Trigger Low to High Threshold Point	1.22	1.33	1.49	V
V_{T-}	Schmitt Trigger High to Low Threshold Point	0.87	1.02	1.2	V
V_{TPU}	Threshold Point with Pull-up Resistor Enabled	1.01	1.15	1.33	V
V_{TPD}	Threshold Point with Pull-down Resistor Enabled	1.03	1.19	1.38	V
$V_T^+{}_{PU}$	Schmitt Trigger Low to High Threshold Point with Pull-up Resistor Enabled	1.2	1.31	1.46	V
$V_T^-{}_{PU}$	Schmitt Trigger High to Low Threshold Point with Pull-up Resistor Enabled	0.85	1	1.16	V
$V_T^+{}_{PD}$	Schmitt Trigger Low to High Threshold Point with Pull-down Resistor Enabled	1.23	1.35	1.51	V
$V_T^-{}_{PD}$	Schmitt Trigger High to Low Threshold Point with Pull-down Resistor Enabled	0.87	1.03	1.21	V
I_I	Input Leakage Current @ V_I = 1.8V or 0V	-	-	±10µ	A
I_{OZ}	Tri-state Output Leakage Current @ V_O = 1.8V or 0V	-	-	±10µ	A
R_{SPU}	Strong Pull-up Resistor	-	-	-	Ω
R_{PU}	Pull-up Resistor	26k	47k	72k	Ω
R_{PD}	Pull-down Resistor	27k	54k	267k	Ω
V_{OL}	Output Low Voltage	-	-	0.4	V
V_{OH}	Output High Voltage	2.4	-	-	V
I_{OL}	Low Level Output Current @ V_{OL}(max)				

	(DS2,DS1,DS0) = '000'	4.5	7.1	10.0	mA
	(DS2,DS1,DS0) = '001'	6.7	10.6	14.9	mA
	(DS2,DS1,DS0) = '010'	9.0	14.1	19.7	mA
	(DS2,DS1,DS0) = '011'	11.2	17.6	24.4	mA
	(DS2,DS1,DS0) = '100'	13.4	21.0	29.1	mA
	(DS2,DS1,DS0) = '101'	15.6	24.4	33.6	mA
	(DS2,DS1,DS0) = '110'	17.7	27.7	38.1	mA
	(DS2,DS1,DS0) = '111'	19.9	30.9	42.4	mA
I_{OH}	High Level Output Current @ V_{OH}(min)				
	(DS2,DS1,DS0) = '000'	4.5	6.5	8.7	mA
	(DS2,DS1,DS0) = '001'	6.8	9.7	13.0	mA
	(DS2,DS1,DS0) = '010'	9.1	12.9	17.4	mA
	(DS2,DS1,DS0) = '011'	11.3	16.1	21.6	mA
	(DS2,DS1,DS0) = '100'	13.6	19.3	25.9	mA
	(DS2,DS1,DS0) = '101'	15.8	22.5	30.2	mA
	(DS2,DS1,DS0) = '110'	18.1	25.7	34.5	mA
	(DS2,DS1,DS0) = '111'	20.3	28.9	38.8	mA

3.3.3 Power Domain VDDIO2 DC Characteristics

Parameter		Min	Nom	Max	Unit
V_{IL}	Input Low Voltage	-0.3	-	0.35*V DDIO	V
V_{IH}	Input High Voltage	0.65*V DDIO	-	1.98	V
V_T	Threshold Point	0.83	0.91	1	V
V_{T+}	Schmitt Trigger Low to High Threshold Point	0.95	1.03	1.12	V

V_{T-}	Schmitt Trigger High to Low Threshold Point	0.71	0.8	0.9	V
V_{TPU}	Threshold Point with Pull-up Resistor Enabled	0.82	0.9	1	V
V_{TPD}	Threshold Point with Pull-down Resistor Enabled	0.84	0.92	1	V
V_{T^+PU}	Schmitt Trigger Low to High Threshold Point with Pull-up Resistor Enabled	0.95	1.02	1.11	V
V_{T^-PU}	Schmitt Trigger High to Low Threshold Point with Pull-up Resistor Enabled	0.7	0.79	0.89	V
V_{T^+PD}	Schmitt Trigger Low to High Threshold Point with Pull-down Resistor Enabled	0.96	1.05	1.12	V
V_{T^-PD}	Schmitt Trigger High to Low Threshold Point with Pull-down Resistor Enabled	0.72	0.81	0.91	V
I_I	Input Leakage Current @ V_I = 1.8V or 0V	-	-	±10µ	A
I_{OZ}	Tri-state Output Leakage Current @ V_O = 1.8V or 0V	-	-	±10µ	A
R_{SPU}	Strong Pull-up Resistor	-	-	-	Ω
R_{PU}	Pull-up Resistor	55k	79k	121k	Ω
R_{PD}	Pull-down Resistor	51k	87k	169k	Ω
V_{OL}	Output Low Voltage	-	-	0.45	V
V_{OH}	Output High Voltage	1.35	-	-	V
I_{OL}	Low Level Output Current @ V_{OL}(max)				
	(DS1,DS0) = ‘00’	7.6	12.8	18.0	mA
	(DS1,DS0) = ‘01’	15.2	25.3	35.5	mA
	(DS1,DS0) = ‘10’	22.6	37.4	52.2	mA
	(DS1,DS0) = ‘11’	29.7	49.0	67.9	mA
I_{OH}	High Level Output Current @ V_{OH}(min)				
	(DS1,DS0) = ‘00’	4.8	10.8	18.9	mA
	(DS1,DS0) = ‘01’	9.5	21.5	37.4	mA

	(DS1,DS0) = '10'	14.3	32.1	55.9	mA
	(DS1,DS0) = '11'	18.9	42.4	73.9	mA

3.4 Audio Codec

3.4.1 Electrical Characteristics

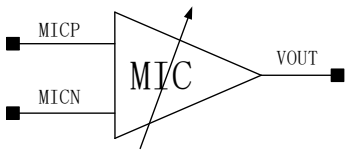
Test conditions: CODEC_AVD=1.8V,VDD=0.9V,TA=25℃,1KHz Sine Input, Fs=48KHz

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Microphone Bias						
Bias Voltage	V_{MICB}	-	0.8*CODEC_AVD	-	0.975*CODEC_AVD	V
Bias Current	I_{MICB}	-	-	-	3	mA
Microphone Gain Boost PGA						
Programmable Gain	G_{BST}	-	0	-	20	dB
Input Resistance	R_{IN}	-	8	-	88	KΩ
Input Capacitance	C_{IN}	-	-	10	-	pF
ALC PGA						
Programmable Gain	G_{ALC}	-	-18	-	28.5	dB
Gain Step Size	-	-	-	1.5	-	dB
ADC						
Signal to Noise Ratio	SNR	A-weighted	-	90	-	dB
Total Harmonic Distortion	THD	-3dBFS input	-	-81	-	dB
Channel Separation	-	-	-	80	-	dB
Headphone Output Driver						
Programmable Gain	G_{DRV}	-	-39	-	6	dB
Gain Step Size	-	-	-	1.5	-	dB

Output Resistance	R_{OUT}	-	-	-	1	Ω
Output Capacitance	C_{OUT}	-	-	20	-	pF
Power Supply Rejection	P_{SRR}	1KHz	-	55	-	dB
Headphone Output						
Signal to Noise Ratio	SNR	A-weighted	-	92	-	dB
Total Harmonic Distortion	THD	60mW16Ω load	-	-70	-	dB
		30mW32Ω load	-	-75	-	dB
		-3dBFS output 600Ω load	-	-80	-	dB
Channel Separation	-	-	-	80	-	dB

3.4.2 Analog Interface Description

3.4.2.1 Microphone input



There are two inputs channels named left ADC channel and right ADC channel. In the each channel, there are two inputs which are configured as differential input by the microphone PGA(MICL and MICR).

In the left channel, microphone inputs are MICPL and MICNL. In the right channel, microphone inputs are MICPR and MICRL.

Microphone PGA has a gain range from 0dB to 20dB.

3.4.2.2 ALC

Automatic Level Control (ALC) function is included to adjust the signal level, which is input into ADC. ALC will measure the signal magnitude and compare it to defined threshold. Then it will adjust the ALC controlled PAG (ALC_L and ALC_R) gain according to the comparison result.

The programmable gain range of ALC controlled PAG is from -18dB to +28.5dB. The tuning step is 1.5dB.

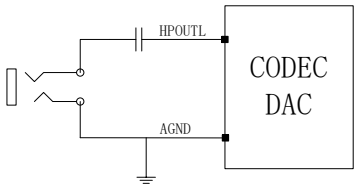
3.4.2.3 DAC OUTPUT

Support headphone output or line output configurations. The output can drive load through DC-blocking capacitor.

In the configuration using DC-blocking capacitor, shown in the following figure, the headphone ground is connected to the real ground. The capacitance and the resistance determine the lower cut-off frequency. For instance, if 600Ω load and 4.7uF DC-blocking capacitor is used, the lower cut-off frequency is:

$$f = \frac{1}{2 \times RC} = \frac{1}{2 \times 600 \times 4.7 \times 10^{-6}} = 56.5Hz$$

The DC-blocking capacitor can be increased to lower the cut-off frequency for better bass response.



The out driver has a gain range from -39dB to +6dB with a tuning step of 1.5dB.

3.4.2.4 Microphone Bias

The output of the Microphone bias is used for bias external microphones. The bias voltage can vary from 0.8*CODEC_AVDD to 0.975* CODEC_AVDD with a step of 0.025* CODEC_AVDD.

Microphone PGA has four gains to amplify the input signal, that is, 0dB, 20dB, 30dB and 40dB.

3.5 MIPI Tx D-PHY

MIPI D-PHY contains tunable source termination and pre-emphasis to enable high speed operation. The Transceiver meets the AC specification below across all operating conditions specified.

3.5.1 DC Specifications

Table 3-5 HS Transmitter DC Specifications

Parameter	Description	Min	Nom	Max	Unit	Note
V_{CMTX}	HS TX static Common-mode voltage	150	200	250	mV	1
$\lvert\Delta V_{CMTX(1,0)}\rvert$	V_{CMTX} mismatch when output is Differential-1 or Differential-0	-	5	-	mV	2
$\lvert V_{OD}\rvert$	HS transmit differential voltage	140	200	270	mV	1
$\lvert\Delta V_{OD}\rvert$	V_{OD} mismatch when output is Differential-1 or Differential-0	-	-	14	mV	2
V_{OHHS}	HS output high voltage	-	-	360	mV	1
Z_{OS}	Single ended output impedance	40	50	62.5	ohm	-
ΔZ_{OS}	Single ended output impedance mismatch	-	-	10	%	-

NOTES:

1. Value when driving into load impedance anywhere in the Z_{ID} range
2. It is recommended that the implementer minimize ΔV_{OD} and $\Delta V_{CMTX(1,0)}$ in order to minimize radiation and optimize signal integrity

Table 3-6 LP Transmitter DC Specification

Parameter	Description	Min	Nom	Max	Unit	Note
V_{OH}	The venin output high level	1.08	1.2	1.32	V	-
V_{OL}	The venin output low level	-50	-	50	mV	-
Z_{OLP}	Output impedance of LP transmitter	110	-	-	Ω	1

NOTES:

1. Though no maximum value for Z_{OLP} is specified. The LP transmitter output impedance shall ensure that the T_{RLP}/T_{FLP} specification is met

3.5.2 AC Specifications

Table 3-7 HS Transmitter AC Specifications

Parameter	Description	Min	Nom	Max	Unit	Note
$\triangle V_{CMTX(HF)}$	Common-mode variations above 450MHz	-	-	15	mV_{RMS}	-
$\triangle V_{CMTX(LF)}$	Common-mode variations between 50MHz-450MHz	-	-	25	mV_{PEAK}	-
T_R and T_F	20%-80% rise time and fall time	-	-	0.3	UI	1,2
		-	-	0.35	UI	1,3
		100	-	-	ps	4
		-	-	0.4	UI	5
		50	-	-	ps	6

NOTES:

1. UI is equal to 1/(2*fh)
2. Applicable when supporting maximum HS bit rates ≤ 1 Gbps (UI≥1ns)
3. Applicable when supporting maximum HS bit rates > 1 Gbps(UI≤1ns) but less than 1.5 Gbps(UI ≥ 0.667ns)
4. Applicable when supporting maximum HS bit rates ≤ 1.5 Gbps. However, to avoid excessive radiation, bit rates ≤ 1.5 Gbps should not use values below 100 ps and bit rates ≤ 1.5 Gbps should not use values below 150 ps

Table 3-8 LP Transmitter AC specifications

Parameter	Description		Min	Nom	Max	Unit	Note
T_{RLP}/T_{FLP}	15%-85% rise time and fall time		-	-	25	ns	1
T_{REOT}	30%-85% rise time and fall time		-	-	35	ns	5,6
$T_{LP-PULSE-TX}$	Pulse width of exclusive-OR clock the LP	First LP exclusive-OR clock pulse after stop state or last pulse before stop state	40	-	0.4	ns	4
		All other pulses	20	-	-		

$T_{LP-PER-TX}$	Period of the LP exclusive-OR clock	90	-	-	ns	-
$\delta V/\delta t_{SR}$	Slew rate @ C_{LOAD} = 0pF	-	-	500	mV/ns	1,3,7,8
	Slew rate @ C_{LOAD} = 5pF	-	-	300	mV/ns	1,3,7,8
	Slew rate @ C_{LOAD} = 20pF	-	-	250	mV/ns	1,3,7,8
	Slew rate @ C_{LOAD} = 70pF	-	-	150	mV/ns	1,3,7,8
	Slew rate @ C_{LOAD} = 0 to 70pF(Falling Edge Only)	30	-	-	mV/ns	1,2,3,12
		25	-	-	mV/ns	1,2,13,16
	Slew rate @ C_{LOAD} = 0 to 70pF(Rising Edge Only)	30	-	-	mV/ns	1,3,9,12
		25	-	-	mV/ns	1,3,13,15
	Slew rate @ C_{LOAD} = 0 to 70pF(Rising Edge Only)	30-0.075*($V_{O,INST}$ - 700	-	-	mV/ns	1,3,10,11,12
		30-0.075*($V_{O,INST}$ - 700	-	-	-	1,3,10,14,13
C_{LOAD}	Load capacitance	0	-	70	pF	1

NOTES:

1. C_{LOAD} includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be < 10 pF. The distributed line capacitance can be up to 50 pF for a transmission line with 2ns delay
2. When the output voltage is between 400mV and 930mV
3. Measured as average across any 50mV segment of the output signal transition
4. This parameter value can be lower than TLPX due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters
5. The rise-time of T_{REOT} starts from the HS common-level at the moment the differential amplitude drops below 70mV, due to stopping the differential drive

6. With an additional load capacitance C_{CM} between 0 and 60pF on the termination center tap at RX side of the Lane
7. This value represents a corner point in a piecewise linear curve
8. When the output voltage is in the range specified by VPIN(absmax)
9. When the output voltage is between 400mV and 700mV
10. Where $V_{O,INST}$ is the instantaneous output voltage, VDP or VDN, in millivolts
11. When the output voltage is between 700mV and 930mV
12. Applicable when the supported data rate ≤ 1.5 Gbps
13. Applicable when the supported data rate > 1.5 Gbps
14. When the output voltage is between 550mV and 790mV
15. When the output voltage is between 400mV and 550mV
16. When the output voltage is between 400mV and 790mV

3.6 MIPI Rx D-PHY

MIPI D-PHY meets the DC and AC specification below across all operating conditions specified.

3.6.1 DC Specifications

Table 3-9 HS Receiver DC Specifications

Parameter	Description	Min	Nom	Max	Unit	Note
$V_{CMRX(DC)}$	Common-mode voltage HS receive	70	-	300	mV	1,2
V_{IDTH}	Differential input high threshold	-	-	70	mV	3
		-	-	40	mV	4
V_{IDTL}	Differential input low threshold	-70	-	-	mV	3
		-40	-	-	mV	4
V_{IHHS}	Single-ended input high voltage	-	-	460	mV	1
V_{ILHS}	Single-ended input low voltage	-40	-	-	mV	1
$V_{TERM-EN}$	Single ended threshold for HS termination enable	-	-	450	mV	-

Z_{ID}	Differential input impedance	80	100	125	ohm	-

NOTES:

1. Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz
2. This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz
3. For devices supporting data rates ≤ 1.5 Gbps
4. For devices supporting data rates > 1.5 Gbps

Table 3-10 LP Receiver DC Specification

Parameter	Description	Min	Nom	Max	Unit	Note
V_{IH}	Logic 1 input voltage	880	-	-	mV	1
		740	-	-	mV	2
V_{IL}	Logic 0 input voltage, not in ULP state	-	-	550	mV	-
$V_{IL-ULPS}$	Logic 0 input voltage, ULP state	-	-	300	mV	-
V_{HYST}	Input hysteresis	25	-	-	mV	-

NOTES:

1. Applicable when the supported data rate ≤ 1.5 Gbps
2. Applicable when the supported data rate > 1.5 Gbps

3.6.2 AC Specifications

Table 3-11 HS Receiver AC Specifications

Parameter	Description	Min	Nom	Max	Unit	Note
$\triangle V_{CMRX(HF)}$	Common-mode interference beyond 450MHz	-	-	100	mV	2,5
		-	-	50	mV	2,6
$\triangle V_{CMRX(LF)}$	Common-mode interference 50MHz-450MHz	-50	-	50	mV	1,4,5
		-25	-	25	mV	1,4,6

CCM	Common-mode termination	-	-	60	pF	3

NOTES:

1. Excluding 'static' ground shift of 50mV
2. $\Delta V_{CMRX(HF)}$ is the peak amplitude of a sine wave superimposed on the receiver inputs
3. For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification
4. Voltage difference compared to the DC average common-mode potential
5. For devices supporting data rates ≤ 1.5 Gbps
6. For devices supporting data rates > 1.5 Gbps

Table 3-12 LP Receiver AC specifications

Parameter	Description	Min	Nom	Max	Unit	Note
e_{SPIKE}	Input pulse rejection	-	-	300	V.ps	1,2,3
T_{MIN-RX}	Minimum pulse width response	20	-	-	ns	4
V_{INT}	Peak interference amplitude	-	-	200	mV	-
f_{INT}	Interference frequency	450	-	-	MHz	-

NOTES:

1. Time-voltage integration of a spike above V_{IL} when being in LP-0 state or below V_{IH} when being in LP-1 state
2. An impulse less than this will not change the receiver state
3. In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers
4. An input pulse greater than this shall toggle the output

3.7 USB 2.0 OTG PHY

3.7.1 DC/AC Specifications

Table 3-13 Transmitter Specification

Description	Min	Typ	Max	Unit
USB_AVD33	3.0	3.3	3.6	V
USB_AVD09	0.81	0.9	0.99	V
High input level(V_{IH})	-	1.2	-	V
Low input level(V_{IL})	-	0	-	V
Output resistance(R_{OUT}) Classic mode(V_{OUT} = 0 or 3.3V) HS mode(V_{OUT} = 0 to 800mV)	40.5	45	49.5	ohms
	40.5	45	49.5	ohms
Output capacitance(seen from D+ or D-)(C_{OUT})	-	-	3	pF
Differential output signal high Classic(LS/FS); I_O = 0mA(V_{OH})	2.97	3.3	3.63	V
Classic(LS/FS); I_O = 6mA	2.2	2.7	-	
HS mode; I_O = 0mA	360	400	440	mV
Differential output signal low Classic(LS/FS); I_O = 0mA(V_{OL})	-0.33	0	0.33	V
Classic(LS/FS); I_O = 6mA	-	0.3	0.8	
HS mode; I_O = 0mA	-40	0	40	mV
Output Common Mode Voltage Classic(LS/FS) mode(V_M)	1.45	1.65	1.85	V
HS mode	0.175	0.2	0.225	V
Rise and fall time LS mode	75	87.5	300	ns
(T_R/T_F) FS mode	4	12	20	ns
HS mode	0.8	1.0	1.2	ns
Vring into load	-	-	10	%
Propagation delay(data to D+/D-) LS mode	30	TBD	300	ns
FS mode	0		12	ns
HS mode	-		-	ns
Propagation delay(tx_en to D+/D-) Classic mode (TPZH/TPZL)	-	-	2	ns
HS mode	-	-	2	ns

Adaptive termination acquisition	-	-	7.5	7.5MHz Cycles

Table 3-14 Receiver Specifications

Description	Min	Typ	Max	Unit
USB_AVD33	3.0	3.3	3.6	V
Receiver sensitivity(RSENS)				
Classic mode		+-250		mV
HS mode		+-25		mV
Receiver common mode(RCM)				
Classic mode	0.8	1.65	2.5	V
HS mode(differential and squelch comparator)	0.1	0.2	0.3	V
HS mode(disconnect comparator)	0.5	0.6	0.7	V
Input capacitance(seen at D+ or D-)	-	-	3	pF
Squelch threshold	100	-	150	mV
Disconnect threshold	570	600	664	mV
High output level(V_{OH})	-	1.8	-	V
Low output level(V_{OL})	-	0	-	V
Propagation delay(TP)				
Classic mode(D+/D- to cl_diff_rx)			16	ns
Classic mode(D+/D- to se_datap_rx or se_datam_rx)			8	ns
HS mode(D+/D- to input of DLL)			1	ns

Table 3-15 Reference Specification

Description	Min	Typ	Max	Unit
VCCBG	3.0	3.3	3.6	V

Bandgap voltage(5% tolerance)	1.18	1.25	1.312	V
Current reference(2% tolerance)	290	300	306	uA
Power	-	-	6	mW
Reference_en to stable voltage reference	-	-	4	us

Table 3-16 Clock and Data Recovery Specification

Description	Min	Typ	Max	Unit
USB_AVD09	0.81	0.9	0.99	V
Bit loss *The total bit loss through a receive path is 4 bit times. This is divided between the Rx un-squelching circuitry and the DLL.	-	-	4	bits
Latency(intrinsic)	-	-	4	clock cycles
Latency(elasticity buffer)	-	-	17	clock cycles

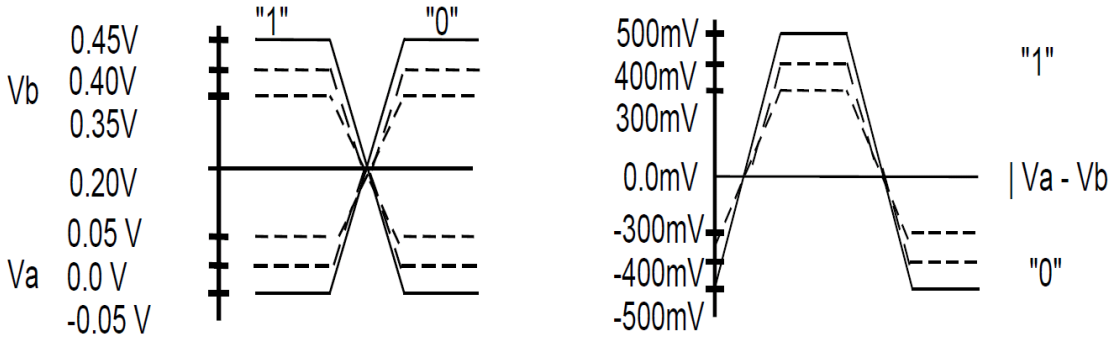


Figure 3-1 Single Ended Signal Swing **Differential Signal Swing**

Table 3-17 VBUS DC Parameters

Parameter	Symbol	Min	Typ	Max	Unit

VBUS Voltage					
VBUS Output Voltage	VBUS	4.6	-	5.25	V
VBUS_VALID Comparator Threshold	-	4.4	4.5	4.6	V
SESSION_VALID Comparator Threshold	-	1.0	1.4	1.8	V
B_SESSION_END Comparator Threshold	-	0.4	0.5	0.6	V
Pullup/Pulldown Resistor Specifications(DP,DM,UID)					
Pulldown Resistor on DP	-	14.5	15	16	KΩ
Pulldown Resistor on DM	-	14.5	15	16	KΩ
Pullup Resistor on DP	-	2.35	2.4	2.5	KΩ
Pullup Resistor in DM	-	2.35	2.4	2.5	KΩ
UID Pullup Resistor	-	160	200	240	KΩ

3.8 Power On, Reset and BOOT

3.8.1 Power-On Timing

The external voltage regulator and other power-on devices must provide the T40N processor with a specific sequence of power and resets to ensure proper operation. Figure 3-2 shows this sequence and Table 3-18 gives the timing parameters. Following are the name of the power.

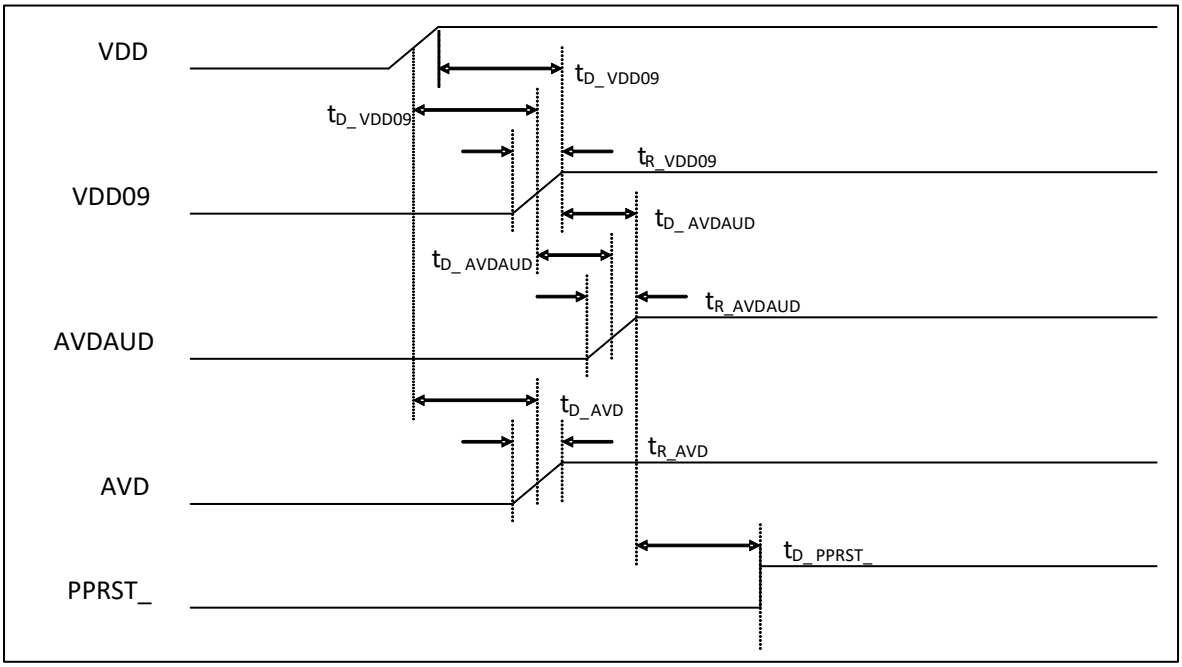
- VDD09: all 0.9V power supplies: VDD, CSI_VCC09, DSI_VCCA09, USB_AVDD09, PLL_VDD
- VMEM: DDRVDD, VDDMEM
- VDDIO18: all other digital IO: VDDIO, VDDIO18, VDDIO18_DVP, VDDIO3318_DVP, PLL_AVDD, SADC_AVDD, CODEC_AVDD, USB_AVD18, CSI_VCCA18, DSI_VCCA18, DDRPLL_VCCA
- VDDIO33: VDDIO33, VDDIO3318_DVP, USB_AVD33

Table 3-18 Power-On Timing Parameters

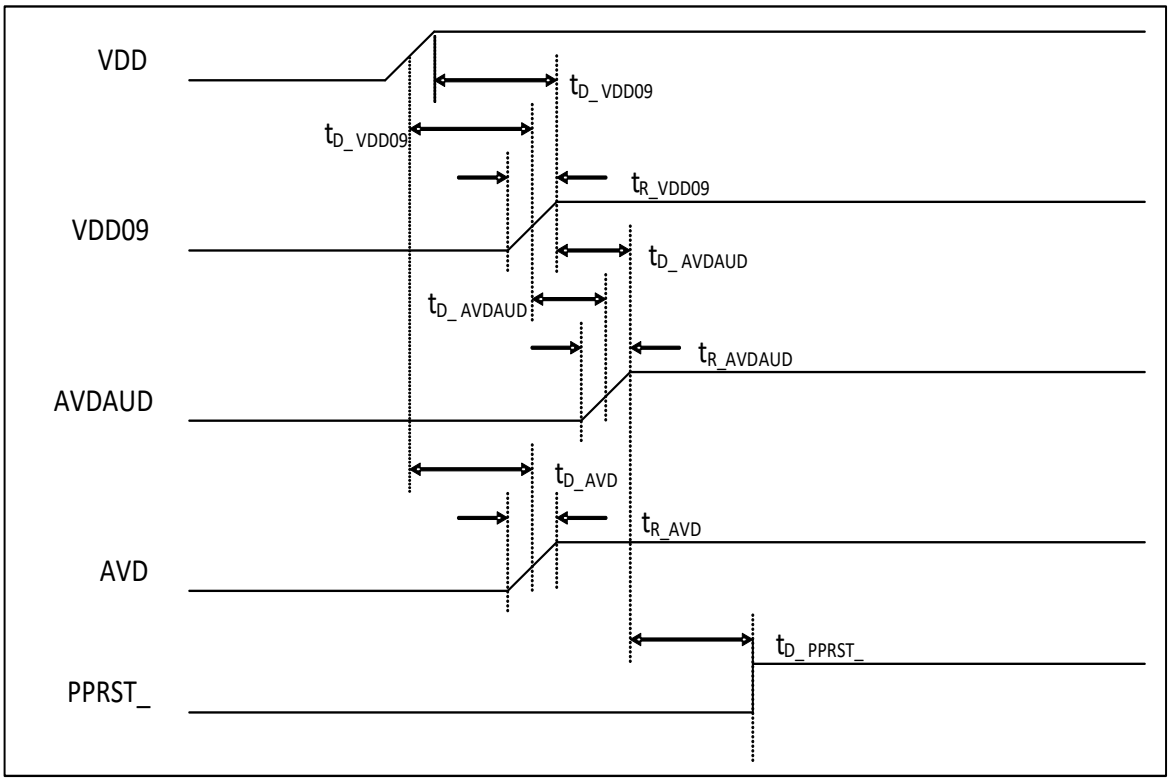
Symbol	Parameter	Min	Max	Unit
$t_{R\_VDDIO18}$	VDDIO18 rise time[1]	0	-	ms
t_{D_VMEM}	Delay between VDDIO18 arriving 50% to VMEM arriving 50%	0	-	ms
$t_{D\_VDDIO33}$	Delay between VMEM arriving 50% to VDDIO33 arriving 50%	0	-	ms
t_{D_VDD09}	Delay between VDDIO33 arriving 50% to VDD09 arriving 50%	0	-	ms
$t_{D\_PPRST\_}$	Delay between VDDIO18 stable and PPRST_ de-asserted	TBD[2]	–	ms[2]

NOTES:

- [1]: The power rise time is defined as 10% to 90%.
- [2]: The PPRST_ must be kept at least 100us. After PPRST_ is de-asserted, the corresponding chip reset will be extended at least 40ms.



PPRST_ reset mode



POR reset mode

Figure 3-2 Power-On Timing Diagram

3.8.2 Reset procedure

There are 3 reset sources: 1. PPRST_ pin reset; 2. POR hardware reset and 3.WDT timeout reset . After reset, program start from boot.

- PPRST_ pin reset.

  This reset is triggered when PPRST_ pin is put to logic 0. It happens in power on RTC power and RESET-KEY pressed to reset the chip from unknown dead state. The reset end time is about 1M EXCLK cycles after rising edge of PPRST_.

- POR(Power-On-Reset) hardware reset.

  The chip POR circuit provides reliable reset function for general applications. Powered by 1.8V analog supply and monitors 0.8V digital and 1.8V analog supply. It generates reset signal to digital logic. Set low if analog supply or digital supply is below the threshold voltage(typical 1.35V threshold for 1.8V supply and 0.6V threshold for 0.8V supply), and will be set high if both of analog supply and digital supply exceed the threshold voltage.

- WDT reset.

  This reset happens in case of WDT timeout. The reset keeps for about a few RTCLK cycles.

After reset, all GPIO shared pins are put to GPIO input function(excluded JTAG pins) and most of their internal pull-up/down resistor are set to on, see “2.5Pin Description” for details. The oscillators are on.

3.8.3 BOOT

The boot sequence of the T40N is controlled by boot_sel[1:0]. The configuration is shown as follow:

Table 3-19 Boot Configuration of T40N

boot_sel[1:0]	Boot method
00	MMC/SD boot @ MSC0 (MMC/SD use GPIO Port B. MSC1 use GPIO Port C)
01	SFC boot @ CS4 (SPI boot)
10	NOR boot @ CS2(just for FPGA testing)
11	USB boot @USB2.0 device, EXTCLK=24MHz

Note:

1. When SFC boot start failure, the program in bootrom will go into MSC0 boot, If it is boot from MMC/SD card at MSC0, its function pins MSC0_D0, MSC0_CLK, MSC0_CMD are initialized, the boot program loads the maximum 100KB code from MMC/SD card to cache and jump to it. Only one data bus which is MSC1_D0 is used.

2. When MSC0 boot start failure, the program in bootrom will go into MSC1 boot，If it is boot from MMC/SD card at MSC1, its function pins MSC1_D0, MSC1_CLK, MSC1_CMD are initialized, the boot program loads the maximum 100KB code from MMC/SD card to cache and jump to it. Only one data bus which is MSC1_D0 is used. If MSC1 boot start failure, jump to USB boot.

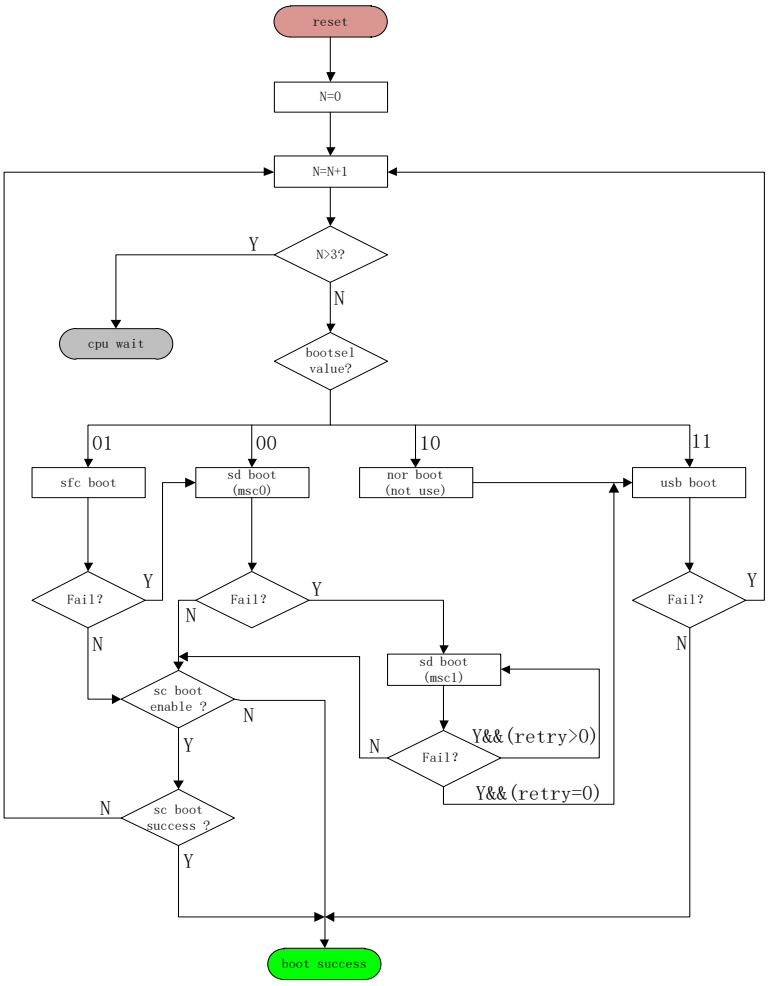


Figure 3-3 Boot sequence diagram of T40N

As shown in boot sequence Block Diagram，After reset, the boot program on the internal boot ROM executes as follows:

1 Disable all interrupts and read boot_sel[0] and boot_sel[1] to determine the boot method.

2 There 26KB backup reading failed, the 26KB backup at 128th, 256 th , …, and finally 1024th page will be tried in consecutive order.

3 If it is boot from MMC/SD card at MSC0, its function pins MSC0_D0, MSC0_CLK, MSC0_CMD are initialized, the boot program loads the maximum 100KB code from MMC/SD card to cache and jump to it. Only one data bus which is MSC0_D0 is used.

4 If it is boot from USB, a block of code will be received through USB cable connected with host PC and be stored in cache. Then branch to this area in cache.

5 If it is boot from SPI nor/nand at SFC, its function pins SFC_CLK,SFC_CE, SFC_DR,SFC_DT, SFC_WP,SFC_HOLD are initialized,the boot program loads the maximum 100KB code from SPI NAND/NOR flash to cache and jump to it.