SY898533L

Precision Differential 3.3V Low-Skew LVPECL 1:4 Fanout Buffer

Features

- Provides Four Differential 3.3V LVPECL Copies
- Selects between Differential CLK, /CLK, or LVPECL Clock Inputs
- CLK, /CLK Pair Accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL Input Levels
- PCLK, /PCLK Pair Accepts LVPECL, CML, SSTL Input Levels
- Guaranteed AC Performance over Temperature and Supply Voltage:
  - 650 MHz Maximum Output Frequency
  - <1.4 ns Propagation Delay (In-to-Q)
  - <30 ps Output Skew
  - <150 ps Part-to-Part Skew
  - Additive Phase Jitter, RMS: 145 fs (Typical)
- 3.3V ±5% Supply Voltage
- 0°C to +70°C Operating Temperature Range
- Available in a 20-Lead TSSOP Package

Applications

- SONET Clock Distribution
- Backplane Distribution

Markets

- LAN/WAN
- Enterprise Servers
- ATE
- Test and Measurement

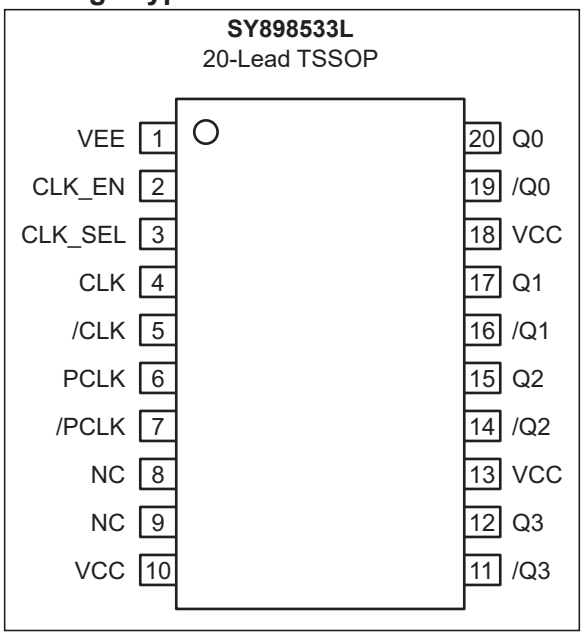
General Description

The SY898533L is a 3.3V, low-skew, 1:4 LVPECL fanout buffer with two selectable clock input pairs. Most standard differential input levels can be applied to the CLK, /CLK pair while LVPECL, CML, or SSTL input levels can be applied to the PCLK, /PCLK pair. To eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin, the clock enable is synchronized with the input signal.

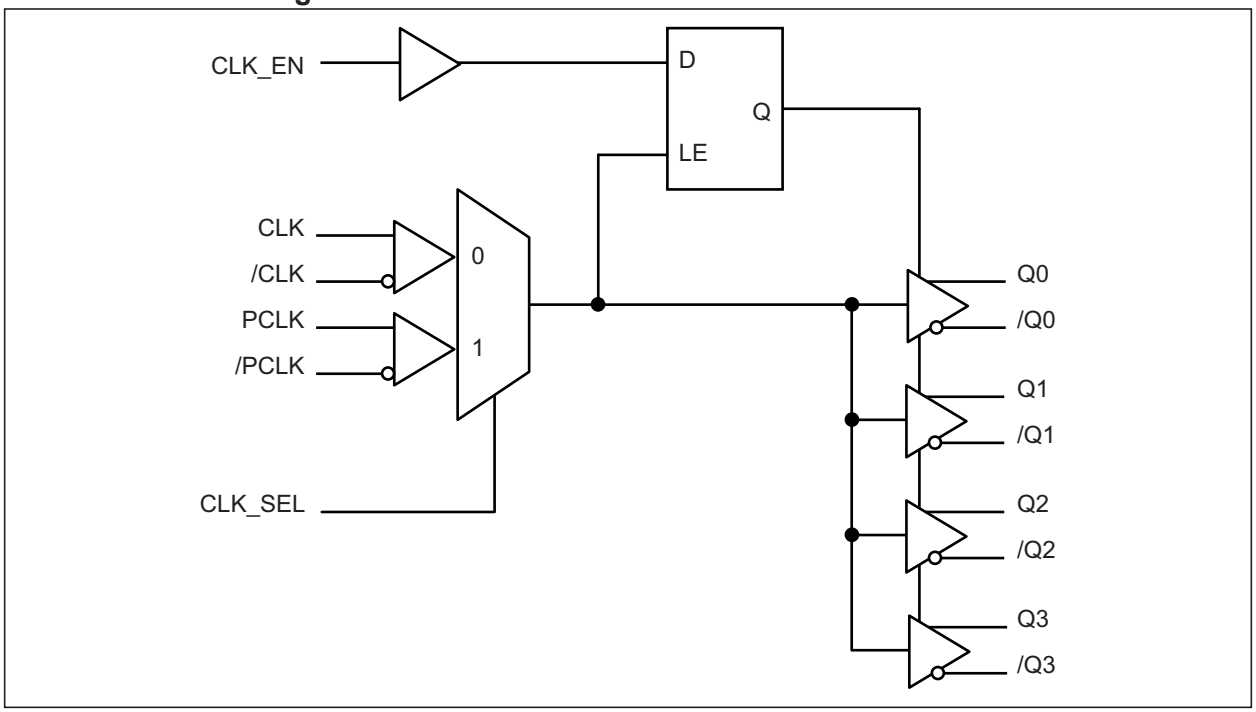
The SY898533L operates from a 3.3V ±5% supply and is guaranteed over the 0°C to +70°C temperature range. The SY898533L is part of Microchip's high-speed, Precision Edge® product line.

Package Type

SY898533L
20-Lead TSSOP



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{CC}) ..... –0.5V to +4.6V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC} + 0.5V
LVPECL Continuous Output Current (I_{OUT}) ..... 50 mA
LVPECL Surge Output Current (I_{OUT}) ..... 100 mA
Lead Temperature (Soldering, 20 sec.) ..... +260°C
Storage Temperature (T_S) ..... –65°C to +150°C

Operating Ratings ‡

Supply Voltage (V_{CC}) ..... +3.135V to +3.465V
Ambient Temperature (T_A) ..... 0°C to +70°C
Package Thermal Resistance (TSSOP, θ_{JA}, Still-Air) ..... 73.2°C/W (Note 1)

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: θ_{JA} value is determined for a 4-layer board in still air unless otherwise stated.

TABLE 1-1: DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{CC} = 3.3V ±5%; T_A = 0°C to +70°C, unless otherwise stated. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply						
Power Supply	V_{CC}	3.135	3.3	3.465	V	—
Power Supply Current	I_{EE}	—	—	50	mA	No load, max. V_{CC}
LVCMOS/LVTTL						
Input High Voltage	V_{IH}	2	—	V_{CC}+0.3	V	—
Input Low Voltage	V_{IL}	–0.3	—	0.8	V	—
Input High Current	I_{IH}	—	—	5	µA	CLK_EN, V_{IN} = V_{CC} = 3.465V
		—	—	150		CLK_SEL, V_{IN} = V_{CC} = 3.465V
Input Low Current	I_{IL}	–150	—	—	µA	CLK_EN, V_{IN} = 0V, V_{CC} = 3.465V
		–5	—	—		CLK_SEL, V_{IN} = 0V, V_{CC} = 3.465V
Differential						
Input High Current	I_{IH}	—	—	150	µA	CLK, V_{IN} = V_{CC} = 3.465V
		—	—	5		/CLK, V_{IN} = V_{CC} = 3.465V
Input Low Current	I_{IL}	–5	—	—	µA	CLK, V_{IN} = 0.5V, V_{CC} = 3.465V
		–150	—	—		/CLK, V_{IN} = 0.5V, V_{CC} = 3.465V
Peak-to-Peak Input Voltage	V_{PP}	0.15	—	1.3	V	—
Common Mode Input Voltage	V_{CMR}	V_{EE}+0.5	—	V_{CC}– 0.85	V	Note 2, Note 3
LVPECL						
Input High Current	I_{IH}	—	—	150	µA	PCLK, V_{IN} = V_{CC} = 3.465V
		—	—	5		/PCLK, V_{IN} = V_{CC} = 3.465V
Input Low Current	I_{IL}	–5	—	—	µA	PCLK, V_{IN} = 0V, V_{CC} = 3.465V
		–150	—	—		/PCLK, V_{IN} = 0V, V_{CC} = 3.465V

TABLE 1-1: DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: V_{CC} = 3.3V ±5%; T_A = 0°C to +70°C, unless otherwise stated. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Peak-to-Peak Input Voltage	V_{PP}	0.3	—	1	V	—
Common Mode Input Voltage	V_{CMR}	V_{EE}+1.5	—	V_{CC}	V	Note 2, Note 3
Output High Voltage	V_{OH}	V_{CC}– 1.4	—	V_{CC}– 0.9	V	Note 4
Output Low Voltage	V_{OL}	V_{CC}– 2.0	—	V_{CC}– 1.7	V	Note 4
Peak-to-Peak Output Voltage Swing	V_{SWING}	0.6	—	1.0	V	—

Note 1: The circuit is designed to meet the DC specifications shown in the table above after thermal equilibrium has been established.

2: Maximum input voltage for PCLK and /PCLK is V_{CC} + 0.3V for single-ended applications.

3: V_{IH} is defined as the common mode voltage.

4: 50Ω to V_{CC} – 2V terminated outputs.

TABLE 1-2: AC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{CC} = 3.3V ±5%; R_L = 50Ω to V_{CC} – 2V; T_A = 0°C to +70°C, unless otherwise stated. Note 1.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Maximum Operating Frequency	f_{MAX}	650	—	—	MHz	—
Differential Propagation Delay IN-to-Q	t_{PD}	1.0	—	1.4	ns	f ≤ 650 MHz
Output-to-Output Skew	t_{SKEW}	—	—	30	ps	Note 2
Part-to-Part Skew		—	—	150		Note 3
Additive Phase Jitter	t_{JITTER}	—	145	—	fs_{RMS}	Note 4, 12 kHz to 20 MHz @ 622 MHz
Output Rise/Fall Time	t_r/t_f	300	—	700	ps	20% to 80% @ 50 MHz
Output Duty Cycle	ODC	47	—	53	%	—

Note 1: High-frequency AC parameters are guaranteed by design and characterization.

2: Output-to-Output skew is measured between two different outputs under identical transitions.

3: Part-to-Part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs. This parameter is defined in accordance with JEDEC Standard 65.

4: Driving only one input clock.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Maximum Junction Temperature	T_J	—	—	+125	°C	—
Lead Temperature	—	—	—	+260	°C	Soldering, 20 sec.
Storage Temperature	T_S	–65	—	+150	°C	—
Ambient Operating Temperature	T_A	0	—	+70	°C	Note 1
Package Thermal Resistance						
Thermal Resistance, 20-Ld TSSOP	θ_{JA}	—	73.2	—	°C/W	Still-Air

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

V_{CC} = 3.3V, V_{EE} = 0V, V_{IN} = 800 mV, R_L = 50Ω to V_{CC} – 2V; T_A = 25°C, unless otherwise stated.

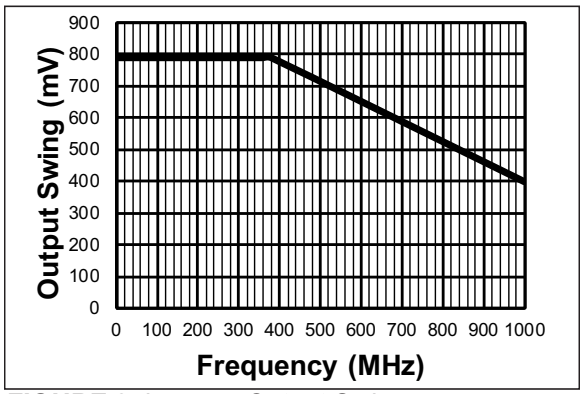


FIGURE 2-1: *Output Swing vs. Frequency.*

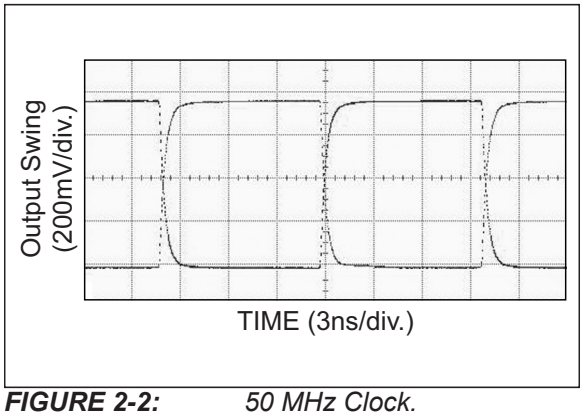


FIGURE 2-2: *50 MHz Clock.*

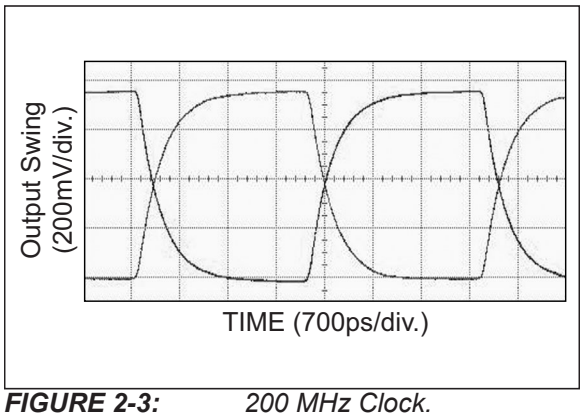


FIGURE 2-3: *200 MHz Clock.*

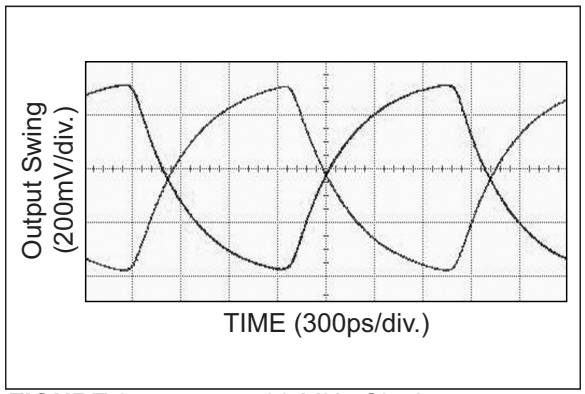


FIGURE 2-4: *500 MHz Clock.*

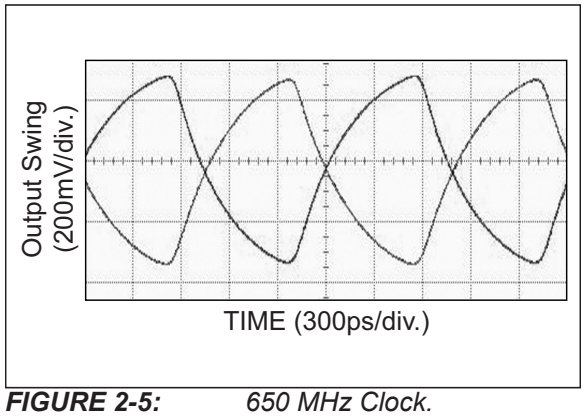


FIGURE 2-5: *650 MHz Clock.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: SY898533L PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	VEE	Ground.
2	CLK_EN	Single-Ended Input: This TTL/CMOS input disables and enables the Q0-Q3 outputs. It is internally connected to a 50 kΩ pull-up resistor and will default to a logic high state if left open. When disabled, Q goes low and /Q goes high. CLK_EN being synchronous, outputs will be enabled/disabled following a rising and a falling edge of the input clock. V_{TH} is approximately 1.5V.
3	CLK_SEL	Single-Ended Input: This single-ended TTL/CMOS-compatible input selects the input to the multiplexer. Note that this input is internally connected to a 50 kΩ pull-down resistor and will default to logic low state if left open. V_{TH} is approximately 1.5V.
4, 5	CLK, /CLK	Differential Input: This input pair is a differential signal input to the device. This input accepts AC- or DC-coupled signals. CLK is internally connected to a 28 kΩ pull-down resistor and will default to a logic low state if left open while /CLK is connected to a 50 kΩ pull-up resistor and will default to a logic high state if left open. This input pair is selected when CLK_SEL is set to logic low.
6, 7	PCLK, /PCLK	Differential Input: This input pair is a differential signal input to the device. This input accepts AC- or DC-coupled signals. PCLK is internally connected to a 50 kΩ pull-down resistor and will default to a logic low state if left open while /PCLK is connected to a 50 kΩ pull-up resistor and will default to a logic high state if left open. This input pair is selected when CLK_SEL is set to logic high.
8, 9	NC	Unused Pins.
10, 13, 18	VCC	Positive Power Supply Pins: Bypass with 0.1 µF||0.01 µF low-ESR capacitors as close to the VCC pins as possible.
20, 19 17, 16 15, 14 12, 11	Q0, /Q0 Q1, /Q1 Q2, /Q2 Q3, /Q3	LVPECL Differential Output Pairs: Differential buffered output copies of the selected input signal. The output swing is typically 800 mV. Unused output pairs may be left floating with no impact on jitter. These differential LVPECL outputs are a logic function of the CLK, /CLK and PCLK, /PCLK, and CLK_SEL inputs. See Table 3-2.

TABLE 3-2: TRUTH TABLE

Inputs			Outputs	
CLK_EN	**CLK_SEL**	**Selected Source**	**Q0:Q3**	**/Q0:/Q3**
0	0	CLK, /CLK	Disabled:Low	Disabled:High
0	1	PCLK, /PCLK	Disabled:Low	Disabled:High
1	0	CLK, /CLK	CLK	/CLK
1	1	PCLK, /PCLK	PCLK	/PCLK

4.0 TIMING DIAGRAMS

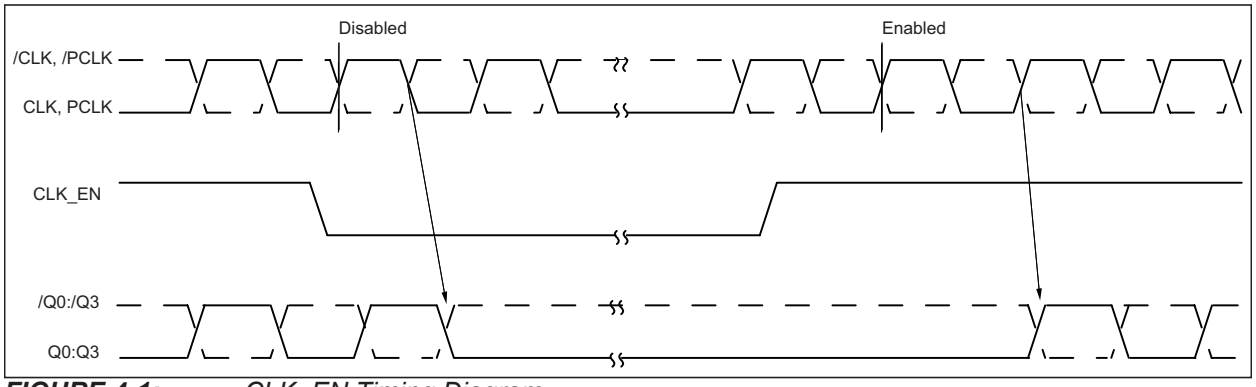


FIGURE 4-1: *CLK_EN Timing Diagram.*

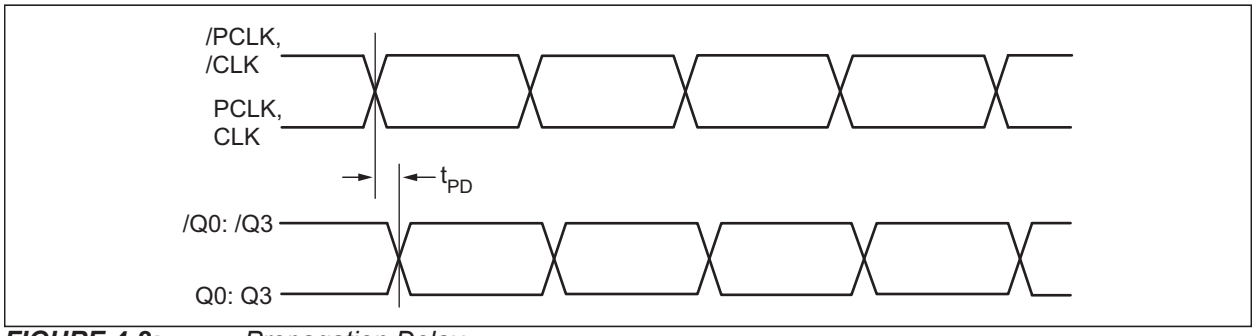


FIGURE 4-2: *Propagation Delay.*

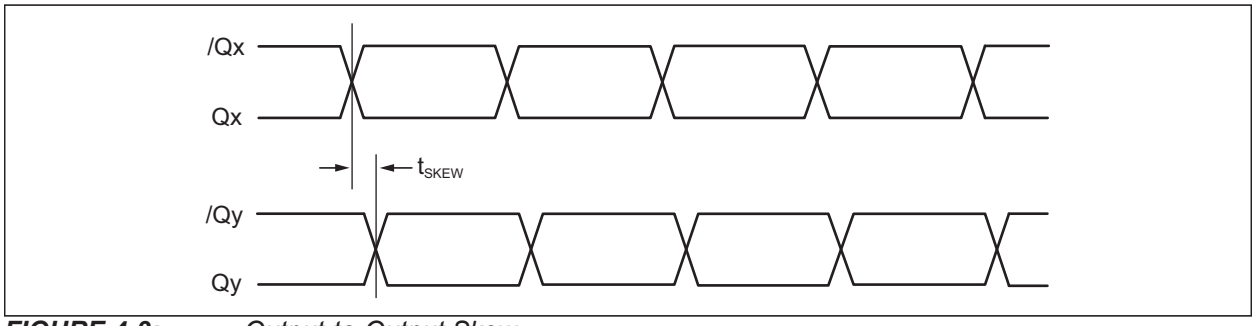


FIGURE 4-3: *Output-to-Output Skew.*

5.0 CLK, /CLK INPUT INTERFACE APPLICATIONS

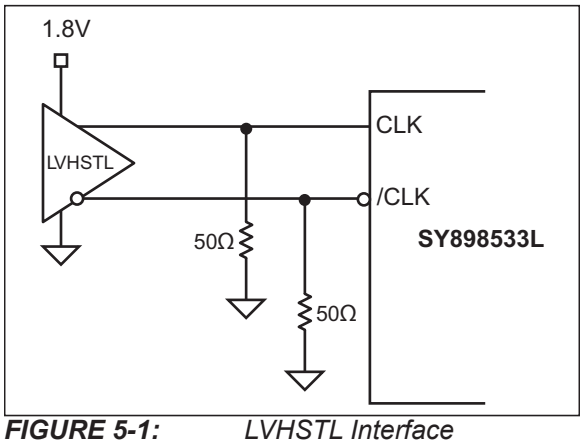


FIGURE 5-1: *LVHSTL Interface (DC-Coupled).*

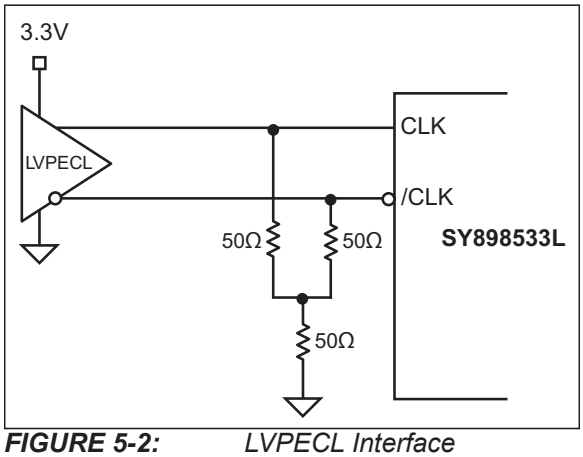


FIGURE 5-2: *LVPECL Interface (DC-Coupled).*

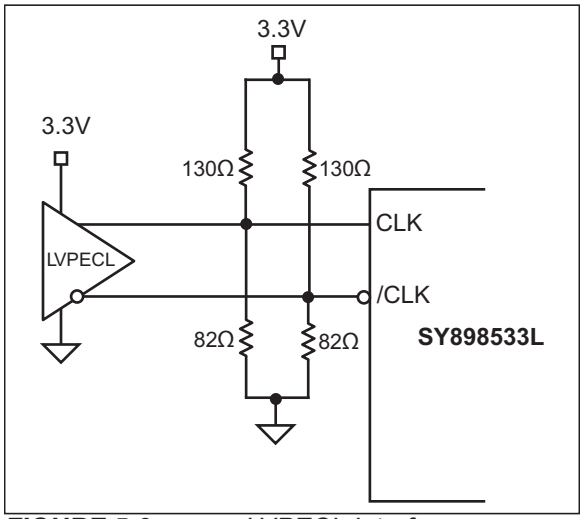


FIGURE 5-3: *LVPECL Interface (DC-Coupled).*

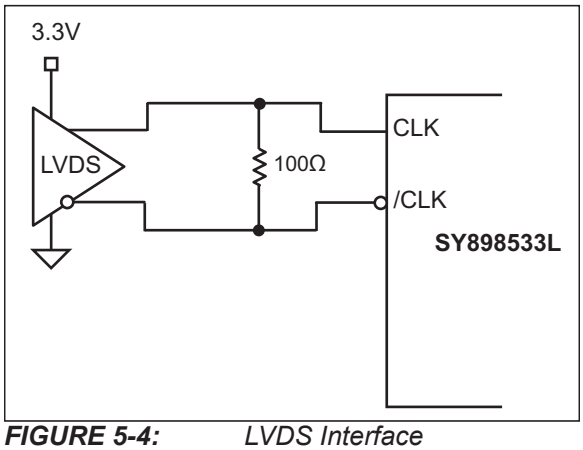


FIGURE 5-4: *LVDS Interface (DC-Coupled).*

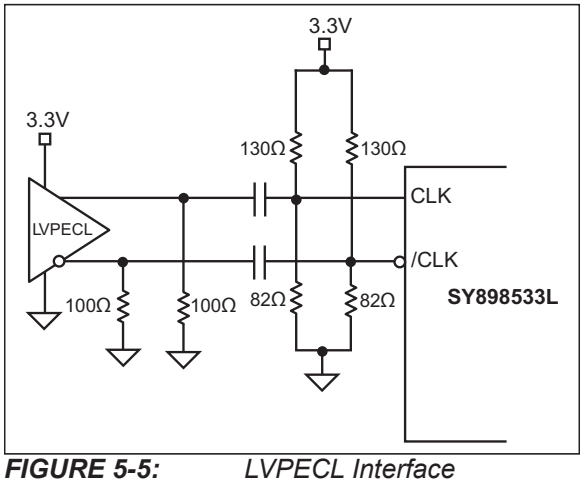


FIGURE 5-5: *LVPECL Interface (AC-Coupled).*

6.0 PCLK, /PCLK INPUT INTERFACE APPLICATIONS

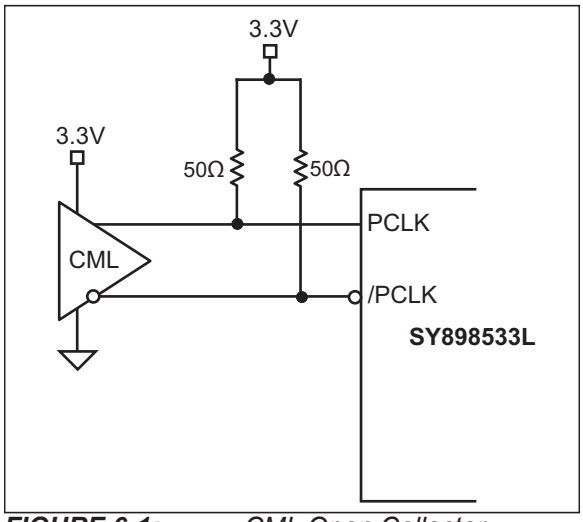


FIGURE 6-1: *CML Open Collector Interface (DC-Coupled).*

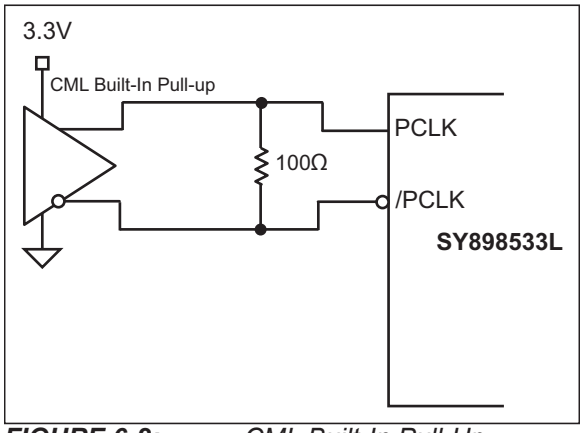


FIGURE 6-2: *CML Built-In Pull-Up Interface (DC-Coupled).*

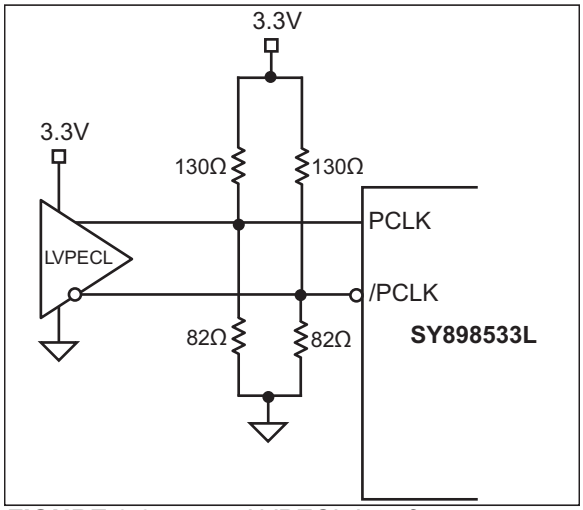


FIGURE 6-3: *LVPECL Interface (DC-Coupled).*

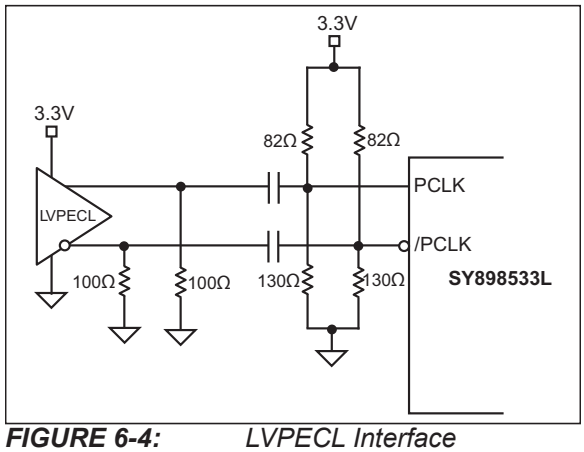


FIGURE 6-4: *LVPECL Interface (AC-Coupled).*

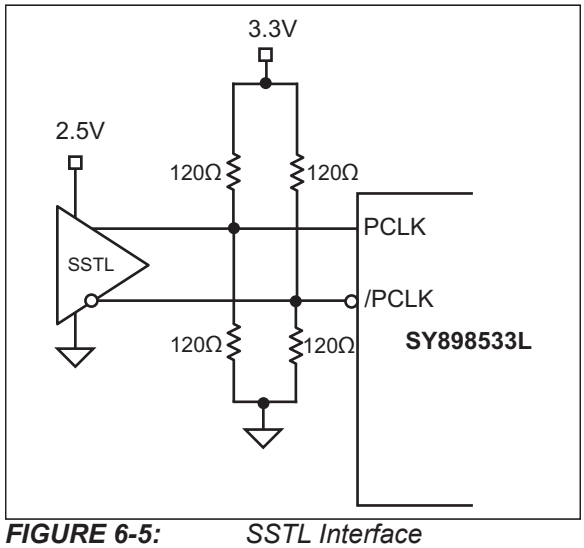


FIGURE 6-5: *SSTL Interface (DC-Coupled).*

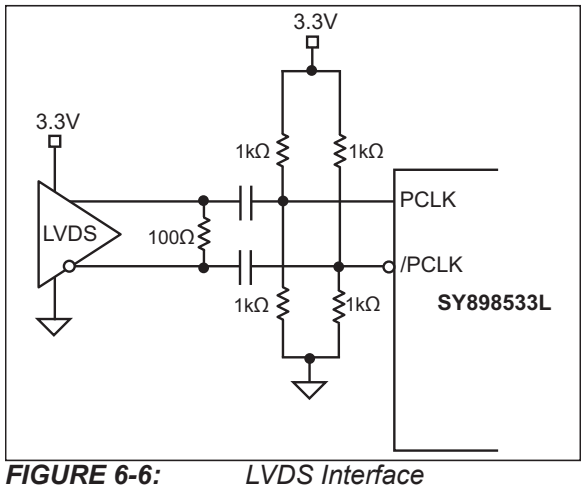


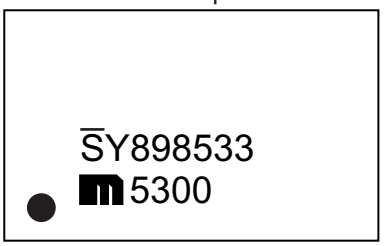
FIGURE 6-6: *LVDS Interface (AC-Coupled).*

7.0 PACKAGING INFORMATION

7.1 Package Marking Information

20-Lead TSSOP*

Example

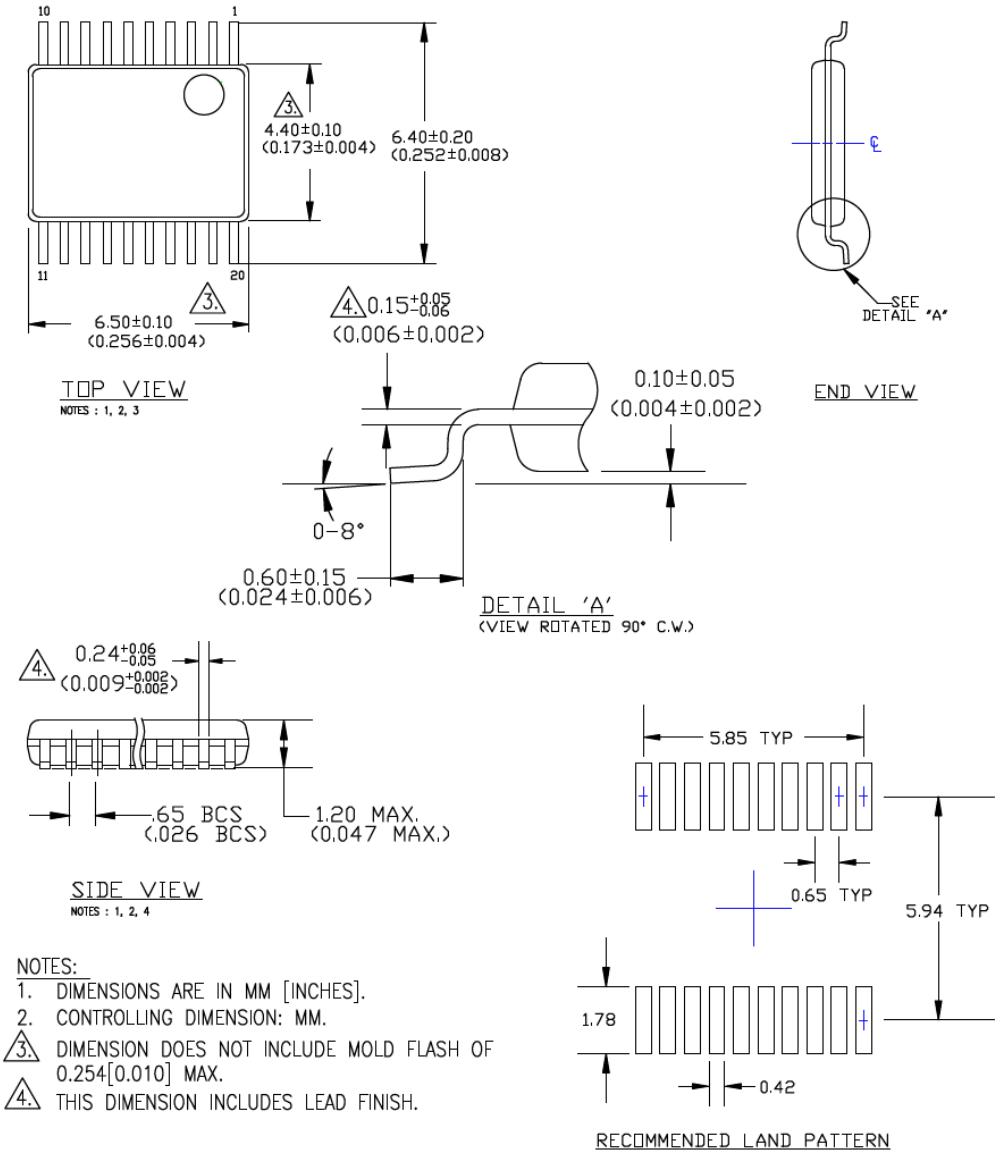


Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	SSS	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

20-Lead TSSOP Package Outline and Recommended Land Pattern

TITLE
20 LEAD TSSOP PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	TSSOP-20LD-PL-1	UNIT	MM [INCH]



NOTES:
1. DIMENSIONS ARE IN MM [INCHES].
2. CONTROLLING DIMENSION: MM.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OF 0.254[0.010] MAX.
4. THIS DIMENSION INCLUDES LEAD FINISH.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

APPENDIX A: REVISION HISTORY

Revision A (April 2019)

- Converted Micrel document SY898533L to Microchip data sheet DS20006043A.
- Minor text changes throughout.
- Updated Additive Phase Jitter value in Features.
- Updated Additive Phase Jitter value and conditions in Table 1-2.
- Updated temperature range in the following sections: Features, General Description, Operating Ratings ‡, Table 1-1, Table 1-2, Product Identification System.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	X	X	-XX
Device	Voltage Option	Package Type	Temperature Range	Special Processing

Device:	SY898533:	Precision Differential 3.3V Low-Skew LVPECL 1:4 Fanout Buffer	
Voltage Option:	L	=	3.3V Only
Package Type:	K	=	20-Lead TSSOP
Temperature Range:	Z	=	0°C to +70°C
Special Processing:	<blank>=		74/Tube
	TR	=	1,000/Reel

Examples:

a) SY898533LKZ: SY898533, 3.3V Voltage Option, 20-Lead TSSOP, 0°C to 70°C Temperature Range, 74/Tube

b) SY898533LKZ-TR: SY898533, 3.3V Voltage Option, 20-Lead TSSOP, 0°C to 70°C Temperature Range, 1,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

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