Filterless, High Efficiency, Mono 2.8 W, Class-D Audio Amplifier

Data Sheet **SSM2305**

FEATURES

- **Filterless Class-D amplifier with Σ-Δ modulation**
- **No sync necessary when using multiple Class-D amplifiers from Analog Devices, Inc.**
- **2.8 W into 4 Ω load and 1.6 W into 8 Ω load at 5.0 V supply with <10% total harmonic distortion (THD)**
- **89% efficiency at 5.0 V, 1.3 W into 8 Ω speaker**
- **>98 dB signal-to-noise ratio (SNR)**
- **Single-supply operation from 2.5 V to 5.5 V**
- **20 nA ultralow shutdown current**
- **Short-circuit and thermal protection**
- **Available in 8-lead, 3 mm × 3 mm LFCSP and MSOP**
- **Pop-and-click suppression**
- **Built-in resistors reduce board component count**
- **Fixed and user-adjustable gain configurations**

APPLICATIONS

- **Mobile phones**
- **MP3 players**
- **Portable gaming**
- **Portable electronics**
- **Educational toys**

GENERAL DESCRIPTION

The SSM2305 is a fully integrated, high efficiency, Class-D audio amplifier designed to maximize performance for mobile phone applications. The application circuit requires a minimum of external components and operates from a single 2.5 V to 5.5 V supply. It is capable of delivering 2.2 W of continuous output power with less than 1% THD + N driving a 4 Ω load from a 5.0 V supply. It has built-in thermal shutdown and output short-circuit protection.

The SSM2305 features a high efficiency, low noise modulation scheme that does not require external LC output filters. The modulation provides high efficiency even at low output power. The SSM2305 operates with 90% efficiency at 1.3 W into 8 Ω or 83% efficiency at 2.2 W into 4 Ω from a 5.0 V supply and has an SNR of >98 dB. Spread-spectrum pulse density modulation is used to provide lower EMI-radiated emissions compared with other Class-D architectures.

The SSM2305 has a micropower shutdown mode with a maximum shutdown current of 30 nA. Shutdown is enabled by applying a Logic 0 to the $\overline{SD}$ pin. The device also includes pop-and-click suppression circuitry. This minimizes voltage glitches at the output during turn-on and turn-off, thus reducing audible noise on activation and deactivation.

The fully differential input of the SSM2305 provides excellent rejection of common-mode noise on the input. Input coupling capacitors can be omitted if the dc input common-mode voltage is approximately $V_{DD}/2$.

The SSM2305 has excellent rejection of power supply noise, including noise caused by GSM transmission bursts and RF rectification. PSRR is typically 60 dB at 217 Hz.

The default gain of the SSM2305 is 18 dB, but users can reduce the gain by using a pair of external resistors.

The SSM2305 is specified over the commercial temperature range (−40°C to +85°C). It is available in both an 8-lead, 3 mm × 3 mm lead frame chip scale package (LFCSP) and an 8-lead mini small outline package (MSOP).

FUNCTIONAL BLOCK DIAGRAM

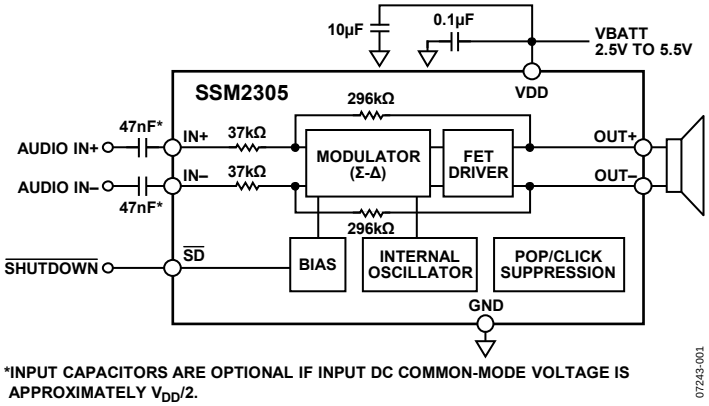

Figure 1.

Rev. B Document Feedback

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TABLE OF CONTENTS

REVISION HISTORY

5/2016—Rev. A to Rev. B

Changed CP-8-2 to CP-8-13 ... Throughout
Changes to Figure 2 and Table 4 ... 5
Updated Outline Dimensions ... 14
Changes to Ordering Guide ... 14

7/2008—Rev. 0 to Rev. A

Changes to Figure 1 ... 1
Change to Shutdown Current Parameter, Table 1 ... 3
Change to Differential Input Impedance Parameter, Table 1 ... 3
Added Exposed Pad Notation to Figure 2 ... 5
Change to Figure 24 ... 9
Changes to Figure 32 and Figure 33 ... 11
Changes to Gain Section ... 12
Updated Outline Dimensions ... 14

3/2008—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 5.0 V, T_A = 25°C, R_L = 8 Ω + 33 µH, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DEVICE CHARACTERISTICS						
Output Power	P_O	R_L = 8 Ω, THD = 1%, f = 1 kHz, BW = 20 kHz		1.34		W
		R_L = 8 Ω, THD = 1%, f = 1 kHz, BW = 20 kHz, V_{DD} = 3.6 V		0.68		W
		R_L = 8 Ω, THD = 10%, f = 1 kHz, BW = 20 kHz		1.67		W
		R_L = 8 Ω, THD = 10%, f = 1 kHz, BW = 20 kHz, V_{DD} = 3.6 V		0.85		W
		R_L = 4 Ω, THD = 1%, f = 1 kHz, BW = 20 kHz		2.22		W
		R_L = 4 Ω, THD = 1%, f = 1 kHz, BW = 20 kHz, V_{DD} = 3.6 V		1.1		W
		R_L = 4 Ω, THD = 10%, f = 1 kHz, BW = 20 kHz		2.8		W
		R_L = 4 Ω, THD = 10%, f = 1 kHz, BW = 20 kHz, V_{DD} = 3.6 V		1.3		W
Efficiency	η	P_O = 1.3 W, 8 Ω		89		%
Total Harmonic Distortion + Noise	THD + N	P_O = 1 W into 8 Ω, f = 1 kHz		0.02		%
		P_O = 0.5 W into 8 Ω, f = 1 kHz, V_{DD} = 3.6 V		0.02		%
Input Common-Mode Voltage Range	V_{CM}		1.0		V_{DD} − 1	V
Common-Mode Rejection Ratio	$CMRR_{GSM}$	V_{CM} = 2.5 V ± 100 mV at 217 Hz, output referred		55		dB
Average Switching Frequency	f_{SW}			280		kHz
Differential Output Offset Voltage	V_{OOS}	G = 18 dB		2.0		mV
POWER SUPPLY						
Supply Voltage Range	V_{DD}	Guaranteed from PSRR test	2.5		5.5	V
Power Supply Rejection Ratio	PSRR	V_{DD} = 2.5 V to 5.0 V, dc input floating	70	85		dB
	$PSRR_{GSM}$	V_{RIPPLE} = 100 mV at 217 Hz, inputs ac GND, C_{IN} = 0.1 µF		60		dB
Supply Current	I_{SY}	V_{IN} = 0 V, no load		3.2		mA
		V_{IN} = 0 V,		3.3		mA
		V_{IN} = 0 V, no load, V_{DD} = 3.6 V		2.8		mA
		V_{IN} = 0 V, V_{DD} = 3.6 V		2.9		mA
		V_{IN} = 0 V, no load, V_{DD} = 2.5 V		2.4		mA
		V_{IN} = 0 V, V_{DD} = 2.5 V		2.4		mA
Shutdown Current	I_{SD}	$\overline{SD}$ = GND		20	30	nA
GAIN CONTROL						
Closed-Loop Gain	Av			18		dB
Differential Input Impedance	Z_{IN}	$\overline{SD}$ = V_{DD}		37		kΩ
SHUTDOWN CONTROL						
Input Voltage High	V_{IH}	I_{SY} ≥ 1 mA		1.2		V
Input Voltage Low	V_{IL}	I_{SY} ≤ 300 nA		0.5		V
Wake-Up Time	t_{WU}	$\overline{SD}$ rising edge from GND to V_{DD}		30		ms
Shutdown Time	t_{SD}	$\overline{SD}$ falling edge from V_{DD} to GND		5		µs
Output Impedance	Z_{OUT}	$\overline{SD}$ = GND		>100		kΩ
NOISE PERFORMANCE						
Output Voltage Noise	e_n	V_{DD} = 3.6 V, f = 20 Hz to 20 kHz, inputs are ac grounded, A_V = 18 dB, A-weighted		40		µV
Signal-to-Noise Ratio	SNR	P_O = 1.4 W, R_L = 8 Ω		98		dB

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings apply at T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	V_{DD}
Common-Mode Input Voltage	V_{DD}
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−65°C to +165°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

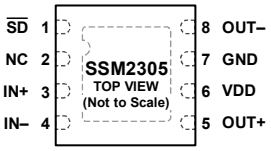
Table 3.

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead, 3 mm × 3 mm LFCSP	62	20.8	°C/W
8-Lead MSOP	210	45	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES:
1. NC = NO CONNECT.
2. EXPOSED PAD IS NOT CONNECTED INTERNALLY. FOR INCREASED RELIABILITY OF THE SOLDER JOINTS AND MAXIMUM THERMAL CAPABILITY IT IS RECOMMENDED THAT THE PAD BE SOLDERED TO THE GROUND PLANE.

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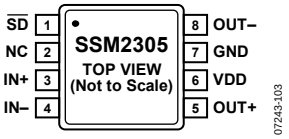
Figure 2. LFSCP Pin Configuration



NC = NO CONNECT

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Figure 3. MSOP Pin Configuration

Table 4. Pin Function Descriptions

Pin No.			
LFCSP	**MSOP**	**Mnemonic**	**Description**
1	1	$\overline{SD}$	Shutdown Input. Active low digital input.
2	2	NC	No Connect. This pin has no function; tie it to GND.
3	3	IN+	Noninverting Input.
4	4	IN–	Inverting Input.
5	5	OUT+	Noninverting Output.
6	6	VDD	Power Supply.
7	7	GND	Ground.
8	8	OUT–	Inverting Output.
0	N/A[1]	EPAD	Exposed Pad. The exposed pad is not connected internally. For increased reliability of the solder joints and maximum thermal capability it is recommended that the pad be soldered to the ground plane.

[1] N/A means not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

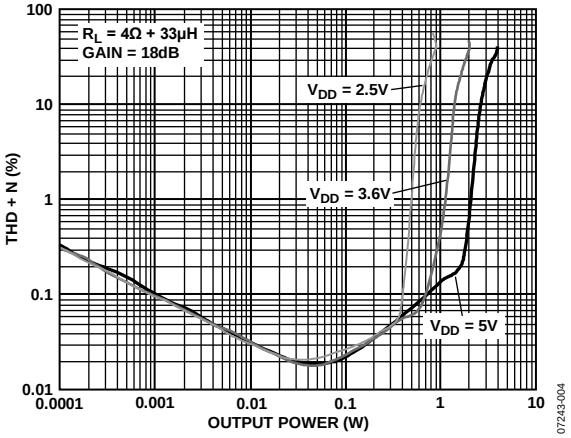

Figure 4. THD + N vs. Output Power into 4 Ω + 33 µH, A_V = 18 dB

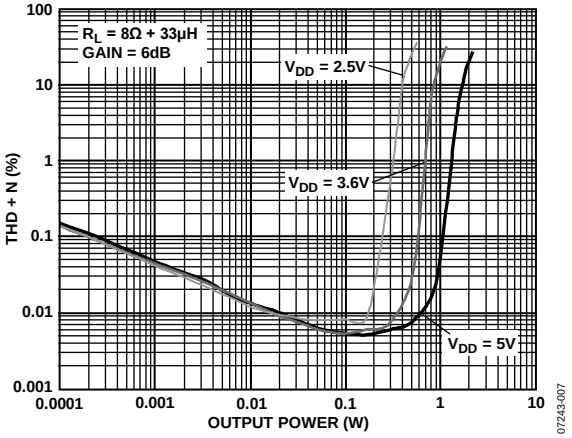

Figure 7. THD + N vs. Output Power into 8 Ω + 33 µH, A_V = 6 dB

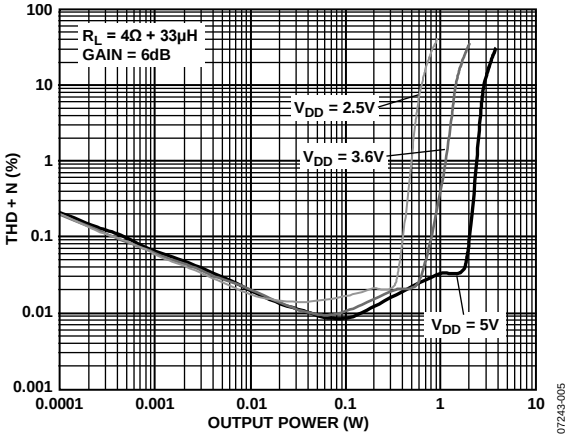

Figure 5. THD + N vs. Output Power into 4 Ω + 33 µH, A_V = 6 dB

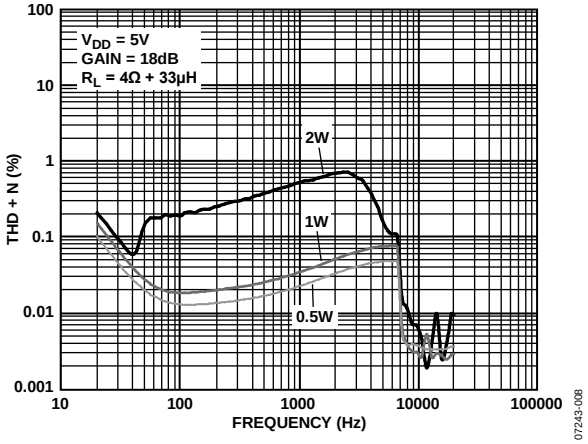

Figure 8. THD + N vs. Frequency, V_{DD} = 5 V, R_L = 4 Ω + 33 µH, A_V = 18 dB

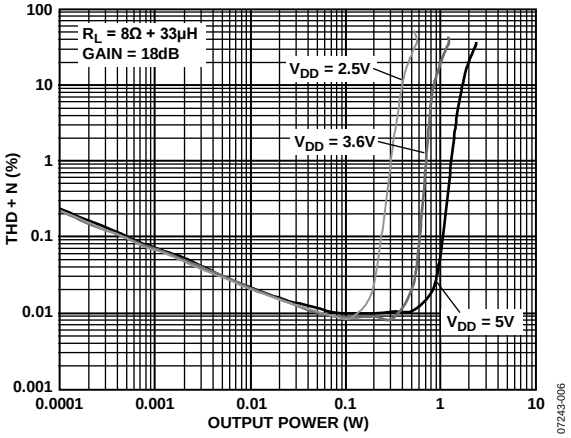

Figure 6. THD + N vs. Output Power into 8 Ω + 33 µH, A_V = 18 dB

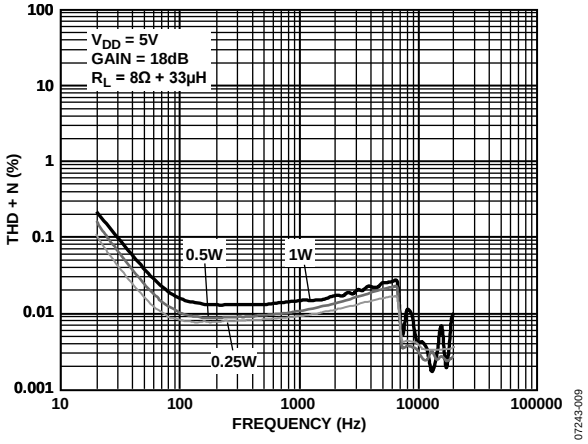

Figure 9. THD + N vs. Frequency, V_{DD} = 5 V, R_L = 8 Ω + 33 µH, A_V = 18 dB

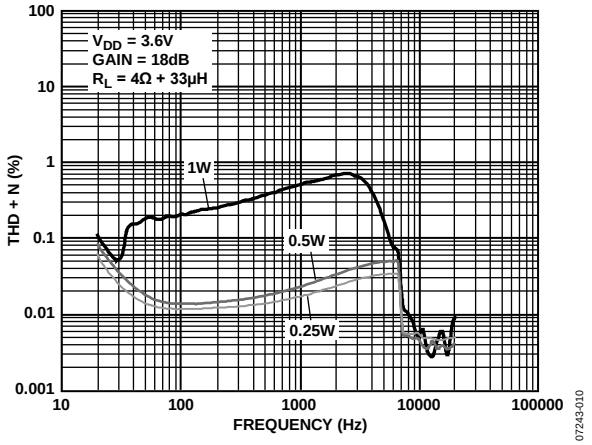

Figure 10. THD + N vs. Frequency, V_{DD} = 3.6 V, R_L = 4 Ω + 33 µH, A_V = 18 dB

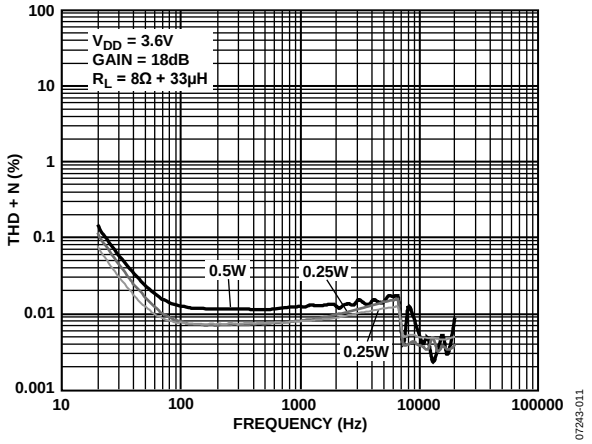

Figure 11. THD + N vs. Frequency, V_{DD} = 3.6 V, R_L = 8 Ω + 33 µH, A_V = 18 dB

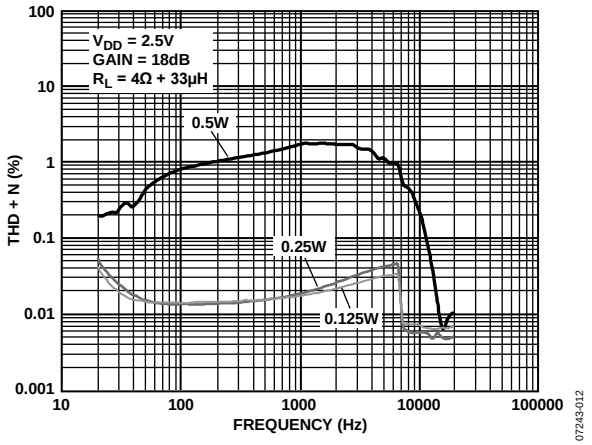

Figure 12. THD + N vs. Frequency, V_{DD} = 2.5 V, R_L = 4 Ω + 33 µH, A_V = 18 dB

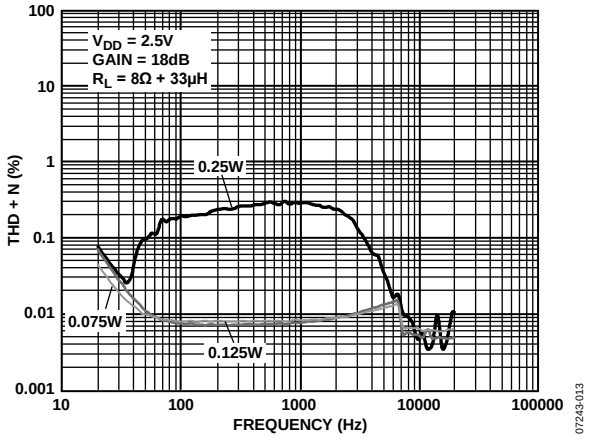

Figure 13. THD + N vs. Frequency, V_{DD} = 2.5 V, R_L = 8 Ω + 33 µH, A_V = 18 dB

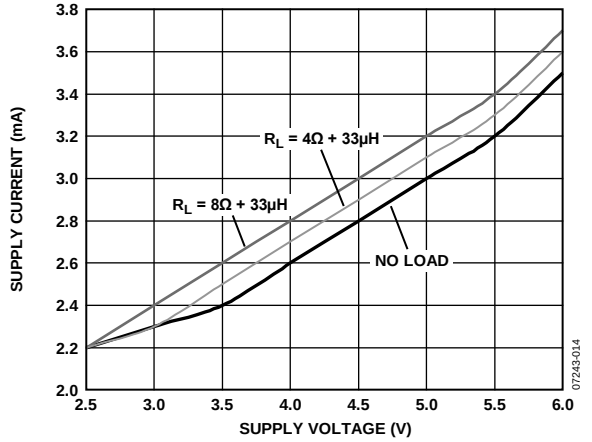

Figure 14. Supply Current vs. Supply Voltage

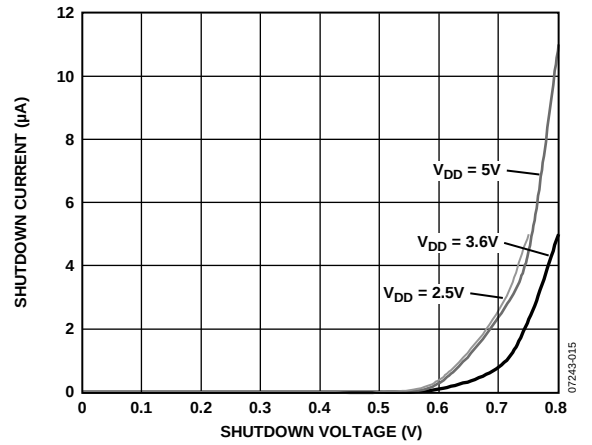

Figure 15. Shutdown Current vs. Shutdown Voltage

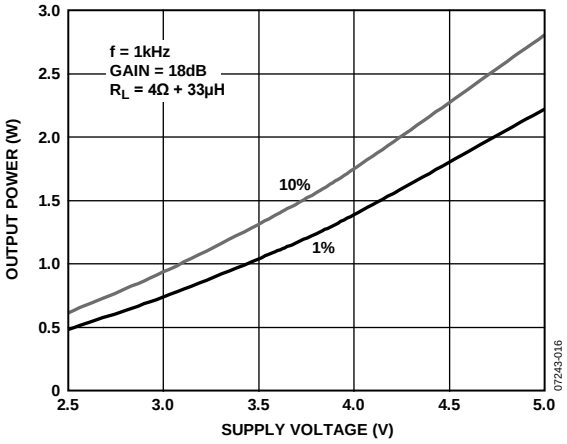

Figure 16. Maximum Output Power vs. Supply Voltage, R_L = 4 Ω + 33 µH, A_V = 18 dB

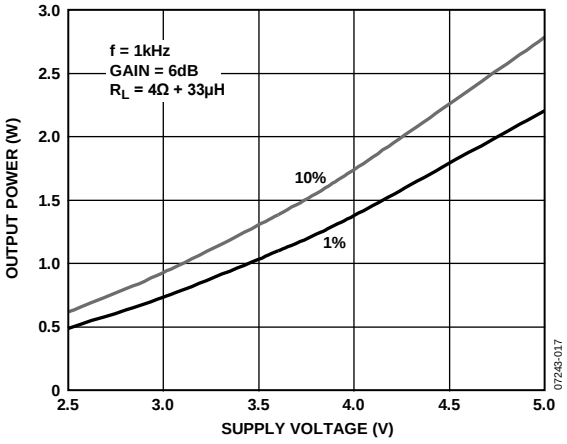

Figure 17. Maximum Output Power vs. Supply Voltage, R_L = 4 Ω + 33 µH, A_V = 6 dB

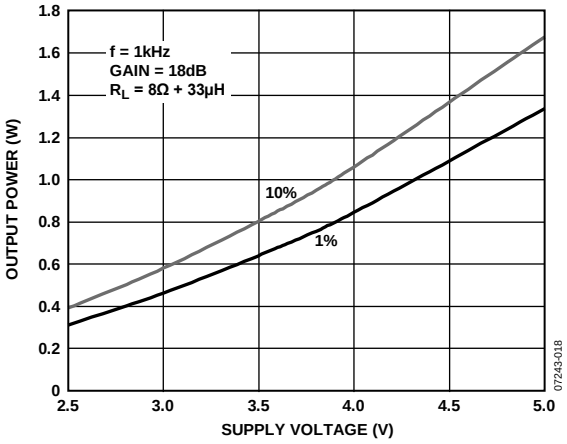

Figure 18. Maximum Output Power vs. Supply Voltage, R_L = 8 Ω + 33 µH, A_V = 18 dB

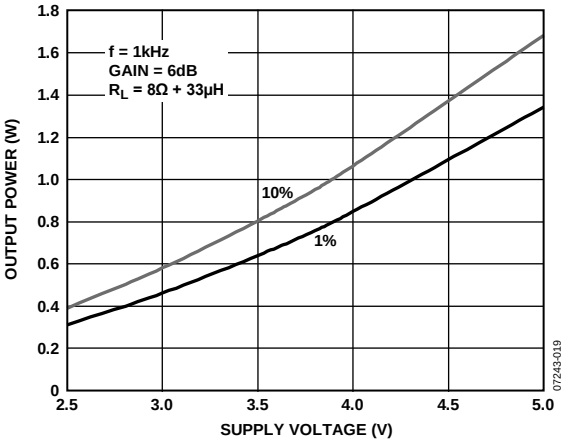

Figure 19. Maximum Output Power vs. Supply Voltage, R_L = 8 Ω + 33 µH, A_V = 6 dB

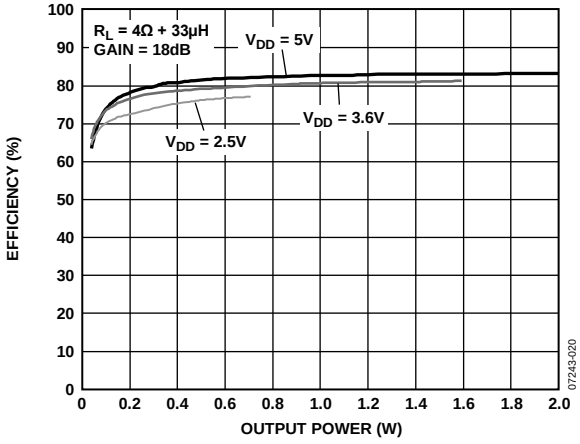

Figure 20. Efficiency vs. Output Power into 4 Ω + 33 µH

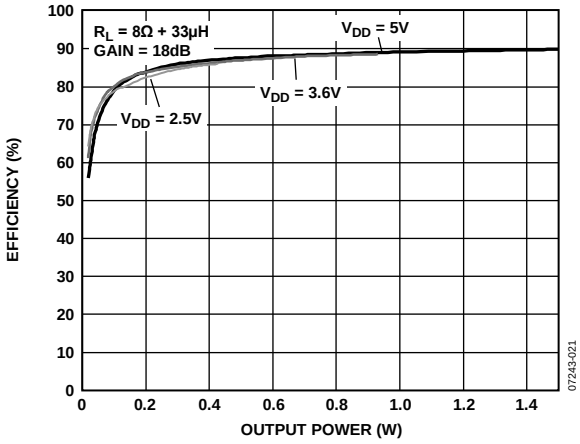

Figure 21. Efficiency vs. Output Power into 8 Ω + 33 µH

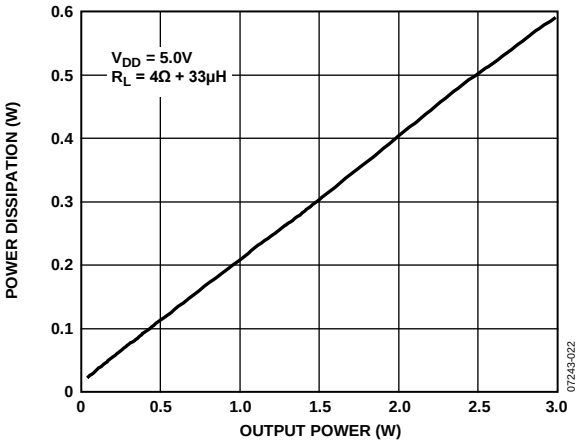

Figure 22. Power Dissipation vs. Output Power into 4 Ω + 33 µH at V_{DD} = 5.0 V

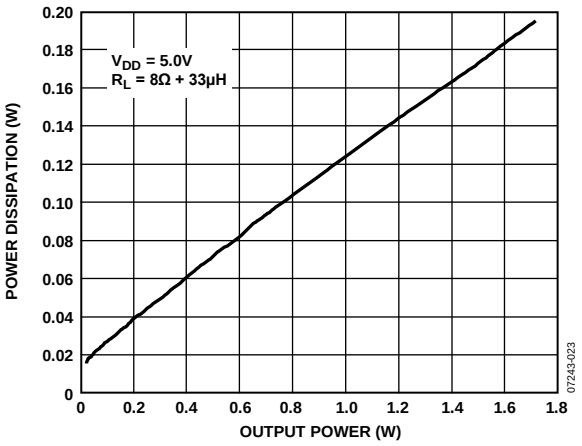

Figure 23. Power Dissipation vs. Output Power into 8 Ω + 33 µH at V_{DD} = 5.0 V

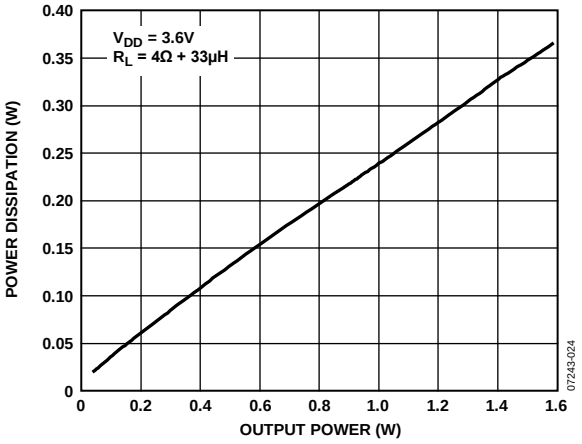

Figure 24. Power Dissipation vs. Output Power into 4 Ω + 33 µH at V_{DD} = 3.6 V

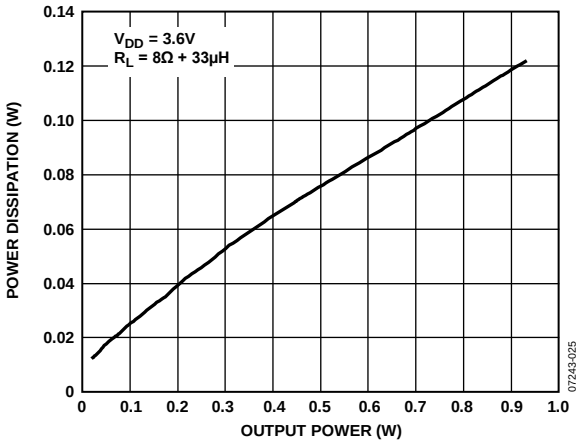

Figure 25. Power Dissipation vs. Output Power into 8 Ω + 33 µH at V_{DD} = 3.6 V

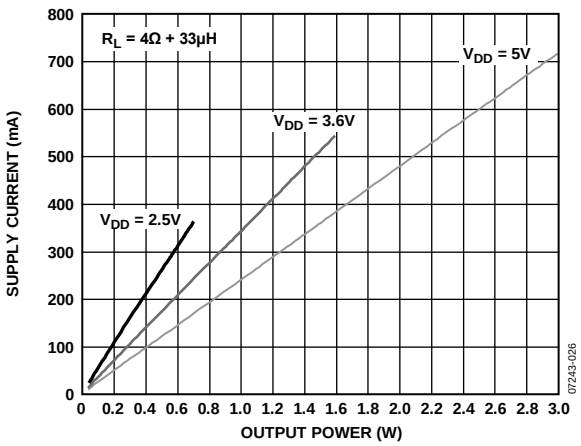

Figure 26. Supply Current vs. Output Power into 4 Ω + 33 µH

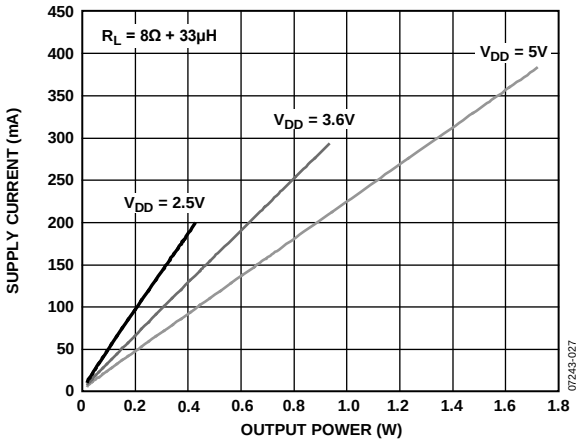

Figure 27. Supply Current vs. Output Power into 8 Ω + 33 µH

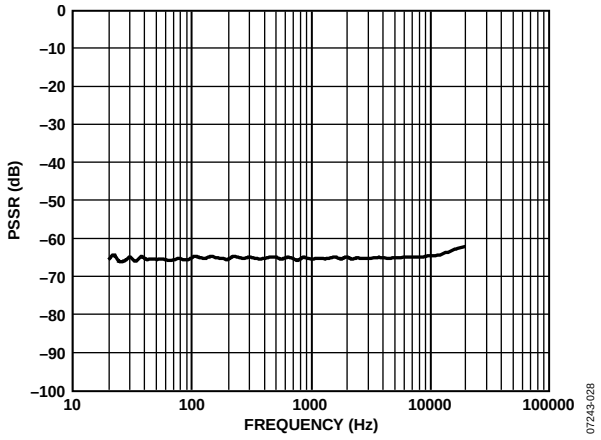

Figure 28. Power Supply Rejection Ratio vs. Frequency

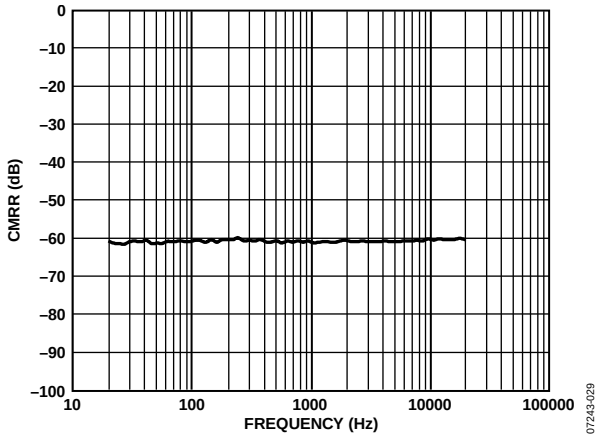

Figure 29. Common-Mode Rejection Ratio vs. Frequency

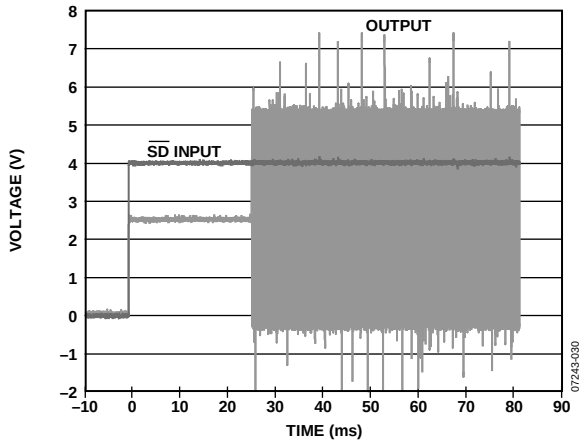

Figure 30. Turn-On Response

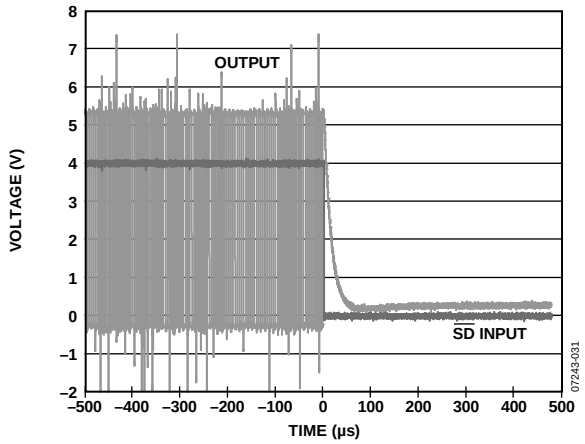

Figure 31. Turn-Off Response

APPLICATIONS INFORMATION

OVERVIEW

The SSM2305 mono Class-D audio amplifier features a filterless modulation scheme that greatly reduces the external components count that, in turn, conserves board space, thereby reducing systems cost. The SSM2305 does not require an output filter, relying instead on the inherent inductance of the speaker coil and the natural filtering of the speaker and human ear to fully recover the audio component of the square wave output. Most Class-D amplifiers use some variation of pulse-width modulation (PWM), but the SSM2305 uses Σ-Δ modulation to determine the switching pattern of the output devices, resulting in a number of important benefits. Σ-Δ modulators do not produce a sharp peak with many harmonics in the AM frequency band, as pulse-width modulators often do. Σ-Δ modulation provides the benefits of reducing the amplitude of spectral components at high frequencies, that is, reducing EMI emission that might otherwise be radiated by speakers and long cable traces. Due to the inherent spread-spectrum nature of Σ-Δ modulation, the need for oscillator synchronization is eliminated for designs incorporating multiple SSM2305 amplifiers.

The SSM2305 also offers protection circuits for overcurrent and temperature protection.

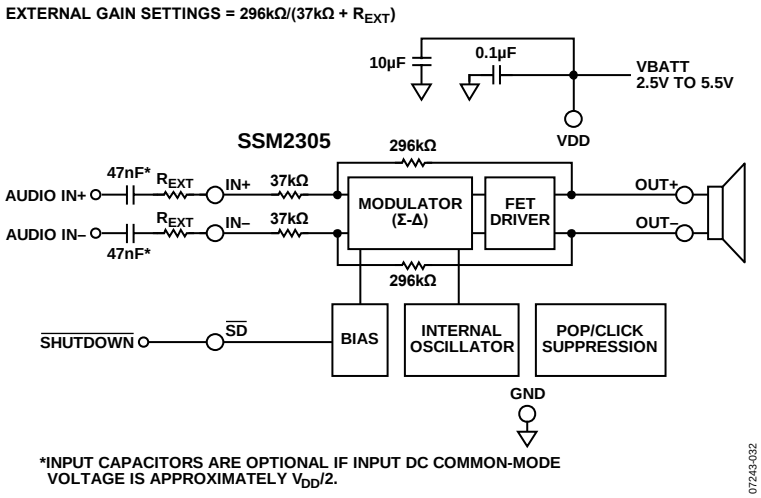

Figure 32. Differential Input Configuration, User-Adjustable Gain

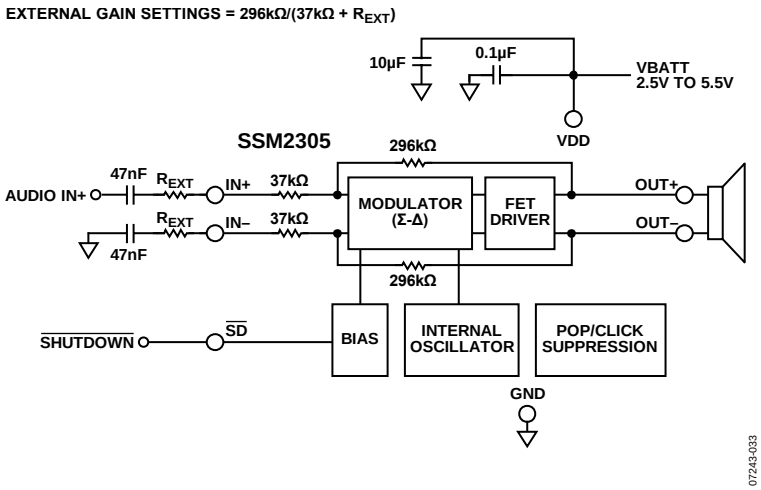

Figure 33. Single-Ended Input Configuration, User-Adjustable Gain

GAIN

The SSM2305 has a default gain of 18 dB that can be reduced by using a pair of external resistors with a value calculated as follows:

$$External\ Gain\ Settings = 296\ k\Omega/(37\ k\Omega + R_{EXT})$$

POP-AND-CLICK SUPPRESSION

Voltage transients at the output of audio amplifiers can occur when shutdown activates or deactivates. Voltage transients as low as 10 mV can be heard as audio pops in the speaker. Clicks and pops can also be classified as undesirable audible transients generated by the amplifier system and, therefore, as not coming from the system input signal. Such transients can be generated when the amplifier system changes its operating mode. For example, the following can be sources of audible transients: system power-up/power-down, mute/unmute, input source change, and sample rate change. The SSM2305 has a pop-and-click suppression architecture that reduces these output transients, resulting in noiseless activation and deactivation.

OUTPUT MODULATION DESCRIPTION

The SSM2305 uses three-level, Σ-Δ output modulation. Each output is able to swing from GND to VDD, and vice versa. Ideally, when no input signal is present, the output differential voltage is 0 V because there is no need to generate a pulse. In a real-world situation, there are always noise sources present. Due to this constant presence of noise, a differential pulse generates when it is required in response to this stimulus. A small amount of current flows into the inductive load when the differential pulse is generated. However, most of the time output differential voltage is 0 V due to the Analog Devices patented three-level, Σ-Δ output modulation. This feature ensures that the current flowing through the inductive load is small.

When the user wants to send an input signal, an output pulse is generated to follow the input voltage. The differential pulse density is increased by raising the input signal level. Figure 34 depicts three-level, Σ-Δ output modulation with and without input stimuli.

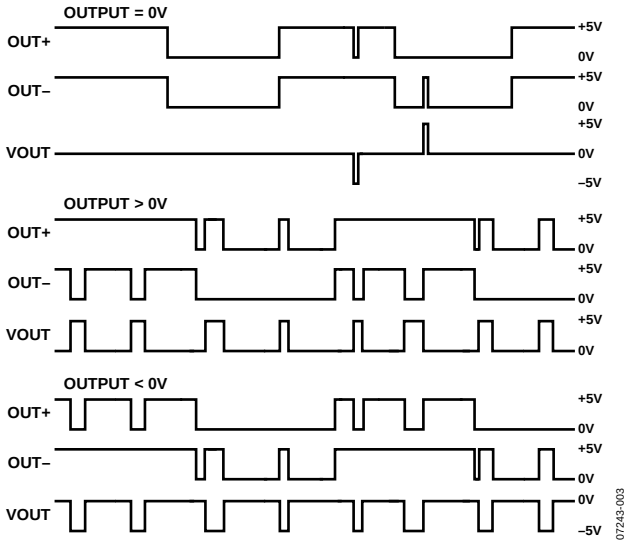

Figure 34. 3-Level, Σ-Δ Output Modulation with and Without Input Stimuli

LAYOUT

As output power continues to increase, care needs to be taken to lay out PCB traces and wires properly between the amplifier, load, and power supply. A good practice is to use short, wide PCB tracks to decrease voltage drops and minimize inductance. Ensure that track widths are at least 200 mil for every inch of track length for lowest dc resistance (DCR), and use 1 oz or 2 oz of copper PCB traces to further reduce IR drops and inductance. A poor layout increases voltage drops, consequently affecting efficiency. Use large traces for the power supply inputs and amplifier outputs to minimize losses due to parasitic trace resistance.

Proper grounding guidelines help improve audio performance, minimize crosstalk between channels, and prevent switching noise from coupling into the audio signal. To maintain high output swing and high peak output power, the PCB traces that connect the output pins to the load and supply pins should be as wide as possible to maintain the minimum trace resistances. It is also recommended that a large ground plane be used for minimum impedances.

In addition, good PCB layouts isolate critical analog paths from sources of high interference. Separate high frequency circuits (analog and digital) from low frequency circuits.

Properly designed multilayer PCBs can reduce EMI emission and increase immunity to the RF field by a factor of 10 or more compared with double-sided boards. A multilayer board allows a complete layer to be used for the ground plane, whereas the ground plane side of a double-sided board is often disrupted with signal crossover.

If the system has separate analog and digital ground and power planes, place the analog ground plane underneath the analog power plane, and, similarly, place the digital ground plane underneath the digital power plane. There should be no overlap between analog and digital ground planes or analog and digital power planes.

INPUT CAPACITOR SELECTION

The SSM2305 does not require input coupling capacitors if the input signal is biased from 1.0 V to V_{DD} − 1.0 V. Input capacitors are required if the input signal is not biased within this recommended input dc common-mode voltage range, if high-pass filtering is needed, or if using a single-ended source. If high-pass filtering is needed at the input, the input capacitor, together with the input resistor of the SSM2305, forms a high-pass filter whose corner frequency is determined by the following equation:

$$f_C = 1/(2\pi \times R_{IN} \times C_{IN})$$

The input capacitor can significantly affect the performance of the circuit. Not using input capacitors degrades both the output offset of the amplifier and the dc PSRR performance.

PROPER POWER SUPPLY DECOUPLING

To ensure high efficiency, low total harmonic distortion (THD), and high PSRR, proper power supply decoupling is necessary. Noise transients on the power supply lines are short duration voltage spikes. Although the actual switching frequency can range from 10 kHz to 100 kHz, these spikes can contain frequency components that extend into the hundreds of megahertz. The power supply input needs to be decoupled with a good quality low ESL, low ESR capacitor, usually of around 4.7 µF. This capacitor bypasses low frequency noises to the ground plane. For high frequency transient noise, use a 0.1 µF capacitor as close as possible to the VDD pin of the device. Placing the decoupling capacitor as close as possible to the SSM2305 helps maintain efficient performance.

OUTLINE DIMENSIONS

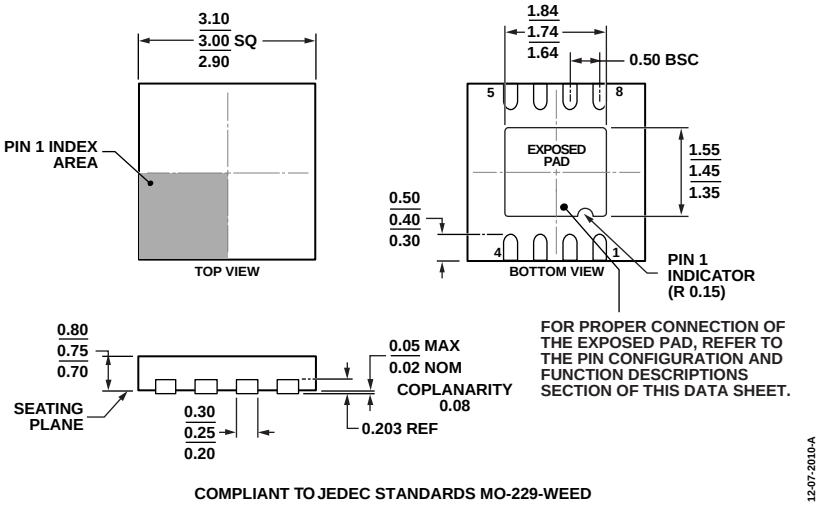

Figure 35. 8-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-8-13)
Dimensions shown in millimeters

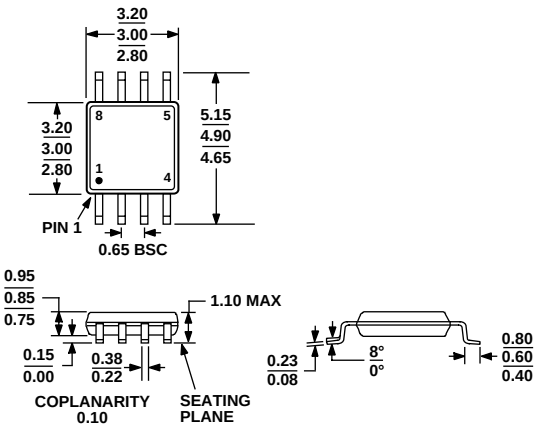

Figure 36. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
SSM2305CPZ-R2	−40°C to +85°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	CP-8-13	Y10
SSM2305CPZ-REEL	−40°C to +85°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	CP-8-13	Y10
SSM2305CPZ-REEL7	−40°C to +85°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	CP-8-13	Y10
SSM2305RMZ-R2	−40°C to +85°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	Y10
SSM2305RMZ-REEL	−40°C to +85°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	Y10
SSM2305RMZ-REEL7	−40°C to +85°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	Y10
SSM2305-EVALZ		Evaluation Board with LFCSP Model		

[1] Z = RoHS Compliant Part.

NOTES

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