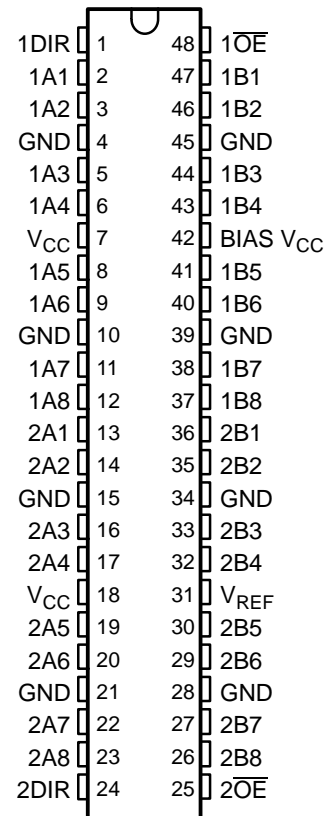


FEATURES

- Member of the Texas Instruments Widebus™ Family
- TI-OPC™ Circuitry Limits Ringing on Unevenly Loaded Backplanes
- OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference
- Bidirectional Interface Between GTLP Signal Levels and LVTTTL Logic Levels
- LVTTTL Interfaces Are 5-V Tolerant
- Medium-Drive GTLP Outputs (50 mA)
- LVTTTL Outputs (–24 mA/24 mA)
- GTLP Rise and Fall Times Designed for Optimal Data-Transfer Rate and Signal Integrity in Distributed Loads
- I_{off} , Power-Up 3-State, and BIAS V_{CC} Support Live Insertion
- Bus Hold on A-Port Data Inputs
- Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

DGG OR DGV PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The SN74GTLPH16945 is a medium-drive, 16-bit bus transceiver that provides LVTTTL-to-GTLP and GTLP-to-LVTTTL signal-level translation. It is partitioned as two 8-bit transceivers. The device provides a high-speed interface between cards operating at LVTTTL logic levels and a backplane operating at GTLP signal levels. High-speed (about three times faster than standard TTL or LVTTTL) backplane operation is a direct result of GTLP's reduced output swing (<1 V), reduced input threshold levels, improved differential input, OEC™ circuitry, and TI-OPC™ circuitry. Improved GTLP OEC and TI-OPC circuits minimize bus-settling time and have been designed and tested using several backplane models. The medium drive allows incident-wave switching in heavily loaded backplanes with equivalent load impedance down to 19 Ω .

GTLP is the Texas Instruments (TI™) derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTLPH16945 is given only at the preferred higher noise margin GTLP, but the user has the flexibility of using this device at either GTL ($V_{TT} = 1.2$ V and $V_{REF} = 0.8$ V) or GTLP ($V_{TT} = 1.5$ V and $V_{REF} = 1$ V) signal levels.

Normally, the B port operates at GTLP signal levels. The A-port and control inputs operate at LVTTTL logic levels, but are 5-V tolerant and are compatible with TTL and 5-V CMOS inputs. V_{REF} is the B-port differential input reference voltage.



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SN74GTLPH16945

16-BIT LVTTTL-TO-GTLP BUS TRANSCEIVER

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DESCRIPTION/ORDERING INFORMATION (CONTINUED)

This device is fully specified for live-insertion applications using I_{off} , power-up 3-state, and BIAS V_{CC} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS V_{CC} circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

This GTLP device features TI-OPC circuitry, which actively limits overshoot caused by improperly terminated backplanes, unevenly distributed cards, or empty slots during low-to-high signal transitions. This improves signal integrity, which allows adequate noise margin to be maintained at higher frequencies.

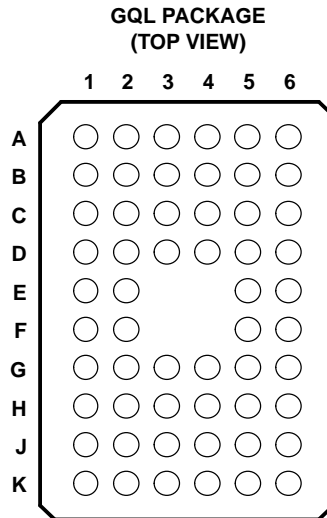
Active bus-hold circuitry holds unused or undriven LVTTTL data inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, the output-enable (\overline{OE}) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

| T_A | PACKAGE (1) | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|-------------|---------------|-----------------------|------------------|
| –40°C to 85°C | TSSOP – DGG | Tape and reel | SN74GTLPH16945GR | GTLPH16945 |
| | TVSOP – DGV | Tape and reel | SN74GTLPH16945VR | GL945 |
| | VFBGA – GQL | Tape and reel | SN74GTLPH16945KR | GL945 |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



TERMINAL ASSIGNMENTS⁽¹⁾

| | 1 | 2 | 3 | 4 | 5 | 6 |
|----------|------|-----|-----------------|----------------------|-----|-------------------|
| A | 1DIR | NC | NC | NC | NC | 1 \overline{OE} |
| B | 1A2 | 1A1 | GND | GND | 1B1 | 1B2 |
| C | 1A4 | 1A3 | V _{CC} | BIAS V _{CC} | 1B3 | 1B4 |
| D | 1A6 | 1A5 | GND | GND | 1B5 | 1B6 |
| E | 2A8 | 1A7 | | | 1B7 | 1B8 |
| F | 2A1 | 2A2 | | | 2B2 | 2B1 |
| G | 2A3 | 2A4 | GND | GND | 2B4 | 2B3 |
| H | 2A5 | 2A6 | V _{CC} | V _{REF} | 2B6 | 2B5 |
| J | 2A7 | 2A8 | GND | GND | 2B8 | 2B7 |
| K | 2DIR | NC | NC | NC | NC | 2 \overline{OE} |

(1) NC – No internal connection

FUNCTIONAL DESCRIPTION

The SN74GTLPH16945 is a medium-drive (50 mA), 16-bit bus transceiver partitioned as two 8-bit segments and is designed for asynchronous communication between data buses. The device transmits data from the A port to the B port or from the B port to the A port, depending on the logic level at the direction-control (DIR) input. \overline{OE} can be used to disable the device so the buses effectively are isolated. Data polarity is noninverting.

For A-to-B data flow, when \overline{OE} is low and DIR is high, the B outputs take on the logic value of the A inputs. When \overline{OE} is high, the outputs are in the high-impedance state.

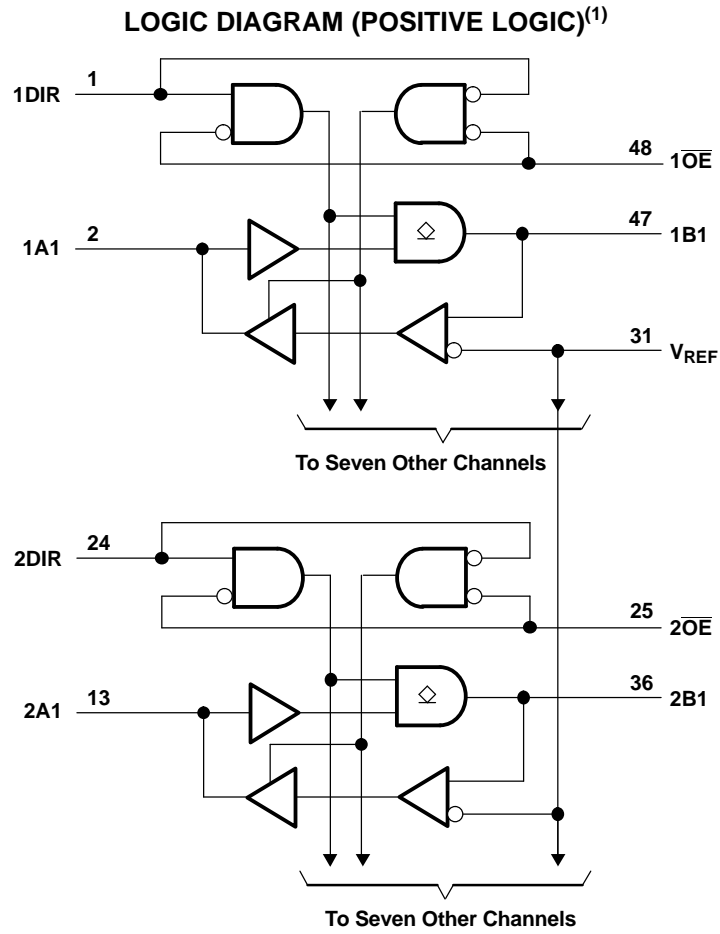
The data flow for B to A is similar to that of A to B, except \overline{OE} and DIR are low.

FUNCTION TABLE

| INPUTS | | OUTPUT | MODE |
|-----------------|-----|------------------|------------------|
| \overline{OE} | DIR | | |
| H | X | Z | Isolation |
| L | L | B data to A port | True transparent |
| L | H | A data to B port | |

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(1) Pin numbers shown are for the DGG and DGV packages.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT | |
|---------------------------|--|---------------------------|------|------|------|
| V_{CC} BIAS V_{CC} | Supply voltage range | -0.5 | 4.6 | V | |
| V_I | Input voltage range ⁽²⁾ | A-port and control inputs | -0.5 | 7 | V |
| | | B port and V_{REF} | -0.5 | 4.6 | |
| V_O | Voltage range applied to any output in the high-impedance or power-off state | A port | -0.5 | 7 | V |
| | | B port | -0.5 | 4.6 | |
| I_O | Current into any output in the low state | A port | | 48 | mA |
| | | B port | | 100 | |
| I_O | Current into any A-port output in the high state ⁽³⁾ | | 48 | mA | |
| | Continuous current through each V_{CC} or GND | | ±100 | mA | |
| I_{IK} | Input clamp current | $V_I < 0$ | | -50 | mA |
| I_{OK} | Output clamp current | $V_O < 0$ | | -50 | mA |
| θ_{JA} | Package thermal impedance ⁽⁴⁾ | DGG package | | 70 | °C/W |
| | | DGV package | | 58 | |
| | | GQL package | | 42 | |
| T_{stg} | Storage temperature range | -65 | 150 | °C | |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) This current flows only when the output is in the high state and $V_O > V_{CC}$.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

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Recommended Operating Conditions⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾

| | | MIN | NOM | MAX | UNIT | |
|---------------------------|------------------------------------|-----------------|------------------|------------------|--------------|---|
| V_{CC} BIAS V_{CC} | Supply voltage | 3.15 | 3.3 | 3.45 | V | |
| V_{TT} | Termination voltage | GTL | 1.14 | 1.2 | 1.26 | V |
| | | GTLP | 1.35 | 1.5 | 1.65 | |
| V_{REF} | Reference voltage | GTL | 0.74 | 0.8 | 0.87 | V |
| | | GTLP | 0.87 | 1 | 1.1 | |
| V_I | Input voltage | B port | | V_{TT} | V | |
| | | Except B port | | V_{CC} | | |
| V_{IH} | High-level input voltage | B port | $V_{REF} + 0.05$ | | V | |
| | | Except B port | 2 | | | |
| V_{IL} | Low-level input voltage | B port | | $V_{REF} - 0.05$ | V | |
| | | Except B port | | 0.8 | | |
| I_{IK} | Input clamp current | | | -18 | mA | |
| I_{OH} | High-level output current | A port | | -24 | mA | |
| I_{OL} | Low-level output current | A port | | 24 | mA | |
| | | B port | | 50 | | |
| $?t/?V$ | Input transition rise or fall rate | Outputs enabled | | 10 | ns/V | |
| $?t/?V_{CC}$ | Power-up ramp rate | 20 | | | μ s/V | |
| T_A | Operating free-air temperature | -40 | | 85 | $^{\circ}$ C | |

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
- (2) Proper connection sequence for use of the B-port I/O precharge feature is GND and BIAS $V_{CC} = 3.3$ V first, I/O second, and $V_{CC} = 3.3$ V last, because the BIAS V_{CC} precharge circuitry is disabled when any V_{CC} pin is connected. The control and V_{REF} inputs can be connected anytime, but normally are connected during the I/O stage. If B-port precharge is not required, any connection sequence is acceptable but, generally, GND is connected first.
- (3) V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.
- (4) V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT} . TI-OPC circuitry is enabled in the A-to-B direction and is activated when $V_{TT} > 0.7$ V above V_{REF} . If operated in the A-to-B direction, V_{REF} should be set to within 0.6 V of V_{TT} to minimize current drain.

Electrical Characteristics

over recommended operating free-air temperature range for GTLP (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|------------------|----------------|--|------------------------------------|--|-----|--------------------|----------|---------------|
| V_{IK} | | $V_{CC} = 3.15\text{ V}$, | $I_I = -18\text{ mA}$ | | | | -1.2 | V |
| V_{OH} | A port | $V_{CC} = 3.15\text{ V to }3.45\text{ V}$, | $I_{OH} = -100\text{ }\mu\text{A}$ | | | $V_{CC} - 0.2$ | | V |
| | | $V_{CC} = 3.15\text{ V}$ | $I_{OH} = -12\text{ mA}$ | | | 2.4 | | |
| | | | $I_{OH} = -24\text{ mA}$ | | | 2 | | |
| V_{OL} | A port | $V_{CC} = 3.15\text{ V to }3.45\text{ V}$, | $I_{OL} = 100\text{ }\mu\text{A}$ | | | | 0.2 | V |
| | | | $I_{OL} = 12\text{ mA}$ | | | | 0.4 | |
| | | $V_{CC} = 3.15\text{ V}$ | $I_{OL} = 24\text{ mA}$ | | | | 0.5 | |
| | B port | $V_{CC} = 3.15\text{ V to }3.45\text{ V}$, | $I_{OL} = 100\text{ }\mu\text{A}$ | | | | 0.2 | |
| | | | $I_{OL} = 10\text{ mA}$ | | | | 0.2 | |
| | | $V_{CC} = 3.15\text{ V}$ | $I_{OL} = 40\text{ mA}$ | | | | 0.4 | |
| | | | $I_{OL} = 50\text{ mA}$ | | | | 0.55 | |
| I_I | Control inputs | $V_{CC} = 3.45\text{ V}$, | $V_I = 0\text{ or }5.5\text{ V}$ | | | | ± 10 | μA |
| $I_{OZH}^{(2)}$ | A port | $V_{CC} = 3.45\text{ V}$ | $V_O = V_{CC}$ | | | | 10 | μA |
| | B port | | $V_O = 1.5\text{ V}$ | | | | 10 | |
| $I_{OZL}^{(2)}$ | A and B ports | $V_{CC} = 3.45\text{ V}$, | $V_O = \text{GND}$ | | | | -10 | μA |
| $I_{BHL}^{(3)}$ | A port | $V_{CC} = 3.15\text{ V}$, | $V_I = 0.8\text{ V}$ | | | | 75 | μA |
| $I_{BHH}^{(4)}$ | A port | $V_{CC} = 3.15\text{ V}$, | $V_I = 2\text{ V}$ | | | | -75 | μA |
| $I_{BHLO}^{(5)}$ | A port | $V_{CC} = 3.45\text{ V}$, | $V_I = 0\text{ to }V_{CC}$ | | | | 500 | μA |
| $I_{BHHO}^{(6)}$ | A port | $V_{CC} = 3.45\text{ V}$, | $V_I = 0\text{ to }V_{CC}$ | | | | -500 | μA |
| I_{CC} | A or B port | $V_{CC} = 3.45\text{ V}$, $I_O = 0$, V_I (A-port or control input) = V_{CC} or GND, V_I (B port) = V_{TT} or GND | Outputs high | | | | 50 | mA |
| | | | Outputs low | | | | 50 | |
| | | | Outputs disabled | | | | 50 | |
| $?I_{CC}^{(7)}$ | | $V_{CC} = 3.45\text{ V}$, One A-port or control input at $V_{CC} - 0.6\text{ V}$, Other A-port or control inputs at V_{CC} or GND | | | | | 1.5 | mA |
| C_i | Control inputs | $V_I = 3.15\text{ V or }0$ | | | | 4.5 | 5 | pF |
| C_{io} | A port | $V_O = 3.15\text{ V or }0$ | | | | 7.5 | 9 | pF |
| | B port | $V_O = 1.5\text{ V or }0$ | | | | 7.5 | 9 | |

(1) All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

(2) For I/O ports, the parameters I_{OZH} and I_{OZL} include the input leakage current.

(3) The bus-hold circuit can sink at least the minimum low sustaining current at V_{ILmax} . I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{ILmax} .

(4) The bus-hold circuit can source at least the minimum high sustaining current at V_{IHmin} . I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IHmin} .

(5) An external driver must source at least I_{BHLO} to switch this node from low to high.

(6) An external driver must sink at least I_{BHHO} to switch this node from high to low.

(7) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

Hot-Insertion Specifications for A Port

over recommended operating free-air temperature range

| PARAMETER | TEST CONDITIONS | | | MIN | MAX | UNIT |
|------------|---------------------------------------|--------------------------------------|---|-----|----------|---------------|
| I_{off} | $V_{CC} = 0$, | BIAS $V_{CC} = 0$, | V_I or $V_O = 0\text{ to }5.5\text{ V}$ | | 10 | μA |
| I_{OZPU} | $V_{CC} = 0\text{ to }1.5\text{ V}$, | $V_O = 0.5\text{ V to }3\text{ V}$, | $\overline{OE} = 0$ | | ± 30 | μA |
| I_{OZPD} | $V_{CC} = 1.5\text{ V to }0$, | $V_O = 0.5\text{ V to }3\text{ V}$, | $\overline{OE} = 0$ | | ± 30 | μA |

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Live-Insertion Specifications for B Port

over recommended operating free-air temperature range

| PARAMETER | TEST CONDITIONS | | | MIN | MAX | UNIT |
|---------------------------|-----------------------------|-----------------------------------|---|----------|------|---------|
| I_{off} | $V_{CC} = 0,$ | BIAS $V_{CC} = 0,$ | V_I or $V_O = 0$ to 1.5 V | 10 | | μA |
| I_{OZPU} | $V_{CC} = 0$ to 1.5 V, | BIAS $V_{CC} = 0,$ | $V_O = 0.5$ V to 1.5 V, $\overline{OE} = 0$ | ± 30 | | μA |
| I_{OZPD} | $V_{CC} = 1.5$ V to 0, | BIAS $V_{CC} = 0,$ | $V_O = 0.5$ V to 1.5 V, $\overline{OE} = 0$ | ± 30 | | μA |
| I_{CC} (BIAS V_{CC}) | $V_{CC} = 0$ to 3.15 V | BIAS $V_{CC} = 3.15$ V to 3.45 V, | V_O (B port) = 0 to 1.5 V | 5 | | mA |
| | $V_{CC} = 3.15$ V to 3.45 V | | | 10 | | μA |
| V_O | $V_{CC} = 0,$ | BIAS $V_{CC} = 3.3$ V, | $I_O = 0$ | 0.95 | 1.05 | V |
| I_O | $V_{CC} = 0,$ | BIAS $V_{CC} = 3.15$ V to 3.45 V, | V_O (B port) = 0.6 V | -1 | | μA |

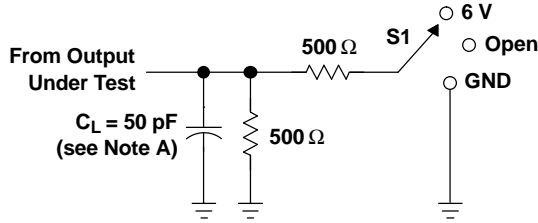
Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature,
 $V_{TT} = 1.5$ V and $V_{REF} = 1$ V for GTLP (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|-----------|-----------------------------------|-------------|-----|--------------------|-----|------|
| t_{PLH} | A | B | 2.1 | | 6.3 | ns |
| t_{PHL} | | | 2.1 | | 6.3 | |
| t_{en} | \overline{OE} | B | 2 | | 6.9 | ns |
| t_{dis} | | | 2 | | 6.9 | |
| t_r | Rise time, B outputs (20% to 80%) | | 2.5 | | | ns |
| t_f | Fall time, B outputs (80% to 20%) | | 2.1 | | | ns |
| t_{PLH} | B | A | 2.1 | | 5.3 | ns |
| t_{PHL} | | | 2.1 | | 5.3 | |
| t_{en} | \overline{OE} | A | 0.3 | | 5.7 | ns |
| t_{dis} | | | 0.3 | | 5.7 | |

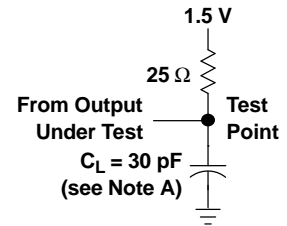
(1) All typical values are at $V_{CC} = 3.3$ V, $T_A = 25^\circ C$.

PARAMETER MEASUREMENT INFORMATION

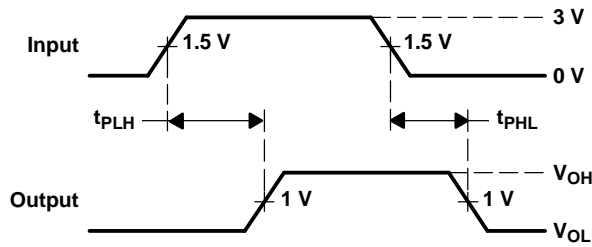


LOAD CIRCUIT FOR A OUTPUTS

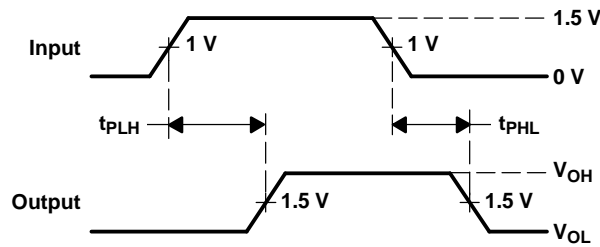
| TEST | S1 |
|-------------------|------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | 6 V |
| t_{PHZ}/t_{PZH} | GND |



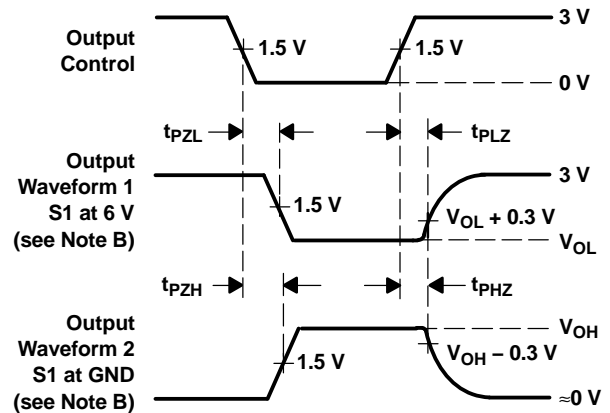
LOAD CIRCUIT FOR B OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(A port to B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to A port)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port)

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR \approx 10 MHz, $Z_O = 50 \Omega$, $t_r \approx 2$ ns, $t_f \approx 2$ ns.
 D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

Distributed-Load Backplane Switching Characteristics

The preceding switching characteristics table shows the switching characteristics of the device into a lumped load (Figure 1). However, the designer's backplane application probably is a distributed load. The physical representation is shown in Figure 2. This backplane, or distributed load, can be approximated closely to a resistor inductance capacitance (RLC) circuit, as shown in Figure 3. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer better understand the performance of the GTLP device in this typical backplane. See www.ti.com/sc/gtlp for more information.

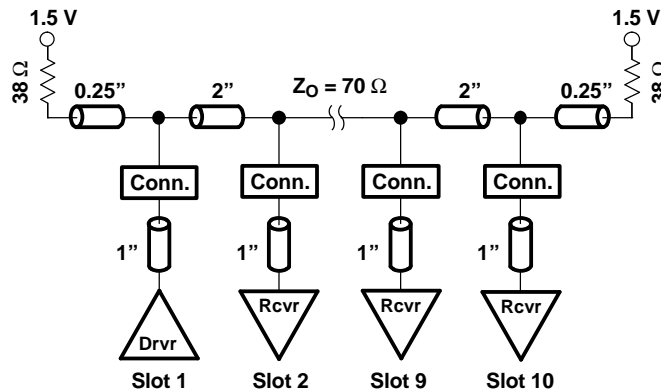


Figure 2. Medium-Drive Test Backplane

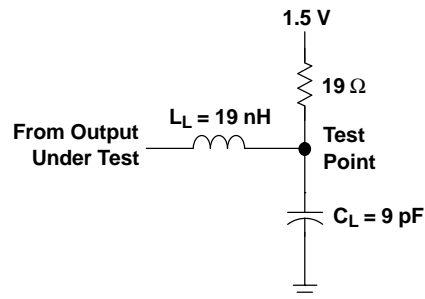


Figure 3. Medium-Drive RLC Network

Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature,
 $V_{TT} = 1.5\text{ V}$ and $V_{REF} = 1\text{ V}$ for GTLP (see Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TYP ⁽¹⁾ | UNIT |
|-----------|-----------------------------------|----------------|--------------------|------|
| t_{PLH} | A | B | 4.3 | ns |
| t_{PHL} | | | 4.3 | |
| t_{en} | \overline{OE} | B | 5 | ns |
| t_{dis} | | | 4.4 | |
| t_r | Rise time, B outputs (20% to 80%) | | 1 | ns |
| t_f | Fall time, B outputs (80% to 20%) | | 2 | ns |

(1) All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$. All values are derived from TI-SPICE models.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|---------|
| SN74GTLPH16945GR | ACTIVE | TSSOP | DGG | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | GTLPH16945 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74GTLPH16945GR | TSSOP | DGG | 48 | 2000 | 330.0 | 24.4 | 8.6 | 13.0 | 1.8 | 12.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74GTLPH16945GR | TSSOP | DGG | 48 | 2000 | 367.0 | 367.0 | 45.0 |

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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