DATA SHEET

SKY13561-670LF: 0.4 to 2.7 GHz SP8T MIPI Diversity Switch

Applications

- 2G/3G/4G multimode cellular handsets (LTE, UMTS, CDMA2000, EDGE, GSM, TDD-LTE, TD-SCDMA)
- Embedded data cards

Features

- High isolation and linearity
- Broadband frequency range: 0.4 to 2.7 GHz
- Integrated MIPI interface
- Small QFN (20-pin, 2.5 x 2.5 x 0.75 mm) package (MSL1, 260 °C per JEDEC J-STD-020)

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04–0074.

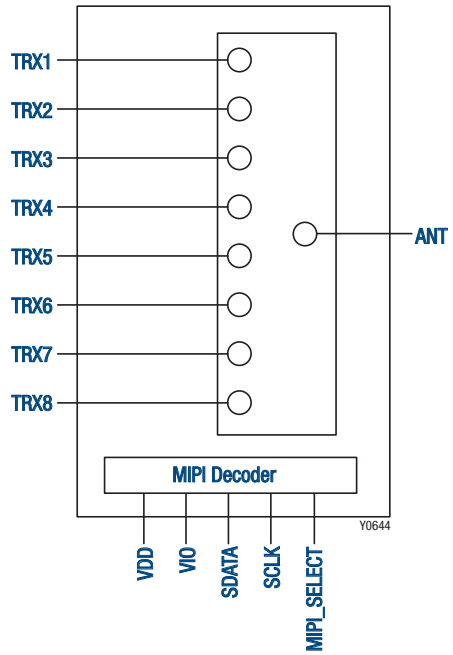


Figure 1. SKY13561-670LF Block Diagram

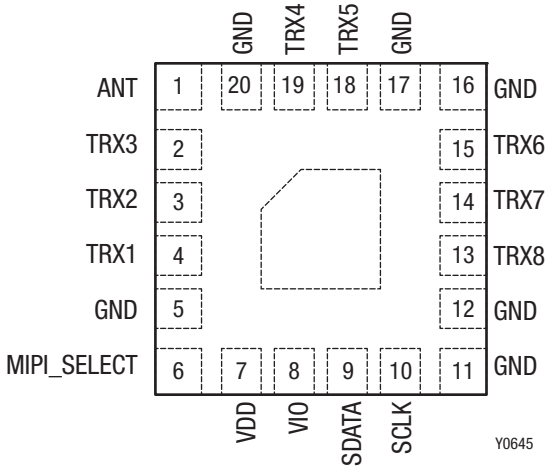


Figure 2. SKY13561-670LF Pinout – 20-Pin QFN (Top View)

Description

The SKY13561-670LF is a single-pole, eight-throw (SP8T) antenna switch with an integrated Mobile Industry Processor Interface (MIPI) controller. Using an advanced switching technology, the SKY13561-670LF maintains low insertion loss and high isolation, which makes it an ideal choice for UMTS, CDMA2000, EDGE, GSM, and LTE applications.

The design features eight linear TRX ports. The switch has an excellent triple beat ratio and 2nd/3rd Order Intermodulation Distortion (IMD2/IMD3) performance.

Switching is controlled by the MIPI decoder. There is an external MIPI select pin that enables how the switch responds to power mode triggers. When this pin is grounded, the switch responds to any of the power mode triggers. When this pin is left open, the switch responds to individual power mode triggers. No external DC blocking capacitors are required on the RF paths as long as no DC voltage is applied.

The SKY13561-670LF is manufactured in a compact, 2.5 x 2.5 x 0.75 mm, 20-pin surface-mount Quad Flat No-Lead (QFN) package. A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

Table 1. SKY13561-670LF Signal Descriptions (Note 1)

Pin	Name	Description	Pin	Name	Description
1	ANT	Antenna port.	11	GND	Ground.
2	TRX3	Transmit/receive port 3. This pin is either connected directly to or is disconnected from pin 1, depending on the applied control data.	12	GND or N/C	Ground or no connection.
3	TRX2	Transmit/receive port 2. This pin is either connected directly to or is disconnected from pin 1, depending on the applied control data.	13	TRX8	Transmit/receive port 8. Can also be used for GSM power level. This pin is either connected directly to or is disconnected from pin 1, depending on the applied control data.
4	TRX1	Transmit/receive port 1. This pin is either connected directly to or is disconnected from pin 1, depending on the applied control data.	14	TRX7	Transmit/receive port 7. This pin is either connected directly to or is disconnected from pin 1, depending on the applied control data.
5	GND	Ground.	15	TRX6	Transmit/receive port 6. This pin is either connected directly to or is disconnected from pin 1, depending on the applied control data.
6	MIPI_SELECT	MIPI interface select. When this pin is grounded, the switch responds to any of the power mode triggers. When this pin is left open, the switch is RFFE MIPI compliant and responds to individual power mode triggers.	16	GND or N/C	Ground or no connection.
7	VDD	DC power supply.	17	GND	Ground.
8	VIO	MIPI decoder enable/reference voltage.	18	TRX5	Transmit/receive port 5, can also be used for GSM power level. This pin is either connected directly to or is disconnected from pin 1, depending on the applied control data.
9	SDATA	Data input/output.	19	TRX4	Transmit/receive port 4, can also be used for GSM power level. This pin is either connected directly to or is disconnected from pin 1, depending on the applied control data.
10	SCLK	Clock signal.	20	GND	Ground.

Note 1: Bottom ground paddles must be connected to ground.

Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY13561-670LF are provided in Table 2. Electrical specifications are provided in Tables 3 and 4.

IMD2 and IMD3 test conditions for various frequencies are listed in Tables 5 and 6, respectively.

Triple Beat Ratio (TBR) test conditions for bands 2 and 5 are listed in Table 7.

Figure 3 illustrates the test setup used to measure intermodulation products. This industry standardized test is used to simulate the WCDMA Band 1 linearity of the antenna switch. A +20 dBm Continuous Wave (CW) signal, f_{FUND}, is sequentially applied to all TRX ports, while a –15 dBm CW blocker signal, f_{BLK}, is applied to the ANT port.

The resulting 3rd Order Intermodulation Distortion (IMD3), f_{RX}, is measured over all phases of f_{FUND}. The SKY13561-670LF exhibits exceptional performance for all TRXx ports.

Figures 4 and 5 provide the timing diagrams for register write commands and read commands, respectively.

Table 8 provides the insertion loss and return loss matrix. Table 9 shows the isolation matrix for ANT to OFF arms. Table 10 shows the isolation matrix for ON to OFF arms.

Table 11 describes the register content and programming read/write sequences. Refer to the *MIPI Alliance Specification for RF Front-End Control Interface (RFFE)*, v1.10 (26 July 2011) for additional information on MIPI programming sequences and MIPI bus specifications.

Table 12 provides the Register_0 logic.Table 13 describes the register parameters and bit values.

Table 2. SKY13561-670LF Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Minimum	Maximum	Units
Supply voltage	V_{DD}	2.5	5.0	V
MIPI decoder enable/reference voltage	VIO		2	V
Clock signal voltage	SCLK		VIO	V
Data signal voltage	SDATA		VIO	V
RF input power: TRX4 TRX5, TRX8 Other TRXx arms	P_{IN}		 +36 +34 +31	 dBm dBm dBm
Storage temperature	T_{STG}	–55	+150	°C
Operating temperature	T_{OP}	–30	+90	°C

Note 1: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

***CAUTION**: Although this device is designed to be as robust as possible, electrostatic discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.*

Table 3. SKY13561-670LF DC Electrical Specifications (Note 1)
(V_{DD} = 2.85 V, T_{OP} = +25 °C, Characteristic Impedance [Z_0] = 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Supply voltage	V_{DD}		2.50	2.85	4.8	V
Supply current, active mode	I_{DD}			45	80	µA
Interface supply voltage	VIO		1.65	1.80	1.95	V
Interface signal: High Low	SDATA		 0.8 × VIO		 0.2 × VIO	 V V
Control current: High Low					 10 5	 µA µA

Note 1: Performance is guaranteed only under the conditions listed in this table.

Table 4. SKY13561-670LF RF Electrical Specifications (1 of 2) (Note 1)
(V_{DD} = 2.85 V, T_{OP} = +25 °C, Characteristic Impedance [Z_0] = 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Operating frequency	f		0.4		2.7	GHz
Insertion loss	IL	TRX1-3 and 6-7: Up to 960 MHz 1710 to 1980 MHz 1980 to 2690 MHz TRX 4, 5, and 8: Up to 960 MHz 1710 to 1980 MHz 1980 to 2690 MHz	 	 0.65 0.7 0.95 0.5 0.65 0.7	 0.8 0.9 1.15 0.7 0.8 0.9	 dB dB dB dB dB dB
Antenna to any off TRXx port	Iso	Up to 960 MHz 1710 to 1980 MHz 1980 to 2690 MHz	32 22 19	35 25 22.5		dB dB dB
Return loss	RL	Up to 2.7 GHz: TRX1 to 3 TRX4 to 8	 11 16	 15 21		 dB dB
Large signal harmonic	2fo, 3fo	fo = 710 to 915 MHz All TRXx: P_{IN} = +27 dBm, VSWR = 1:1 P_{IN} = +27 dBm, VSWR = 5:1		 –60 –55	 –50 –45	 dBm dBm
		fo = 1710 to 1980 MHz All TRXx: P_{IN} = +27 dBm, VSWR = 1:1 P_{IN} = +27 dBm, VSWR = 5:1		 –65 –55	 –55 –48	 dBm dBm
		fo = 1980 to 2690 MHz All TRXx: P_{IN} = +27 dBm, VSWR = 1:1 P_{IN} = +27 dBm, VSWR = 5:1		 –62 –54	 –52 –45	 dBm dBm

Table 4. SKY13561-670LF RF Electrical Specifications (2 of 2) (Note 1)
(V_{DD} = 2.85 V, T_{OP} = +25 °C, Characteristic Impedance [Z_0] = 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
2nd Order Intermodulation Distortion	IMD2	See test conditions in Table 5		–110	–100	dBm
3rd Order Intermodulation Distortion	IMD3	See test conditions in Table 6		–110	–100	dBm
Triple Beat Ratio	TBR	See test conditions in Table 7	+51	+81		dBc
Turn-on time	t_{ON}	From application of V_{DD} and VIO			20	µs
Switching speed	t_S	Port to port		2	5	µs

Note 1: Performance is guaranteed only under the conditions listed in this table.

Table 5. IMD2 Test Conditions

Band	Transmit Frequency (MHz)	Transmit Power (dBm)	Frequency Blocker, Low (MHz)	Frequency Blocker, High (MHz)	Power Blocker (dBm)	Receive Frequency (MHz)
1 (IMT)	1950.0	+20	190	4090	–15	2140.0
2 (PCS)	1880.0		80	3840		1960.0
4 (DCS)	1732.0		400	3864		2132.0
5 (US Cell)	836.5		45	1718		881.5
7 (2600)	2535.0		120	5190		2655.0
8 (900)	897.0		45	1839		942.0

Table 6. IMD3 Test Conditions

Band	Transmit Frequency (MHz)	Transmit Power (dBm)	Frequency Blocker (MHz)	Power Blocker (dBm)	Receive Frequency (MHz)
1 (IMT)	1950.0	+20	1760.0	–15	2140.0
2 (PCS)	1880.0		1800.0		1960.0
4 (DCS)	1732.0		1332.0		2132.0
5 (US Cell)	836.5		791.5		881.5
7 (2600)	2535.0		2415.0		2655.0
8 (900)	897.0		852.0		942.0

Table 7. Triple Beat Ratio Test Conditions

Band	Transmit Frequency 1 (MHz)	Transmit Power 1 (dBm)	Transmit Frequency 2 (MHz)	Transmit Power 2 (dBm)	Frequency Blocker @ ANT (MHz)	Power Blocker (dBm)	TBR Product Frequency (MHz)
2	1880.0	+21.5	1881.0	+21.5	1960.0	–30	1960.0 ±1
5	836.5		837.5		881.5		881.5 ±1

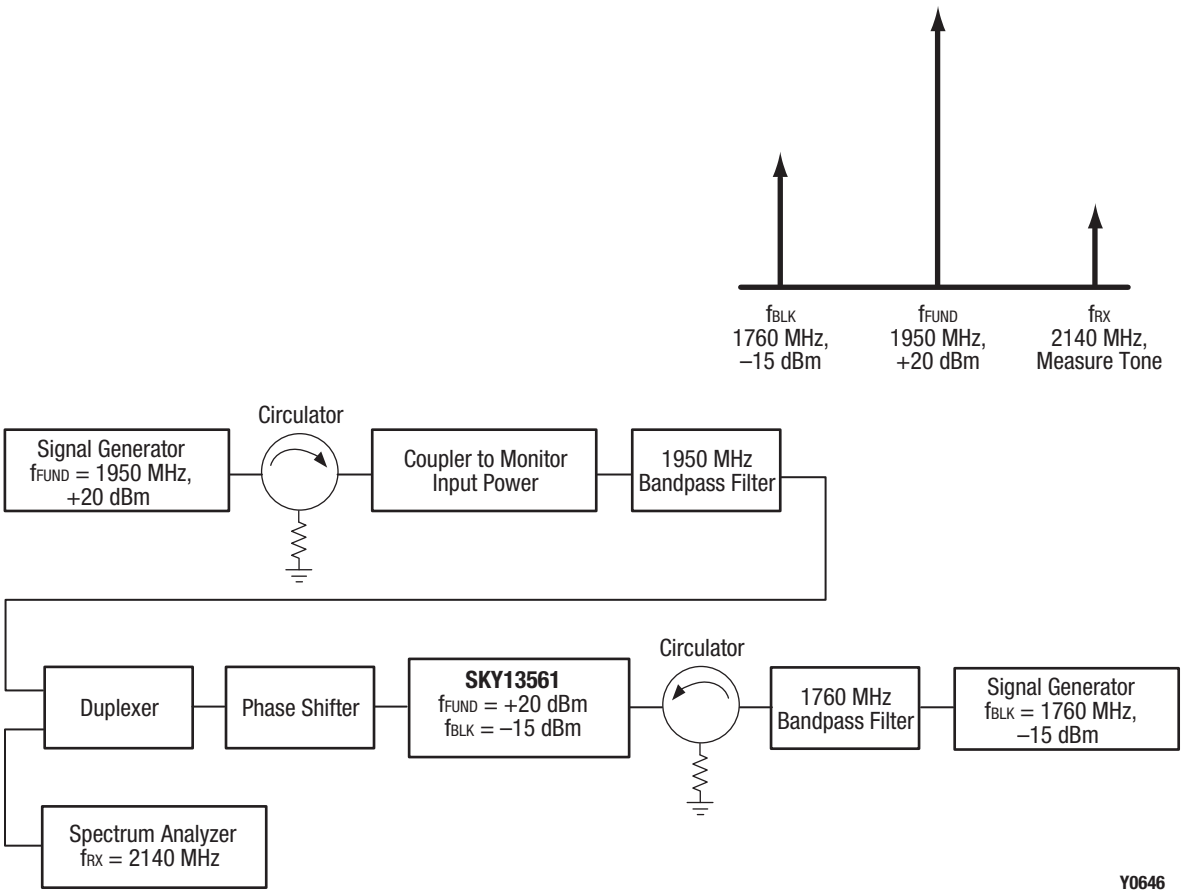


Figure 3. 3rd Order Intermodulation Test Setup

Table 8. Insertion Loss and Return Loss Matrix

On Throw	Frequency (GHz)	IL (dB)	RL_Pole (dB)	RL_Throw (dB)
TRX01	0.96	–0.62	–20	–20
TRX01	1.96	–0.65	–20	–21
TRX01	2.69	–0.82	–17	–20
TRX02	0.96	–0.63	–19	–19
TRX02	1.96	–0.65	–19	–19
TRX02	2.69	–0.85	–16	–18
TRX03	0.96	–0.64	–18	–18
TRX03	1.96	–0.67	–18	–18
TRX03	2.69	–0.95	–14	–15
TRX04	0.96	–0.46	–21	–20
TRX04	1.96	–0.47	–21	–21
TRX04	2.69	–0.52	–24	–22
TRX05	0.96	–0.50	–21	–21
TRX05	1.96	–0.50	–22	–21
TRX05	2.69	–0.55	–26	–21
TRX06	0.96	–0.59	–21	–22
TRX06	1.96	–0.62	–22	–22
TRX06	2.69	–0.70	–23	–22
TRX07	0.96	–0.58	–21	–21
TRX07	1.96	–0.61	–22	–22
TRX07	2.69	–0.69	–23	–22
TRX08	0.96	–0.51	–23	–24
TRX08	1.96	–0.56	–24	–22
TRX08	2.69	–0.61	–21	–18

Table 9. Isolation Matrix ANT to OFF Arms

ANT\OFF ARM	Frequency (GHz)	TRX01	TRX02	TRX03	TRX04	TRX05	TRX06	TRX07	TRX08
ANT	0.96		–45	–39	–52	–45	–51	–52	–42
ANT	1.96		–41	–36	–49	–42	–49	–50	–40
ANT	2.69		–28	–26	–43	–35	–41	–43	–32
ANT	0.96	–48		–44	–51	–46	–52	–52	–42
ANT	1.96	–44		–39	–49	–43	–49	–50	–40
ANT	2.69	–31		–25	–43	–35	–42	–43	–32
ANT	0.96	–51	–49		–50	–47	–52	–53	–42
ANT	1.96	–47	–44		–48	–44	–49	–50	–40
ANT	2.69	–34	–29		–41	–35	–42	–43	–32
ANT	0.96	–47	–43	–39		–54	–58	–56	–43
ANT	1.96	–44	–40	–36		–50	–55	–53	–40
ANT	2.69	–37	–33	–28		–36	–46	–46	–33
ANT	0.96	–46	–42	–38	–46		–59	–66	–43
ANT	1.96	–43	–39	–35	–42		–55	–63	–40
ANT	2.69	–36	–32	–28	–33		–43	–48	–33
ANT	0.96	–45	–41	–37	–58	–44		–40	–44
ANT	1.96	–42	–38	–34	–55	–41		–36	–42
ANT	2.69	–36	–32	–28	–44	–34		–29	–34
ANT	0.96	–45	–41	–37	–55	–44	–45		–43
ANT	1.96	–42	–38	–34	–53	–42	–42		–42
ANT	2.69	–36	–32	–28	–44	–34	–32		–35
ANT	0.96	–45	–41	–37	–54	–45	–50	–40	
ANT	1.96	–42	–38	–34	–52	–42	–47	–38	
ANT	2.69	–36	–32	–28	–42	–35	–38	–30	

Table 10. Isolation Matrix ON Arms to OFF Arms

ANT\OFF ARM	Frequency (GHz)	TRX01	TRX02	TRX03	TRX04	TRX05	TRX06	TRX07	TRX08
TRX01	0.96		–34	–47	–43	–55	–58	–56	–43
TRX01	1.96		–26	–34	–35	–45	–50	–49	–36
TRX01	2.69		–23	–30	–33	–41	–46	–46	–33
TRX02	0.96	–35		–36	–43	–54	–58	–56	–43
TRX02	1.96	–27		–26	–35	–44	–49	–48	–36
TRX02	2.69	–24		–23	–33	–41	–46	–46	–33
TRX03	0.96	–41	–37		–43	–52	–56	–56	–43
TRX03	1.96	–33	–28		–35	–42	–48	–48	–36
TRX03	2.69	–30	–25		–33	–39	–45	–45	–33
TRX04	0.96	–58	–50	–47		–38	–51	–53	–43
TRX04	1.96	–45	–40	–36		–30	–43	–45	–35
TRX04	2.69	–42	–37	–33		–28	–41	–43	–33
TRX05	0.96	–54	–47	–44	–35		–45	–49	–43
TRX05	1.96	–44	–38	–35	–27		–37	–41	–35
TRX05	2.69	–41	–36	–33	–25		–36	–39	–32
TRX06	0.96	–53	–46	–43	–41	–56		–32	–40
TRX06	1.96	–43	–37	–34	–33	–45		–25	–33
TRX06	2.69	–41	–36	–32	–31	–41		–23	–30
TRX07	0.96	–53	–46	–42	–42	–57	–34		–35
TRX07	1.96	–43	–37	–34	–34	–46	–27		–28
TRX07	2.69	–41	–36	–32	–32	–42	–25		–26
TRX08	0.96	–53	–46	–42	–42	–57	–42	–35	
TRX08	1.96	–43	–37	–34	–34	–46	–35	–28	
TRX08	2.69	–41	–35	–32	–32	–42	–33	–26	

Table 11. Command Sequence Bit Definitions

Type	SSC	C11-C8	C7	C6-C5	C4	C3-C0	Parity Bits	BPC	Extended Operation					
									DA7(1)-DA0(1)	Parity Bits	BPC	DA7(n)-DA0(n)	Parity Bits	BPC
Reg0 Write	Y	SA[3:0]	1	Data[6:5]	Data[4]	Data{3:0]	Y	Y	–	–	–	–	–	–
Reg Write	Y	SA[3:0]	0	10	Addr[4]	Addr[3:0]	Y	–	Data[7:0]	–	–	–	Y	Y
Reg Read	Y	SA[3:0]	0	11	Addr[4]	Addr[3:0]	Y	Y	Data[7:0]	–	–	–	Y	Y

Legend:
SSC = Sequence start command
C = Command frame bits
DA = Data/address frame bits
BPC = Bus park cycle
BC = Byte count (# of consecutive addresses)

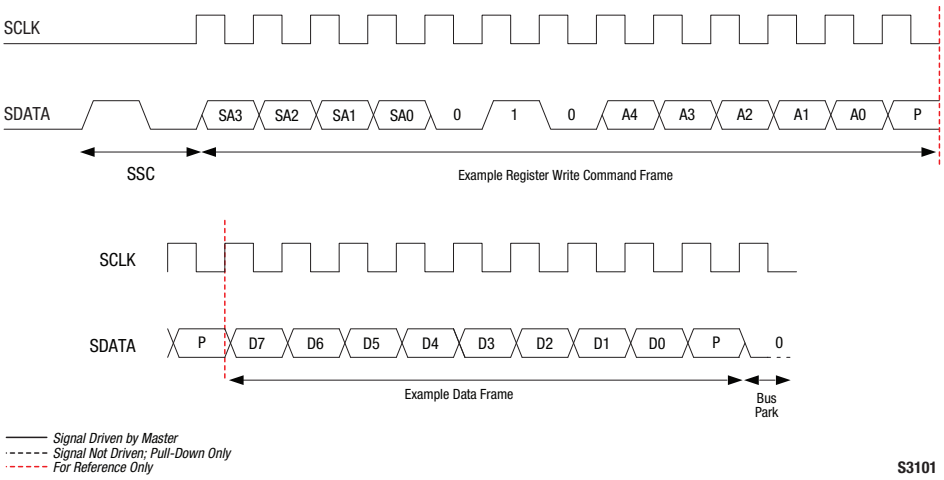


Figure 4. Register Write Command Timing Diagram

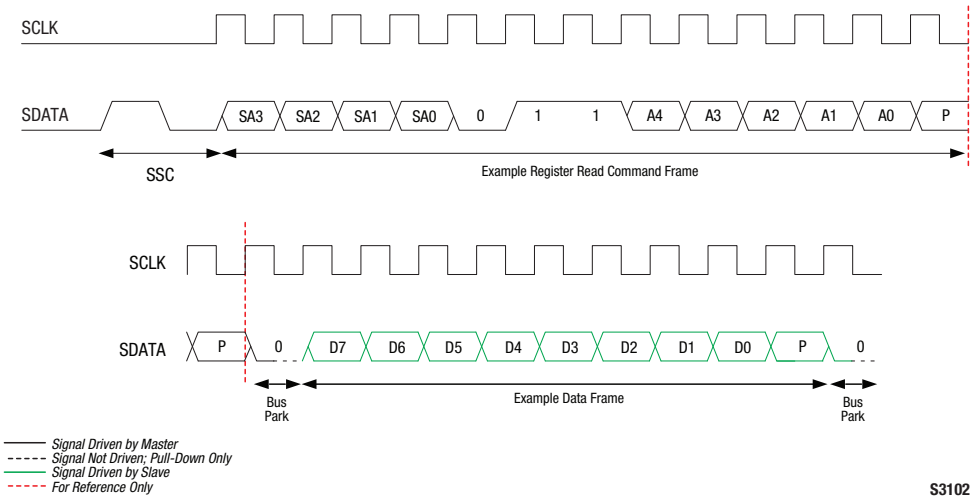


Figure 5. Register Read Command Timing Diagram

Table 12. Register_0 Truth Table

Antenna Path	Register_0 Bits							
	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Sleep mode (standby)	X	0	0	0	0	0	0	0
TRX1	X	0	0	0	0	1	1	1
TRX2	X	0	0	0	1	0	0	1
TRX3	X	0	0	0	1	0	1	1
TRX4	X	0	0	0	1	0	1	0
TRX5	X	0	0	0	1	0	0	0
TRX6	X	0	0	0	0	0	0	1
TRX7	X	0	0	0	0	0	1	0
TRX8	X	0	0	0	0	0	1	1
Isolation mode (warm-up)	X	1	1	1	1	1	1	1

Table 13. Register Description and Programming (1 of 3)

Register		Parameter	Description	Default (Binary)
Name	Address (Hex)			
Register_0	0000	MODE_CTRL	Bits[7:0]: Switch control. See Table 8 for logic	–
RFFE_STATUS	001A	SOFTWARE RESET	Bit[7]: Resets all data to default values except for USID, GSID, or the contents of the PM_TRIG Register. 0 = Normal operation 1 = Software reset	0
		COMMAND_FRAME_PARITY_ERR	Bit[6]: Command sequence received with parity error – discard command.	0
		COMMAND_LENGTH_ERR	Bit[5]: Command length error.	0
		ADDRESS_FRAME_PARITY_ERR	Bit[4]: Address frame parity error =1.	0
		DATA_FRAME_PARITY_ERR	Bit[3]: Data frame with parity error.	0
		READ_UNUSED_REG	Bit[2]: Read command to an invalid address.	0
		WRITE_UNUSED_REG	Bit[1]: Write command to an invalid address.	0
		BID_GID_ERR	Bit[0]: Read command with a BROADCAST_ID (refer to the *MIPI Alliance Specification*) or GSID.	0

Table 13. Register Description and Programming (2 of 3)

Register		Parameter	Description	Default (Binary)
Name	Address (Hex)			
GROUP_SID	001B	Reserved	Bits[7:4]: Reserved	0000
		GSID	Bits[3:0]: Group slave ID	0000
PM_TRIG (Note 1)	001C	PWR_MODE	Bits[7:6]: 00 = Normal operation (active) 01 = Default settings (startup) 10 = Low power (low power) 11 = Reserved	00
		Trigger_Mask_2	Bit[5]: If this bit is set, trigger 2 is disabled. When all triggers are disabled, if writing to a register that is associated with trigger 2, the data goes directly to the destination register.	0
		Trigger_Mask_1	Bit[4]: If this bit is set, trigger 1 is disabled. When all triggers are disabled, if writing to a register that is associated with trigger 1, the data goes directly to the destination register.	0
		Trigger_Mask_0	Bit[3]: If this bit is set, trigger 0 is disabled. When all triggers are disabled, if writing to a register that is associated with trigger 0, the data goes directly to the destination register.	0
		Trigger_2	Bit[2]: If this bit is set, data is loaded into the trigger 2 registers.	0
		Trigger_1	Bit[1]: If this bit is set, data is loaded into the trigger 1 registers (unsupported).	0
		Trigger_0	Bit[0]: If this bit is set, data is loaded into the trigger 0 registers (unsupported).	0
PRODUCT_ID	001D	PRODUCT_ID	Bits[7:0]: This is a read-only register. However, during the programming of the Unique Slave Identifier (USID), a write command sequence is performed on this register but the value is not changed.	01011111

Table 13. Register Description and Programming (3 of 3)

Register		Parameter	Description	Default (Binary)
Name	Address (Hex)			
MANUFACTURER_ID	001E	MANUFACTURER_ID	Bits[7:0]: Read-only register	10100101
MAN_USID	001F	Reserved	Bits[7:6]: Reserved	00
		MANUFACTURER_ID	Bits[5:4]: Read-only register	01
		USID	Bits[3:0]: Programmable USID. A write to these bits programs the USID.	1010

Note 1: Unlike the complete independence between triggers 0, 1, and 2, and also between the associated trigger masks 0, 1, and 2, respectively, as described in the MIPI RFFE Specification, this device uses additional interactions between the provided trigger functions.

The delayed application of updated data to all triggerable registers in this device may be accomplished using any of the three triggers (0, 1, or 2), provided that the particular trigger used is not currently masked off. If multiple triggers are enabled, any or all of those are sufficient to cause the data to be transferred from shadow registers to destination registers for all triggerable registers in the device.

It is also necessary to disable all three triggers (i.e., set all three trigger masks) to ensure that data written to any triggerable register will immediately be written to the destination register at the conclusion of the RFFE command sequence where the data is written.

Evaluation Board Description

The SKY13561-670LF Evaluation Board is used to test the performance of the SKY13561-670LF SP8T Switch. An Evaluation Board schematic diagram is provided in Figure 6. A recommended ESD protection circuit diagram is provided in Figure 7. An assembly drawing for the Evaluation Board is shown in Figure 8.

Package Dimensions

The PCB layout footprint for the SKY13561-670LF is provided in Figure 9. Typical case markings are shown in Figure 10. Package dimensions for the 20-pin QFN are shown in Figure 11, and tape and reel dimensions are provided in Figure 12.

Package and Handling Information

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY13561-670LF is rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *Solder Reflow Information*, document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

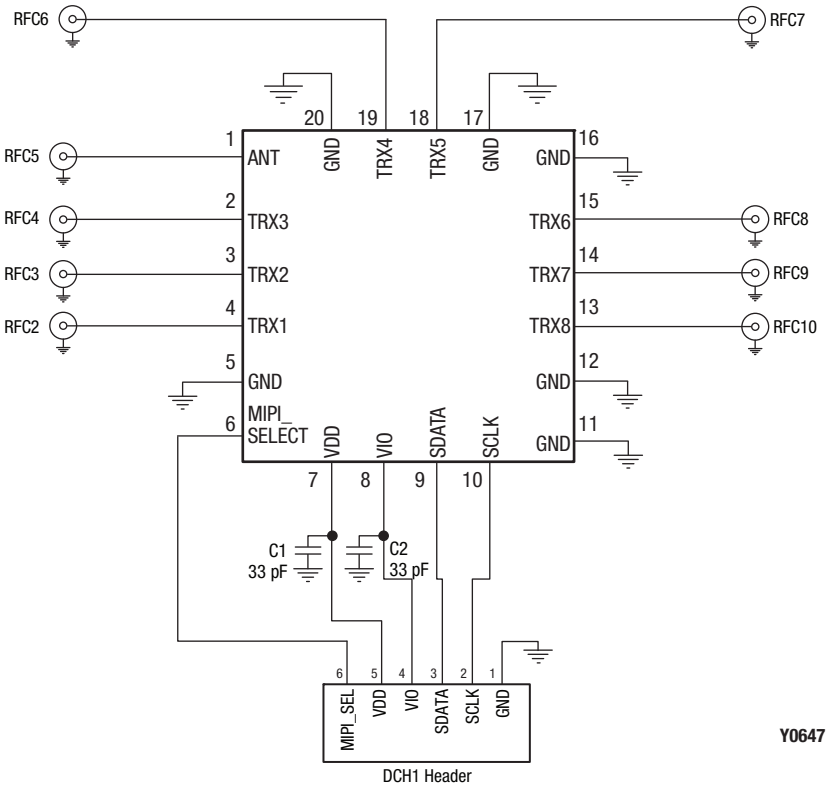


Figure 6. SKY13561-670LF Evaluation Board Schematic

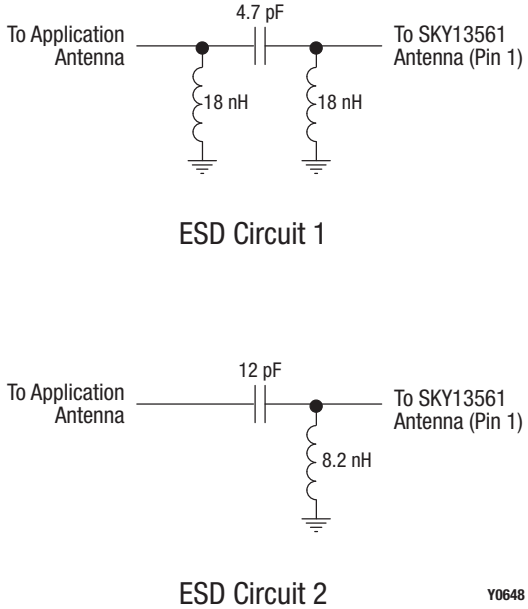


Figure 7. SKY13561-670LF Recommended ESD Protection Circuits

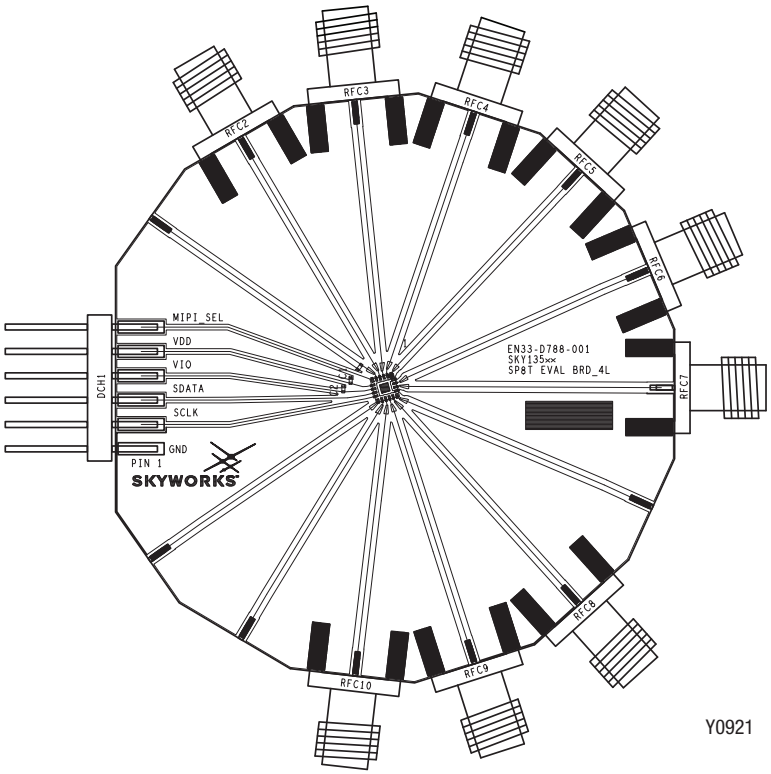


Figure 8. SKY13561-670LF Evaluation Board Assembly Diagram

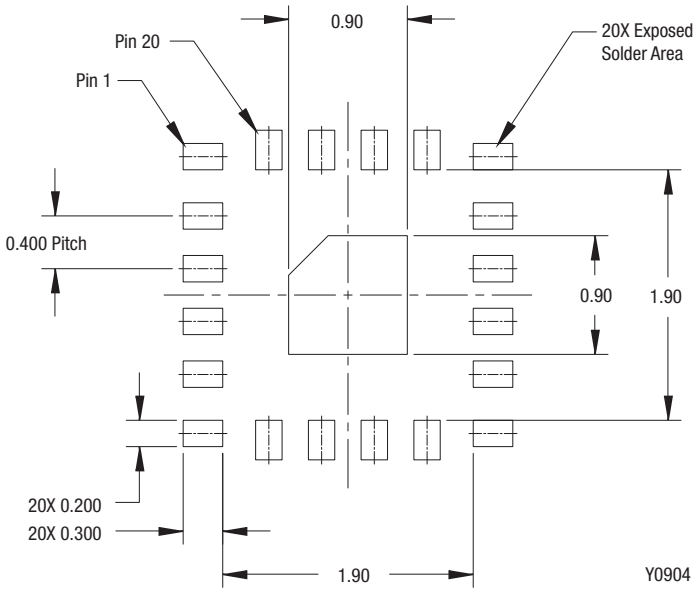


Figure 9. SKY13561-670LF PCB Layout Footprint
(Top View)

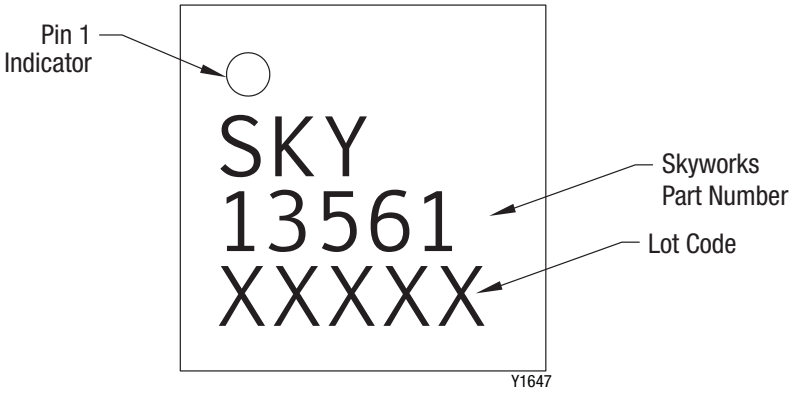
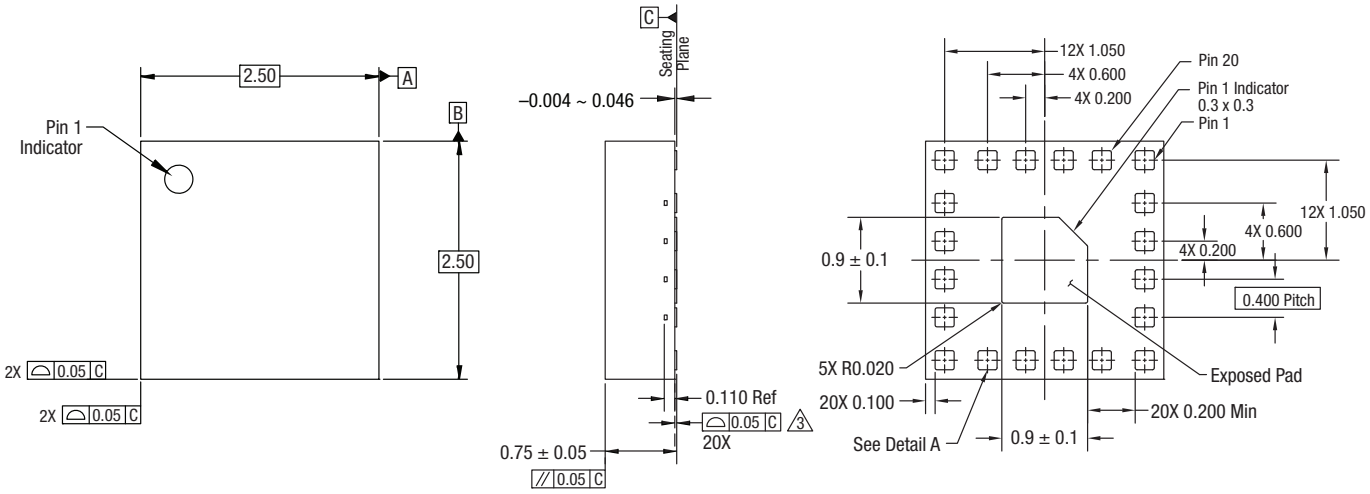
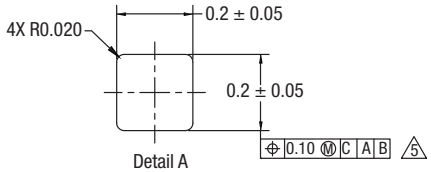


Figure 10. Typical Part Markings (Top View)



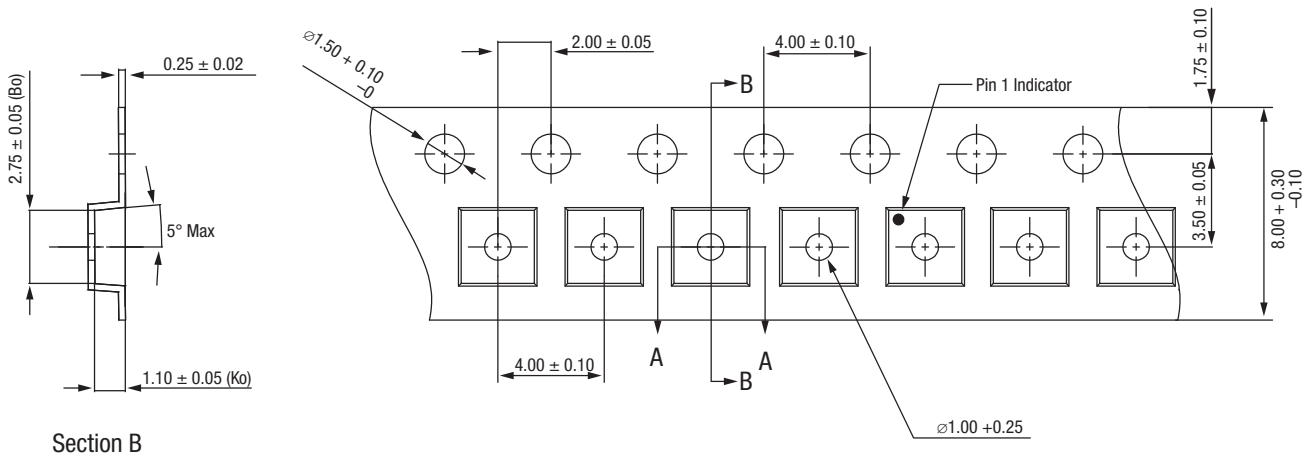
Notes:

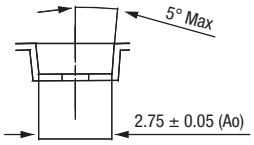
1. *Dimensions and tolerances according to ASME Y14.5M-1994.*
2. *All measurements are in millimeters.*
3. *Coplanarity applies to the terminals and all other bottom surface metallization.*
4. *Plating requirement per source control drawing 2504.*
5. *Dimension applies to metallized terminal. If the terminal has a radius on its end, the width dimension should not be measured in that radius area.*



Y0900

Figure 11. SKY13561-670LF 20-Pin QFN Package Dimensions





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Notes:

1. *Carrier tape: black conductive polycarbonate or polystyrene.*
2. *Cover tape material: transparent conductive.*
3. *ESD-surface resistivity shall be ≤ 1 x 10^{10} Ω/square per EIA, JEDEC TNR Specification.*
4. *10-sprocket hole pitch cumulative tolerance: ±0.20 mm.*
5. *Ao and Bo measurement point to be 0.30 mm from bottom pocket.*
6. *All dimensions are in millimeters.*

Figure 12. SKY13561-670LF Tape and Reel Dimensions

Ordering Information

Model Name	Manufacturing Part Number	Evaluation Board Part Number
SKY13561-670LF: 0.4 to 2.7 GHz SP8T Diversity Switch with MIPI Interface	SKY13561-670LF	EN33-D788-001