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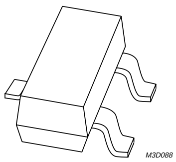


SI2304DS

N-channel enhancement mode field-effect transistor

Rev. 01 — 17 August 2001 **Product data**

1. Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™[1] technology

Product availability:

SI2304DS in SOT23.

2. Features

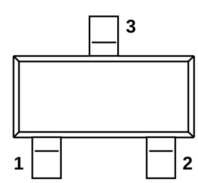
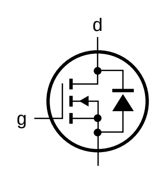
- TrenchMOS™ technology
- Very fast switching
- Subminiature surface mount package.

3. Applications

- Battery management
- High speed switch
- Low power DC to DC converter.

4. Pinning information

Table 1: Pinning - SOT23, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)	 **SOT23**	
2	source (s)		
3	drain (d)		

1. TrenchMOS is a trademark of Koninklijke Philips Electronics N.V.

5. Quick reference data

Table 2: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage (DC)	T_j = 25 to 150 °C	–	–	30	V
I_D	drain current (DC)	T_{sp} = 25 °C; V_{GS} = 5 V	–	–	1.7	A
P_{tot}	total power dissipation	T_{sp} = 25 °C	–	–	0.83	W
T_j	junction temperature		–	–	150	°C
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 500 mA	–	–	117	mΩ
		V_{GS} = 4.5 V; I_D = 500 mA	–	–	190	mΩ

6. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	T_j = 25 to 150 °C	–	30	V
V_{DGR}	drain-gate voltage (DC)	T_j = 25 to 150 °C; R_{GS} = 20 kΩ	–	30	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_{sp} = 25 °C; V_{GS} = 5 V; Figure 2 and 3	–	1.7	A
		T_{sp} = 100 °C; V_{GS} = 5 V; Figure 2 and 3	–	1.1	A
I_{DM}	peak drain current	T_{sp} = 25 °C; pulsed; $t_p \leq 10$ µs	–	7.5	A
P_{tot}	total power dissipation	T_{sp} = 25 °C; Figure 1	–	0.83	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–65	+150	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	T_{sp} = 25 °C	–	0.83	A
I_{SM}	peak source (diode forward) current	T_{sp} = 25 °C; pulsed; $t_p \leq 10$ µs	–	3.3	A

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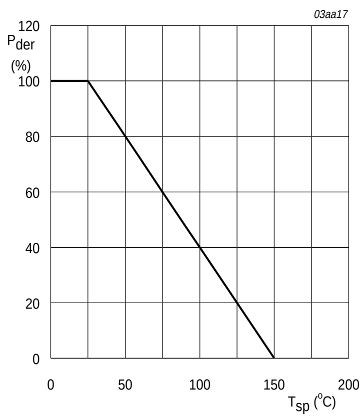
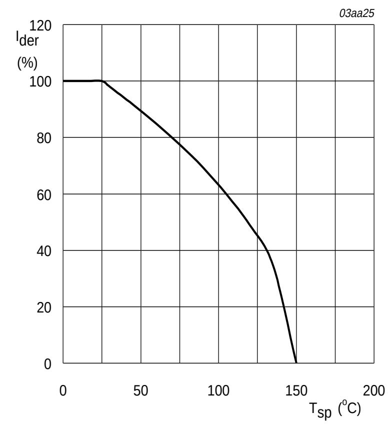


$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

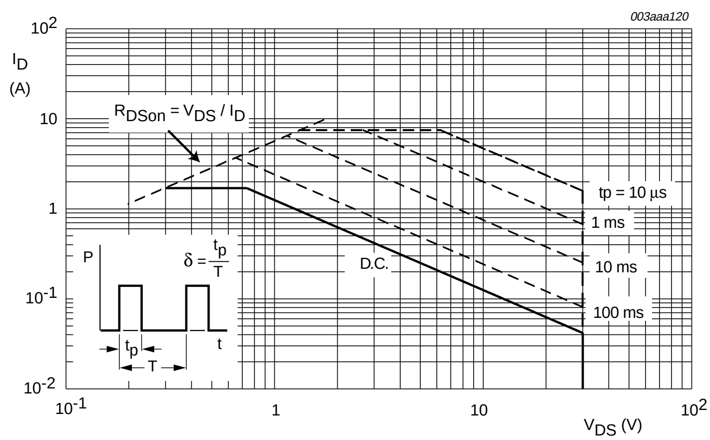
Fig 1. Normalized total power dissipation as a function of solder point temperature.



$V_{GS} \geq 10$ V

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature.



$T_{sp} = 25°C$; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

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7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	mounted on a metal clad substrate; Figure 4	100	K/W

7.1 Transient thermal impedance

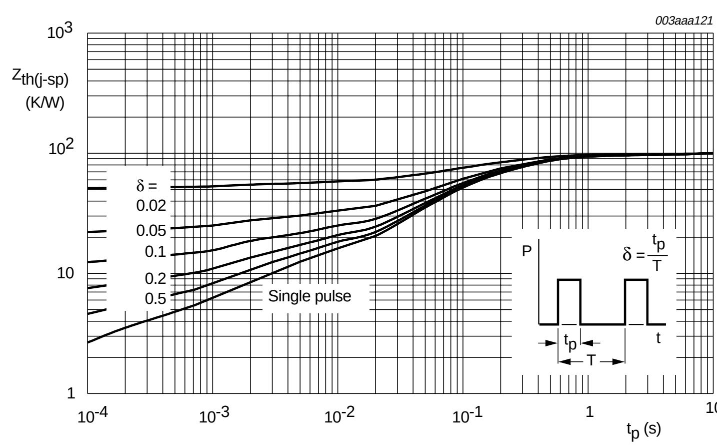

Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration.

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8. Characteristics

Table 5: Characteristics

T_j = 25 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 µA; V_{GS} = 0 V				
		T_j = 25 °C	30	40	–	V
		T_j = –55 °C	27	–	–	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; Figure 9				
		T_j = 25 °C	1.5	2	–	V
		T_j = 150 °C	0.5	–	–	V
		T_j = –55 °C	–	–	2.7	V
I_{DSS}	drain-source leakage current	V_{DS} = 30 V; V_{GS} = 0 V				
		T_j = 25 °C	–	0.01	0.5	µA
		T_j = 150 °C	–	–	10	µA
I_{GSS}	gate-source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	–	10	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 500 mA; Figure 7 and 8				
		T_j = 25 °C	–	–	117	mΩ
		V_{GS} = 4.5 V; I_D = 500 mA				
		T_j = 25 °C	–	–	190	mΩ
		T_j = 150 °C	–	–	300	mΩ
Dynamic characteristics						
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 1 A	1.4	2.5	–	S
$Q_{g(tot)}$	total gate charge	V_{DD} = 15 V; V_{GS} = 10 V; I_D = 0.5 A; Figure 13	–	4.6		nC
Q_{gs}	gate-source charge		–	0.6	–	nC
Q_{gd}	gate-drain (Miller) charge		–	1.35	1.83	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 10 V; f = 1 MHz; Figure 11	–	147	195	pF
C_{oss}	output capacitance		–	65	78	pF
C_{rss}	reverse transfer capacitance		–	41	56	pF
$t_{d(on)}$	turn-on delay time	V_{DD} = 15 V; R_L = 15 Ω; V_{GS} = 10 V	–	4	6	ns
t_r	rise time		–	7.5	12	ns
$t_{d(off)}$	turn-off delay time		–	18	35	ns
t_f	fall time		–	13	19	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	I_S = 0.83 A; V_{GS} = 0 V; Figure 12	–	0.7	1.2	V
t_{rr}	reverse recovery time	I_S = 1 A; dI_S/dt = –100 A/µs; V_{GS} = 0 V; V_{DS} = 25 V	–	69	–	ns

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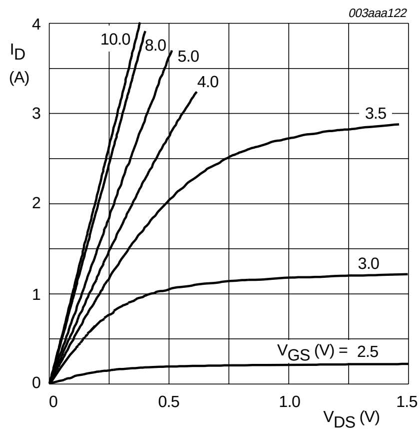
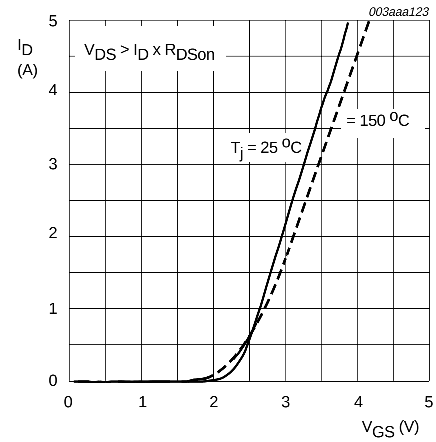


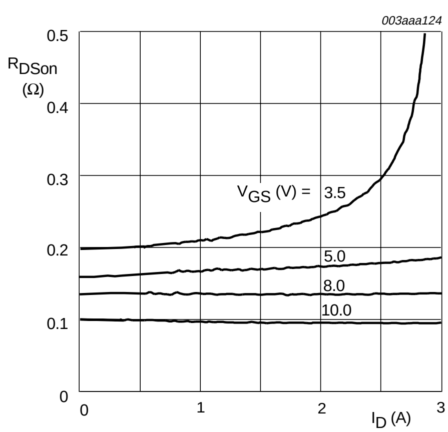
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



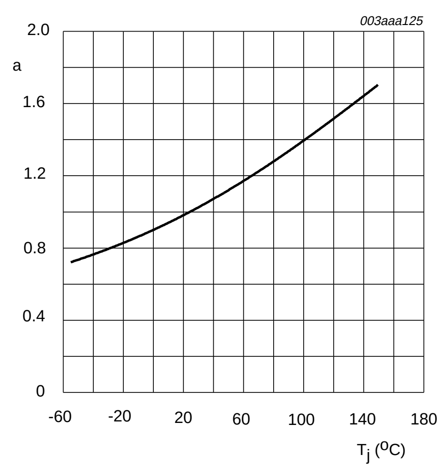
T_j = 25 °C and 175 °C; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



T_j = 25 °C

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 8. Normalized drain source on-state resistance factor as a function of junction temperature.

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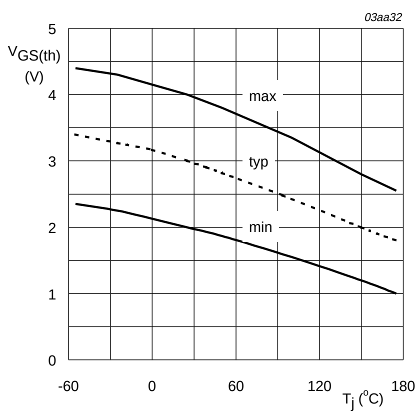
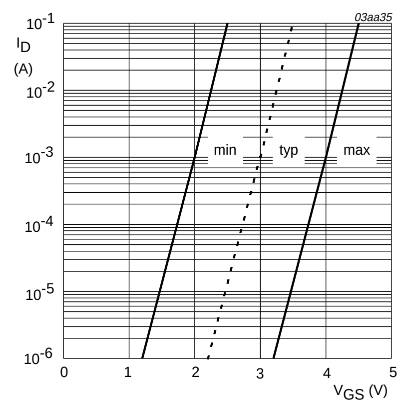


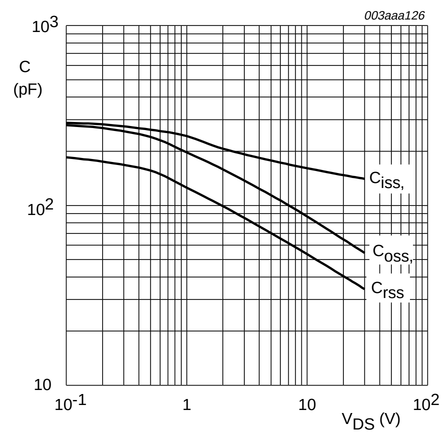
I_D = 1 mA; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



T_j = 25 °C; V_{DS} = 5 V

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



V_{GS} = 0 V; f = 1 MHz

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.

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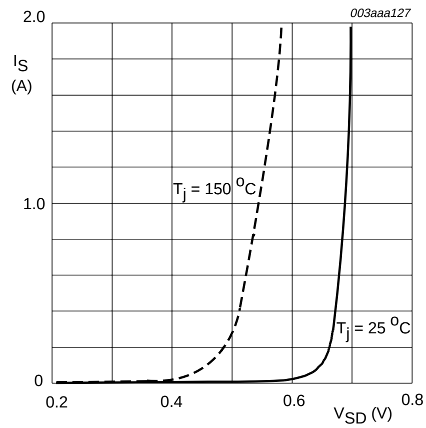
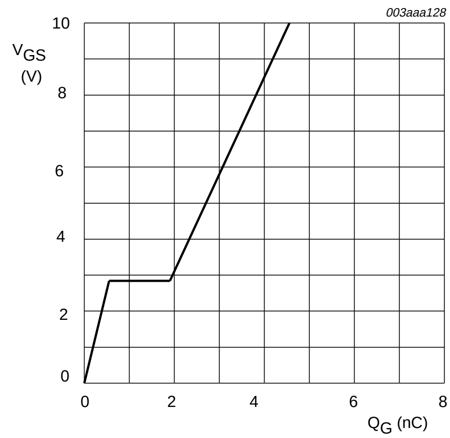


T_j = 25 °C and 150 °C; V_{GS} = 0 V

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



I_D = 0.5 A; V_{DD} = 15 V

Fig 13. Gate-source voltage as a function of gate charge; typical values.

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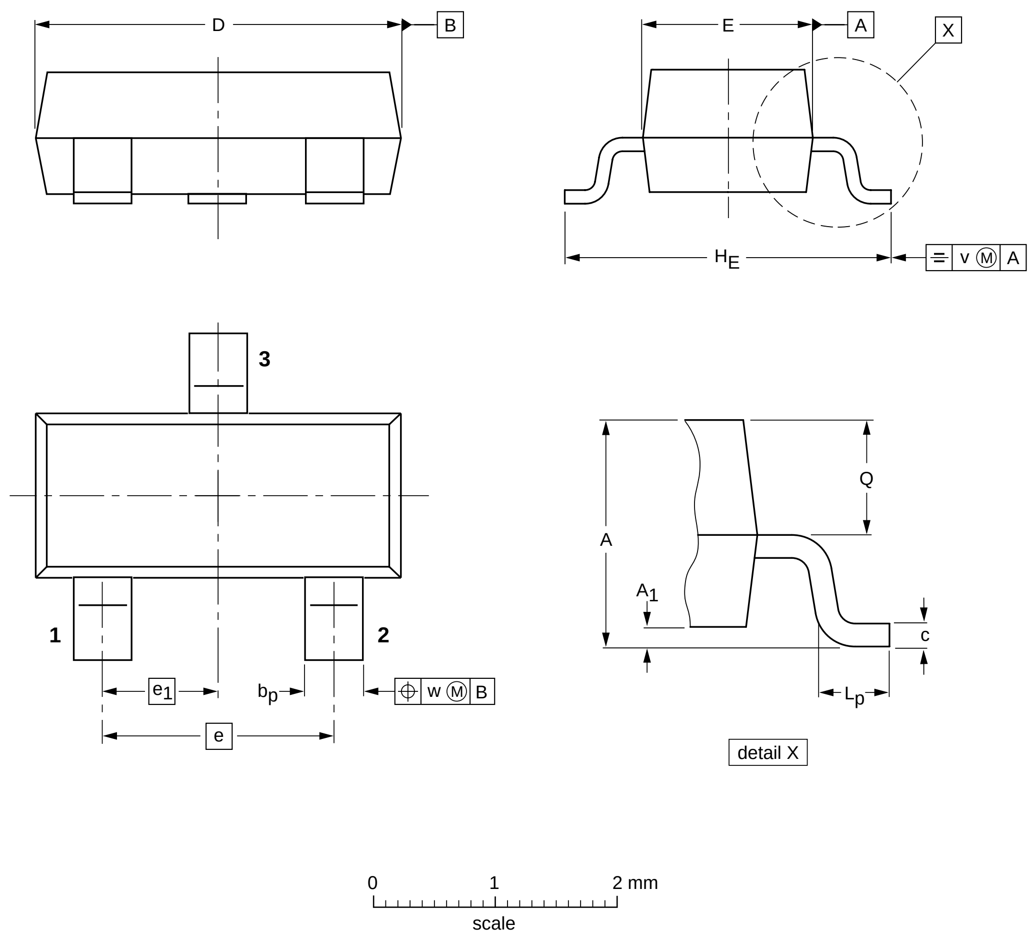
9. Package outline

Plastic surface mounted package; 3 leads **SOT23**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max.	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT23		TO-236AB				~~97-02-28~~ 99-09-13

Fig 14. SOT23.

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10. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
01	20010817	-	Product data; initial version

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11. Data sheet status

Data sheet status[1]	Product status[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

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