Rev.1.7_00

This IC, developed by CMOS technology, is a high-accuracy Hall effect latch IC that operates with high temperature and high-withstand voltage.

The output voltage changes when this IC detects the intensity level of magnetic flux density and a polarity change. Using this IC with a magnet makes it possible to detect the rotation status in various devices.

This IC includes a reverse voltage protection circuit and an output current limit circuit.

High-density mounting is possible by using the small SOT-23-3 package.

Due to its high-accuracy magnetic characteristics, this IC can make operation's dispersion in the system combined with magnet smaller.

ABLIC Inc. offers a "magnetic simulation service" that provides the ideal combination of magnets and our Hall effect ICs for customer systems. Our magnetic simulation service will reduce prototype production, development period and development costs. In addition, it will contribute to optimization of parts to realize high cost performance.

For more information regarding our magnetic simulation service, contact our sales office.

**Caution**  **This product can be used in vehicle equipment and in-vehicle equipment. Before using the product in the purpose, contact to ABLIC Inc. is indispensable.**

# ■ Features

- Pole detection: Bipolar latch
- Output logic[1]: $V_{OUT}$ = "L" at S pole detection
  $V_{OUT}$ = "H" at S pole detection
- Output form[1]: Nch open-drain output,
  Nch driver + built-in pull-up resistor
- Magnetic sensitivity[1]: $B_{OP}$ = 3.0 mT typ.
  $B_{OP}$ = 6.0 mT typ.
- Chopping frequency: $f_C$ = 500 kHz typ.
- Output delay time: $t_D$ = 8.0 μs typ.
- Power supply voltage range: $V_{DD}$ = 3.5 V to 26.0 V
- Built-in regulator
- Built-in reverse voltage protection circuit
- Built-in output current limit circuit
- Operation temperature range: Ta = −40°C to +125°C
- Lead-free (Sn 100%), halogen-free
- AEC-Q100 qualified[2]

[1]. The option can be selected.
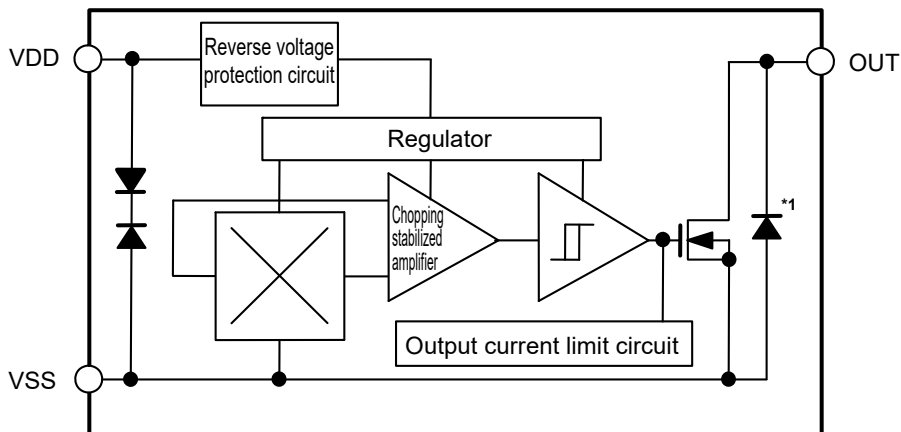[2]. Contact our sales office for details.

# ■ Applications

- Automobile equipment
- Home appliance
- DC brushless motor
- Housing equipment
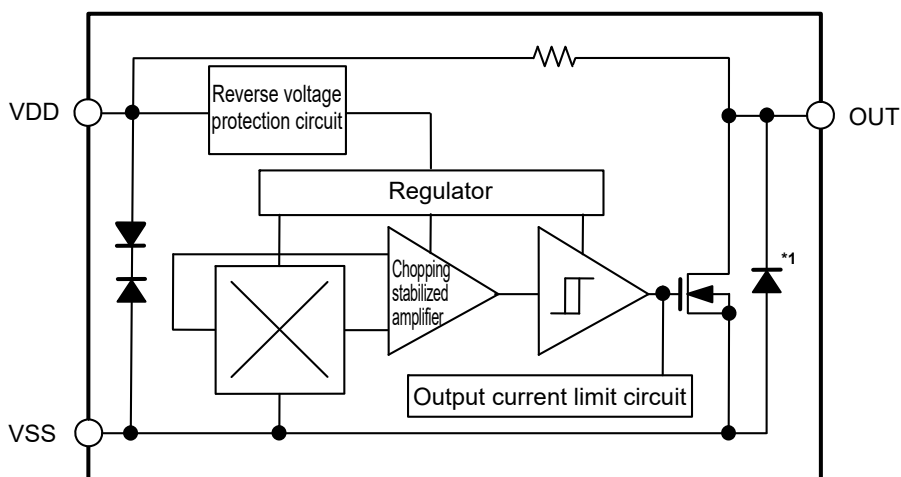- Industrial equipment

# ■ Package

- SOT-23-3

■ **Block Diagrams**

1. **Nch open-drain output product**



**\*1.** Parasitic diode

**Figure 1**

2. **Nch driver + built-in pull-up resistor product**
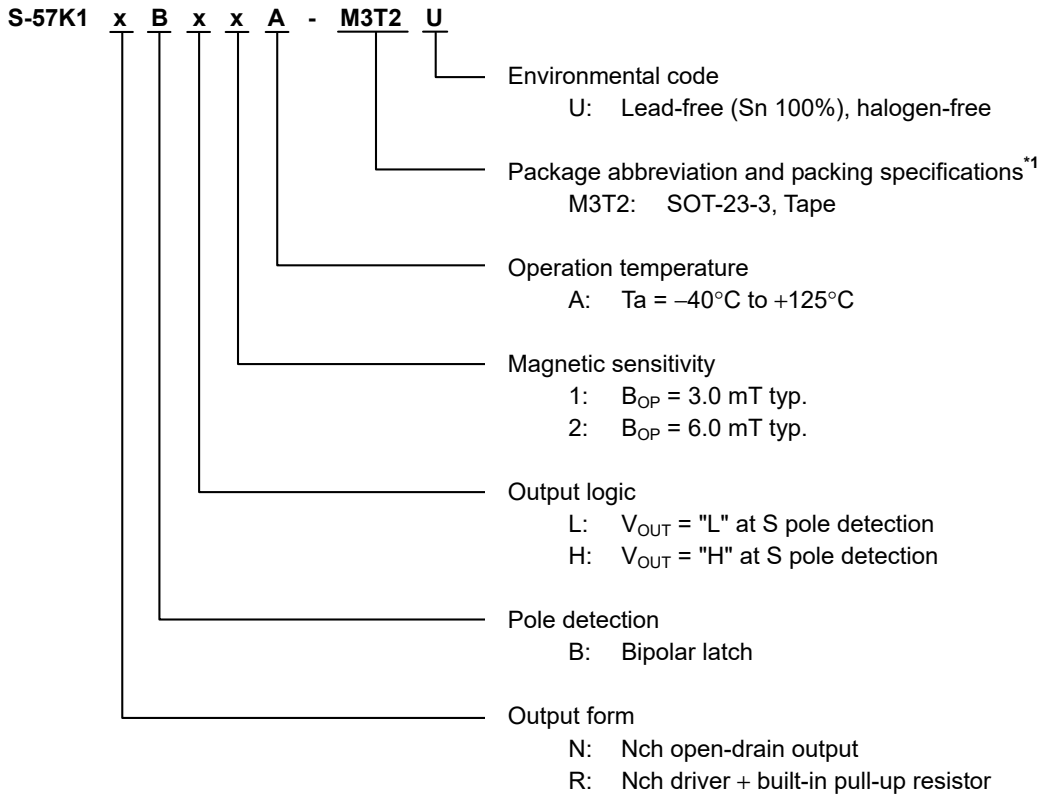


**\*1.** Parasitic diode

**Figure 2**

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## ■ AEC-Q100 Qualified

This IC supports AEC-Q100 for operation temperature grade 1.
Contact our sales office for details of AEC-Q100 reliability specification.

## ■ Product Name Structure

### 1. Product name

**S-57K1** x **B** x x **A** - **M3T2 U**

Environmental code
  U:  Lead-free (Sn 100%), halogen-free

Package abbreviation and packing specifications[1]
  M3T2:  SOT-23-3, Tape

Operation temperature
  A:  Ta = −40°C to +125°C

Magnetic sensitivity
  1:  $B_{OP}$ = 3.0 mT typ.
  2:  $B_{OP}$ = 6.0 mT typ.

Output logic
  L:  $V_{OUT}$ = "L" at S pole detection
  H:  $V_{OUT}$ = "H" at S pole detection

Pole detection
  B:  Bipolar latch

Output form
  N:  Nch open-drain output
  R:  Nch driver + built-in pull-up resistor

**[1].** Refer to the tape drawing.

### 2. Package

**Table 1   Package Drawing Codes**

| Package Name | Dimension | Tape | Reel |
|---|---|---|---|
| SOT-23-3 | MP003-C-P-SD | MP003-C-C-SD | MP003-Z-R-SD |

### 3. Product name list

**Table 2**

| Product Name | Output Form | Pole Detection | Output Logic | Magnetic Sensitivity ($B_{OP}$) |
|---|---|---|---|---|
| S-57K1NBL1A-M3T2U | Nch open-drain output | Bipolar latch | $V_{OUT}$ = "L" at S pole detection | 3.0 mT typ. |
| S-57K1NBL2A-M3T2U | Nch open-drain output | Bipolar latch | $V_{OUT}$ = "L" at S pole detection | 6.0 mT typ. |
| S-57K1NBH1A-M3T2U | Nch open-drain output | Bipolar latch | $V_{OUT}$ = "H" at S pole detection | 3.0 mT typ. |
| S-57K1RBL1A-M3T2U | Nch driver + built-in pull-up resistor | Bipolar latch | $V_{OUT}$ = "L" at S pole detection | 3.0 mT typ. |

**Remark**   Please contact our sales office for products other than the above.
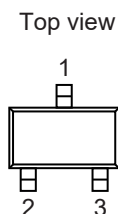
## ■ Pin Configuration

### 1. SOT-23-3

Top view



**Figure 3**

**Table 3**

| Pin No. | Symbol | Description |
|---------|--------|-------------|
| 1 | VSS | GND pin |
| 2 | VDD | Power supply pin |
| 3 | OUT | Output pin |

## ■ Absolute Maximum Ratings

**Table 4**

(Ta = +25°C unless otherwise specified)

| Item | | Symbol | Absolute Maximum Rating | Unit |
|------|--|--------|-------------------------|------|
| Power supply voltage | | $V_{DD}$ | $V_{SS} - 28.0$ to $V_{SS} + 28.0$ | V |
| Output current | | $I_{OUT}$ | 20 | mA |
| Output voltage | Nch open-drain output product | $V_{OUT}$ | $V_{SS} - 0.3$ to $V_{SS} + 28.0$ | V |
| | Nch driver + built-in pull-up resistor product | | $V_{SS} - 0.3$ to $V_{DD} + 0.3$ | V |
| Junction temperature | | $T_j$ | −40 to +150 | °C |
| Operation ambient temperature | | $T_{opr}$ | −40 to +125 | °C |
| Storage temperature | | $T_{stg}$ | −40 to +150 | °C |

**Caution** The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

## ■ Thermal Resistance Value

**Table 5**

| Item | Symbol | Condition | | Min. | Typ. | Max. | Unit |
|------|--------|-----------|--|------|------|------|------|
| Junction-to-ambient thermal resistance[1] | $\theta_{JA}$ | SOT-23-3 | Board A | – | 200 | – | °C/W |
| | | | Board B | – | 165 | – | °C/W |
| | | | Board C | – | – | – | °C/W |
| | | | Board D | – | – | – | °C/W |
| | | | Board E | – | – | – | °C/W |

**[1].** Test environment: compliance with JEDEC STANDARD JESD51-2A

**Remark** Refer to "■ **Power Dissipation**" and "**Test Board**" for details.

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## ■ Electrical Characteristics

**Table 6**

(Ta = +25°C, $V_{DD}$ = 12.0 V, $V_{SS}$ = 0 V unless otherwise specified)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|
| Power supply voltage | $V_{DD}$ | – | 3.5 | 12.0 | 26.0 | V | – |
| Current consumption | $I_{DD}$ | Nch open-drain output product Average value | – | 3.0 | 4.0 | mA | 1 |
| | | Nch driver + built-in pull-up resistor product Average value, $V_{OUT}$ = "H" | – | 3.0 | 4.0 | mA | 1 |
| Current consumption during reverse connection | $I_{DDREV}$ | Nch open-drain output product $V_{DD}$ = −26.0 V | −1 | – | – | mA | 1 |
| | | Nch driver + built-in pull-up resistor product $V_{DD}$ = −26.0 V | −5 | – | – | mA | 1 |
| Output voltage | $V_{OUT}$ | Nch open-drain output product Output transistor Nch, $V_{OUT}$ = "L", $I_{OUT}$ = 10 mA | – | – | 0.4 | V | 2 |
| | | Nch driver + built-in pull-up resistor product Output transistor Nch, $V_{OUT}$ = "L", $I_{OUT}$ = 10 mA | – | – | 0.5 | V | 2 |
| Output drop voltage | $V_D$ | Nch driver + built-in pull-up resistor product $V_{OUT}$ = "H", $V_D = V_{DD} - V_{OUT}$ | – | – | 20 | mV | 2 |
| Leakage current | $I_{LEAK}$ | Nch open-drain output product Output transistor Nch, $V_{OUT}$ = "H" = 26.0 V | – | – | 10 | μA | 3 |
| Output limit current | $I_{OM}$ | $V_{OUT}$ = 12.0 V | 22 | – | 70 | mA | 3 |
| Output delay time | $t_D$ | – | – | 8.0 | – | μs | – |
| Chopping frequency | $f_C$ | – | – | 500 | – | kHz | – |
| Start up time | $t_{PON}$ | – | – | 20 | – | μs | 4 |
| Output rise time | $t_R$ | Nch open-drain output product C = 20 pF, R = 820 Ω | – | – | 2.0 | μs | 5 |
| | | Nch driver + built-in pull-up resistor product C = 20 pF | – | – | 6.0 | μs | 5 |
| Output fall time | $t_F$ | C = 20 pF, R = 820 Ω | – | – | 2.0 | μs | 5 |
| Pull-up resistor | $R_L$ | Nch driver + built-in pull-up resistor product | 7 | 10 | 13 | kΩ | – |



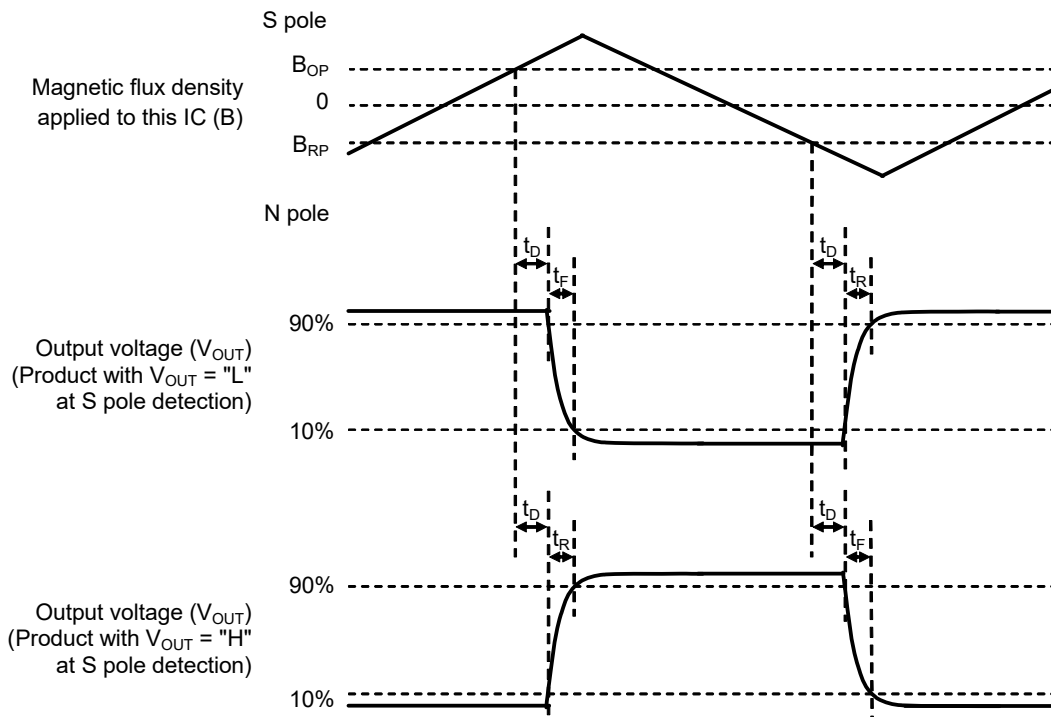**Figure 4  Operation Timing**

## ■ Magnetic Characteristics

### 1.  Product with $B_{OP}$ = 3.0 mT typ.

**Table 7**

(Ta = +25°C, $V_{DD}$ = 12.0 V, $V_{SS}$ = 0 V unless otherwise specified)

| Item | | Symbol | Condition | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|---|
| Operation point[*1] | S pole | $B_{OP}$ | – | 1.5 | 3.0 | 4.5 | mT | 4 |
| Release point[*2] | N pole | $B_{RP}$ | – | –4.5 | –3.0 | –1.5 | mT | 4 |
| Hysteresis width[*3] | | $B_{HYS}$ | $B_{HYS} = B_{OP} - B_{RP}$ | – | 6.0 | – | mT | 4 |

### 2.  Product with $B_{OP}$ = 6.0 mT typ.

**Table 8**

(Ta = +25°C, $V_{DD}$ = 12.0 V, $V_{SS}$ = 0 V unless otherwise specified)

| Item | | Symbol | Condition | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|---|
| Operation point[*1] | S pole | $B_{OP}$ | – | 3.0 | 6.0 | 9.0 | mT | 4 |
| Release point[*2] | N pole | $B_{RP}$ | – | –9.0 | –6.0 | –3.0 | mT | 4 |
| Hysteresis width[*3] | | $B_{HYS}$ | $B_{HYS} = B_{OP} - B_{RP}$ | – | 12.0 | – | mT | 4 |

**[*1].** $B_{OP}$: Operation point

$B_{OP}$ is the value of magnetic flux density when the output voltage ($V_{OUT}$) changes after the magnetic flux density applied to this IC by the magnet (S pole) is increased (by moving the magnet closer).

$V_{OUT}$ retains the status until a magnetic flux density of the N pole higher than $B_{RP}$ is applied.

**[*2].** $B_{RP}$: Release point

$B_{RP}$ is the value of magnetic flux density when the output voltage ($V_{OUT}$) changes after the magnetic flux density applied to this IC by the magnet (N pole) is increased (by moving the magnet closer).

$V_{OUT}$ retains the status until a magnetic flux density of the S pole higher than $B_{OP}$ is applied.

**[*3].** $B_{HYS}$: Hysteresis width

$B_{HYS}$ is the difference of magnetic flux density between $B_{OP}$ and $B_{RP}$.

**Remark**   The unit of magnetic density mT can be converted by using the formula 1 mT = 10 Gauss.

## ■ Test Circuits
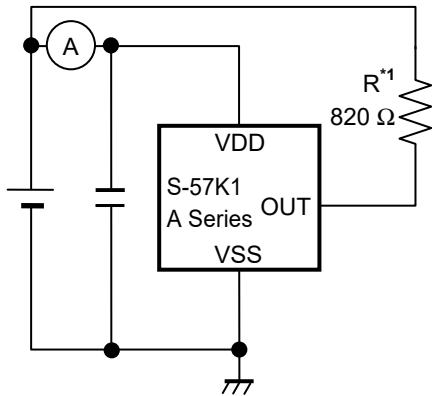
*1.    Resistor (R) is unnecessary for Nch driver + built-in pull-up resistor product.
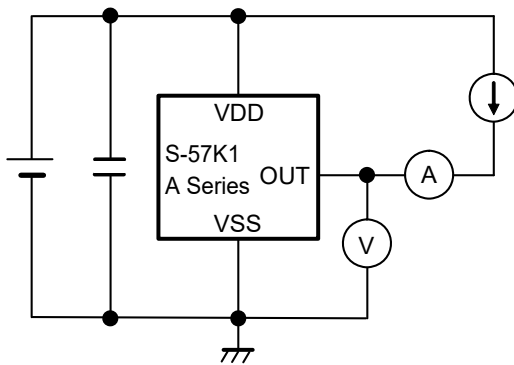
**Figure 5    Test Circuit 1**

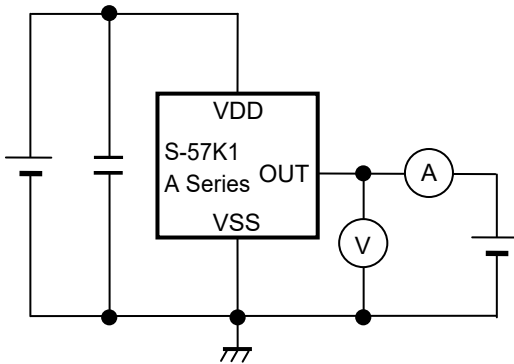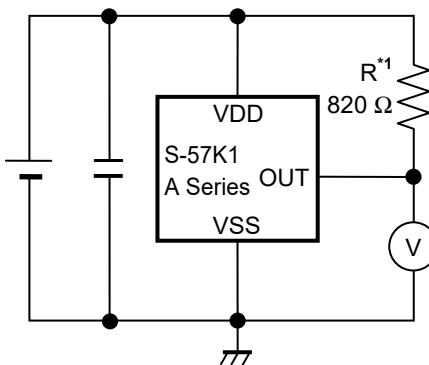**Figure 6    Test Circuit 2**

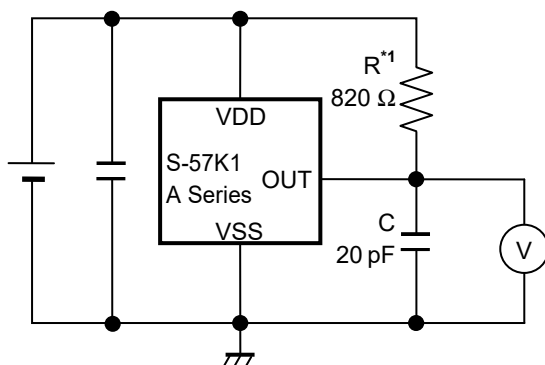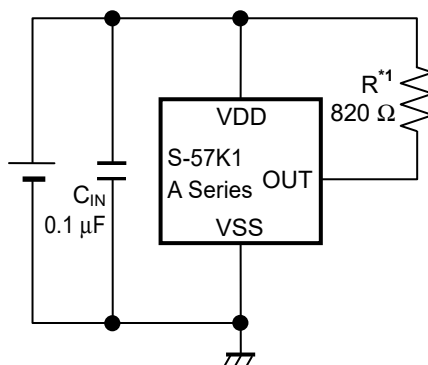**Figure 7    Test Circuit 3**

*1.    Resistor (R) is unnecessary for Nch driver + built-in pull-up resistor product.

**Figure 8    Test Circuit 4**

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**\*1.** Resistor (R) is unnecessary for Nch driver + built-in pull-up resistor product.

**Figure 9    Test Circuit 5**

## ■ Standard Circuit



**\*1.** Resistor (R) is unnecessary for the pull-up resistor built-in product.

**Figure 10**

**Caution   The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constants.**
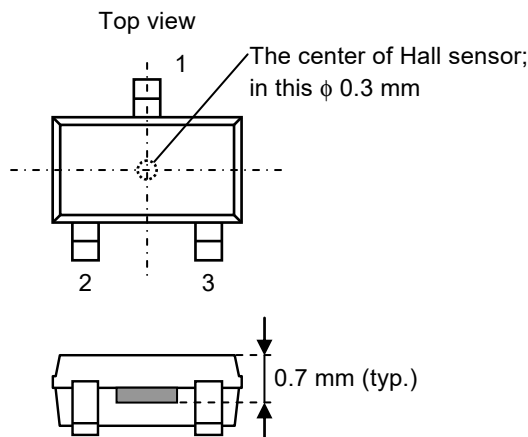
# ■ Operation

### 1. Direction of applied magnetic flux

This IC detects the magnetic flux density which is vertical to the marking surface.
**Figure 11** shows the direction in which magnetic flux is being applied.
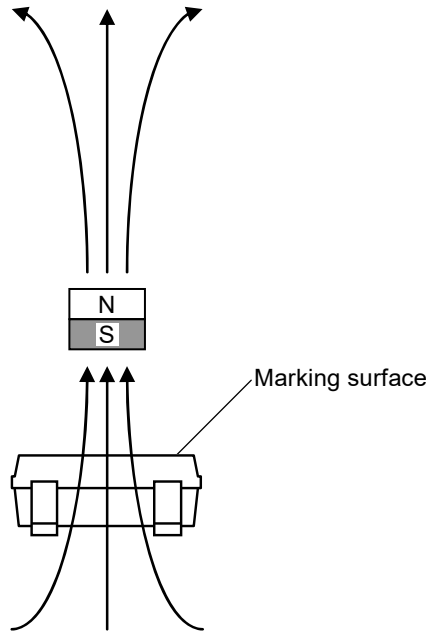


**Figure 11**

### 2. Position of Hall sensor

**Figure 12** shows the position of Hall sensor.
The center of this Hall sensor is located in the area indicated by a circle, which is in the center of a package as described below.
The following also shows the distance (typ. value) between the marking surface and the chip surface of a package.



**Figure 12**

### 3.   Basic operation

This IC changes the output voltage ($V_{OUT}$) according to the level of the magnetic flux density and a polarity change (N pole or S pole) applied by a magnet.

#### 3. 1   Product with $V_{OUT}$ = "L" at S pole detection

When the magnetic flux density of the S pole perpendicular to the marking surface exceeds the operation point ($B_{OP}$) after the S pole of a magnet is moved closer to the marking surface of this IC, $V_{OUT}$ changes from "H" to "L". When the N pole of a magnet is moved closer to the marking surface of this IC and the magnetic flux density of the N pole is higher than the release point ($B_{RP}$), $V_{OUT}$ changes from "L" to "H". In case of $B_{RP} < B < B_{OP}$, $V_{OUT}$ retains the status. **Figure 13** shows the relationship between the magnetic flux density and $V_{OUT}$.
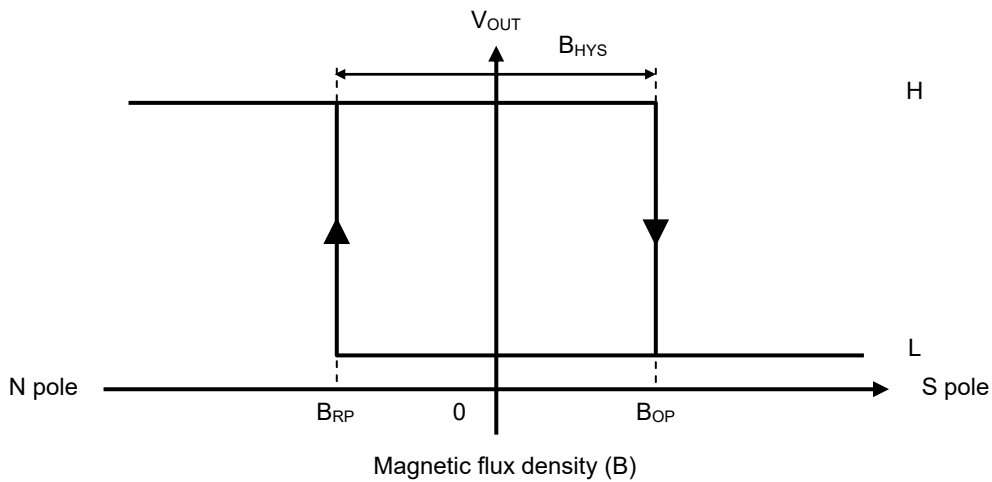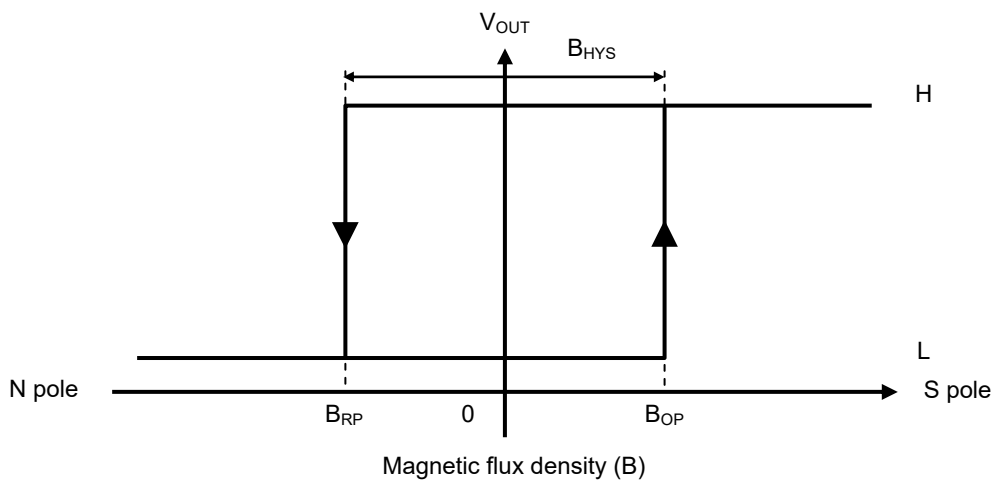


**Figure 13**

#### 3. 2   Product with $V_{OUT}$ = "H" at S pole detection

When the magnetic flux density of the S pole perpendicular to the marking surface exceeds $B_{OP}$ after the S pole of a magnet is moved closer to the marking surface of this IC, $V_{OUT}$ changes from "L" to "H". When the N pole of a magnet is moved closer to the marking surface of this IC and the magnetic flux density of the N pole is higher than $B_{RP}$, $V_{OUT}$ changes from "H" to "L". In case of $B_{RP} < B < B_{OP}$, $V_{OUT}$ retains the status.
**Figure 14** shows the relationship between the magnetic flux density and $V_{OUT}$.
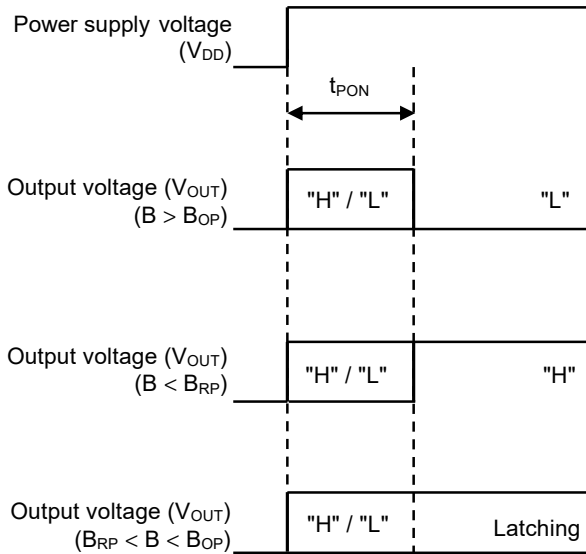


**Figure 14**

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## 4.  Timing chart

**Figure 15** shows the operation timing at power-on.
The initial output voltage at rising of power supply voltage ($V_{DD}$) is either "H" or "L".
In case of $B > B_{OP}$ or $B < B_{RP}$ at the time when the start up time ($t_{PON}$) is passed after rising of $V_{DD}$, this IC outputs $V_{OUT}$ according to the applied magnetic flux density.
In case of $B_{RP} < B < B_{OP}$ at the time when $t_{PON}$ is passed after rising of $V_{DD}$, this IC maintains the initial output voltage.

**Product with $V_{OUT}$ = "L" at S pole detection**                 **Product with $V_{OUT}$ = "H" at S pole detection**
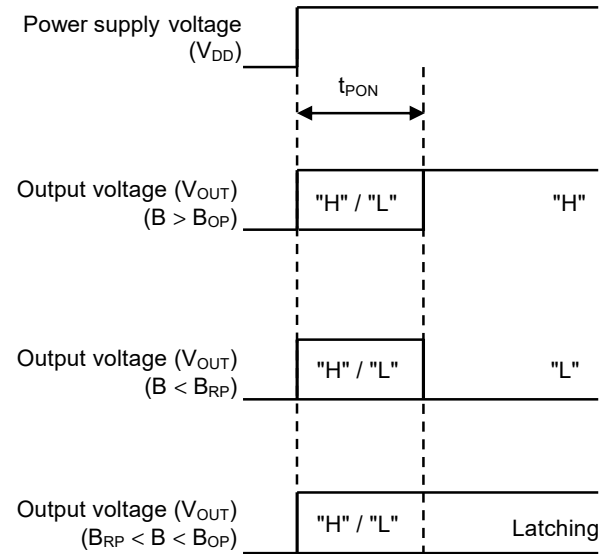


**Figure 15**

# ■ Precautions

- If the impedance of the power supply is high, the IC may malfunction due to a supply voltage drop caused by feed-through current. Take care with the pattern wiring to ensure that the impedance of the power supply is low.

- Note that the IC may malfunction if the power supply voltage rapidly changes. When the IC is used under the environment where the power supply voltage rapidly changes, it is recommended to judge the output voltage of the IC by reading it multiple times.

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.

- Although this IC has a built-in output current limit circuit, it may suffer physical damage such as product deterioration under the environment where the absolute maximum ratings are exceeded.

- Although this IC has a built-in reverse voltage protection circuit, it may suffer physical damage such as product deterioration under the environment where the absolute maximum ratings are exceeded.

- The application conditions for the power supply voltage, the pull-up voltage, and the pull-up resistor should not exceed the power dissipation.

- Large stress on this IC may affect the magnetic characteristics. Avoid large stress which is caused by the handling during or after mounting the IC on a board.

- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.
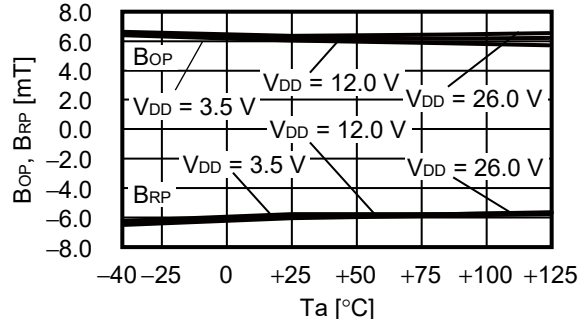
**ABLIC Inc.**

# ■ Characteristics (Typical Data)

### 1. Operation point, release point ($B_{OP}$, $B_{RP}$) vs. Temperature (Ta)
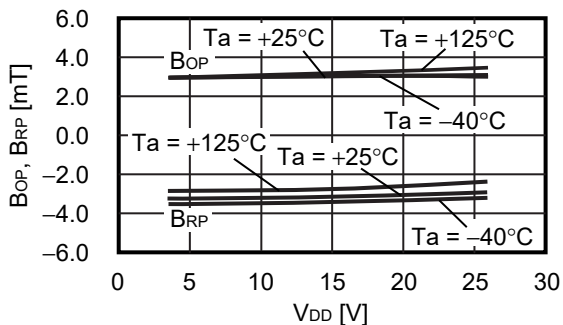
#### 1. 1 S-57K1xBx1A
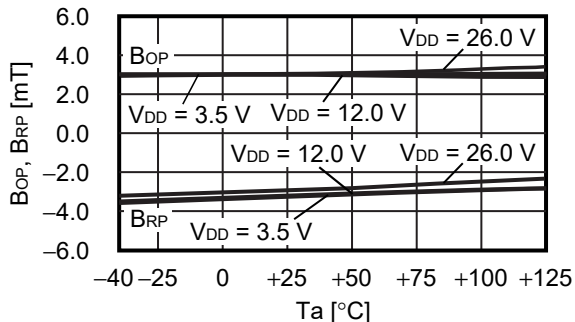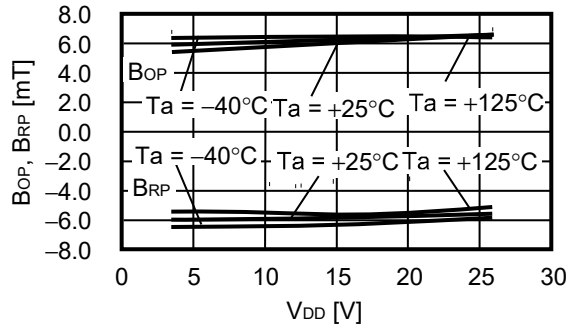


#### 1. 2 S-57K1xBx2A



### 2. Operation point, release point ($B_{OP}$, $B_{RP}$) vs. Power supply voltage ($V_{DD}$)
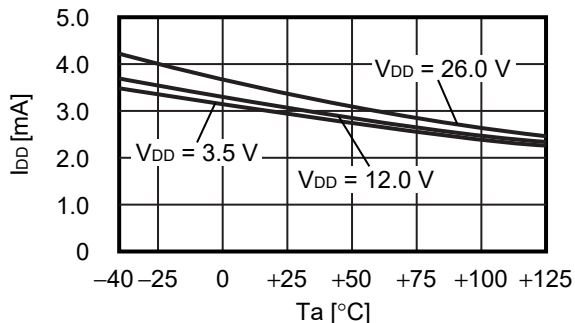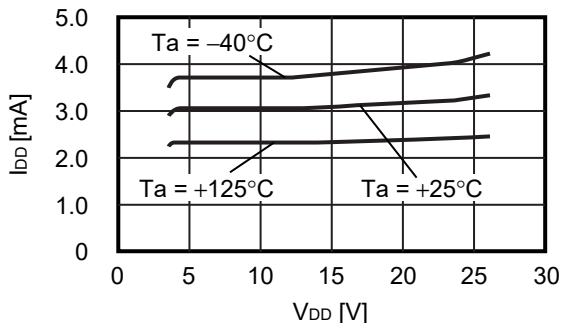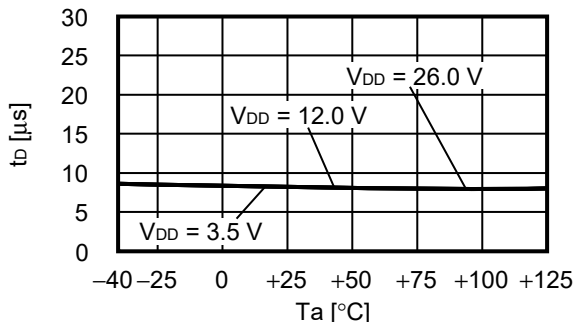
#### 2. 1 S-57K1xBx1A



#### 2. 2 S-57K1xBx2A



### 3. Current consumption ($I_{DD}$) vs. Temperature (Ta)



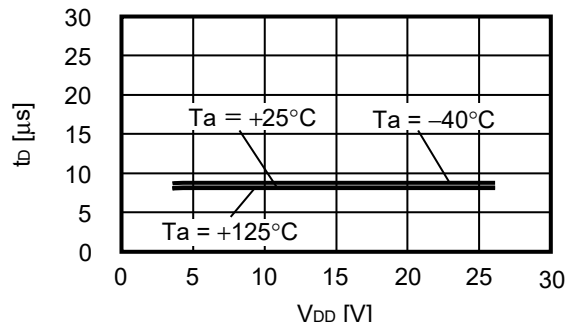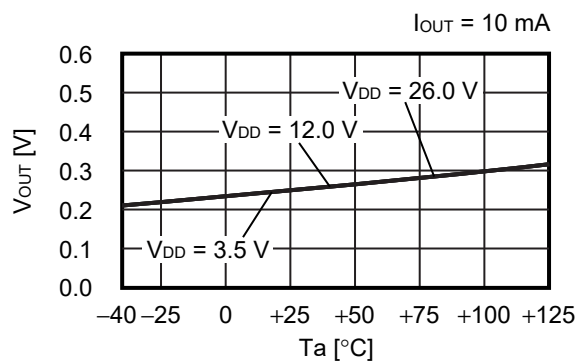### 4. Current consumption ($I_{DD}$) vs. Power supply voltage ($V_{DD}$)



### 5. Output delay time ($t_D$) vs. Temperature (Ta)



### 6. Output delay time ($t_D$) vs. Power supply voltage ($V_{DD}$)



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13

**7.  Output voltage ($V_{OUT}$) vs. Temperature (Ta)**

$I_{OUT}$ = 10 mA



**8.  Output voltage ($V_{OUT}$)**
   **vs. Power supply voltage ($V_{DD}$)**

$I_{OUT}$ = 10 mA



**ABLIC Inc.**
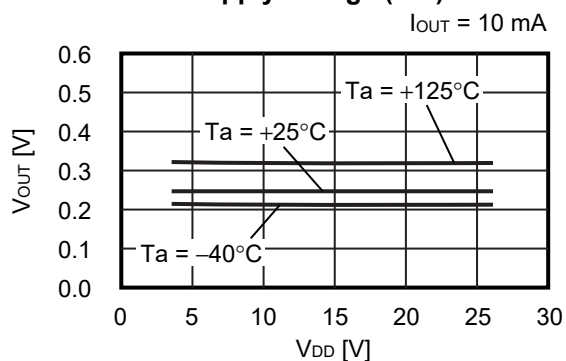
# ■ Power Dissipation

**SOT-23-3**
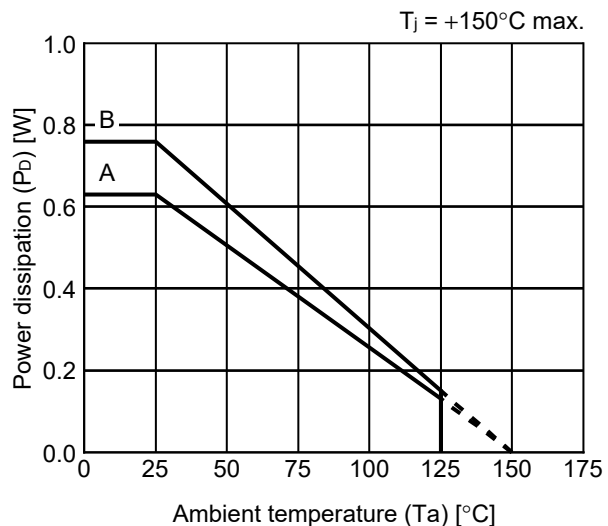


| Board | Power Dissipation (P_D) |
|-------|-------------------------|
| A | 0.63 W |
| B | 0.76 W |
| C | – |
| D | – |
| E | – |

# SOT-23-3/3S/5/6  Test Board

○ IC Mount Area

**(1) Board A**
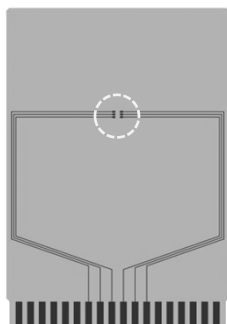


| Item | | Specification |
|---|---|---|
| Size [mm] | | 114.3 x 76.2 x t1.6 |
| Material | | FR-4 |
| Number of copper foil layer | | 2 |
| Copper foil layer [mm] | 1 | Land pattern and wiring for testing: t0.070 |
| | 2 | - |
| | 3 | - |
| | 4 | 74.2 x 74.2 x t0.070 |
| Thermal via | | - |

**(2) Board B**
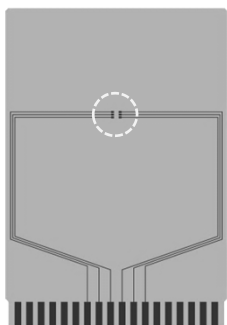


| Item | | Specification |
|---|---|---|
| Size [mm] | | 114.3 x 76.2 x t1.6 |
| Material | | FR-4 |
| Number of copper foil layer | | 4 |
| Copper foil layer [mm] | 1 | Land pattern and wiring for testing: t0.070 |
| | 2 | 74.2 x 74.2 x t0.035 |
| | 3 | 74.2 x 74.2 x t0.035 |
| | 4 | 74.2 x 74.2 x t0.070 |
| Thermal via | | - |

No. SOT23x-A-Board-SD-2.0

ABLIC Inc.

2.9±0.2

1

1.6

2.8 +0.2 -0.3

2    3

0.95±0.1

1.9±0.2

0.45

0.16 +0.1 -0.06

1.1±0.1

1.3max.

0.4±0.1

0 to 0.1
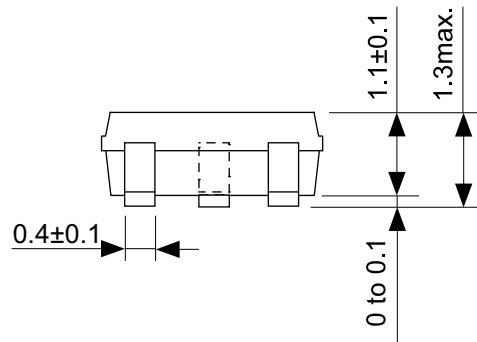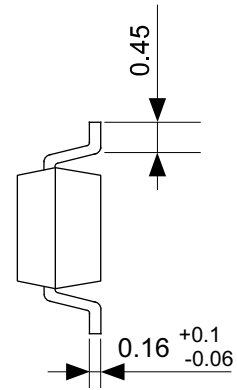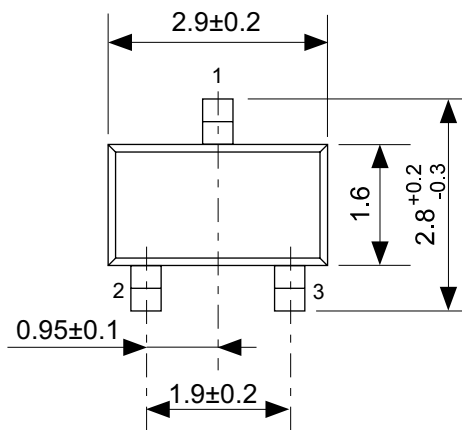
No. MP003-C-P-SD-1.1

| TITLE | SOT233-C-PKG Dimensions |
|-------|-------------------------|
| No. | MP003-C-P-SD-1.1 |
| ANGLE | ⊕ ◁ |
| UNIT | mm |
| | |

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ø1.5 +0.1 -0

2.0±0.1

4.0±0.1

1.75±0.1

3.5±0.1

8.0±0.3

3.28±0.2

0.23±0.1

1.4±0.2

ø1.0 +0.25 -0

4.0±0.1

3.2±0.2

1

2    3

Feed direction
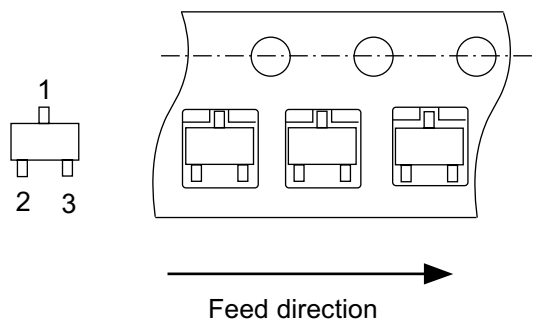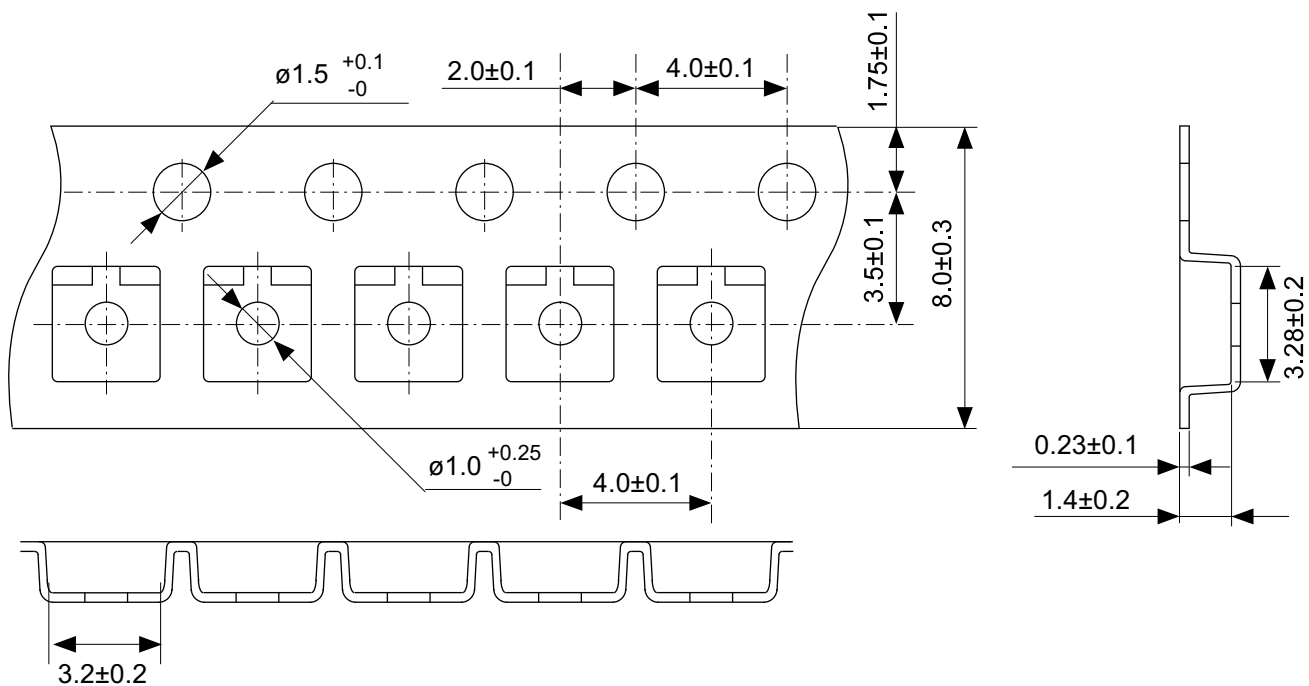
No. MP003-C-C-SD-2.0

| TITLE | SOT233-C-Carrier Tape |
|-------|----------------------|
| No. | MP003-C-C-SD-2.0 |
| ANGLE | |
| UNIT | mm |
| | |
| ABLIC Inc. | |

12.5max.

$\varnothing 180 \, ^{+0}_{-3}$

9.2±0.5
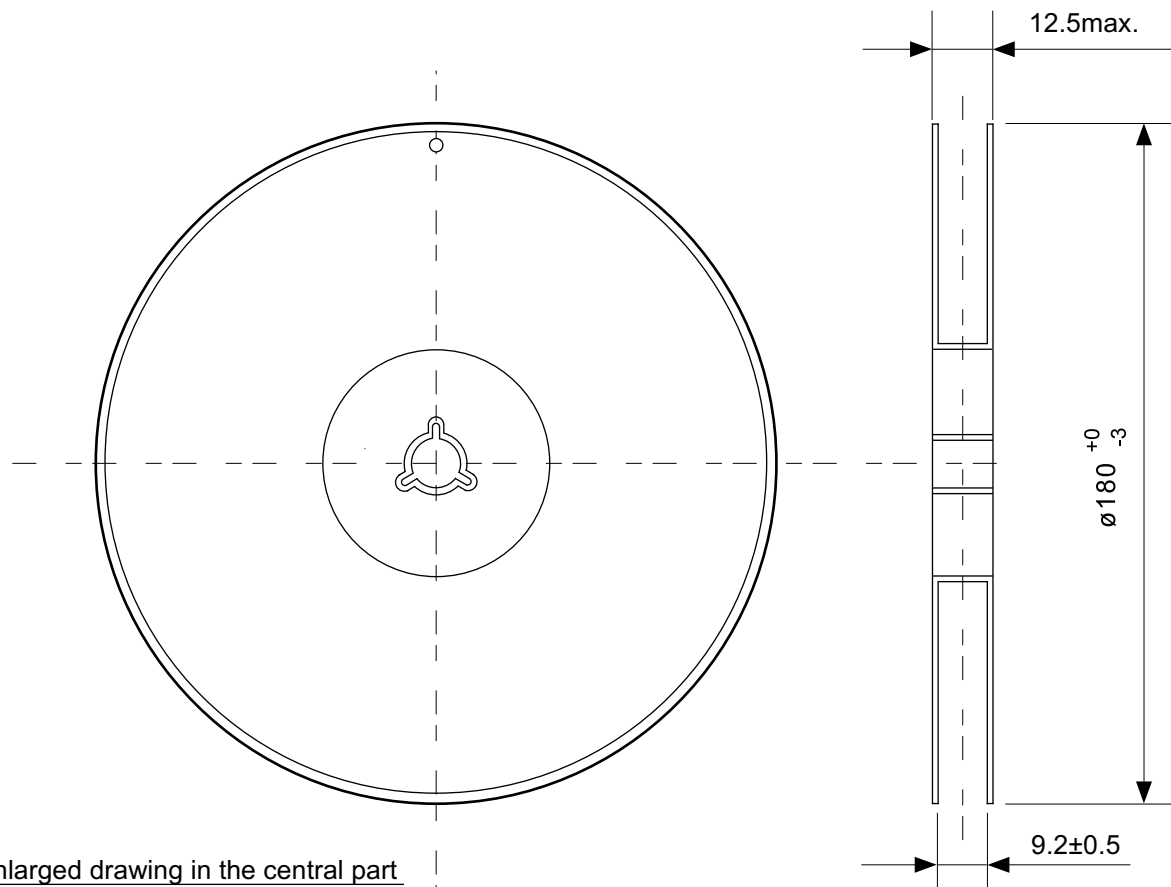
Enlarged drawing in the central part

$\varnothing 21\pm0.8$

$\varnothing 13\pm0.2$

2.0±0.5
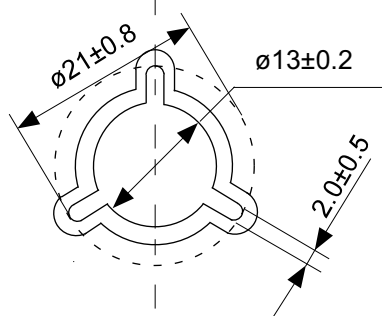
No. MP003-Z-R-SD-1.0

| TITLE | SOT233-C-Reel | | |
|---|---|---|---|
| No. | MP003-Z-R-SD-1.0 | | |
| ANGLE | | QTY. | 3,000 |
| UNIT | mm | | |
| | | | |
| ABLIC Inc. | | | |

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2.4-2019.07

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