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PIN-SELECTABLE INTERVAL TIMER IC

Rev.1.0_00

The interval timer IC allows for intermittent system operation by inputting a signal to the system at fixed periods of time.
The S-35730 outputs the interval signal (clock pulse).
One interval signal (clock pulse frequency) can be selected from "32.768 kHz", "32 Hz", "1.024 kHz", and "1 Hz" according to the SET0 pin and the SET1 pin settings.

■ Features

- Interval signal output function (Clock pulse output function): Selectable interval signal (clock pulse frequency), with an output control pin
- Low current consumption: 4.0 μA typ. (Quartz crystal: C_L = 6.0 pF, V_{DD} = 3.0 V, ENBL pin = "H", Ta = +25°C, FOUT pin output = 32.768 kHz)
- Wide range of operation voltage: 1.8 V to 5.5 V
- Built-in 32.768 kHz crystal oscillation circuit
- Operation temperature range: Ta = −40°C to +85°C
- Lead-free (Sn 100%), halogen-free

■ Applications

- IoT communications device
- Monitoring device
- Security device
- Battery system
- Energy harvesting system

■ Package

- TMSOP-8

■ Block Diagram

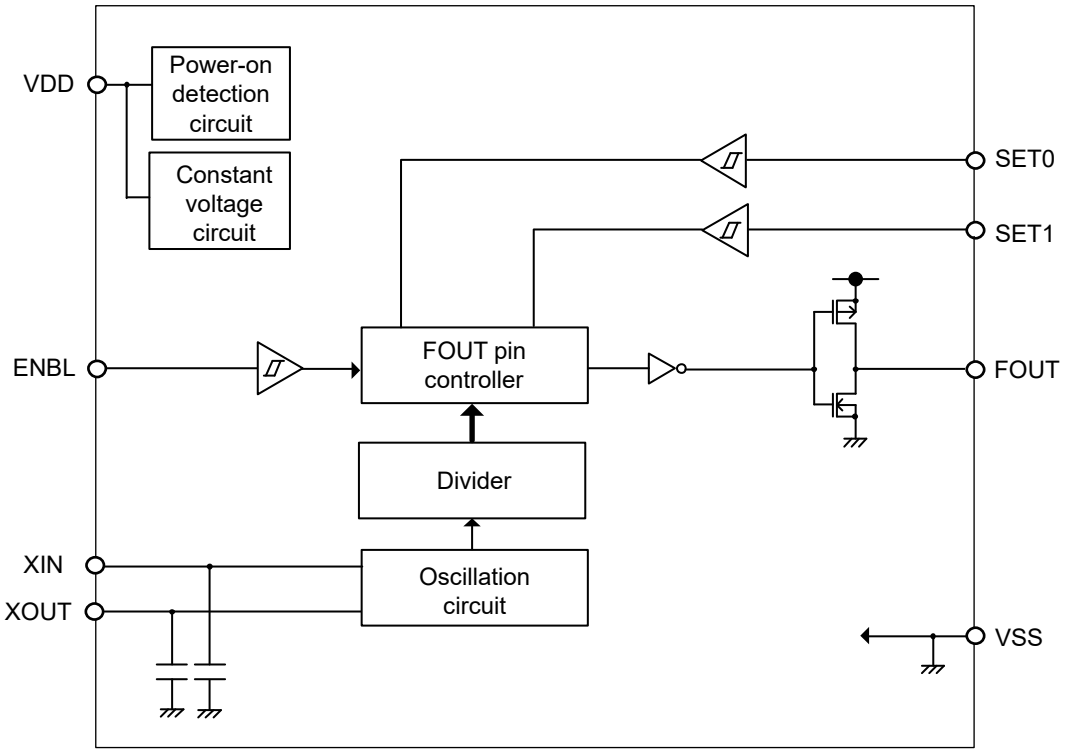
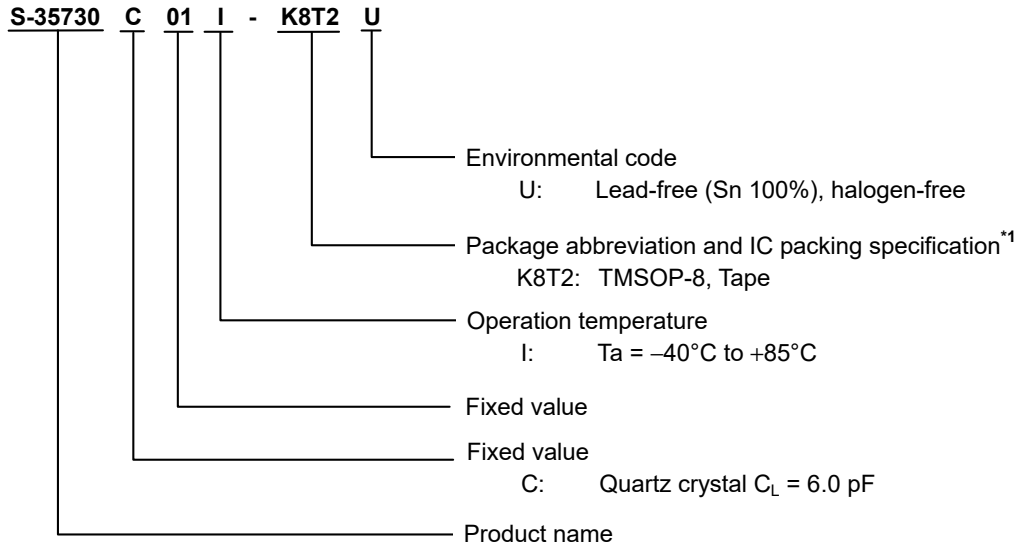


Figure 1

■ Product Name Structure

1. Product name



***1.** Refer to the tape drawing.

2. Package

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel
TMSOP-8	FM008-A-P-SD	FM008-A-C-SD	FM008-A-R-SD

3. Product name list

Table 2

Product Name	FOUT Pin Output Form	SET0 Pin, SET1 Pin Settings (SET0, SET1)			
		0, 0	0, 1	1, 0	1, 1
S-35730C01I-K8T2U	CMOS output	32.768 kHz	32 Hz	1.024 kHz	1 Hz

■ Pin Configuration

1. TMSOP-8

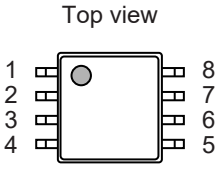


Figure 2

Table 3 List of Pins

Pin No.	Symbol	Description	I/O	Configuration
1	ENBL	Input pin for clock pulse output control	Input	CMOS input
2	XOUT	Connection pins for quartz crystal	–	–
3	XIN			
4	VSS	GND pin	–	–
5	FOUT	Output pin for clock pulse	Output	CMOS output
6	SET0	Input pins for clock pulse frequency setting	Input	CMOS input
7	SET1			
8	VDD	Pin for positive power supply	–	–

■ Pin Functions

1. SET0, SET1 (Input for clock pulse frequency setting) pins

These pins input the clock pulse frequency setting signals.
One clock pulse frequency can be selected from "32.768 kHz", "32 Hz", "1.024 kHz", and "1 Hz" according to the SET0 pin and the SET1 pin settings. Regarding the clock pulse frequency, refer to "**1. Clock pulse frequency**" in "**■ FOUT Pin Clock Pulse Output**".

2. ENBL (Input for clock pulse output control) pin

This pin controls the clock pulse output from the FOUT pin. The clock pulse is output from the FOUT pin when the ENBL pin is "H". The FOUT pin is fixed when the ENBL pin is "L".

3. FOUT (Output for clock pulse) pin

This pin outputs the clock pulse. Regarding the operation of the clock pulse output, refer to "**2. ENBL pin and clock pulse output of FOUT pin** " in "**■ FOUT Pin Clock Pulse Output**".
Besides, the FOUT pin output form is CMOS output.

4. XIN, XOUT (Connection for quartz crystal) pins

Connect a quartz crystal between the XIN pin and the XOUT pin.

5. VDD (Positive power supply) pin

Connect this pin with a positive power supply. Regarding the values of voltage to be applied, refer to "**■ Recommended Operation Conditions**".

6. VSS pin

Connect this pin to GND.

■ Equivalent Circuits of Pins

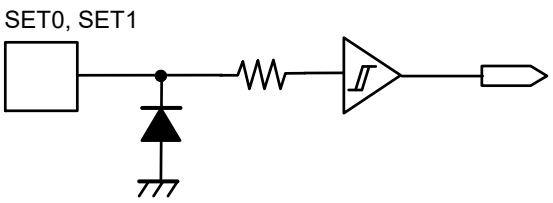


Figure 3 SET0 Pin, SET1 Pin

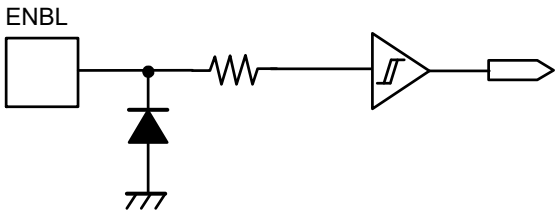


Figure 4 ENBL Pin

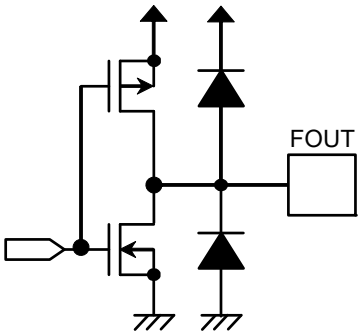


Figure 5 FOUT Pin

■ Absolute Maximum Ratings

Table 4

Item	Symbol	Applied Pin	Absolute Maximum Rating	Unit
Power supply voltage	V_{DD}	–	V_{SS} – 0.3 to V_{SS} + 6.5	V
Input voltage	V_{IN}	SET0, SET1, ENBL	V_{SS} – 0.3 to V_{SS} + 6.5	V
Output voltage	V_{OUT}	FOUT	V_{SS} – 0.3 to V_{DD} + 0.3 ≤ V_{SS} + 6.5	V
Operation ambient temperature*1	T_{opr}	–	–40 to +85	°C
Storage temperature	T_{stg}	–	–55 to +150	°C

***1.** Conditions with no condensation or frost. Condensation or frost causes short-circuiting between pins, resulting in a malfunction.

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Recommended Operation Conditions

Table 5

(V_{SS} = 0 V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operation power supply voltage	V_{DD}	Ta = –40°C to +85C	1.8	–	5.5	V

■ Oscillation Characteristics

Table 6

(Ta = +25°C, V_{DD} = 3.0 V, V_{SS} = 0 V unless otherwise specified)
(Quartz crystal (NX3215SD, C_L = 6.0 pF) manufactured by Nihon Dempa Kogyo Co., Ltd.)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	V_{STA}	Within 10 seconds	1.8	–	5.5	V
Oscillation start time	t_{STA}	–	–	–	1	s
IC-to-IC frequency deviation*1	δIC	–	–20	–	+20	ppm

***1.** Reference value

■ DC Electrical Characteristics

Table 7

(Ta = –40°C to +85°C, V_{SS} = 0 V unless otherwise specified)
(Quartz crystal (NX3215SD, C_L = 6.0 pF) manufactured by Nihon Dempa Kogyo Co., Ltd.)

Item	Symbol	Applied Pin	Condition	Min.	Typ.	Max.	Unit
Current consumption 1	I_{DD1}	–	V_{DD} = 3.0 V, ENBL pin = V_{SS}, FOUT pin = no load	–	1.7	3.0	µA
Current consumption 2	I_{DD2}	–	V_{DD} = 3.0 V, ENBL pin = V_{DD}, FOUT pin output = 32.768 kHz, FOUT pin = no load	–	4.0	6.0	µA
High level input leakage current	I_{IZH}	SET0, SET1, ENBL	V_{IN} = V_{DD}	–0.5	–	0.5	µA
Low level input leakage current	I_{IZL}	SET0, SET1, ENBL	V_{IN} = V_{SS}	–0.5	–	0.5	µA
High level output leakage current	I_{OZH}	FOUT	V_{OUT} = V_{DD}	–0.5	–	0.5	µA
Low level output leakage current	I_{OZL}	FOUT	V_{OUT} = V_{SS}	–0.5	–	0.5	µA
High level input voltage	V_{IH}	SET0, SET1, ENBL	–	0.7 × V_{DD}	–	V_{SS} + 5.5	V
Low level input voltage	V_{IL}	SET0, SET1, ENBL	–	V_{SS} – 0.3	–	0.3 × V_{DD}	V
High level output voltage	V_{OH}	FOUT	I_{OH} = –0.4 mA	0.8 × V_{DD}	–	–	V
Low level output voltage	V_{OL}	FOUT	I_{OL} = 2.0 mA	–	–	0.4	V

■ FOUT Pin Clock Pulse Output

1. Clock pulse frequency

One clock pulse frequency can be selected from "32.768 kHz", "32 Hz", "1.024 kHz", and "1 Hz" according to the SET0 pin and the SET1 pin settings. **Table 8** shows the details.

Table 8

Pin Setting		Clock Pulse Frequency
SET0	SET1	
L	L	32.768 kHz
L	H	32 Hz
H	L	1.024 kHz
H	H	1 Hz

2. ENBL pin and clock pulse output of FOUT pin

The FOUT pin outputs the clock pulse when the ENBL pin is "H". The FOUT pin is fixed to "L" when the ENBL pin is "L". Since the input signal of the ENBL pin is not synchronized with the clock pulse output from the FOUT pin, the duty ratio may change when the "H" and "L" of the ENBL pin changes.
The example of the FOUT pin output timing is shown below.

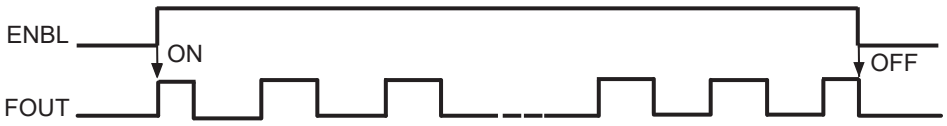


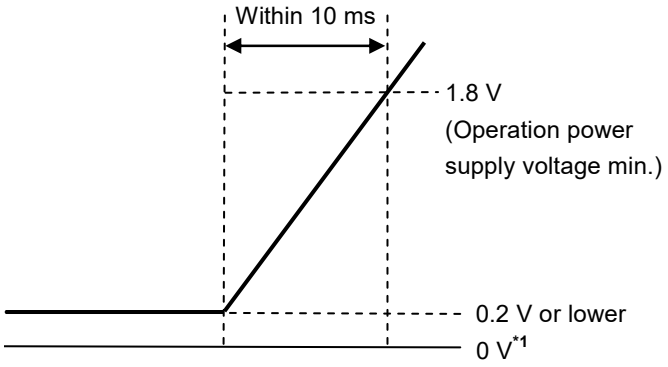
Figure 6 Example of FOUT Pin Output Timing

The SET0 pin and the SET1 pin input signals are not synchronized with the clock pulse output from the FOUT pin as well. Therefore, duty ratio may change if the SET0 pin and the SET1 pin settings are changed when the ENBL pin is "H".

Moreover, since the crystal oscillation circuit is unstable immediately after power-on, regardless of the status of the ENBL pin, the FOUT pin is fixed to "L" for about 0.5 seconds after power-on.

■ Power-on Detection Circuit

In order for the power-on detection circuit to operate normally, raise the power supply voltage of the IC from 0.2 V or lower so that it reaches 1.8 V of the operation power supply voltage minimum value within 10 ms, as shown in **Figure 7**.



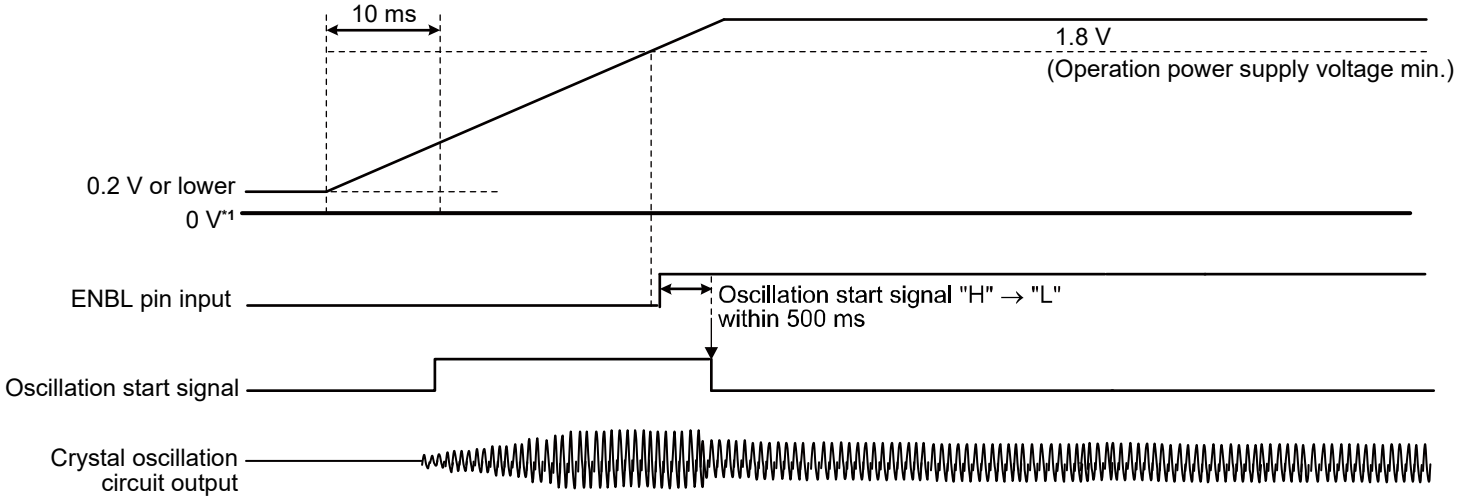
***1.** 0 V means that there is no potential difference between the VDD pin and the VSS pin of the S-35730.

Figure 7 How to Raise Power Supply Voltage

If the power supply voltage of the S-35730 cannot be raised under the above conditions, the power-on detection circuit may not operate normally and an oscillation may not start. In such case, perform the operations shown in "**1. When power supply voltage is raised at ENBL pin = "L"** " and "**2. When power supply voltage is raised at ENBL pin = "H"** ".

1. When power supply voltage is raised at ENBL pin = "L"

Set the ENBL pin to "L" until the power supply voltage reaches 1.8 V or higher. While the ENBL pin is set to "L", the oscillation start signal becomes "H", and the crystal oscillation circuit normally oscillates. If the ENBL pin is set to "H" after the power supply voltage reaches 1.8 V, the oscillation start signal becomes "L" within 500 ms, and the oscillation status is maintained.

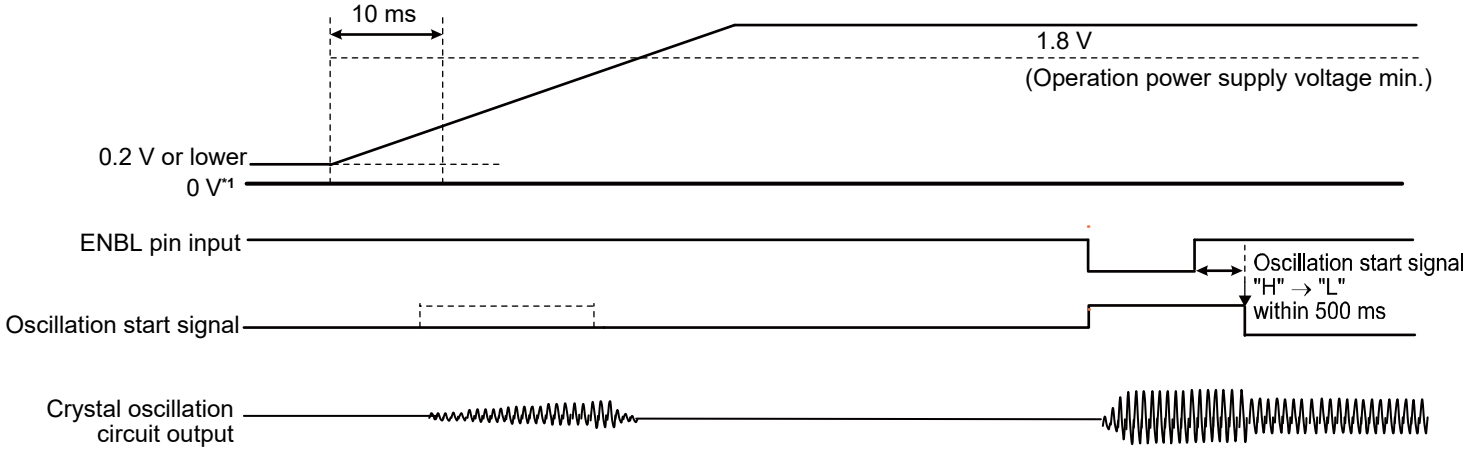


***1.** 0 V means that there is no potential difference between the VDD pin and the VSS pin of the S-35730.

Figure 8 When Power Supply Voltage is Raised at ENBL Pin = "L"

2. When power supply voltage is raised at ENBL pin = "H"

Set the ENBL pin to "L" after the power supply voltage reaches 1.8 V or higher. If the ENBL pin is set to "L" for 500 ms or longer, the oscillation start signal becomes "H", and the crystal oscillation circuit normally oscillates. After that, if the ENBL pin is set to "H", the oscillation start signal becomes "L" within 500 ms, and the oscillation status is maintained.



***1.** 0 V means that there is no potential difference between the VDD pin and the VSS pin of the S-35730.

Figure 9 When Power Supply Voltage is Raised at ENBL Pin = "H"

■ Example of Application Circuit

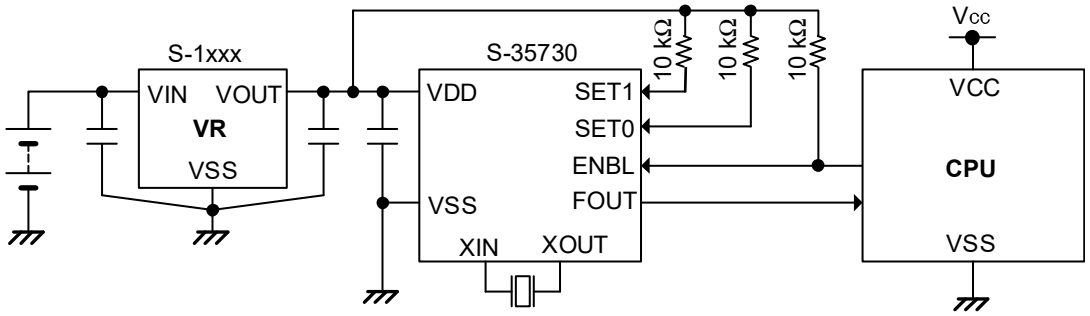


Figure 10

Caution **The above connection diagram does not guarantee operation. Set the constants after performing sufficient evaluation using the actual application**

■ Configuration of Crystal Oscillation Circuit

Since the S-35730 has built-in capacitors (C_g and C_d), adjustment of oscillation frequency is unnecessary.
However, the crystal oscillation circuit is sensitive to external noise and parasitic capacitance (C_P), these effects may become a factor to worsen the clock accuracy. Therefore, the following steps are recommended for optimizing the configuration of the crystal oscillation circuit.

- Locate the bypass capacitor adjacent to the power supply pin of the S-35730.
- Place the S-35730 and the quartz crystal as close to each other as possible, and shorten the wiring.
- Increase the insulation resistance between pins and the board wiring patterns of XIN and XOUT.
- Do not place any signal or power lines close to the crystal oscillation circuit.
- Locate the GND layer immediately below the crystal oscillation circuit.
  (In the case of a multi-layer board, only the layer farthest from the oscillation circuit should be located as the GND layer. Do not locate a circuit pattern on the intermediate layers.)

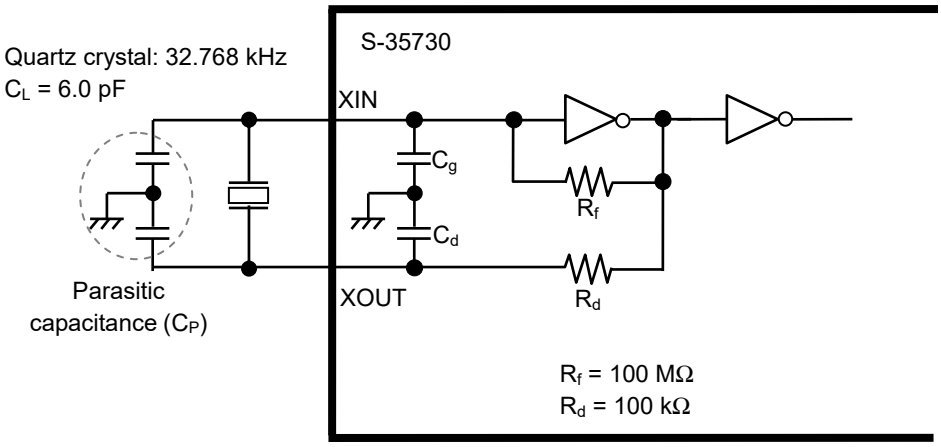


Figure 11 Configuration of Crystal Oscillation Circuit

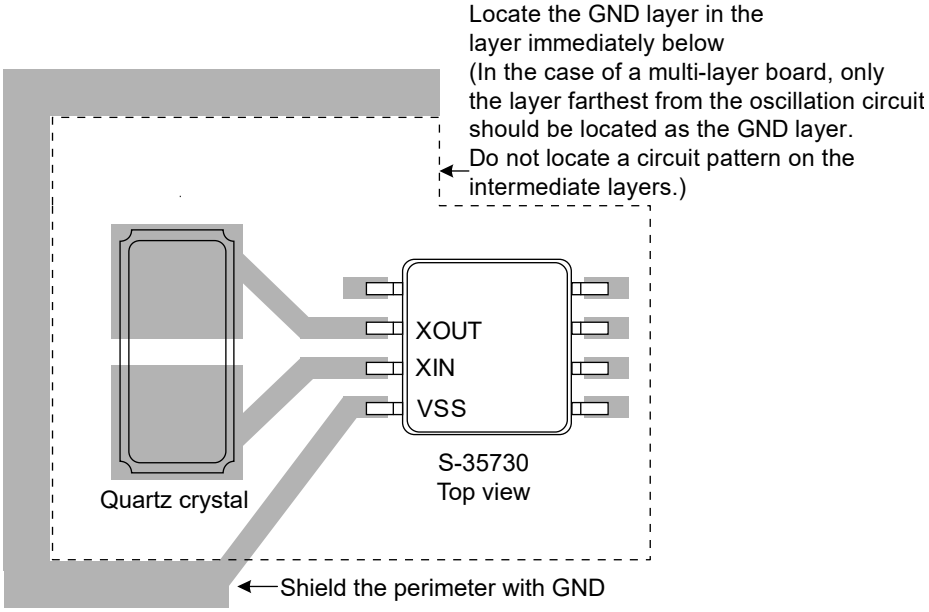


Figure 12 Example of Recommended Connection Pattern Diagram

Caution Oscillation characteristics are subject to the variation of each component such as board parasitic capacitance, parasitic resistance, quartz crystal and external capacitor. When configuring the crystal oscillation circuit, pay sufficient attention for them.

■ Cautions When Using Quartz Crystal

Request a matching evaluation between the IC and a quartz crystal to the quartz crystal maker.

■ Precautions

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
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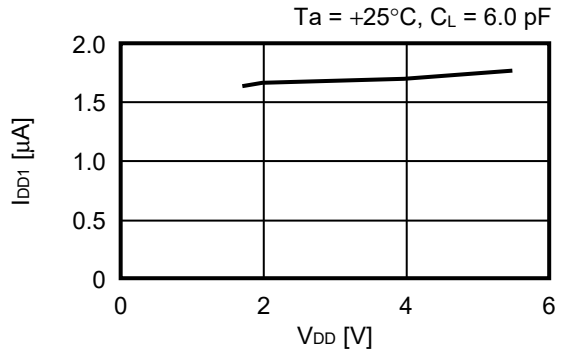
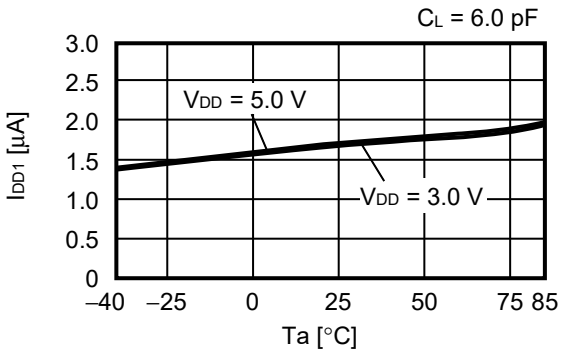
■ Characteristics (Typical Data)

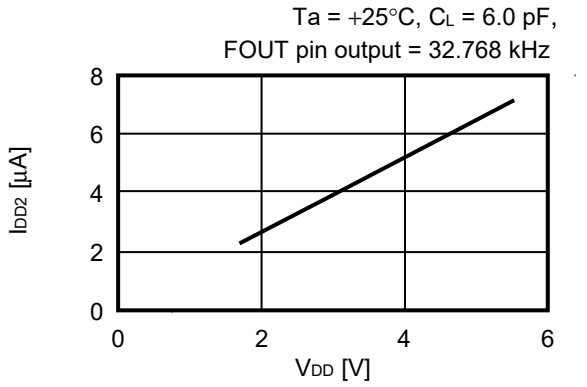
1. Current consumption 1 vs. Power supply voltage characteristics



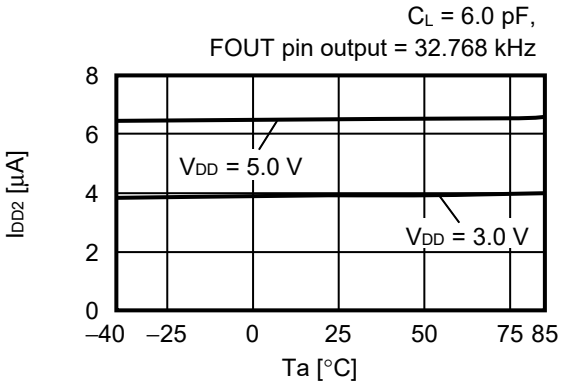
2. Current consumption 1 vs. Temperature characteristics



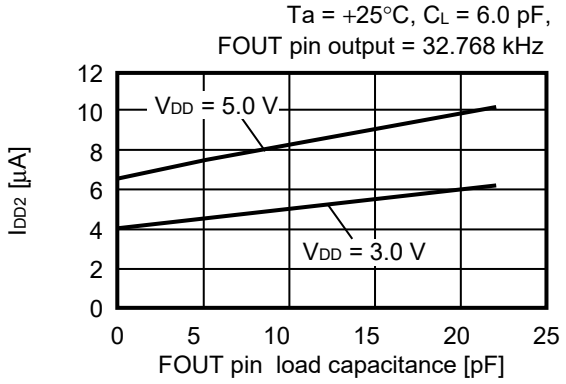
3. Current consumption 2 vs. Power supply voltage characteristics



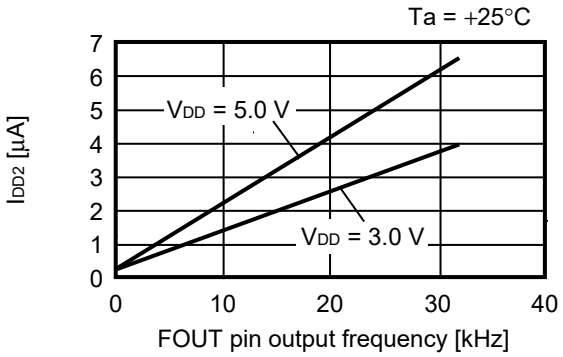
4. Current consumption 2 vs. Temperature characteristics



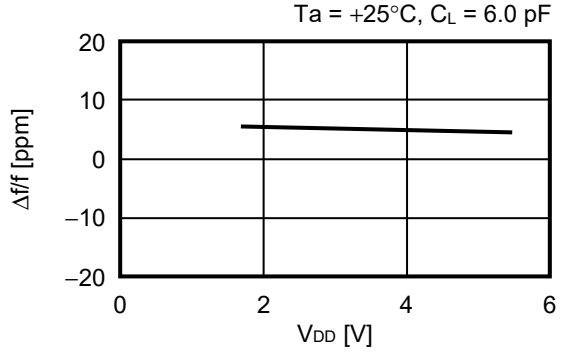
5. Current consumption 2 vs. FOUT pin load capacitance characteristics



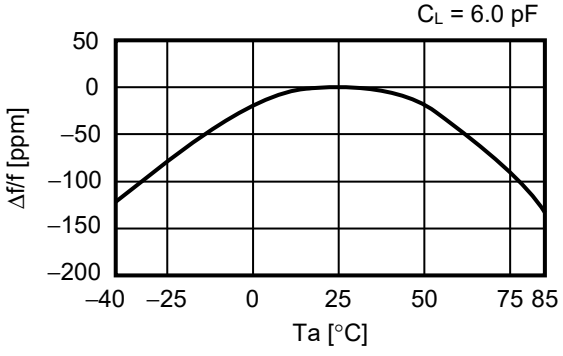
6. Current consumption 2 vs. FOUT pin output frequency characteristics



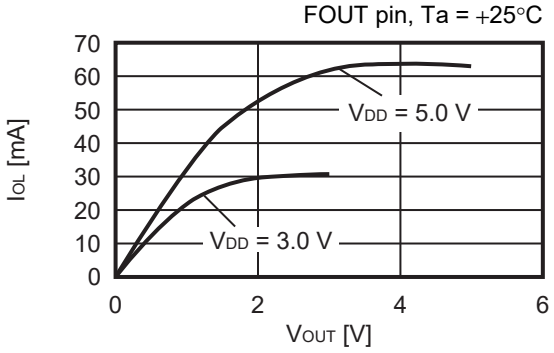
7. Oscillation frequency vs. Power supply voltage characteristics



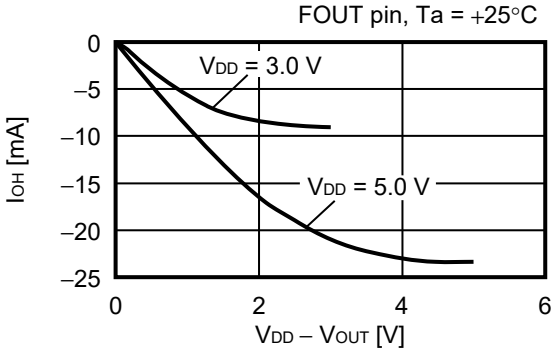
8. Oscillation frequency vs. Temperature characteristics

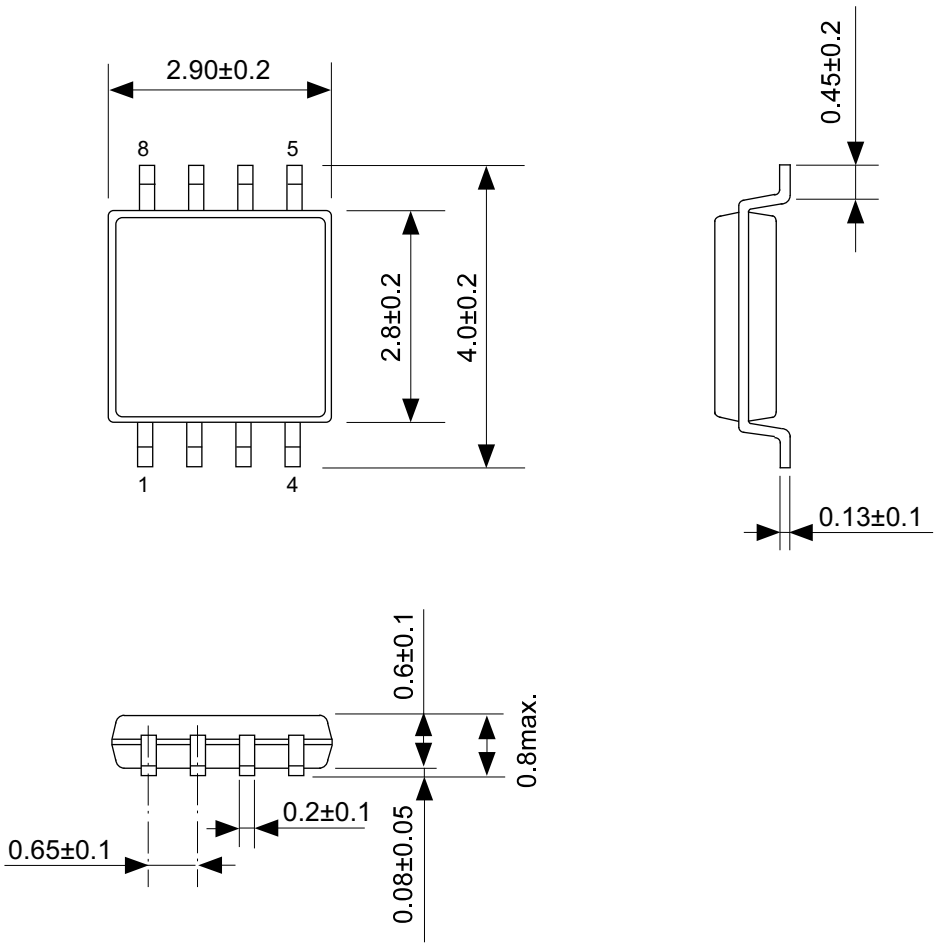


9. Low level output current vs. Output voltage characteristics



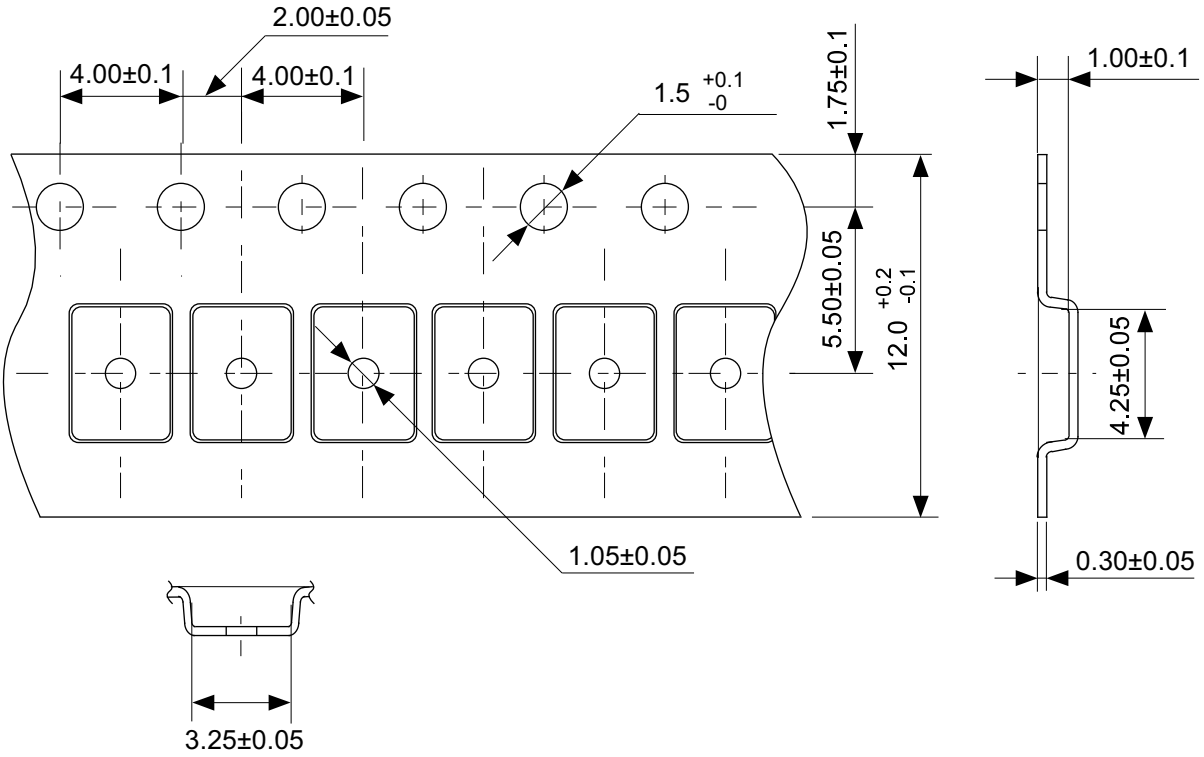
10. High level output current vs. $V_{DD} - V_{OUT}$ characteristics

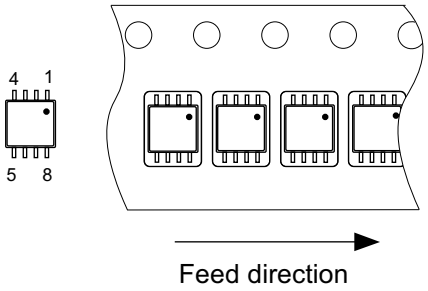




No. FM008-A-P-SD-1.2

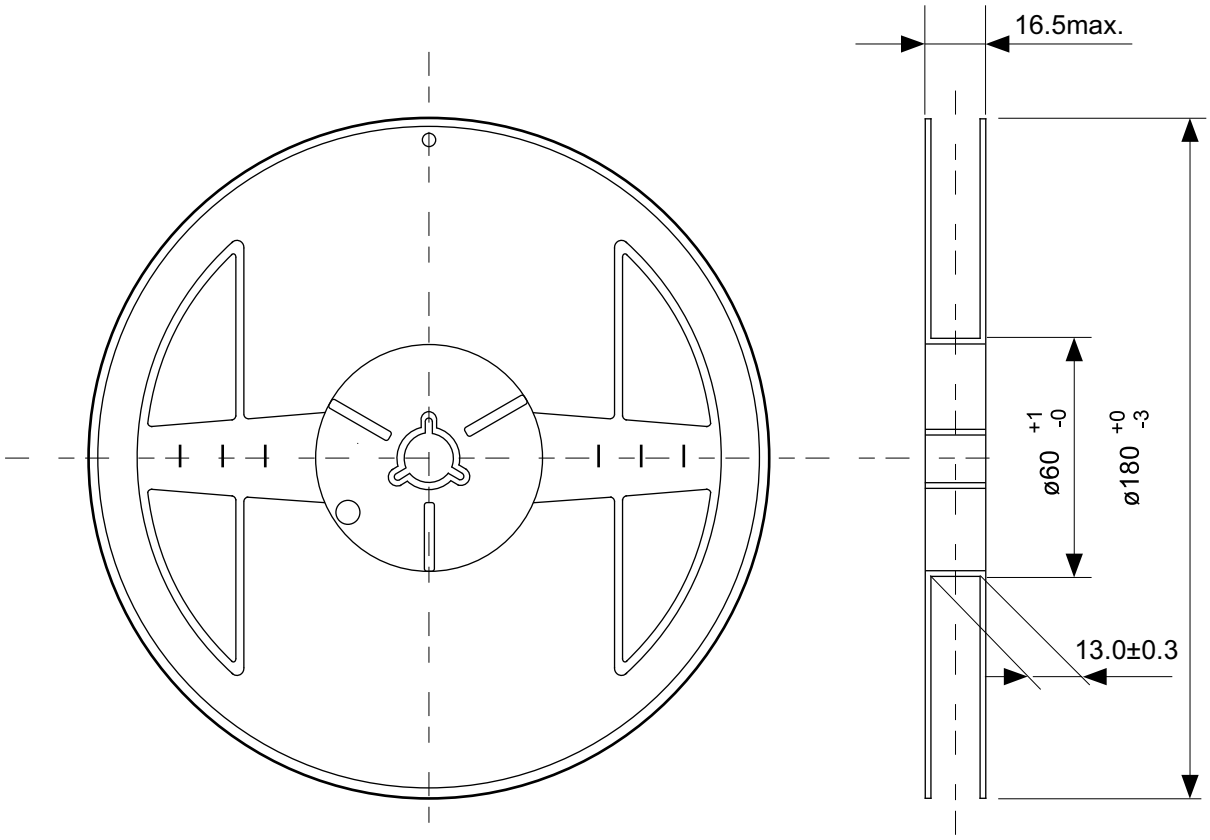
TITLE	TMSOP8-A-PKG Dimensions
No.	FM008-A-P-SD-1.2
ANGLE	
UNIT	mm
ABLIC Inc.	



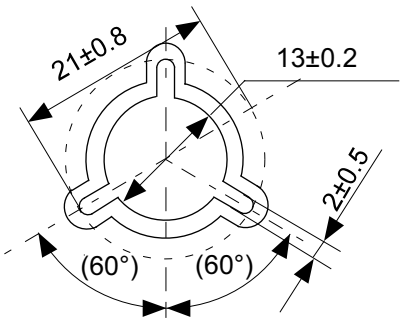


No. FM008-A-C-SD-2.0

TITLE	TMSOP8-A-Carrier Tape
No.	FM008-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	



Enlarged drawing in the central part



No. FM008-A-R-SD-1.0

TITLE	TMSOP8-A-Reel		
No.	FM008-A-R-SD-1.0		
ANGLE		QTY.	4,000
UNIT	mm		
ABLIC Inc.			

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11. The products do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Be careful when handling these with the bare hands to prevent injuries, etc.
12. When disposing of the products, comply with the laws and ordinances of the country or region where they are used.
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14. For more details on the information described herein or any other questions, please contact ABLIC Inc.'s sales representative.
15. This Disclaimers have been delivered in a text using the Japanese language, which text, despite any translations into the English language and the Chinese language, shall be controlling.

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