PFC Controller with Critical Conduction Mode

General Description

The RT7300A is an active Power Factor Correction (PFC) controller with critical conduction mode (CRM) operation that is designed to meet line current harmonic regulations for the applications of AC/DC adapters, electronic ballasts and medium off-line power converters (<300W). The CRM and Feed-Forward schemes provide near unity power factor across a wide range of input voltages and output powers.

The totem-pole gate driver with 600mA sourcing current and 800mA sinking current provides powerful driving capability for power MOSFET to improve conversion efficiency. The RT7300A features an extra low start-up current (≤20μA) and supports a disable function to reduce power consumption in standby mode, which makes it easy to comply with energy saving regulations such as Blue Angel, Energy Star and Energy 2000.

This controller integrates comprehensive safety protection functions for robust designs including input under voltage lockout, output over voltage protection, under voltage protection and cycle-by-cycle current limit.

The RT7300A is a cost-effective solution for PFC power converter with minimum external components. It is available in the SOP-8 package.

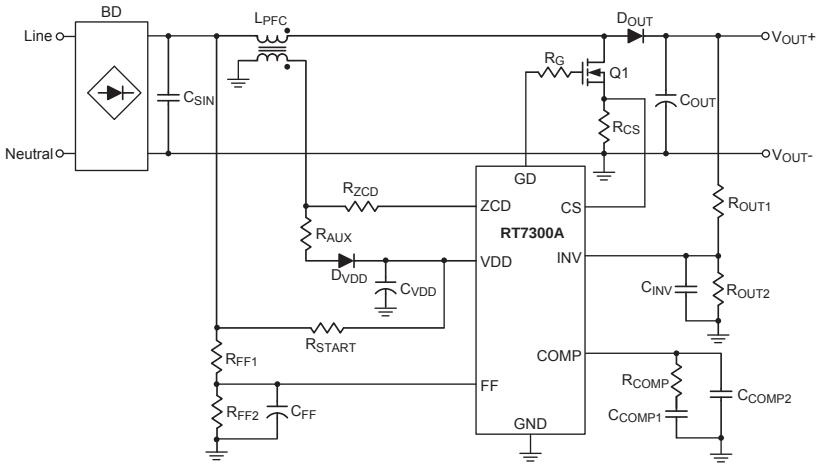
Features

- **Critical Conduction Mode (CRM) Operation**
- **Constant On-Time Control (Voltage Mode)**
- **Near Unity Power Factor**
- **Ultra Low Start-up Current (<20μA)**
- **Input Voltage Feed-Forward Compensation**
- **Wide Supply Voltage Range from 12V to 25V**
- **Totem Pole Gate Driver with 600mA/–800mA**
- **Maximum Frequency Clamping (120kHz)**
- **DCM THD Optimization**
- **Fast Dynamic Response**
- **Light Load Burst Mode Operation**
- **Disable Function**
- **Maximum/Minimum On-Time Limit**
- **Cycle-by-Cycle Current Limit**
- **Output Over Voltage Protection (OVP)**
- **Output Under Voltage Protection (UVP)**
- **Under Voltage Lockout (UVLO)**
- **RoHS Compliant and Halogen Free**

Applications

- Electrical Lamp Ballast
- LED Lighting
- AC/DC Adapter/Charger for Desktop PC, NB, TV, Monitor, Etc.
- Entry-Level Server, Web Server

Simplified Application Circuit



Ordering Information

RT7300A □□

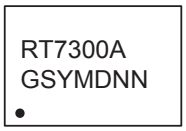
- Package Type
  S : SOP-8
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

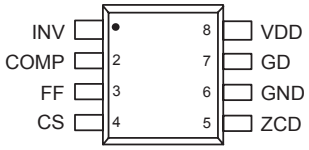
Marking Information



RT7300AGS : Product Number
YMDNN : Date Code

Pin Configurations

(TOP VIEW)

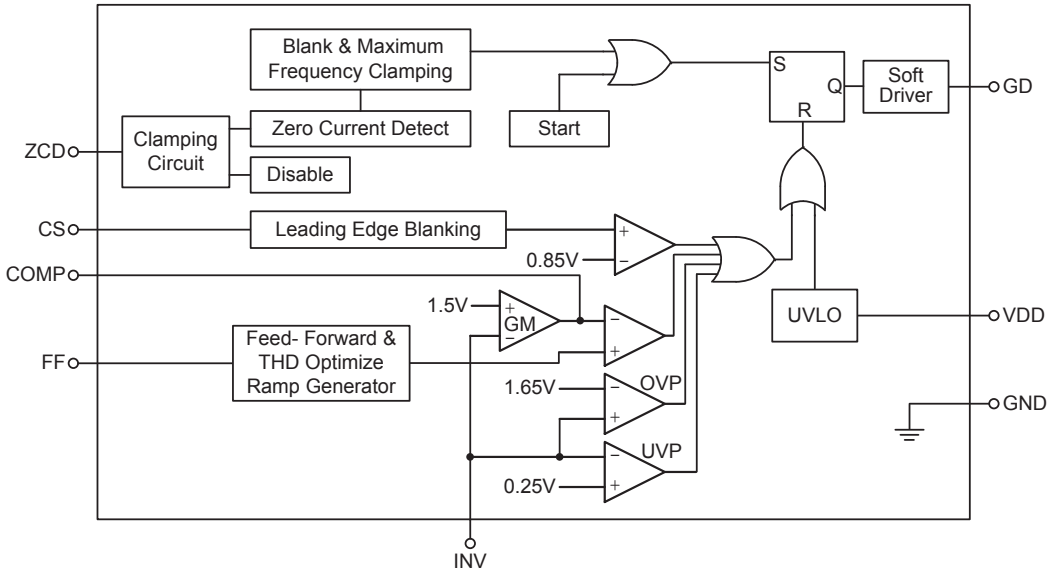


SOP-8

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	INV	Inverting Input of the Internal Error Amplifier. Connect a resistive divider from output voltage to this pin for voltage feedback. It also used for OVP and UVP detections.
2	COMP	Output of the Internal Error Amplifier. Connect a compensation network between this pin and GND for dynamic load performance.
3	FF	Feed-Forward Input for Line Voltage. This pin senses the line input voltage via a resistive divider. Connect a suitable capacitor to filter out the line voltage ripple & noise.
4	CS	Current Sense Input. The current sense resistor between this pin and GND is used for current limit setting.
5	ZCD	Zero Current Detection Input. Input from secondary winding of PFC choke for detecting demagnetization timing of PFC choke. This pin also can be used to enable/disable the controller.
6	GND	Ground of the Controller.
7	GD	Gate Driver Output for External Power MOSFET.
8	VDD	Supply Voltage Input. The controller will be enabled when VDD exceeds V_{ON_TH} (12.45V typ.) and disabled when VDD decreases lower than V_{OFF_TH} (9V typ.).

Function Block Diagram



Operation

Critical Conduction Mode (CRM)

The Critical Conduction Mode is also called Transition Mode or Boundary Mode. Figure 1 shows the CRM operating at the boundary between Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM).

In CRM, the power switch turns on immediately when the inductor current decreases to zero. The CRM is the preferred control method for medium power (<300W) applications due to the features of zero current switching and lower peak current than that in DCM.

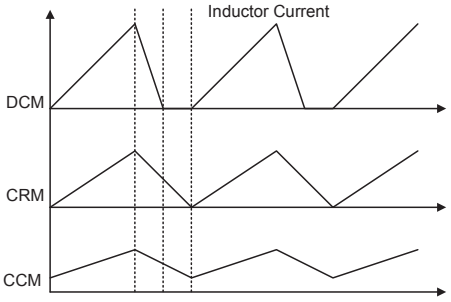


Figure 1. Inductor Current of DCM, CRM and CCM

Constant On-Time Voltage Mode Control

Figure 2 shows a typical Boost converter. When the MOSFET turns on with a fixed on-time (T_{ON}), the inductor current can be calculated by the following equation (1).

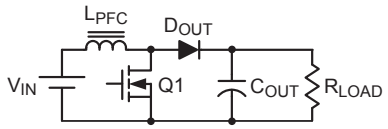


Figure 2. Typical Boost Converter

$$I_{L\_PK} = \frac{V_{IN}}{L_{PFC}} \times T_{ON} \quad (1)$$

If the input voltage is a sinusoidal waveform and rectified by a bridge rectifier, the inductor current can be expressed with equation (2). When the converter operates in CRM with constant on-time voltage mode control, the envelope of inductor peak current will follow the input voltage waveform with in-phase. The average inductor current will be half of the peak current shown as Figure 3. Therefore, the near unity power factor is easy to be achieved by this control scheme.

$$I_{L\_pk} \times |\sin\theta| = \frac{VIN\_pk \times |\sin\theta| \times T_{ON}}{L_{PFC}} \quad (2)$$

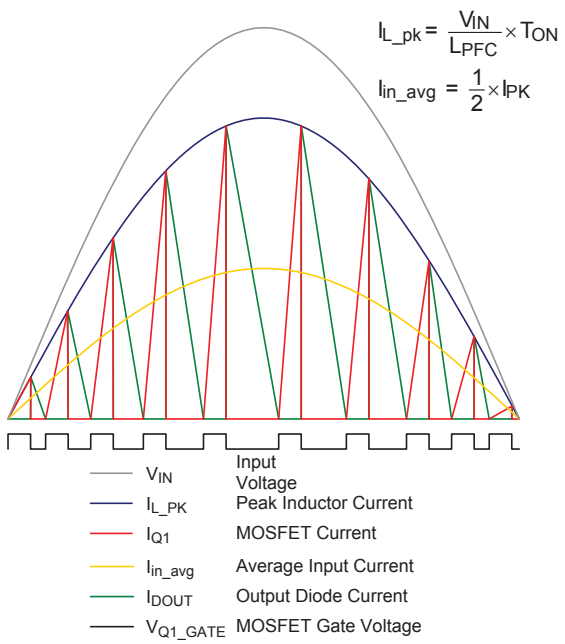


Figure 3. Inductor Current of CRM with Constant On-Time Voltage Mode Control

Under Voltage Lockout

The controller will be enabled when VDD exceeds V_{ON_TH} (12.45V typ.) and disabled when VDD decreases lower than V_{OFF_TH} (9V typ.).

The maximum VDD voltage is set at 27V typically for over voltage protection shown as Figure 4. An internal 29V zener diode is also used to avoid over voltage stress for the internal circuits.

When the VDD is available, the precise reference is generated for internal circuitries such as Error Amplifier, Current Sense, OVP, UVP. The internal reference equips with excellent temperature coefficient performance so that the RT7300A can be operated in varied environments.

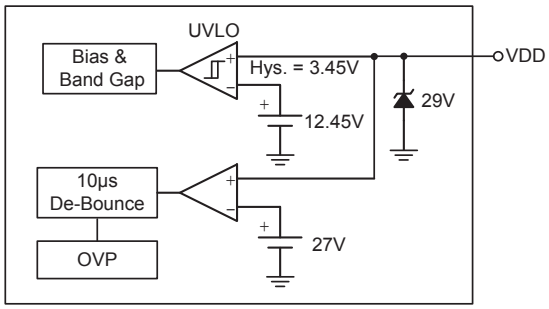


Figure 4. VDD and UVLO

Feedback Voltage Detection

Figure 5 shows the feedback voltage detection circuit. The INV pin is the inverting input of the Error Amplifier with 1.5V reference voltage. Over voltage and under voltage protections are provided with threshold voltage 1.65V and 0.25V respectively. If the INV voltage is over 1.65V or under 0.25V, the gate driver will be disabled to prevent output over voltage condition or feedback open condition. Although the INV is an input pin with high impedance, it is suggested that the bias current of the potential divider should be over 30μA for noise immunity.

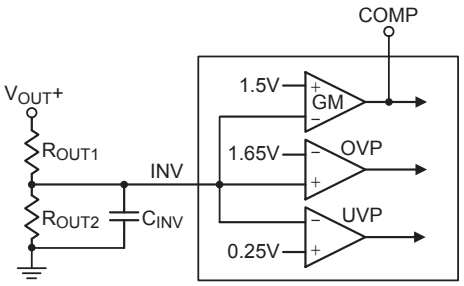


Figure 5. Feedback Voltage Detection

Transconductance Error Amplifier

The RT7300A implements transconductance error amplifier with non-linear GM design to regulate the Boost output voltage and provide fast dynamic response. The transconductance value is 100μA/V in normal operation. When the INV voltage increases over 1.65V or decreases under 1.35V, the output of error amplifier will source or sink 1mA maximum current at COMP pin respectively shown as Figure 6. Thus, the non-linear GM design can provide fast response for the dynamic load of PFC converters even though the bandwidth of control loop is lower than line frequency.

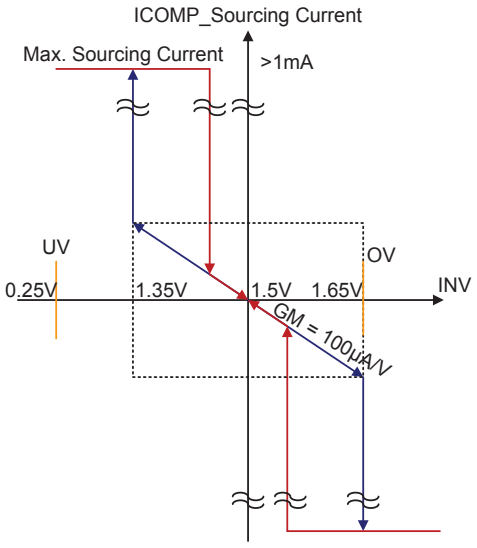


Figure 6. Non-linear GM

Feed-Forward Compensation

The FF pin is an input pin with high impedance to detect the line input voltage shown as Figure 7. A proper voltage divider should be applied to sense the line voltage after bridge diode rectifier. Since the FF voltage is proportional to the line input voltage, it provides a feed-forward signal to compensate the loop bandwidth for high line and low line input conditions.

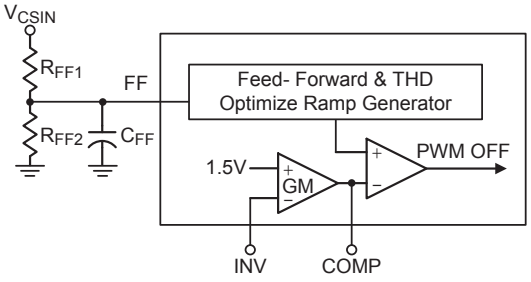


Figure 7. FF Detection Circuit

The constant on-time, T_{ON}, can be derived from the following equations.

$$P_i = \frac{1}{4} \times V_{IN\_pk} \times I_{L\_pk} \qquad I_{L\_pk} = \frac{V_{IN\_pk}}{L_{PFC}} \times T_{ON}$$

$$P_i = \frac{1}{4} \times V_{IN\_pk} \times \frac{V_{IN\_pk}}{L_{PFC}} \times T_{ON} = \frac{1}{4} \times \frac{V_{IN\_pk}^2}{L_{PFC}} \times T_{ON}$$

$$\Rightarrow T_{ON} = \frac{4 \times P_i \times L_{PFC}}{V_{IN\_pk}^2} \quad (3)$$

In RT7300A, the Ton is implemented by a constant current charging a capacitor till V_{Comp} threshold voltage is reached. Therefore, the T_{ON} is a function of V_{comp}.

$$T_{ON} = \frac{C_{ramp} \times V_{Comp}}{I_{ramp}} \quad (4)$$

Then, the V_{Comp} can be derived from equation (3) and (4).

$$\frac{4 \times P_i \times L_{PFC}}{V_{IN\_pk}^2} = \frac{C_{ramp} \times V_{Comp}}{I_{ramp}}$$

$$V_{Comp} = \frac{4 \times P_i \times L_{PFC}}{V_{IN\_pk}^2} \times \frac{I_{ramp}}{C_{ramp}} \quad (5)$$

According to equation (5), the V_{Comp} is reversely proportional to the squared input voltage so that the V_{Comp} has a large variation for the change of line voltage between high and low input voltages. This variation will impact T_{ON}, Burst mode entry level and loop bandwidth.

In order to compensate the variation, the I_{ramp} is designed to be proportional to the squared input voltage shown as equation (6).

$$I_{ramp}(V_{pk}) = k \times V_{IN\_pk}^2 \times gm_{ramp} \quad (6)$$

$$V_{Comp}(FF) = \frac{2 \times P_i \times L_{PFC} \times gm_{ramp}}{C_{ramp}} \quad (7)$$

When k = 0.5, the V_{Comp} is compensated to be proportional to the power only. So, the Ton will be stable to support good power factor for high and low line voltage conditions.

Ramp Generator

The RT7300A provides constant on-time voltage mode control to achieve near unity power factor for the CRM boost converters. Figure 8 shows the Ramp Generator with Feed-Forward compensation and THD optimization circuit for the constant on-time operation.

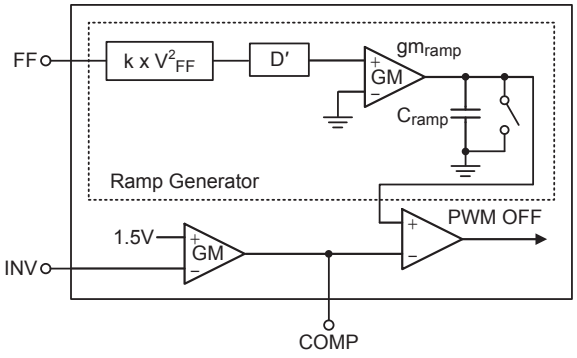


Figure 8. Ramp Generator

The charging current of ramp generator is modulated following the squared FF voltage with line voltage compensation and the THD optimization scheme is implemented to compensate the harmonic distortion when the converter is operated in DCM.

ZCD and Enable Function

In CRM operation, when the power switch turns on, the inductor current increases linearly to the peak value. When the power switch turns off, the inductor current decreases linearly to zero. The zero current can be detected by the ZCD pin with the auxiliary winding of Boost inductor.

Figure 9 and Figure 10 show the ZCD block diagram and related waveforms. The ZCD block diagram provides zero current detection, voltage clamp and shutdown control functions. When the inductor current decreases to zero, the auxiliary winding voltage will turn from high to low. Once the ZCD voltage decreases to the V_{ZCDT} threshold, the controller will generate a signal for gate driver. The hysteresis voltage between the threshold V_{ZCDA} and V_{ZCDT} is designed to avoid mis-triggering. In order to prevent over voltage stress, the ZCD pin voltage is clamped at V_{ZCDH} if the input voltage is too high from the auxiliary winding and the ZCD pin voltage is clamped at V_{ZCDL} if the input voltage is lower than zero.

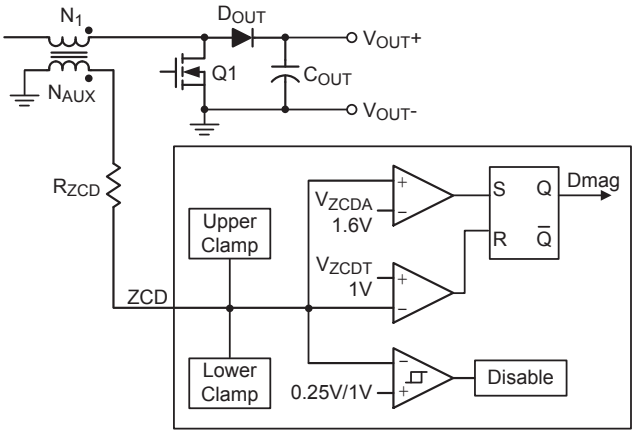


Figure 9. ZCD Block Diagram

The RT7300A provides shutdown function to save power consumption in standby mode. When the ZCD pin is pulled lower than 250mV, the gate driver will be turned off and operate in standby mode with low quiescent current less than 600μA. Once the ZCD pin is released, the controller will be activated.

The RT7300A also provides ZCD time-out detection function. If the controller runs at maximum frequency and there is no ZCD signal being detected after 4μs delay time, the PWM will be turned on for ZCD time-out detection.

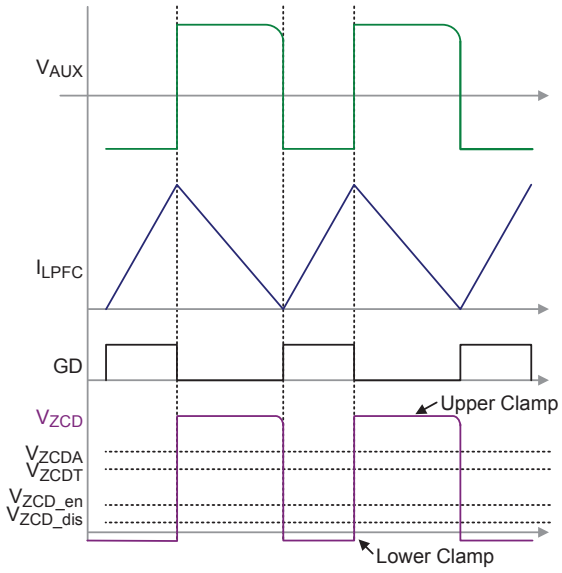


Figure 10. ZCD Related Waveforms

Absolute Maximum Ratings (Note 1)

- Supply Voltage, VDD ---------- –0.3V to 30V
- Gate Driver Output, GD ---------- –0.3V to 20V
- Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C

  SOP-8 ---------- 0.625W
- Package Thermal Resistance (Note 2)

  SOP-8, θ_{JA} ---------- 160°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)

  HBM (Human Body Model) ---------- 2kV

  MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Voltage, VDD ---------- 12V to 25V
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{DD} = 15V, T_A = 25°C, unless otherwise specification)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD Section						
VDD OVP Threshold Voltage	V_{OVP}		25.5	27	28.5	V
VDD OVP De-bounce Time			--	10	--	μs
VDD On Threshold Voltage	V_{ON_TH}		11.45	12.45	13.45	V
VDD Off Threshold Voltage	V_{OFF_TH}		8	9	10	V
Zener Voltage	V_Z		29	--	--	V
Operating Supply Current	I_{DD_OP}	I_{ZCD} = 0, @ GATE = open, 70kHz	--	--	2.5	mA
Quiescent Current	I_Q	Turn on in burst mode @ gate open	--	--	1.7	mA
Standby Current		PFC is disabled	--	--	0.6	mA
Start-Up Current	I_{DD_ST}	Before V_{ON_TH}	--	--	20	μA
ZCD Section						
Upper Clamp Voltage	V_{ZC_DH}	I_{ZCD} = 2.5mA	4.5	4.8	5.5	V
Lower Clamp Voltage	V_{ZC_DL}	I_{ZCD} = –2.5mA	0.3	0.65	--	V
Arming Voltage	V_{ZC_DA}	(Note 5)	--	1.6	--	V
Trigger Voltage	V_{ZC_DT}	(Note 5)	--	1	--	V
Delay Time Between Trigger Point and Gate Turn On			--	100	170	ns
Sourcing Current Capability			–2.5	--	–6.5	mA
Sinking Current Capability			2.5	--	--	mA

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Disable Voltage		V_{ZCD_DIS}		--	--	250	mV
Restart Voltage		V_{ZCD_EN}		1	--	--	V
Pull-High Current After Disable				30	75	100	μA
FF Section							
Input Bias Current		I_{BIAS}	Leakage Current of FF Pin	--	--	1	μA
GM Section							
Non-Inverting Input Reference		V_{REF}	Including Offset, Full VDD Range, T_A = 25°C	1.47	1.5	1.53	V
INV Bias Current				--	--	–1	μA
Transconduction		gm	If $\|V_{ERROR}\|$ < 0.25V	80	100	120	μA/V
Non-linear Gm			Otherwise	--	1	--	mA
COMP Maximum Voltage		V_{COMP_OP}		4.25	--	--	V
PWM Section							
INV OVP Threshold Voltage				1.55	1.65	1.75	V
INV UVP Threshold Voltage				0.18	0.25	0.32	V
INV OVP/UVP De-bounce Time				--	20	--	μs
Burst Mode Entry	Level High	V_{Burst_H}	Measure at COMP Pin	1.85	2.15	2.45	V
	Level Low	V_{Burst_L}	Measure at COMP Pin	1.75	2.05	2.35	
De-bounce Time of Burst Mode				1.5	2	4	μs
Ramp Slope			V_{FF} = 0.8V	--	70	--	mV/μS
Minimum On-Time			$T_{ON(MIN)\_PFC}$ = 3pF x 2.5V / (I_{ZCD} x 0.02), I_{ZCD} = 75μA	4.4	5.4	6.4	μs
Current Sense Section							
Leading Edge Blanking Time		T_{LEB_PFC}	LEB + Delay (Note 6)	240	400	570	ns
Current Sense Threshold Voltage		V_{CS_PFC}		0.74	0.85	0.96	V
Gate Driver Section							
Rising Time		T_R	C_L = 1nF	--	40	80	ns
Falling Time		T_F	C_L = 1nF	--	30	70	ns
Gate Output Clamping Voltage		V_{CLAMP}	V_{DD} = 25V	--	13	--	V
Internal Pull Low Resistor				--	12	--	kΩ
Oscillator Section							
Valley Mask Time		T_{MASK}		7	8.5	10	μs
Duration of Starter		T_{START}		75	130	300	μs
Maximum On-Time		$T_{ON(MAX)\_PFC}$	Maximum $T_{ON(MAX)\_PFC}$	--	50	--	μs

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability

Note 2. θ_{JA} is measured at T_A = 25°C on a low effective thermal conductivity single-layer test board per JEDEC 51-3.

Note 3. Devices are ESD sensitive. Handling precaution is recommended

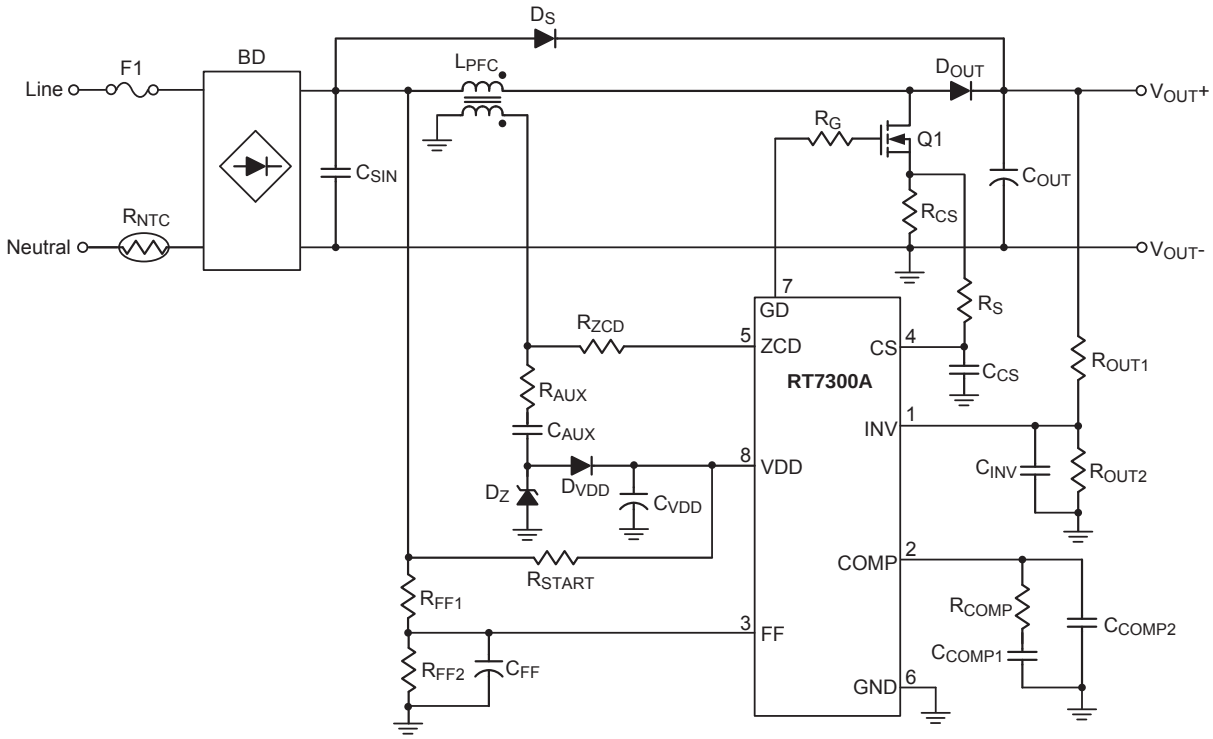
Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Guaranteed by Design.

Note 6. Leading edge blanking time and internal propagation delay time is guaranteed by design.

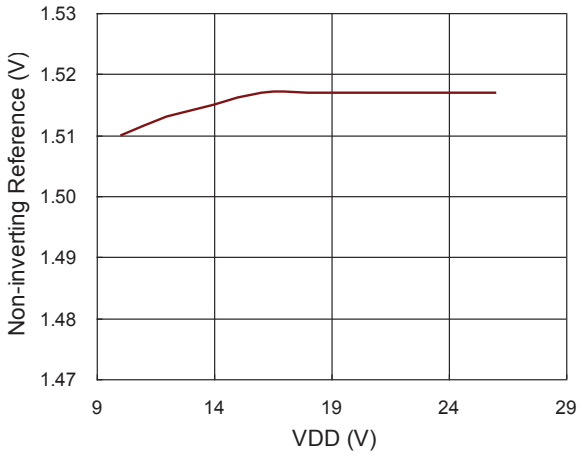
Typical Application Circuit

Boost PFC Pre-Regulator

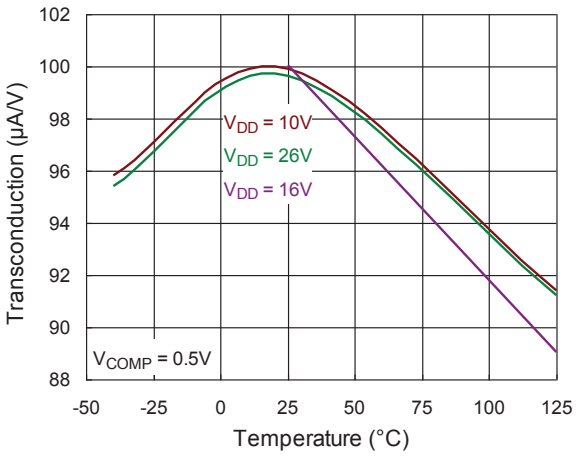


Typical Operating Characteristics

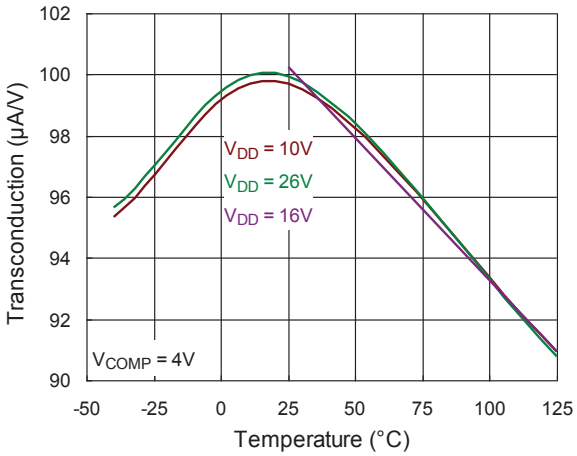
Non-inverting Reference vs. VDD



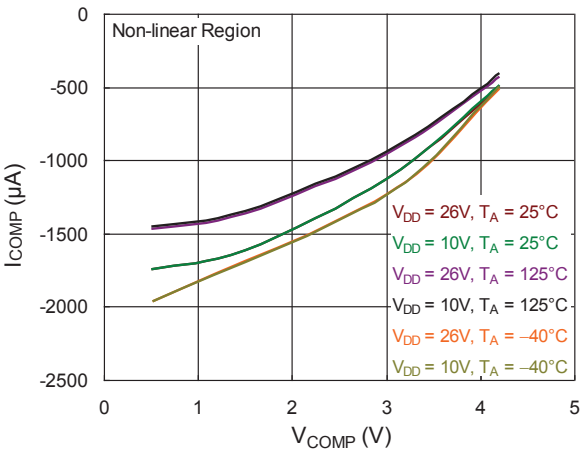
Transconduction vs. Temperature



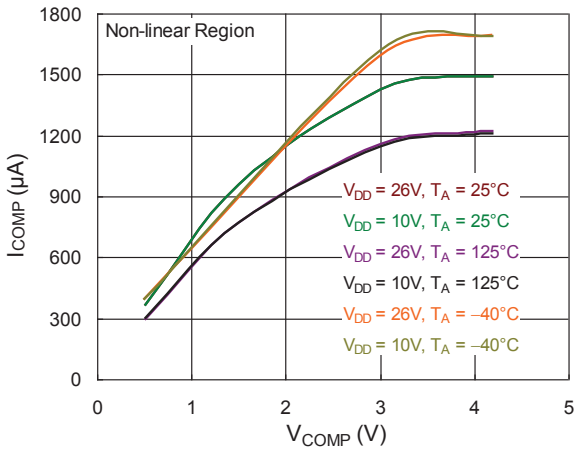
Transconduction vs. Temperature



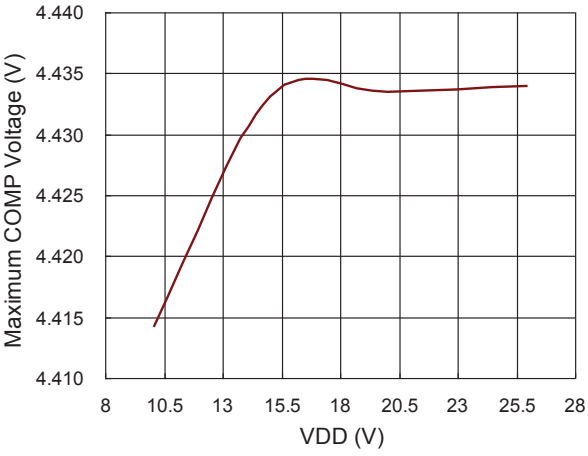
I_{COMP} vs. V_{COMP} (Sourcing)



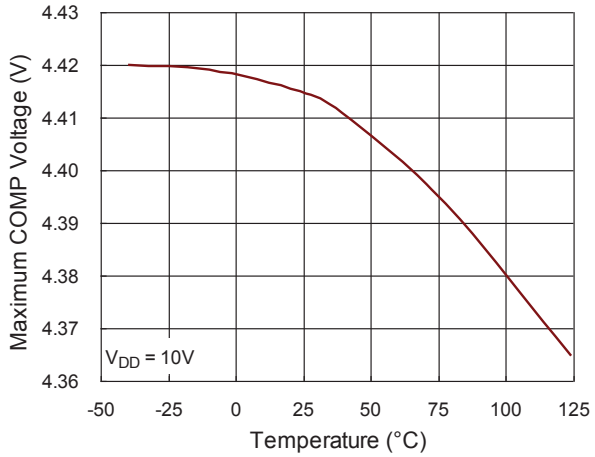
I_{COMP} vs. V_{COMP} (Sinking)



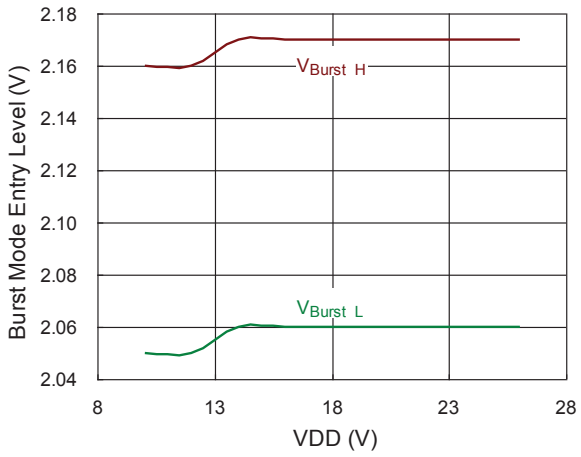
Maximum COMP Voltage vs. VDD



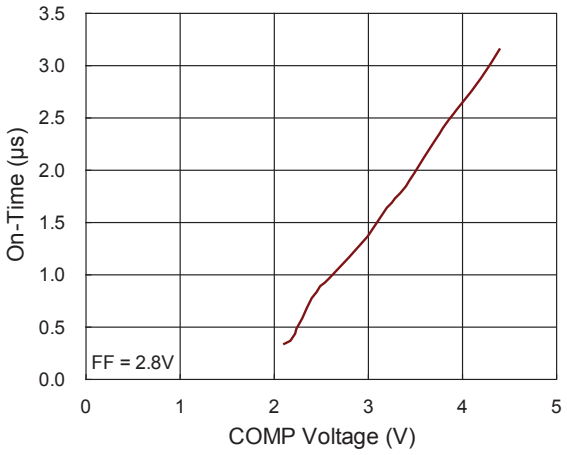
Maximum COMP Voltage vs. Temperature



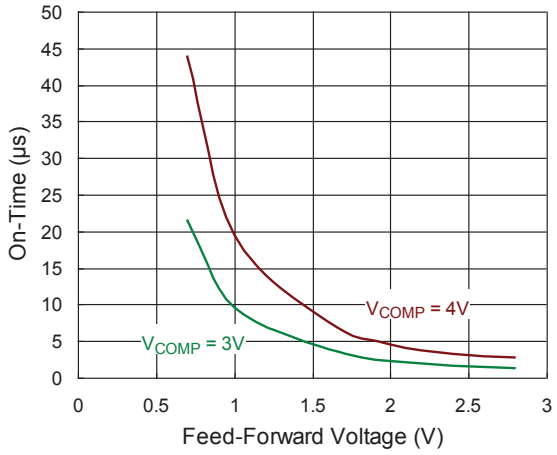
Burst Mode Entry Level vs. VDD



On-Time vs. COMP Voltage



On-Time vs. Feed-Forward Voltage



Application Information

Start-Up Circuit Design

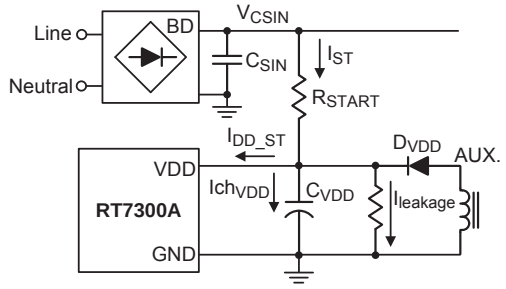


Figure 11. Start-Up Circuit

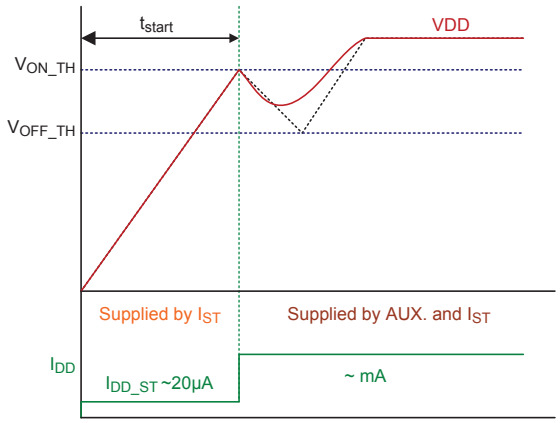


Figure 12. Start-Up Waveforms of VDD and I_{DD}

Figure 11 and Figure 12 show the equivalent start-up circuit and VDD waveform during start-up. In general, the start-up time (t_{start}) is required from system specification. The charging current (Ich_{VDD}) can be estimated by the following equation.

$$Ich_{VDD} = \frac{C_{VDD} \times V_{ON\_TH}}{t_{start}} \quad (8)$$

where C_{VDD} is the capacitor connected between VDD and GND, V_{ON_TH} is the power on threshold (12.45V typ.).

The start-up resistor (R_{start}) connected between V_{CSIN} and VDD should be able to support the charging current (Ich_{VDD}), start-up current (I_{DD_ST}) and leakage current ($I_{leakage}$) of C_{VDD} before the VDD is supported by the auxiliary winding. The maximum start-up resistance can be calculated by the equation (11).

$$R_{Start} = \frac{\sqrt{2} \times Vin_{ac\_min}}{I_{DD\_ST} + Ich_{VDD} + I_{leakage}} \quad (9)$$

where Vin_{ac_min} is the minimum input voltage. Note that the start-up resistor must have adequate voltage rating for reliability. 2 resistors in series can be applied for most of applications.

For example, the system required start-up time is 3sec, Vin_{ac_min} = 75V and maximum I_{DD_ST} = 20μA. If C_{VDD} = 22μF is selected and the leakage current of C_{VDD} can be ignored, the start-up resistor should be less than 772kΩ.

The capacitor C_{FF} is applied to filter out the input ripple voltage. The corner frequency should be lower than line frequency (f_{line}). If the FF pin voltage is not flat, the PF and THD performance will be degraded.

$$\frac{1}{2\pi \times (R_{FF1} \,//\, R_{FF2}) \times C_{FF}} < 0.1 \times f_{line} \quad (10)$$

Boost Inductance Design

Differ from the traditional transient mode PFC, the Boost inductor design is based on the RT7300A internal parameters and the parameter "S".

$$S = \frac{R_{FF1} + R_{FF2}}{R_{FF2}} \quad (11)$$

Assume the maximum input power is Pin, the inductance of the Boost inductor can be derived as following equations.

$$I_{L\_pk} = 2 \times \frac{P_{in}}{V_{IN(MIN)}} \times \sqrt{2}$$

$$= \frac{\sqrt{2} \times V_{IN(MIN)}}{L_{PFC}} \times \frac{V_{COMP} \times C_{Ramp}}{0.5 \times gm_{Ramp} \times \left(\frac{\sqrt{2} \times V_{IN(MIN)}}{S} \times \frac{2}{\pi} \right)^2}$$

$$L_{PFC} = \frac{\pi^2 \times m \times V_{COMP\_OP} \times C_{Ramp} \times S^2}{8 \times P_{in} \times gm_{Ramp}}$$

$$= \frac{m \times S^2}{P_{in}} \times 13.63 \quad (\mu H) \quad (12)$$

where "m" is the ratio of V_{Comp}/V_{Comp_op} which is the derating factor of the maximum power. It's suggested to use 0.6 to 0.9 for the m factor.

Current Limit Setting

The maximum current of the power MOSFET is limited by the current sense resistor between the CS pin and GND. The threshold voltage at CS pin is 0.85V typically. The current sense resistor can be calculated by the equation (15) with the peak current of MOSFET.

$$R_{CS} = \frac{0.85V \times 80\%}{I_{L\_pk}} \quad (13)$$

Zero Current Detection

The zero current of inductor is detected from the auxiliary winding shown as typical application circuit. The R_{ZCD} is used to limit the current into ZCD pin to be lower than 2.5mA. Thus, the R_{ZCD} is determined by the equation as below.

$$R_{ZCD} > \frac{V_{OUT}}{N \times 2.5mA} \quad (14)$$

where V_{OUT} is the output voltage of the PFC converter and N is the turn ratio of auxiliary winding and Boost inductor.

MOSFET Selection

The RT7300A is designed to operate using an external N-channel power MOSFET. Important parameters for the power MOSFET are breakdown voltage (BV_{DSS}), threshold voltage (V_{GS_TH}), on-resistance ($R_{DS(ON)}$), total gate charge (Qg) and maximum current ($I_{D(MAX)}$). The gate driver voltage is from VDD and clamped under 13V typically. Lower Qg characteristics results in lower power losses and lower $R_{DS(ON)}$ results in higher efficiency. For high voltage application, it is important to select a device with low gate charge and balance the power consumption between switching loss and conduction loss.

Diode Selection

Since there is no reverse recovery loss of diode when converter operates in CRM, the diode choosing is based on reverse voltage, forward current and switching speed.

$$I_{D(RMS)} = I_{L\_pk} \times \sqrt{\frac{\sqrt{2} \times V_{IN(MIN)}}{\pi \times V_{OUT}}} \quad (15)$$

$$V_{D(PK)} = V_{OUT} \quad (16)$$

Output Capacitor Selection

The hold-up time and output voltage (V_{OUT}) are the major requirements for determining the output capacitance. The narrow V_{OUT} range can improve the efficiency of DC/DC converter in next power stage. Lower ESR can reduce the power loss of PFC converter and get longer lifetime.

$$C_{OUT(MIN)} = \frac{2 \times P_{IN} \times \eta \times T_{Holdup}}{V_{OUT}^2 \times V_{OUT(MIN)}^2} \quad (17)$$

$$I_{C(RMS)} = \sqrt{I_{L\_pk}^2 \times \frac{\sqrt{2} \times V_{IN(MAX)}}{\pi \times V_{OUT}} - \left(\frac{\eta P_{IN}}{V_{OUT}}\right)^2 + (\text{ac RMS load current})^2} \quad (18)$$

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For SOP-8 package, the thermal resistance, θ_{JA}, is 160°C/W on a standard JEDEC 51-3 single-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (160°C/W) = 0.625W for SOP-8 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 13 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

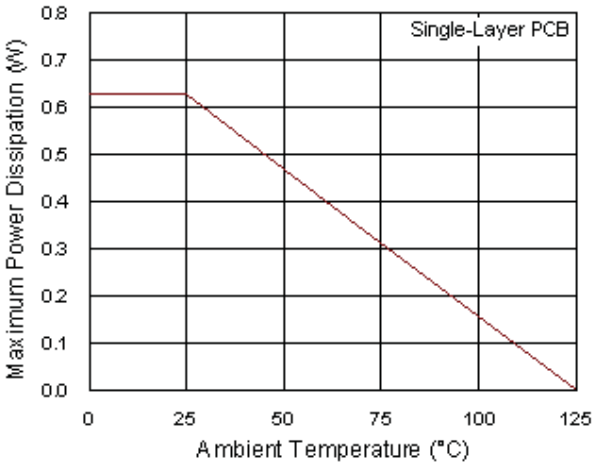


Figure 13. Derating Curve of Maximum Power Dissipation

Layout Considerations

A proper PCB layout can abate unknown noise interference and EMI issue in the switching power supply. Please refer to the guidelines when designing a PCB layout for switching power supply.

- The current path(1) from input capacitor, inductor, MOSFET, R_{CS} return to input capacitor and the current path(2) from input capacitor, inductor, output diode, output filter capacitor return to input capacitor are high frequency current loops. The path(3) from GD pin, MOSFET, R_{CS} to ground is also a high frequency current loop. They must be as short as possible to decrease noise coupling and kept a space to other low voltage traces, such as IC control circuit paths, especially. Besides, the path(4) between MOSFET ground(b) and IC ground(d) is recommended to be as short as possible, too.
- It is good for reducing noise, output ripple and EMI issue to separate ground traces of input capacitor(a), MOSFET(b), auxiliary winding(c) and IC control circuit(d). Finally, connect them together on input capacitor ground(a). The areas of these ground traces should be kept large.
- Placing bypass capacitor for abating noise on IC is highly recommended. The capacitors C_{INV} and C_{CS} should be placed as close to controller as possible.
- In addition, apply sufficient copper area at the anode and cathode terminal of the diode for heat-sinking. It is recommended to apply a larger area at the quiet cathode terminal. A large anode area will induce high-frequency radiated EMI.

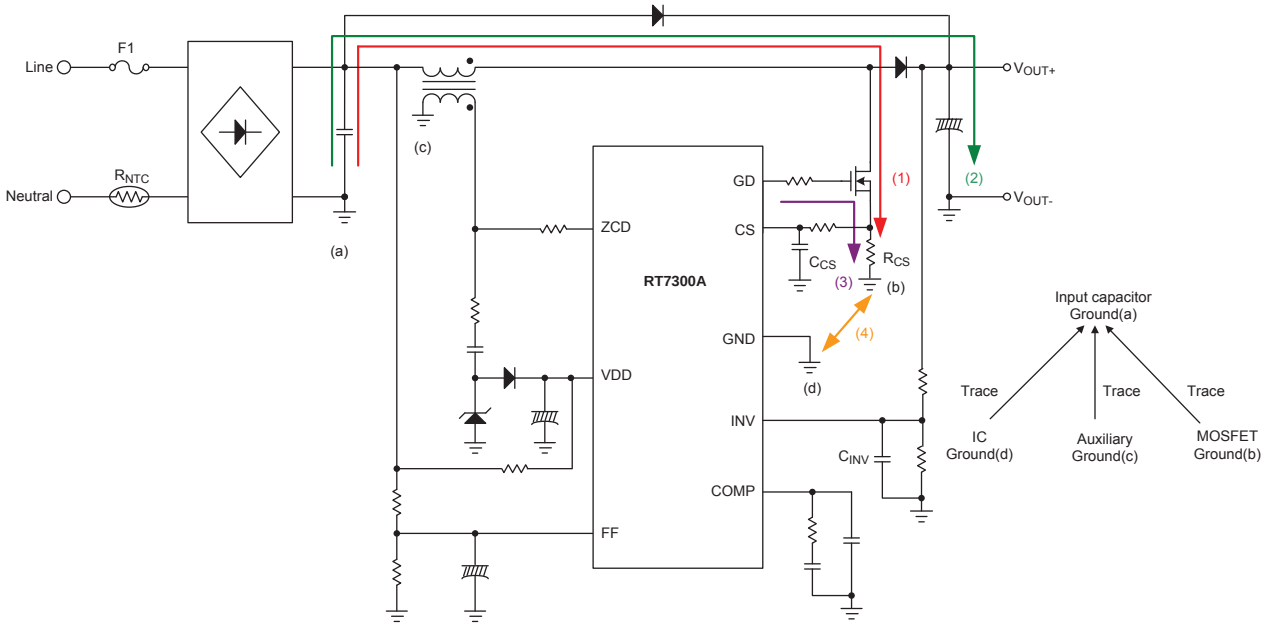
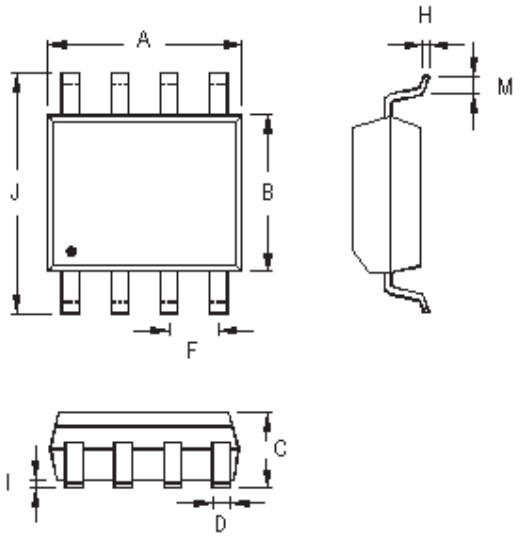


Figure 14. PCB Layout Guide

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.170	0.254	0.007	0.010
I	0.050	0.254	0.002	0.010
J	5.791	6.200	0.228	0.244
M	0.400	1.270	0.016	0.050

8-Lead SOP Plastic Package

Richtek Technology Corporation
14F, No. 8, Tai Yuen 1st Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789