

### Features

- Frequency range : 170MHz to 2100MHz
- SMD seam sealing ceramic package
- Supply voltage : 2.5V, 3.3V
- LVDS output
- Low phase noise and phase jitter
- Tri-state function available
- External dimensions (mm)  
L : 7.0 x W : 5.0 x H : 1.7
- RoHS compliant & Pb free

### Applications

- Networking, Telecommunication, Data communication, Switch, Server, Storage
- Fibre channel, Ethernet, SONET, SATA, SAS, PCI-Express
- Optical module
- Microprocessor, DSP, FPGA, Clock source for ADC and DAC
- Test and measurement

### Electrical Characteristics

| Item  | QTM750DH                   | Conditions                     |
|---|----------------------------|--------------------------------|
| Frequency Range ( $F_0$ )   | 170MHz ~ 2100MHz           |                                |
| Frequency Stability ( $F_{stab}$ ) over Operating Temperature Range ( $T_{OTR}$ ) | $\pm 50$ ppm, $\pm 25$ ppm | -40°C ~ +85°C, Note [1]        |
| Operating Temperature Range ( $T_{OTR}$ )   | -40°C ~ +85°C              |                                |
| Supply Voltage ( $V_{DD}$ )   | 2.5V, 3.3V                 | $V_{DD} \pm 10\%$              |
| Current Consumption ( $I_{DD}$ )  | 100 mA Max.                |                                |
| Output Type   | LVDS                       |                                |
| Output Load   | 100 $\Omega$               |                                |
| Offset Voltage  | 1.25V Typ.                 |                                |
| Differential Output Voltage   | 247mV Min. / 454mV Max.    | 170MHz ~ 700MHz                |
|   | 150mV Min. / 454mV Max.    | 700MHz ~ 2100MHz               |
| Rise & Fall Time ( $T_r / T_f$ )  | 0.5 ns Max.                | 20% ~ 80% of output swing      |
| Duty Cycle  | 45% ~ 55%                  |                                |
| Start-up Time   | 10 ms Max.                 |                                |
| Enable Voltage High, Logic "1"  | 70% $V_{DD}$ Min.          | Input to OE pin<br>Note [2]    |
| Enable Voltage Low, Logic "0"   | 30% $V_{DD}$ Max.          |                                |
| Phase Jitter ( $F_0 = 622.08$ MHz)  | 150fs Typ. / 200fs Max.    | 12kHz ~ 20MHz, RMS             |
| Aging ( $F_{aging}$ )   | $\pm 3$ ppm Max.           | at 25°C $\pm 3$ °C, first year |
| Storage Temperature Range ( $T_{STR}$ )   | -55°C ~ +125°C             |                                |

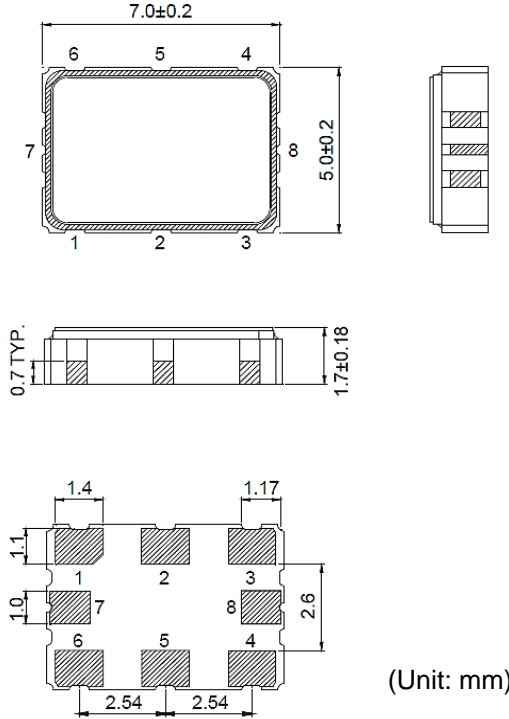
#### Notes:

[1] Inclusive of frequency tolerance at 25°C, variations over temperature, supply voltage and vibration.

[2] Output will be enabled if OE is Logic "1" or Open; Output will be disabled if OE is Logic "0".

[3] The standard testing environment except temperature test is 25°C $\pm 5$ °C, 40%~70% relative humidity.

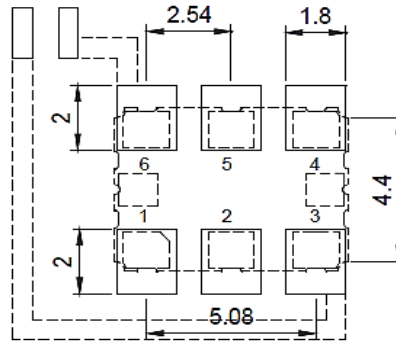
### Dimensions



### Pin function

|       |                         |
|-------|-------------------------|
| Pin 1 | OE                      |
| Pin 2 | NC                      |
| Pin 3 | GND                     |
| Pin 4 | OUT                     |
| Pin 5 | $\overline{\text{OUT}}$ |
| Pin 6 | V <sub>DD</sub>         |
| Pin 7 | NC                      |
| Pin 8 | NC                      |

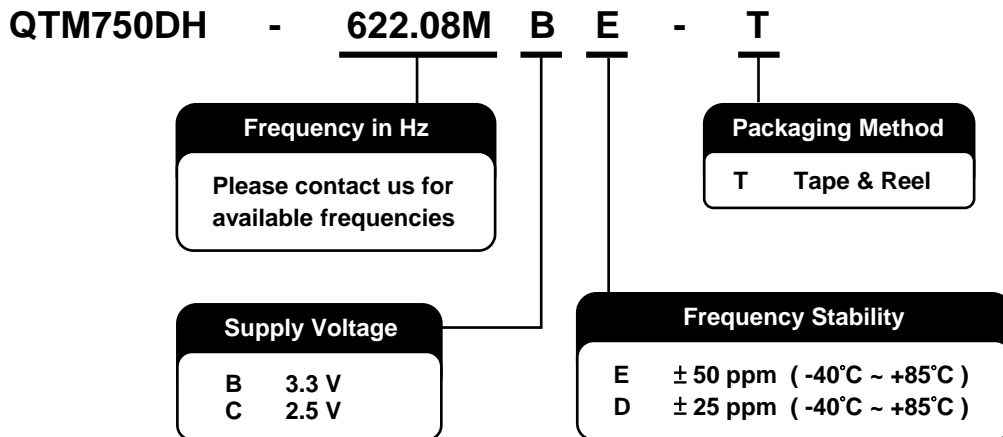
### Recommended pad layout



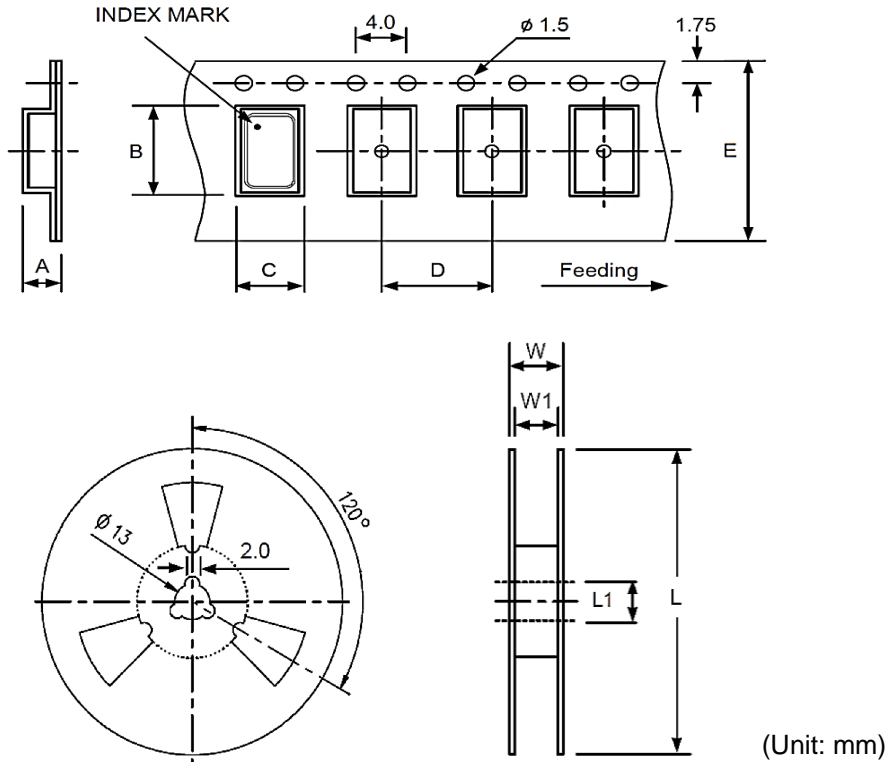
\* Pad dimension tolerance is  $\pm 0.2\text{mm}$

\* Power supply decoupling capacitor is required.

### Ordering Information



### Packing



(Unit: mm)

| DIMENSIONS | A    | B    | C    | D    | E    | L     | L1   | W    | W1   |
|------------|------|------|------|------|------|-------|------|------|------|
|            | 2.00 | 7.90 | 5.45 | 8.00 | 16.0 | 180.0 | 13.0 | 20.5 | 16.0 |

### Reflow Profile

Solder melting point :  $220^\circ\text{C} \pm 10^\circ\text{C}$ , 60 sec. Min., 200 sec. Max.

Peak temperature :  $260^\circ\text{C} \pm 10^\circ\text{C}$ , 10 sec. Min., 30 sec. Max.

