QE202
EMI Reduction IC

Features

- FCC approved method of EMI attenuation
- Non-PLL phase controlled active EMI management architecture
- Generates a 1X low EMI Phase Modulated replication of the input signal
- VDD 1.65V ~ 2.0V, 10MHz to 38MHz
- VDD 2.5V ~ 3.6V, 10MHz to 38MHz
- Multiple Deviation Selections
- Minimum frequency deviation selection capability
- Power Down Mode
- 8-pin WDFN package
- Supports automotive reliability standard:
  AEC-Q100 Grade 1 and Grade 2 certified

Applications

- The QE202 series is targeted towards mobile platforms such as cell phones, MIDs, Netbooks and other "power and space" sensitive applications.

Product Description

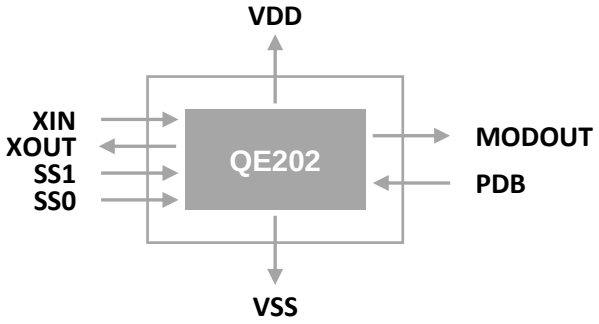
The QE202 is a versatile 1x Active EMI management IC designed to provide system wide reduction of Electromagnetic Interference (EMI) and Radio Frequency Interference (RFI) from clock and data sources. The QE202 allows significant system cost savings by reducing the number of circuit board layers, ferrite beads, shielding and other passive components that are traditionally required to pass EMI regulations.

The QE202 family of mobile active EMI management ICs is unique in its design and is based on the phase controlled active EMI management technology. This allows operation on aperiodic as well periodic signals. By the precise placement of the edges of the reconstructed input signal, the peak energy of the output is distributed over a wider and controlled energy band thereby significantly lowering system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators.

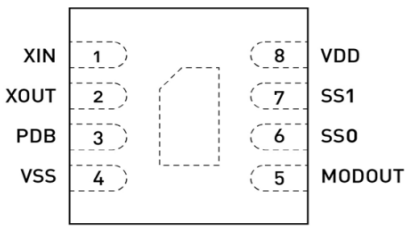
The QE202 has an input frequency range of 10MHz to 38MHz over a wide voltage range of 1.65V to 3.6V. The device can be placed in a “power save mode” by setting the PDB pin to GND where in it draws typically 0.1uA and also sets the MODOUT pin to a High-Z state. The device has two “deviation control pins” SS1 and SS0 to allow flexibility and optimization of both EMI compliance as well as in system design.

The device is available in 8 pin DFN package.

Block Diagram



Pin Configuration



Pin Description

Pin#	Pin Name	Type	Description
1	XIN	I	Crystal Oscillator Input
2	XOUT	O	Crystal Oscillator Output
3	PDB	I	Power Down pin. Active Low. Forces MODOUT to High-Z
4	VSS	P	System ground reference input.
5	MODOUT	O	1X phase modulated buffered output.
6	SS0	I	Deviation Control Pin (refer Functionality Table) Internal Pull-Up Resistor. Recommend external Pull-Down Resistor 0Ω
7	SS1	I	Deviation Control Pin (refer Functionality Table) Internal Pull-Down Resistor Recommend external Pull-Up Resistor 0Ω
8	VDD	O	System Power Supply pin

Operating Conditions

Parameter	Description	Min	Max	Unit
$VDD_{(3.3V)}$	Supply Voltage	1.65	3.6	V
T_A	Operating Temperature (Ambient Temperature)	-40	+125	°C
C_L	Load Capacitance		20	pF
C_{IN}	Input Capacitance		5	pF
Note: Please refer to ordering information for T_A				

Absolute Maximum Rating

Symbol	Parameter	Rating	Unit
V_{in}	Voltage on any pin with respect to Ground	-0.5 to +4.6	V
T_{STG}	Storage temperature	-65 to +125	°C
T_s	Max. Soldering Temperature (10 sec)	260	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22- A114-B)	2	KV
Note: These are stress ratings only and are not implied nor guaranteed for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.			

Functional Table

VDD (V)	Freq. Range (MHz)	Freq. (MHz)	Deviation (%)							
			SS1	SS0	SS1	SS0	SS1	SS0	SS1	SS0
			0	0	0	1	1	0	1	1
1.8	10 ~ 38	12	±0.09		±0.20		±0.28		±0.35	
		24	±0.13		±0.25		±0.30		-	
		27	±0.14		±0.23		±0.26		-	
		37	±0.12		-		-		-	
3.3	10 ~ 38	12	±0.06		±0.12		±0.18		±0.22	
		24	±0.10		±0.19		±0.26		±0.32	
		27	±0.12		±0.23		±0.31		±0.37	
		37	±0.12		±0.23		±0.30		±0.32	
Note: Frequency deviation can vary over voltage and temperature by ±20%.										

DC Electrical Characteristics (3.3 +/-0.3V)

Parameter	Description	Test Conditions		Min	Typ	Max	Unit
VDD	Supply Voltage			3.0	3.3	3.6	V
V_{IH}	Input HIGH Voltage			0.66 * VDD			V
V_{IL}	Input LOW Voltage					0.33 * VDD	V
I_{IH}	Input HIGH Current (pin 5 and 6)	V_{IN} = VDD				10	µA
I_{IL}	Input LOW Current (pin 5 and 6)	V_{IN} = 0V				10	µA
V_{OH}	Output HIGH Voltage	I_{OH} = -8mA		0.75 * VDD			V
V_{OL}	Output LOW Voltage	I_{OL} = +8mA				0.25 * VDD	V
I_{CC}	Static Supply Current	PDB = VSS			0.1	1.0	µA
I_{DD}	Dynamic Supply Current (SS1=1, SS0=1)	27MHz	Unloaded		7.0	8.0	mA
			10pF load		8.0	9.0	
Z_0	Output Impedance				25		Ω

Switching Characteristics (3.3V +/-0.3V)

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
INPUT	Input Frequency		10	24	38	MHz
MODOUT	Output Frequency		10	24	38	MHz
T_d	Duty Cycle[1,2] = (t_2 / t_1)*100	Measured at VDD/2	45	50	55	%
t_3	Output Rise Time [1,2]	Measured between 20% to 80%	0.6	1.5	2.5	nS
t_4	Output Fall Time [1,2]	Measured between 80% to 20%	0.6	1.4	2.5	nS
t_J	Cycle-to-cycle jitter [2]	Unloaded outputs 27MHz		±250		pS

Note:
1. All parameters specified with loaded outputs.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production.

DC Electrical Characteristics (1.8 +/-0.15V)

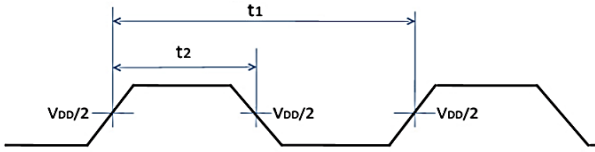
Parameter	Description	Test Conditions		Min	Typ	Max	Unit
VDD	Supply Voltage			1.65	1.8	1.95	V
V_{IH}	Input HIGH Voltage			0.66 * VDD			V
V_{IL}	Input LOW Voltage					0.33 * VDD	V
I_{IH}	Input HIGH Current (pin 5 and 6)	V_{IN} = VDD				10	µA
I_{IL}	Input LOW Current (pin 5 and 6)	V_{IN} = 0V				10	µA
V_{OH}	Output HIGH Voltage	I_{OH} = -4mA		0.75 * VDD			V
V_{OL}	Output LOW Voltage	I_{OL} = +4mA				0.25 * VDD	V
I_{CC}	Static Supply Current	PDB = VSS			0.1	1.0	µA
I_{DD}	Dynamic Supply Current (SS1=1, SS0=1)	27MHz	Unloaded		3.0	4.0	mA
			10pF load		3.5	4.5	
Z_0	Output Impedance				25		Ω

Switching Characteristics (1.8 +/-0.15V)

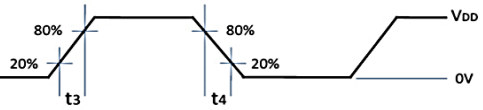
Parameter	Description	Test Conditions	Min	Typ	Max	Unit
INPUT	Input Frequency		10	24	38	MHz
MODOUT	Output Frequency		10	24	38	MHz
T_d	Duty Cycle[1,2] = (t_2 / t_1)*100	Measured at VDD/2	45	50	55	%
t_3	Output Rise Time [1,2]	Measured between 20% to 80%	0.8	1.5	1.8	nS
t_4	Output Fall Time [1,2]	Measured between 80% to 20%	0.8	1.0	1.8	nS
t_J	Cycle-to-cycle jitter [2]	Unloaded outputs 27MHz		±250		pS

Note:
1. All parameters specified with loaded outputs.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production.

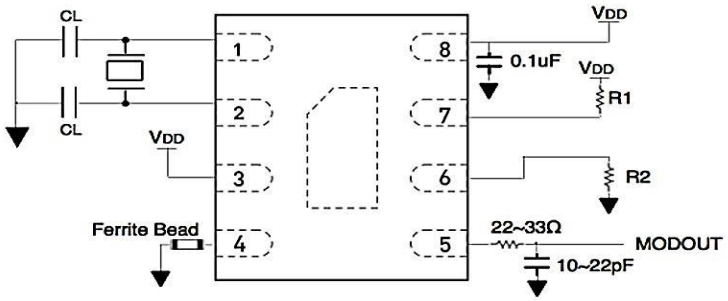
Duty Cycle Timing



All Outputs Rise/Fall Time

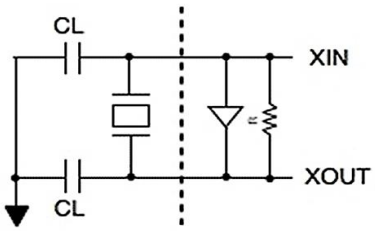


Application Schematic



R1/R2 : Open or 0Ω

Crystal Oscillator Circuit



CL = 2x(Cp-Cs)
Cp: load capacitance of Crystal
Cs: Stray capacitance (PCB trace + Input cap. of IC)

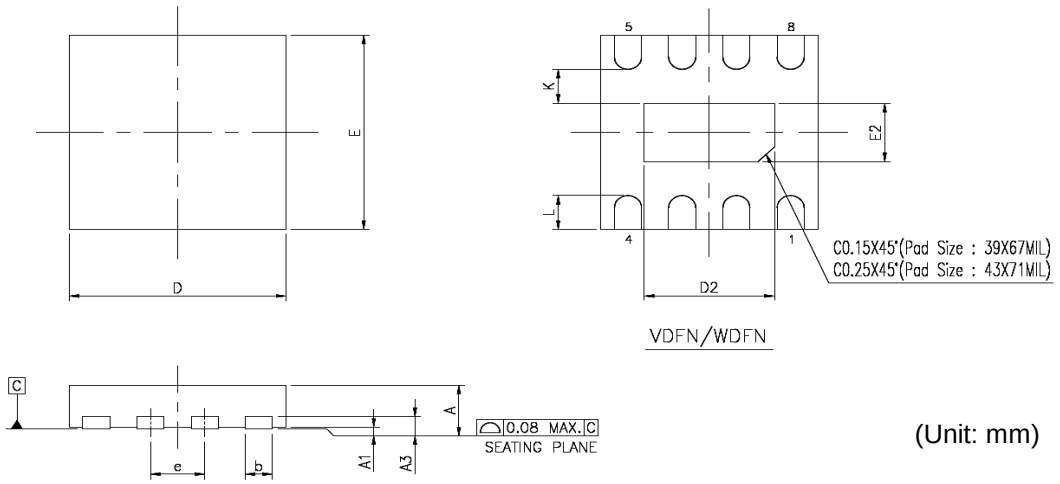
Ordering Information

Part Number	Temp. Grade Indicator	Temp. Grade	Temp. Range
QE202C	C	Commercial	0°C ~ +70°C
QE202 I	I	Industrial	-20°C ~ +85°C
QE202E	E	AEC-Q100, Grade 2	-40°C ~ +105°C
QE202A	A	AEC-Q100, Grade 1	-40°C ~ +125°C

Package Dimension

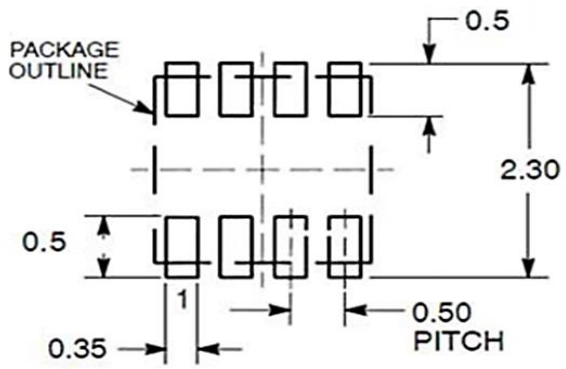
WDFN (X208)

Top View **Bottom View**



(Unit: mm)

Recommended footprint



JEDEC OUTLINE	MO-229		
PKG CODE	WDFN(X208)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.20	0.25	0.30
D	2.00 BSC		
E	2.00 BSC		
e	0.50 BSC		
K	0.20	—	—

	D2			E2			L			LEAD FINISH		JEDEC CODE	VDFN	WDFN	UDFN	TDFN OPTION 1	TDFN OPTION 2
PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF						
⚠2 39*X67* MIL	1.15	1.20	1.25	0.60	0.65	0.70	0.20	0.35	0.45	V	X	N/A	V	V			

"*" is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.

(Unit: mm)