QDD-400G-LR8-S-40-C
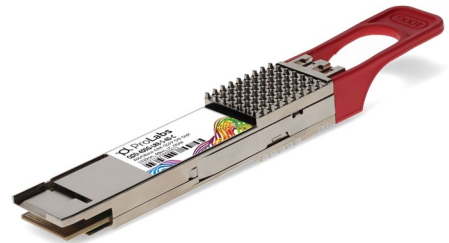
Cisco® QDD-400G-LR8-S-40 Compatible TAA Compliant 400GBase-ER8 QSFP-DD Transceiver (SMF, 8x50G PAM4, 40km, LC, DOM) CMIS 4.0

Features:

- Compliant with IEEE std 802.3cn-2019
- Compliant with QSFP-DD MSA HW Rev 5.1
- Compliant with QSFP-DD CMIS Rev 4.0
- Power dissipation <14W
- Single 3.3V power supply
- Case operating temperature 0°C to 70°C
- Maximum link length of 40km on Single Mode Fiber (SMF)
- 8x50G PAM4 retimed 400GAUI-8 electrical interface
- Class 1/1M Laser
- Duplex LC receptacles
- I2C management interface
- RoHS Compliant

Applications

- 400GBase Ethernet
- Access and Enterprise

Product Description

This Cisco® QDD-400G-LR8-S-40 compatible transceiver provides 400GBase-ER8 8x50G PAM4 throughput up to 40km over single-mode fiber (SMF) at a wavelength of 1310nm using an LC connector. It is built to MSA standards and is uniquely serialized and data-traffic and application tested to ensure that they will integrate into your network seamlessly. Digital optical monitoring (DOM) support is also present to allow access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

ProLabs' transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S. – made or designated country end products."

Regulatory Compliance

- ESD to the Electrical PINs: compatible with MIL-STD-883E Method 3015.4
- ESD to the LC Receptacle: compatible with IEC 61000-4-3
- EMI/EMC compatible with FCC Part 15 Subpart B Rules, EN55022:2010
- Laser Eye Safety compatible with FDA 21CFR, EN60950-1& EN (IEC) 60825-1,2
- RoHS compliant with EU RoHS 2.0 directive 2015/863/EU

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Storage Temperature	T_s	-40		85	°C	
Maximum Supply Voltage	Vcc	-0.5		3.6	V	
Relative Humidity (non-condensing)	RH	5		95	%	
Operating Case Temperature	T_{opr}	0		70	°C	
Relative Humidity (non-condensing)	RH	5		85	%	
Control Input Voltage	V_I	-0.3		Vcc+0.5	V	
Control Output Current	Io	-20		20	mA	
Signaling Speed per Lane	DRL		26.5625		GBd	
Operating Distance		0.002		40	km	1

Notes:

1. Channel insertion loss is 18dB for 40km.

Electrical Characteristics (High Speed Signal- compliant with IEEE 802.3 400GAUI-8)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	Vcc	3.135	3.3	3.465	V	
Maximum Power Dissipation	P$_D$			14	W	
Maximum Power Dissipation, Low Power Mode	P$_{DLP}$			1.5	W	
Instantaneous peak current at hot plug	Icc_IP			5600	mA	
Sustained peak current at hot plug	Icc_SP			4620	mA	
Control Input Voltage High	V$_{IH}$	Vcc*0.7		Vcc+0.3	V	
Control Input Voltage Low	V$_{IL}$	-0.3		Vcc*0.3	V	
Two Wire Serial Interface Clock Rate				400	kHz	
Power Supply Noise				66	mVpp	
Rx Differential Data Output Load			100		Ohm	
Transmitter						
AC Common- mode output Voltage (RMS)				17.5	mV	
Differential Output Voltage				900	mV	
Near end Eye Height, differential		70			mV	
Far-end Eye height, differential		30			mV	
Eye width Far end pre-cursor ratio				2.5	%	
Differential Termination Mismatch				10	%	
Transition Time (min, 20% to 80%)		9.5			ps	
DC common mode Voltage		-350		2850	mV	
Receiver						
Differential pk-pk input Voltage tolerance		900			mV	
Differential termination mismatch				10	%	
Single-ended voltage tolerance range		-0.4		3.3	V	
DC common mode Voltage		-350		2850	mV	
Low Speed Signal (compliant with QSFP-DD HW Rev 5.1						
Module output SCL and SDA	V$_{OL}$	0		0.4	V	
Module Input SCL and SDA	V$_{IL}$	-0.3		Vcc*0.3	V	
	V$_{IH}$	Vcc*0.7		Vcc+0.5	V	
InitMode, ResetL and ModSeIL	V$_{IL}$	-0.3		0.8	V	
	V$_{IH}$	2		Vcc+0.3	V	
IntL		0		0.4	V	
		Vcc-0.5		Vcc+0.3	V	

Optical Characteristics

Parameter		Symbol	Min	Typical	Max	Unit	Notes
Transmitter							
Transmit wavelengths	L0	Λc_0	1272.55	1273.55	1274.54	nm	
	L1	Λc_1	1276.89	1277.89	1278.89	nm	
	L2	Λc_2	1281.25	1282.26	1283.27	nm	
	L3	Λc_3	1285.65	1286.67	1287.68	nm	
	L4	Λc_4	1294.53	1295.56	1296.59	nm	
	L5	Λc_5	1299.02	1300.06	1301.09	nm	
	L6	Λc_6	1303.54	1304.59	1305.63	nm	
	L7	Λc_7	1308.09	1309.14	1310.19	nm	
Side Mode Suppression Ratio		SMSR	30			dB	
Total Average Launch Power		AOP_T			14.6	dBm	
Average Launch Power, each lane		AOPL	0.6		5.6	dBm	1
Outer Optical Modulation Amplitude (OMAouter), each Lane		T_{OMA}	2.4		6.4	dBm	
Difference in Launch Power between any two Lanes (OMAouter)		D_T OMA			4	dB	
Launch Power in OMAouter minus TDECQ, each lane		$T_{OMA,TDECQ}$	1			dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane		TDECQ			3.4	dB	
TDECQ-10log10(Ceg)					3.4	dB	
Average Launch Powr of OFF Transmitter, each land		T_{OFF}			-30	dBm	
Extinction Ratio		ER	6			dB	
RIN15OMA		RIN			-132	dB/Hz	1
Optical Return Loss Tolerance		ORL			15	dB	
Transmitter Reflectance		T_R			-26	dB	2
Receiver							
Receiver wavelengths	L0	Λc_0	1272.55	1273.55	1274.54	nm	
	L1	Λc_1	1276.89	1277.89	1278.89	nm	
	L2	Λc_2	1281.25	1282.26	1283.27	nm	
	L3	Λc_3	1285.65	1286.67	1287.68	nm	
	L4	Λc_4	1294.53	1295.56	1296.59	nm	
	L5	Λc_5	1299.02	1300.06	1301.09	nm	
	L6	Λc_6	1303.54	1304.59	1305.63	nm	
	L7	Λc_7	1308.09	1309.14	1310.19	nm	
Damage Threshold, each Lane		AOPD	-3.4			dBm	

Average Receive Power, each Lane	AOPR	18.6		-4.4	dBm	
Receiver Power (OMAouter), each Lane	OMAR			-3.6	dBm	
Difference in Receiver Power between any two Lanes (OMAouter)	DR_OMA			5.8	dB	
Receiver Reflectance	RR			-26	dB	
Receiver Sensitivity (OMAouter), each Lane	SOMA	-		Max(-16.1, SECQ-17.5)	dBm	3
Stressed Receiver Sensitivity (OMAouter), each Lane	SRS			-14.1	dBm	4
Conditions of stressed receiver sensitivity test:						
Stressed eye closure for PAM4 (SECQ), lane under test			3.4		dB	
SECQ-10log10(Ceg), lane under test				3.4	dB	
OMAouter of each aggressor lane			-8.3		dBm	

Notes:

1. Average launch power, each lane (min) is informative and not the principle of signal strength
2. Transmitter reflectance is defined looking into the transmitter
3. Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with SECQ of 1.4 dB.
4. Measured with conformance test signal at TP3 for the BER = 2.4 x 10^{-4}

Timing for Soft Control and Status Functions

Parameter	Symbol	Min	Max	Unit	Notes
MgmtInit Duration			2000	ms	
ResetL Assert Time	t_reset_init	10		µs	
IntL Assert Time	ton_IntL		200	ms	
IntL Deassert Time	toff_IntL		500	µs	
Rx LOS Assert Time	ton_losf		100	ms	
Flag Assert Time	ton_flag		200	ms	
Mask Assert Time	ton_mask		100	ms	
Mask Deassert Time	toff_mask		100	ms	
Module Select Wait Time	ModSelL Wait Time		N/A		Not support

I/O Timing for Squelch and Disable

Parameter	Symbol	Min	Max	Unit	Notes
Rx Squelch Assert Time	ton_Rxsq		50	ms	
Tx Squelch Assert Time	ton_Txsq		400	ms	
Tx Squelch Deassert Time	toff_Txsq		1500	ms	Based on Modulation
Tx Disable Assert Time (fast mode)	ton_Txdisf		3	ms	
Tx Disable Deassert Time (fast mode)	toff_Txdisf		10	ms	
Rx Output Disable Assert Time	ton_Rxdis		100	ms	
Rx Output Disable Deassert Time	toff_Rxdis		100	ms	
Squelch Disable Assert Time	ton_sqdis		N/A	ms	Not support
Squelch Disable Deassert Time	toff_sqdis		N/A	ms	Not support

Digital Diagnostics

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	±3	ºC	Internal
Voltage	0 to V_{CC}	0.1	V	Internal
Tx Bias Current (Each Lane)	0 to 100	10%	mA	Internal
Tx Output Power (Each Lane)	-0.6 to +5.6	±3	dB	Internal
Rx Receive Power (Each Lane)	-18.6 to -4.4	±3	dB	Internal

Pin Descriptions

Pin	Logic	Symbol	Name/Descriptions
1		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-inverted Data Input
4		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-inverted Data Input
7		GND	Ground
8	LVTTL-I	ModSelL	Module Select
9	LVTTL-I	ResetL	Module Reset
10		VccRx	+3.3V Power Supply Receiver
11	LVCMOS-I/O	SCL	2-wire serial interface clock
12	LVCMOS-I/O	SDA	2-wire serial interface data
13		GND	Ground
14	CML-O	Rx3p	Receiver Non-inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output
16		GND	Ground
17	CML-O	Rx1p	Receiver Non-inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output
19		GND	Ground
20		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-inverted Data Output
23		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-inverted Data Output
26		GND	Ground
27	LVTTL-O	ModPrsL	Module Present
28	LVTTL-O	IntL	Interrupt
29		VccTx	+3.3V Power Supply Transmitter
30		Vcc1	+3.3V Power Supply
31	LVTTL-I	InitMode	Initialization mode
32		GND	Ground
33	CML-I	Tx3p	Transmitter Non-inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input
35		GND	Ground
36	CML-I	Tx1p	Transmitter Non-inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input
38		GND	Ground
39		GND	Ground

40	CML-I	Tx6n	Transmitter Inverted Data Input
41	CML-I	Tx6p	Transmitter Non-inverted Data Input
42		GND	Ground
43	CML-I	Tx8n	Transmitter Inverted Data Input
44	CML-I	Tx8p	Transmitter Non-inverted Data Input
45		GND	Ground
46		Reserved	
47		VS1	Module Vendor Specific 1
48		VccRx1	3.3V Power Supply
49		VS2	Module Vendor Specific 2
50		VS3	Module Vendor Specific 3
51		GND	Ground
52	CML-O	Rx7p	Receiver Non-inverted Data Output
53	CML-O	Rx7n	Receiver Inverted Data Output
54		GND	Ground
55	CML-O	Rx5p	Receiver Non-inverted Data Output
56	CML-O	Rx5n	Receiver Inverted Data Output
57		GND	Ground
58		GND	Ground
59	CML-O	Rx6n	Receiver Inverted Data Output
60	CML-O	Rx6p	Receiver Non-inverted Data Output
61		GND	Ground
62	CML-O	Rx8n	Receiver Inverted Data Output
63	CML-O	Rx8p	Receiver Non-inverted Data Output
64		GND	Ground
65		NC	Not connected
66		Reserved	
67		VccTx1	3.3V Power Supply
68		Vcc2	3.3V Power Supply
69		Reserved	
70		GND	Ground
71	CML-I	Tx7p	Transmitter Non-inverted Data Input
72	CML-I	Tx7n	Transmitter Inverted Data Input
73		GND	Ground
74	CML-I	Tx5p	Transmitter Non-inverted Data Input
75	CML-I	Tx5n	Transmitter Inverted Data Input
76		GND	Ground

Notes:

1. Circuit ground is internally isolated from chassis ground.

MSA Compliant Connector

GND	39		GND	1	
TX6n	40		TX2n	2	
TX6p	41		TX2p	3	
GND	42		GND	4	
TX8n	43		TX4n	5	
TX8p	44		TX4p	6	
GND	45		GND	7	
Reserved	46		ModselL	8	
VS1	47		ResetL	9	
VccRx1	48		VccRx	10	
VS2	49		SCL	11	
VS3	50		SDA	12	
GND	51		GND	13	
RX7p	52		RX3p	14	
RX7n	53		RX3n	15	
GND	54		GND	16	
RX5p	55		RX1p	17	
RX5n	56		RX1n	18	
GND	57		GND	19	

Module Card Edge (Host Side) — **(Module Side)**
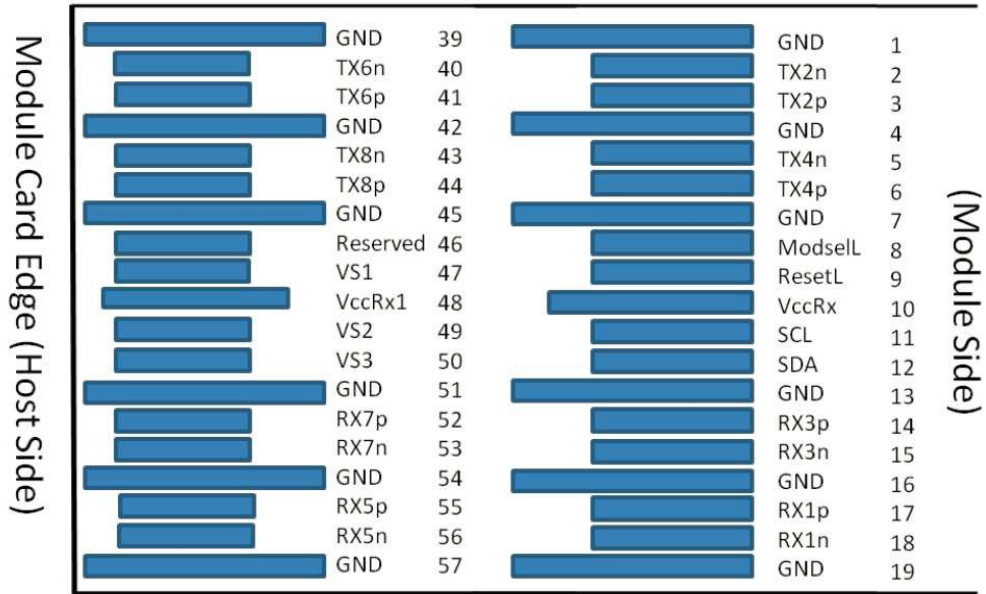
Bottom side viewed from bottom

|				
38	GND		76	GND
37	TX1n		75	TX5n
36	TX1p		74	TX5p
35	GND		73	GND
34	TX3n		72	TX7n
33	TX3p		71	TX7p
32	GND		70	GND
31	InitMode		69	Reserved
30	Vcc1		68	Vcc2
29	VccTx		67	VccTx1
28	IntL		66	Reserved
27	ModPrsL		65	NC
26	GND		64	GND
25	RX4p		63	RX8p
24	RX4n		62	RX8n
23	GND		61	GND
22	RX2p		60	RX6p
21	RX2n		59	RX6n
20	GND		58	GND

(Module Side) — **Module Card Edge (Host Side)**
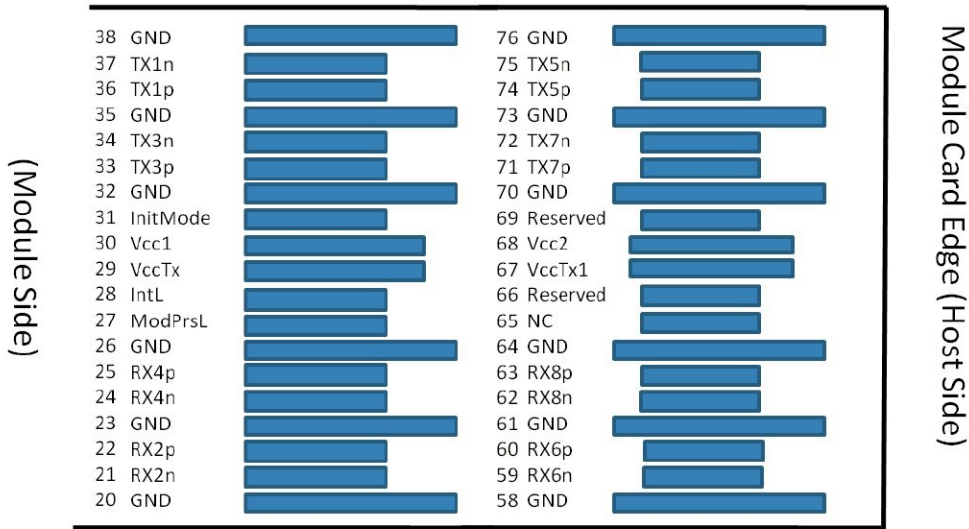
Top side viewed from top

Pin definitions of the module high speed inputs/outputs

Recommended QSFP-DD Host Board Schematic

QSFP-DD Optical Module
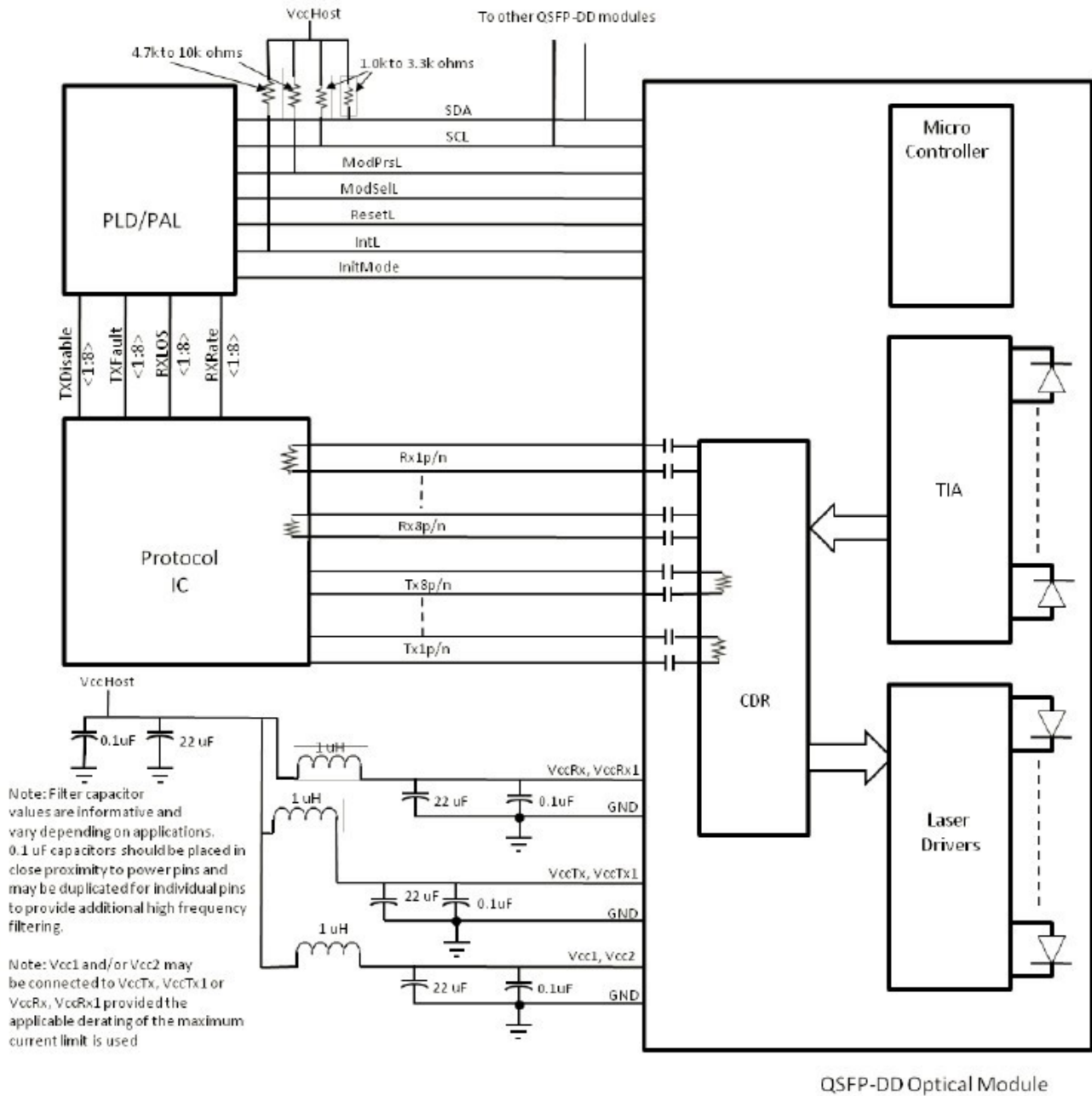
Transceiver Block Diagram
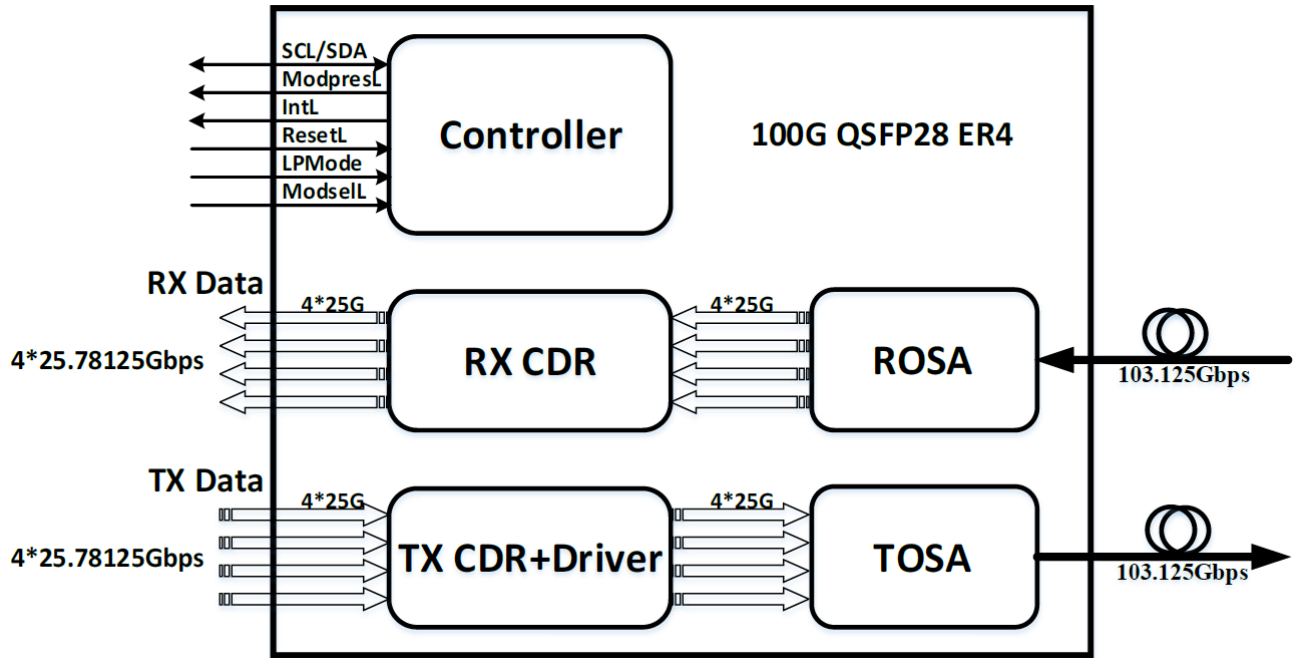
Mechanical Specifications
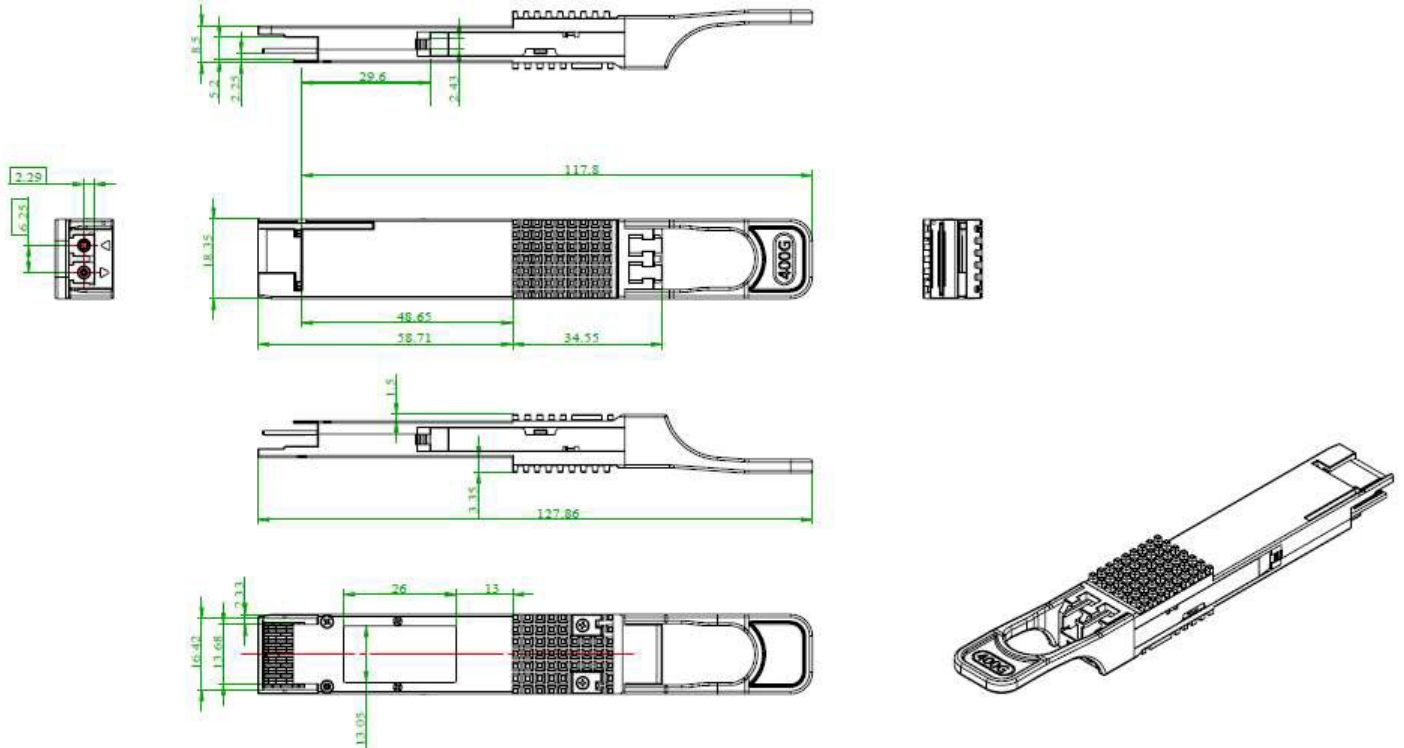
About ProLabs

Our experience comes as standard; for over 15 years ProLabs has delivered optical connectivity solutions that give our customers freedom and choice through our ability to provide seamless interoperability. At the heart of our company is the ability to provide state-of-the-art optical transport and connectivity solutions that are compatible with over 90 optical switching and transport platforms.

Complete Portfolio of Network Solutions

ProLabs is focused on innovations in optical transport and connectivity. The combination of our knowledge of optics and networking equipment enables ProLabs to be your single source for optical transport and connectivity solutions from 100Mb to 400G while providing innovative solutions that increase network efficiency. We provide the optical connectivity expertise that is compatible with and enhances your switching and transport equipment.

Trusted Partner

Customer service is our number one value. ProLabs has invested in people, labs and manufacturing capacity to ensure that you get immediate answers to your questions and compatible product when needed. With Engineering and Manufacturing offices in the U.K. and U.S. augmented by field offices throughout the U.S., U.K. and Asia, ProLabs is able to be our customers best advocate 24 hours a day.

Contact Information

ProLabs US
Email: sales@prolabs.com
Telephone: 952-852-0252

ProLabs UK
Email: salessupport@prolabs.com
Telephone: +44 1285 719 600