PUSB3TB6

ESD protection for ultra high-speed interfaces

23 August 2018 **Product data sheet**

1. General description

The device is designed to protect high-speed interfaces such as SuperSpeed and Hi - Speed USB combination, Secure Digital (SD) card 3.0 and Thunderbolt interfaces against ElectroStatic Discharge (ESD).

The device includes six high-level ESD protection diode structures for ultra high-speed signal lines and is encapsulated in a DFN2111-7 (SOT1358-1) leadless ultra small Surface-Mounted Device (SMD) plastic package.

All signal lines are protected by a special diode structure offering ultra low line capacitance of only 0.27 pF. These diodes utilize a unique snap-back structure in order to provide protection to downstream components from ESD voltages up to ±10 kV contact exceeding IEC 61000-4-2, level 4.

2. Features and benefits

- System ESD protection for USB 2.0 and USB 3.2 combination, SD card 3.0 and Thunderbolt interfaces
- All signal lines with integrated rail-to-rail clamping diodes for downstream ESD protection of ±10 kV exceeding IEC 61000-4-2, level 4
- Matched 0.5 mm trace spacing
- Signal lines with ≤ 0.05 pF matching capacitance between signal pairs
- Line capacitance of only 0.27 pF for each channel
- Design-friendly pass-through signal routing

3. Applications

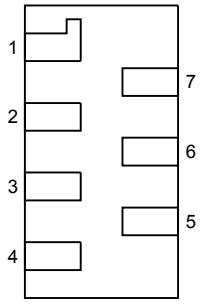
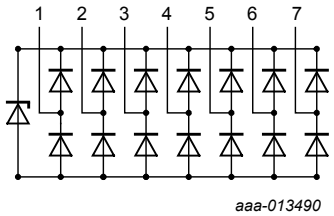
The device is designed for high-speed receiver and transmitter port protection:

- Portable and wearable devices
- Smartphones and tablet PCs
- TVs and monitors
- DVD recorders and players
- Notebooks, main board graphic cards and ports
- Set-top boxes and game consoles

nexperia

4. Pinning information

Table 1. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	CH1	channel 1 ESD protection	 Transparent top view XSON7 (SOT1358-1)	
2	GND	ground[1]		
3	CH2	channel 2 ESD protection		
4	CH3	channel 3 ESD protection		
5	CH4	channel 4 ESD protection		
6	CH5	channel 5 ESD protection		
7	CH6	channel 6 ESD protection		

[1] Any pin can be chosen for ground connection; one pin must be connected to ground.

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
PUSB3TB6	XSON7	plastic, leadless extremely thin small outline package; 7 terminals; 0.5 mm pitch; 1.1 mm x 2.1 mm x 0.5 mm body	SOT1358-1

6. Marking

Table 3. Marking codes

Type number	Marking code
PUSB3TB6	3T

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_I	input voltage			-5.5	5.5	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2, level 4; contact discharge	[1]	-10	10	kV
		IEC 61000-4-2, level 4; air discharge	[1]	-15	15	kV
T_{stg}	storage temperature			-55	125	°C
T_{amb}	ambient temperature			-40	85	°C

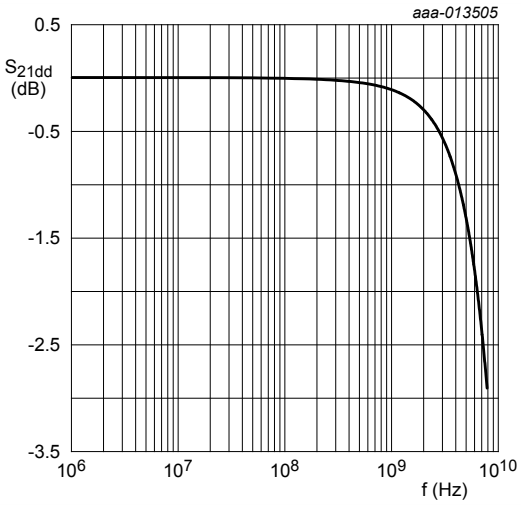
[1] All pins to ground.

8. Characteristics

Table 5. Characteristics

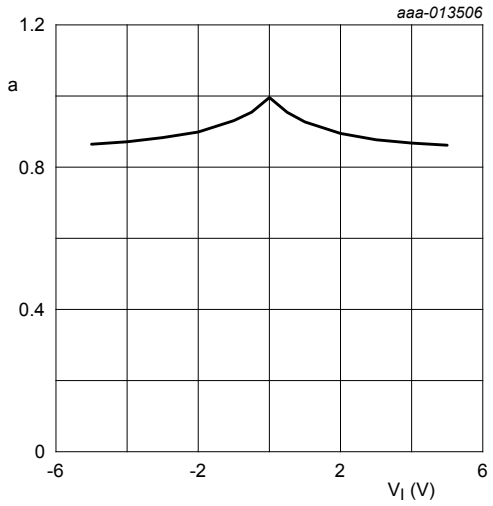
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{BR}	breakdown voltage	I_I = 1 mA; T_{amb} = 25 °C		6	-	-	V
I_{LR}	reverse leakage current	per channel; V_I = 3 V; T_{amb} = 25 °C		-	1	100	nA
C_{line}	line capacitance	f = 1 MHz; V_I = 0 V; T_{amb} = 25 °C	[1]	-	0.27	0.35	pF
ΔC_{line}	line capacitance difference	f = 1 MHz; V_I = 0 V	[1]	-	0.03	0.05	pF
r_{dyn}	dynamic resistance	TLP; positive transient; T_{amb} = 25 °C	[2]	-	0.6	-	Ω
		TLP; negative transient; ; T_{amb} = 25 °C	[2]	-	0.6	-	Ω
		surge; 8/20 µs; ; T_{amb} = 25 °C	[3]	-	0.5	-	Ω
			[3]	-	0.5	-	Ω
V_{CL}	clamping voltage	I_{PP} = 3.5 A; positive transient; T_{amb} = 25 °C	[3]	-	4.8	-	V
		I_{PP} = -3.5 A; negative transient; T_{amb} = 25 °C	[3]	-	-4.8	-	V

[1] The parameter is guaranteed by design.
[2] 100 ns Transmission Line Pulse (TLP), 50 Ω, pulser at 80 ns.
[3] According to IEC 61000-4-5, pulse time t_p = 8/20 µs.



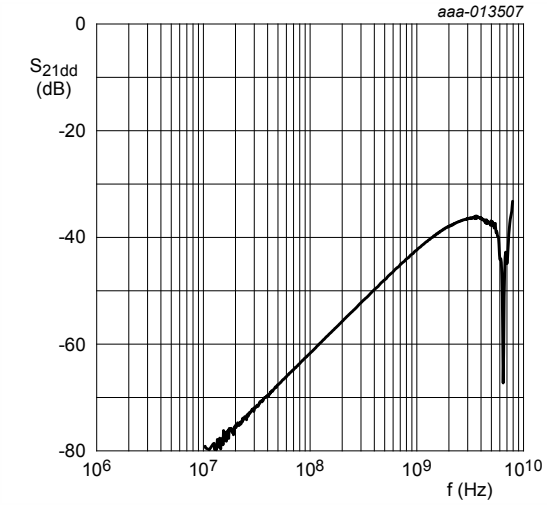
differential mode

Fig. 1. Insertion loss; typical values



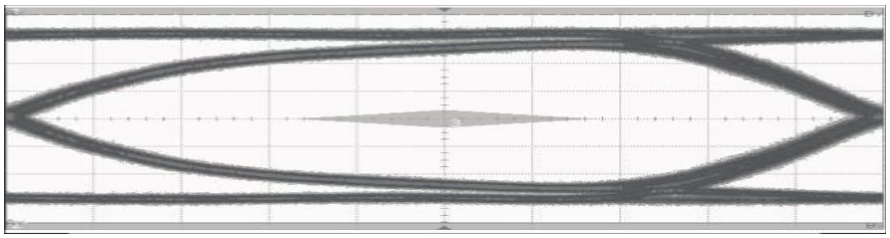
$$a = \frac{C_{line}}{C_{line}(V_I = 0\ V)}$$

Fig. 2. Relative capacitance as a function of input voltage; typical values



normalized to 100 #Ω

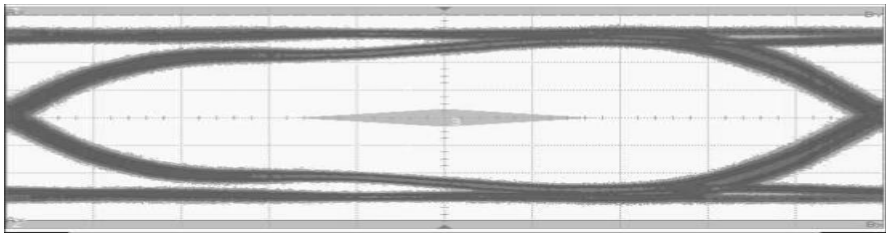
Fig. 3. Crosstalk; typical values



aaa-014154

Data rate: 5 Gbit/s
Vertical scale: 160 mV/div
Horizontal scale: 20 ps/div

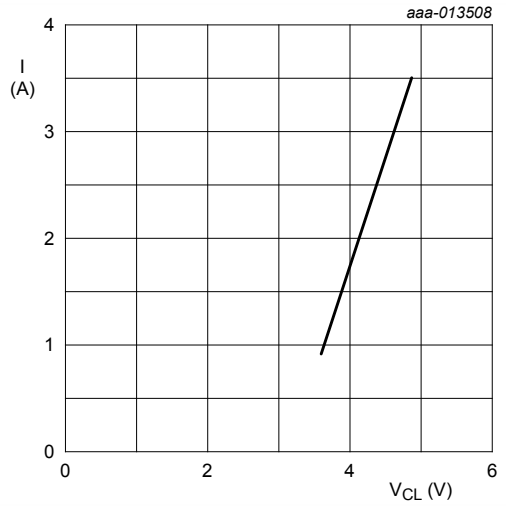
Fig. 4. USB 3.0 eye diagram, PCB with device



aaa-014155

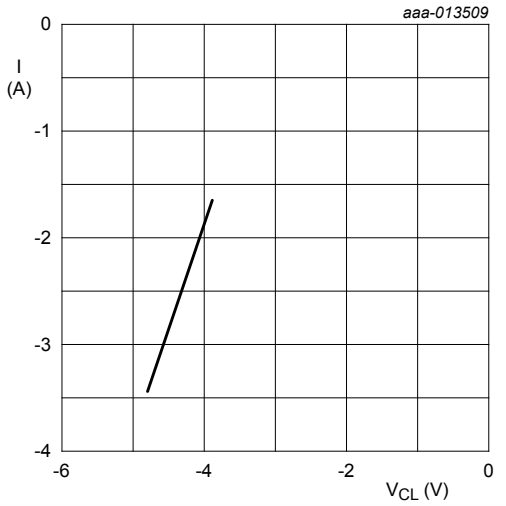
Data rate: 5 Gbit/s
Vertical scale: 162.5 mV/div
Horizontal scale: 20 ps/div

Fig. 5. USB 3.0 eye diagram, PCB without device



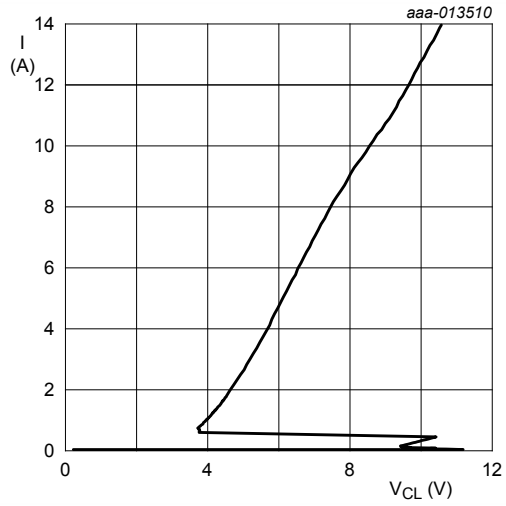
IEC 61000-4-5; t_p = 8/20 µS; positive pulse

Fig. 6. Dynamic resistance with positive clamping; typical values



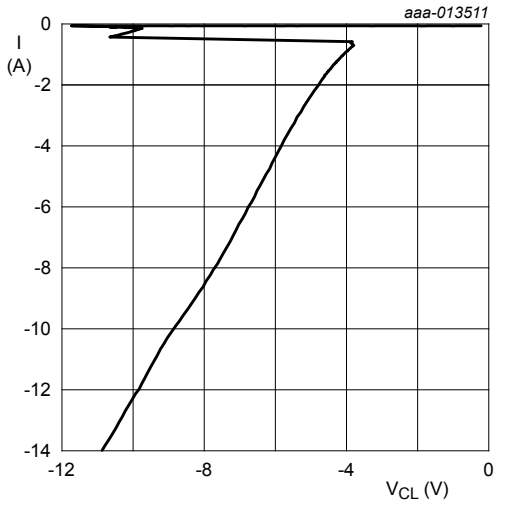
IEC 61000-4-5; t_p = 8/20 µ##s; negative pulse

Fig. 7. Dynamic resistance with negative clamping; typical values



t_p = 100 ns; Transmission Line Pulse (TLP)

Fig. 8. Dynamic resistance with positive clamping; typical values



t_p = 100 ns; Transmission Line Pulse (TLP)

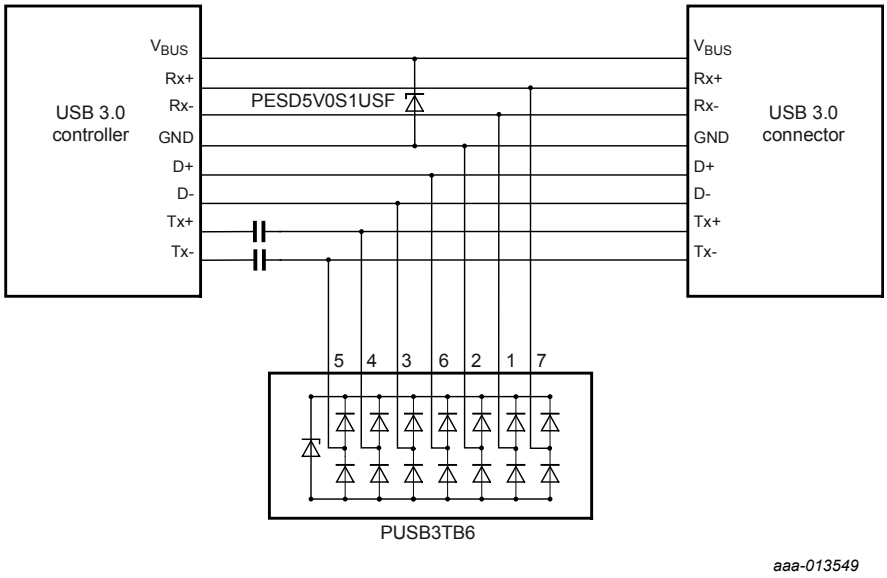
Fig. 9. Dynamic resistance with negative clamping; typical values

9. Application information

The device is designed to provide high-level ESD protection for high-speed serial data buses such as HDMI, DisplayPort, eSATA and LVDS data lines.

Note: When designing the PCB, give careful consideration to impedance matching and signal coupling. Do not connect the signal lines to unlimited current sources like, for example, a battery.

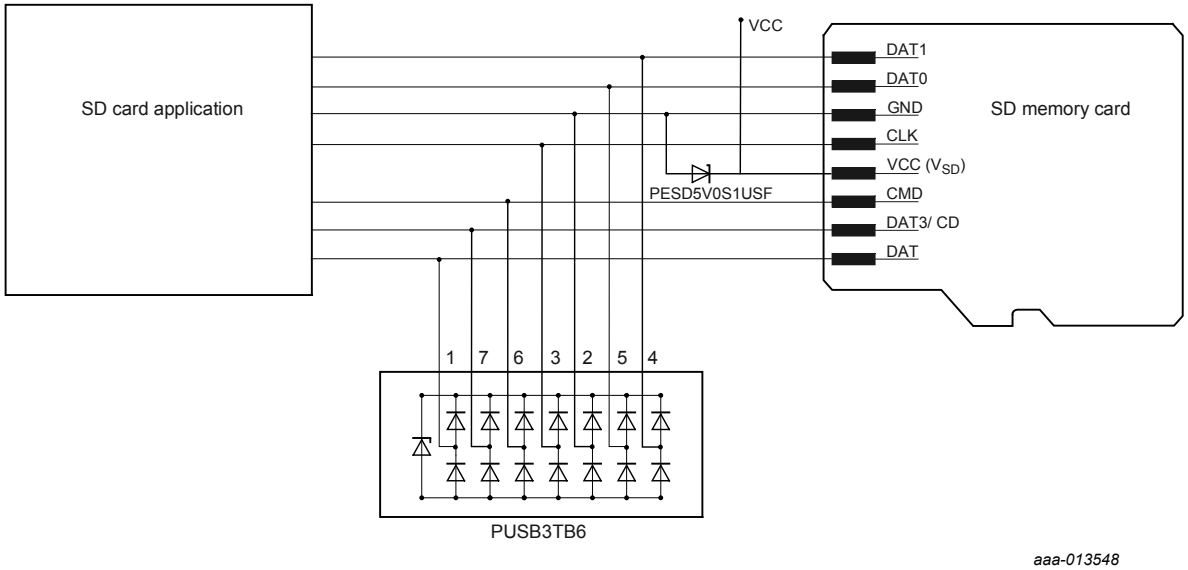
ESD protection schematic diagram for USB 3.0 or USB 2.0 interface is shown on Figure 10.



Any pin can be chosen for ground connection; one pin must be connected to ground

Fig. 10. Demo PCB of ESD protection for USB 3.0 or USB 2.0 interfaces using PUSB3TB6

A basic application diagram for ESD protection of SD card interface is shown on Figure 11. GND can be connected to pin 2 for easy routing or to any other rail-to-rail structure.



Any pin can be chosen for ground connection; one pin must be connected to ground

Fig. 11. Application diagram of SD card ESD protection using PUSB3TB6

Dynamic resistance

The device uses an advanced clamping structure showing a negative dynamic resistance.

This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).

10. Package outline

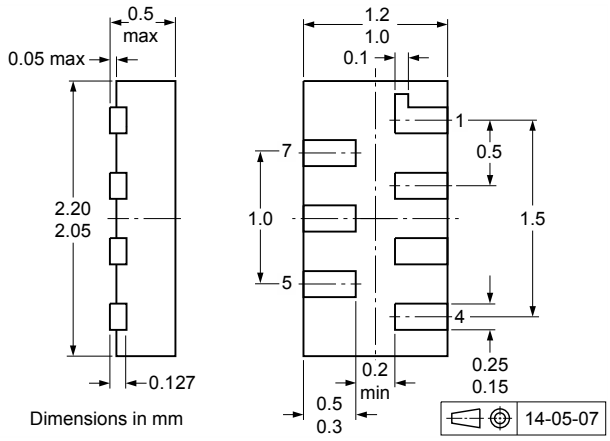


Fig. 12. Package outline XSON7 (SOT1358-1)

11. Soldering

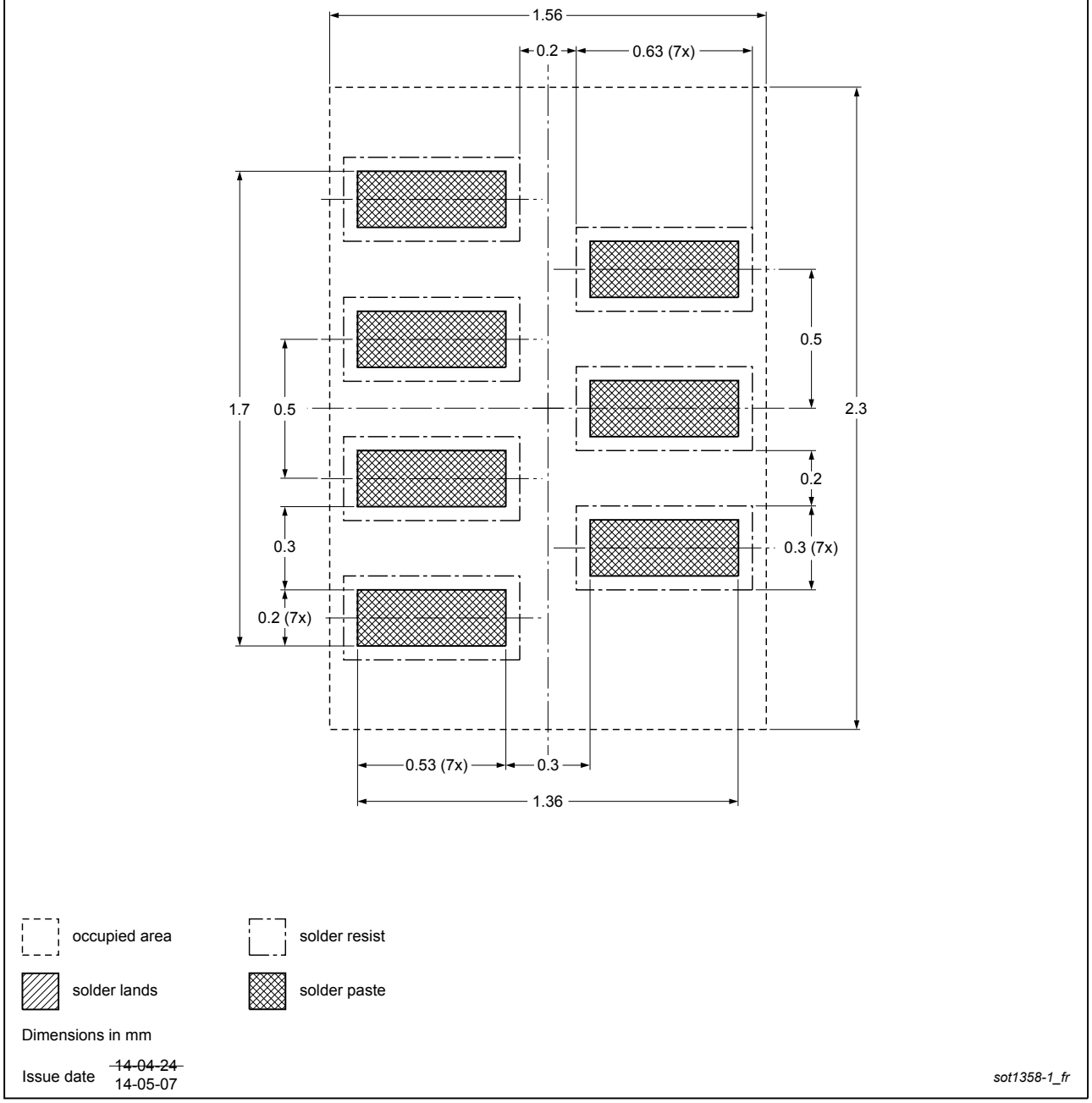


Fig. 13. Reflow soldering footprint for XSON7 (SOT1358-1)

12. Revision history

Table 6. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PUSB3TB6 v.2	20180823	Product data sheet	-	PUSB3TB6 v.1
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate.			
PUSB3TB6 v.1	20140819	Product data sheet	-	-

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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