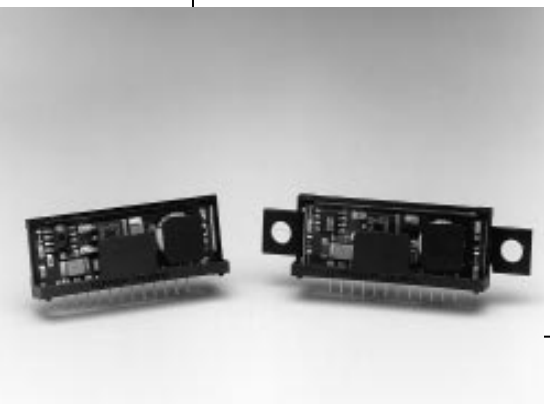
PT6305 Series

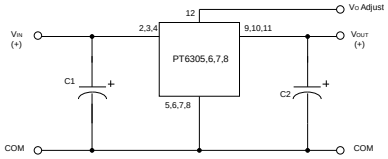
3 AMP HIGH-PERFORMANCE ADJUSTABLE ISR



- Single-Device 5V to 3V Power
- 85% Efficiency
- Small SIP Footprint: 0.36" x 2.00" x 0.60"(H)
- Wide Input Voltage Range: +4.5V to +9.0V
- Internal Short Circuit Protection
- Over-Temperature Protection

The PT6305N is Power Trends' new high performance +5V to +3.3V, 3 Amp, 12-Pin SIP (Single In-line-Package) Integrated Switching Regulator (ISR). This high-performance ISR allows easy integration of low-power 3.3V logic IC's into existing 5V systems without redesigning the central power supply. Only one external capacitor is required for proper operation. The PT6306,7,8 can be used to power high-speed data buses (+2.1V), or the new GTL (+1.2V) logic buses.

Standard Application

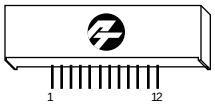


C_1 = Optional electrolytic (100µF)
C_2 = Required 100µF electrolytic (No tantalum)
See capacitor application note on page 43.

Pin-Out Information

Pin No.	Function
1	N/C
2	V_{in}
3	V_{in}
4	V_{in}
5	GND
6	GND

Pin No.	Function
7	GND
8	GND
9	V_{out}
10	V_{out}
11	V_{out}
12	Adjust (See page 40.)



Ordering Information

PT6305□ = +3.3 Volts
PT6306□ = +1.8 Volts
PT6307□ = +2.1 Volts
PT6308□ = +1.2 Volts
(For dimensions, see page 66.)

PT Series Suffix (PT1234X)

Case/Pin Configuration	Heat Tab Configuration: *None*	*Side*
Vertical Through-Hole	N	R
Horizontal Through-Hole	A	G
Horizontal Surface Mount	C	B

(See Thermal Application Notes on page 44 for heat tab application data.)

Specifications

Characteristics (T_a=25°C unless noted)	Symbols	Conditions		PT6305 SERIES Min	Typ	Max	Units
Output Current	I_o	4.5 ≤ V_{in} ≤ V_{in} MAX		0.3	—	3.0**	ADC
Current Limit	I_{cl}	V_{in} = +5V		—	3.6	5.0	ADC
Short Circuit Current	I_{sc}	V_{in} = +5V		—	5.0	—	Apk
Input Voltage Range	V_{in}	0.3A ≤ I_o ≤ 3.0A	PT6305N PT6306N PT6307N PT6308N	4.5 4.5 4.5 4.5	— — — —	9 9 9 6.0	VDC VDC VDC VDC
Static Voltage Tolerance	V_o	V_{in} = +5V, I_o = 3.0A 0°C ≤ T_a ≤ +70°C	PT6305N PT6306N PT6307N PT6308N	3.2 1.7 2.0 1.1	3.3 1.8 2.1 1.2	3.4 1.9 2.2 1.3	VDC VDC VDC VDC
Line Regulation	Reg_{line}	4.5V ≤ V_{in} ≤ 5.5V, I_o = 3.0A		—	±25	±50	mV
Load Regulation	Reg_{load}	V_{in} = +5V, 0.3 ≤ I_o ≤ 3.0A		—	±25	±50	mV
V_o Ripple/Noise pk-pk	V_n	V_{in} = 5V, I_o = 3.0A		—	66	—	mV
Transient Response with C_2 = 100µF	t_{tr} V_{os}	I_o step between 1.5A and 3.0A V_o over/undershoot		— —	200 200	— —	µSec mV
Efficiency	η	V_{in} = +5V, I_o = 1.5A	PT6305N PT6306N PT6307N PT6308N	— — — —	85 74 77 63	— — — —	% % % %
		V_{in} = +5V, I_o = 3.0A	PT6305N PT6306N PT6307N PT6308N	— — — —	80 68 72 57	— — — —	% % % %
Switching Frequency	f_o	4.5 ≤ V_{in} ≤ V_{in} MAX 0.3A ≤ I_o ≤ 3.0A		500	650	800	KHz
Operating Temperature	T_a	Free Air Convection (40-60 LFM) Over V_{in} and I_o Ranges		0	—	+70*	°C
Thermal Resistance	θ_{ja}	Free Air Convection (40-60 LFM)		—	25	—	°C/W
Storage Temperature	T_s	—		-40	—	+125	°C
Mechanical Shock	Per Mil-STD-883D, Method 2002.3 Condition A, 1 msec, Half Sine, mounted to a fixture			—	—	500	G's
Mechanical Vibration	Per Mil-STD-883D, Method 2007.2 Condition A, 20-2000 Hz			—	—	15	G's
Weight	—	—		—	11.2	—	grams
Relative Humidity	—	Non-condensing		0	—	95	%

*See Thermal Derating chart. **The PT6305 Series can be easily paralleled to provide output current in multiples of 3 amps. Please contact a Power Trends' Application Engineer for the appropriate application note. ***Note:*** *The PT6305 Series requires a 100µF electrolytic capacitor for proper operation in all applications.*

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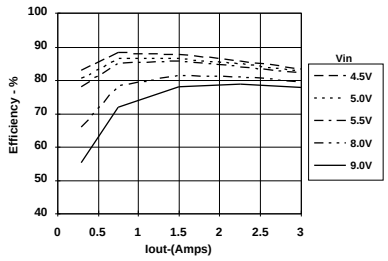
CHARACTERISTIC DATA

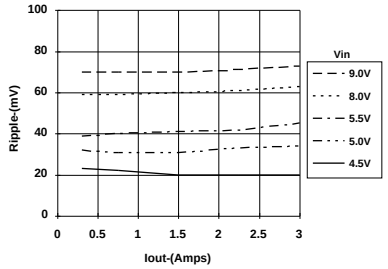
PT6305, 3.3 VDC

(See Note 1)

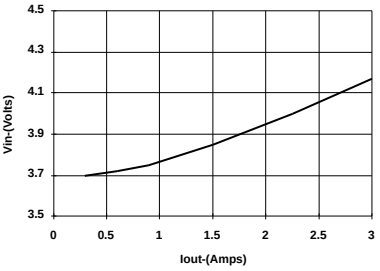
Efficiency vs Output Current



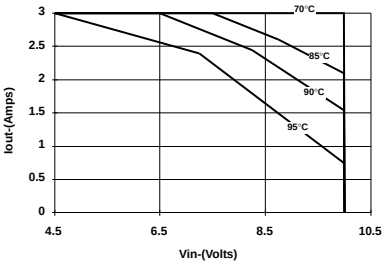
Ripple vs Output Current



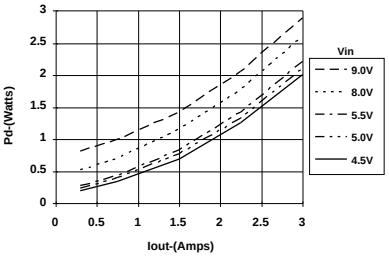
Minimum Input Voltage (See Note 2)



Thermal Derating (T_a) (See Note 3)



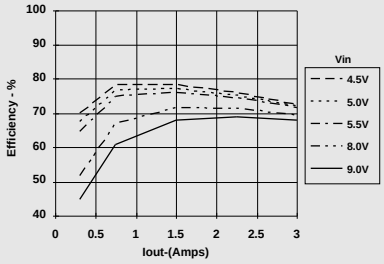
Power Dissipation vs Output Current



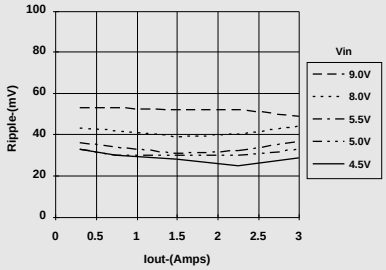
PT6307, 2.1 VDC

(See Note 1)

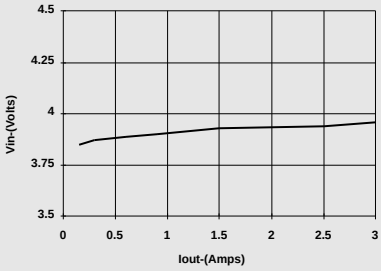
Efficiency vs Output Current



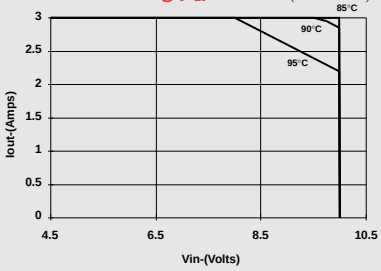
Ripple vs Output Current



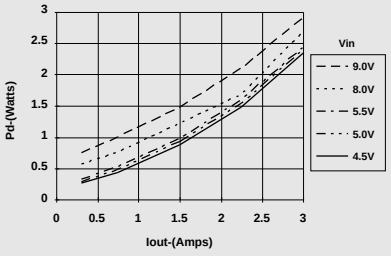
Minimum Input Voltage (See Note 2)



Thermal Derating (T_a) (See Note 3)



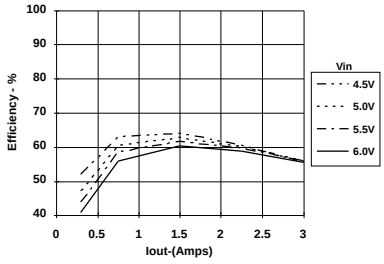
Power Dissipation vs Output Current



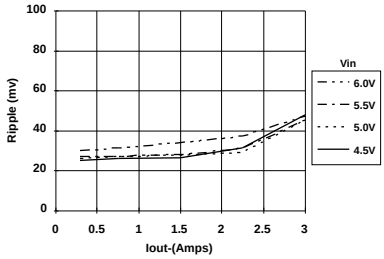
PT6308, 1.2 VDC

(See Note 1)

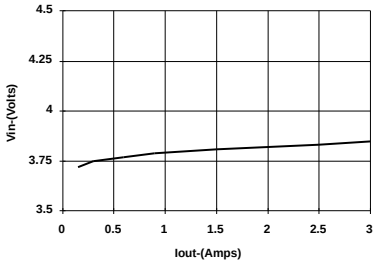
Efficiency vs Output Current



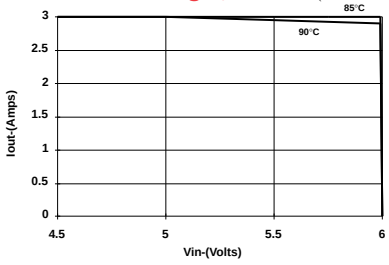
Ripple vs Output Current



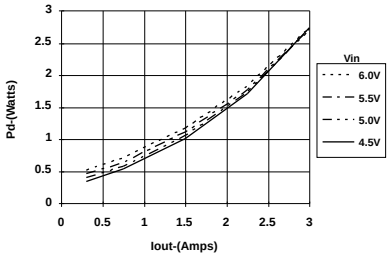
Minimum Input Voltage (See Note 2)



Thermal Derating (T_a) (See Note 3)



Power Dissipation vs Output Current



Note 1: *All data listed in the above graphs, except for derating data, has been developed from actual products tested at 25°C. This data is considered typical data for the ISR.*
Note 2: *Minimum V_{in} data is typical and is not guaranteed. The data corresponds to a 2% output voltage drop.*
Note 3: *Thermal derating graphs are developed in free air convection cooling of 40-60 LFM with no optional heat tab soldered in a printed circuit board. (See Thermal Application Notes).*

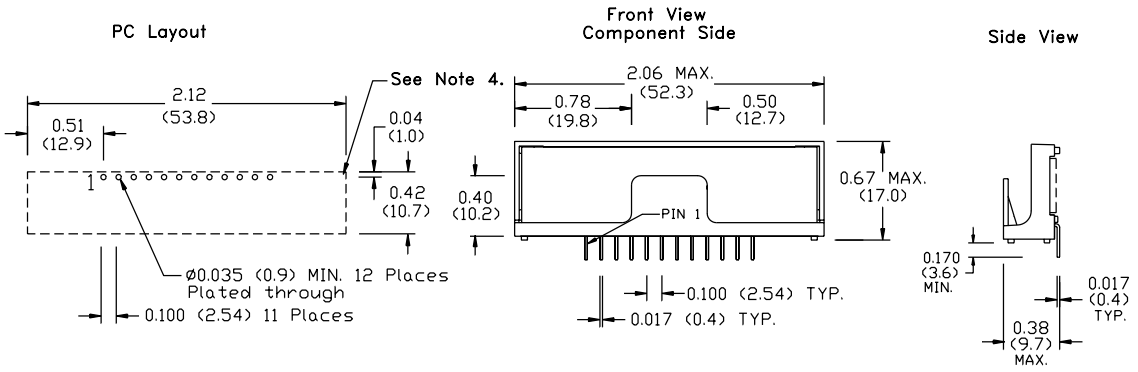
Product families using this package style:
PT6400
PT5060

Package Style 300
Suffix A, C, D, E, N, P

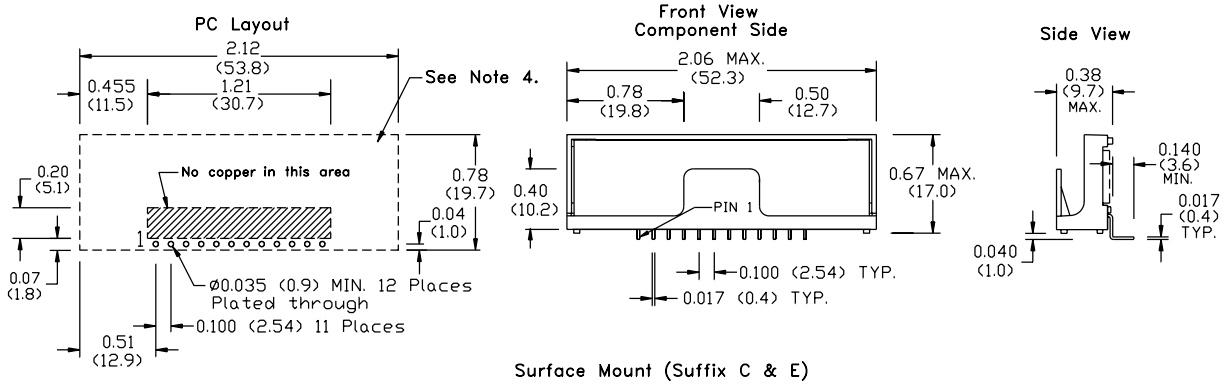
PACKAGE INFORMATION AND DIMENSIONS

Revised 2/11/2000

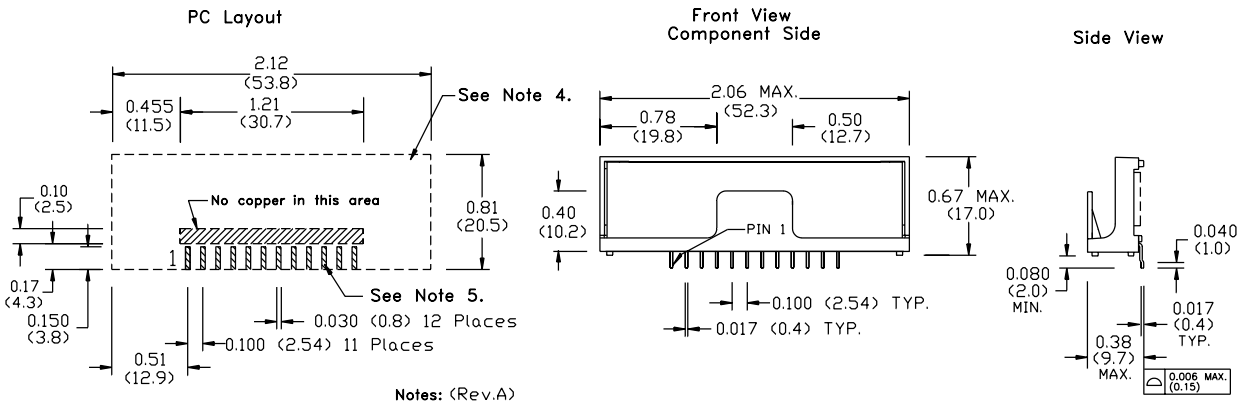
Vertical Through-Hole Mount (Suffix N & P)



Horizontal Through-Hole Mount (Suffix A & D)



Surface Mount (Suffix C & E)



Notes: (Rev.A)

1: All dimensions are in inches (mm).
2: 2 place decimals are ±.030 (±0.8mm).
3: 3 place decimals are ±.010 (±0.3mm).
4: Recommended mechanical keep out area.
5: Power pin connections should utilize two or more vias per input, ground and output pin.

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